United States Patent [19]

Coombe

[11] **3,801,961**

[45] **Apr. 2, 1974**

[54] **SYSTEM FOR PROVIDING A VIDEO DISPLAY HAVING DIFFERING VIDEO DISPLAY FORMATS**

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[73] Assignee: **Reuters Limited,** London, England

[22] Filed: **May 21, 1971**

[21] Appl. No.: **145,858**

[52] **U.S. Cl.** ..... **340/154,** 340/324 AD

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** ..... 340/324 A, 154

[56] **References Cited**

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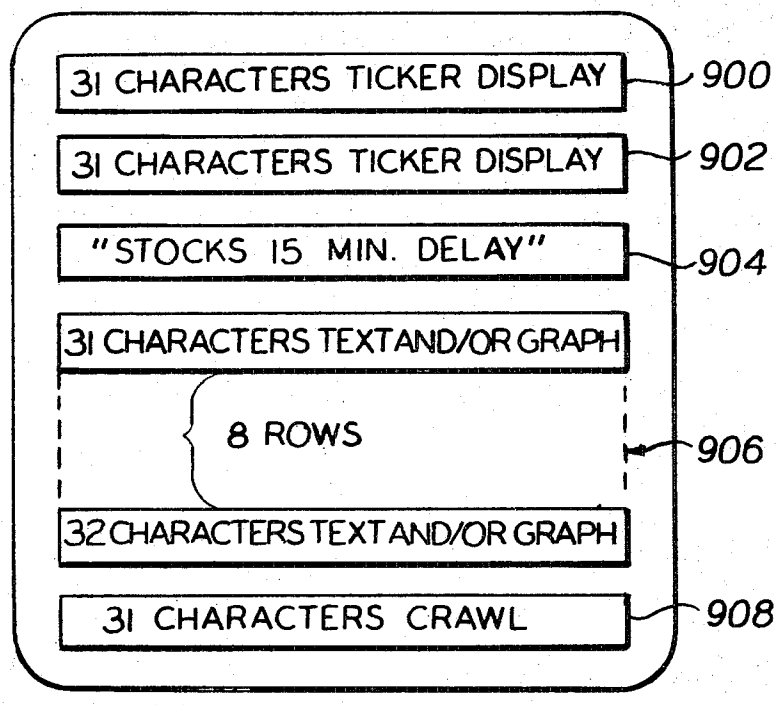
[57] **ABSTRACT**

A system for providing a video character display containing at least two different types of video display formats which are comprised of independently self-generated digital-to-video scan signals. These scan signals are combined to provide a composite video signal which, when supplied to a television display device which utilizes a raster scan-line pattern, provides the various video display formats in different scan-line areas of the display screen. Each of the display formats is individually controllable. The various types of display formats which are provided include a ticker display, a text and/or graph display, and a crawl display. Means are provided for controlling the movement of the character display across the screen so as to vary the rate of movement of the character display across the screen in accordance with the rate of information input to the system. In this manner, a smooth video display format is provided at all input rates. Each display format comprises a plurality of character spaces and the system determines the character to be displayed in the given space on a space-by-space basis.

21 Claims, 13 Drawing Figures



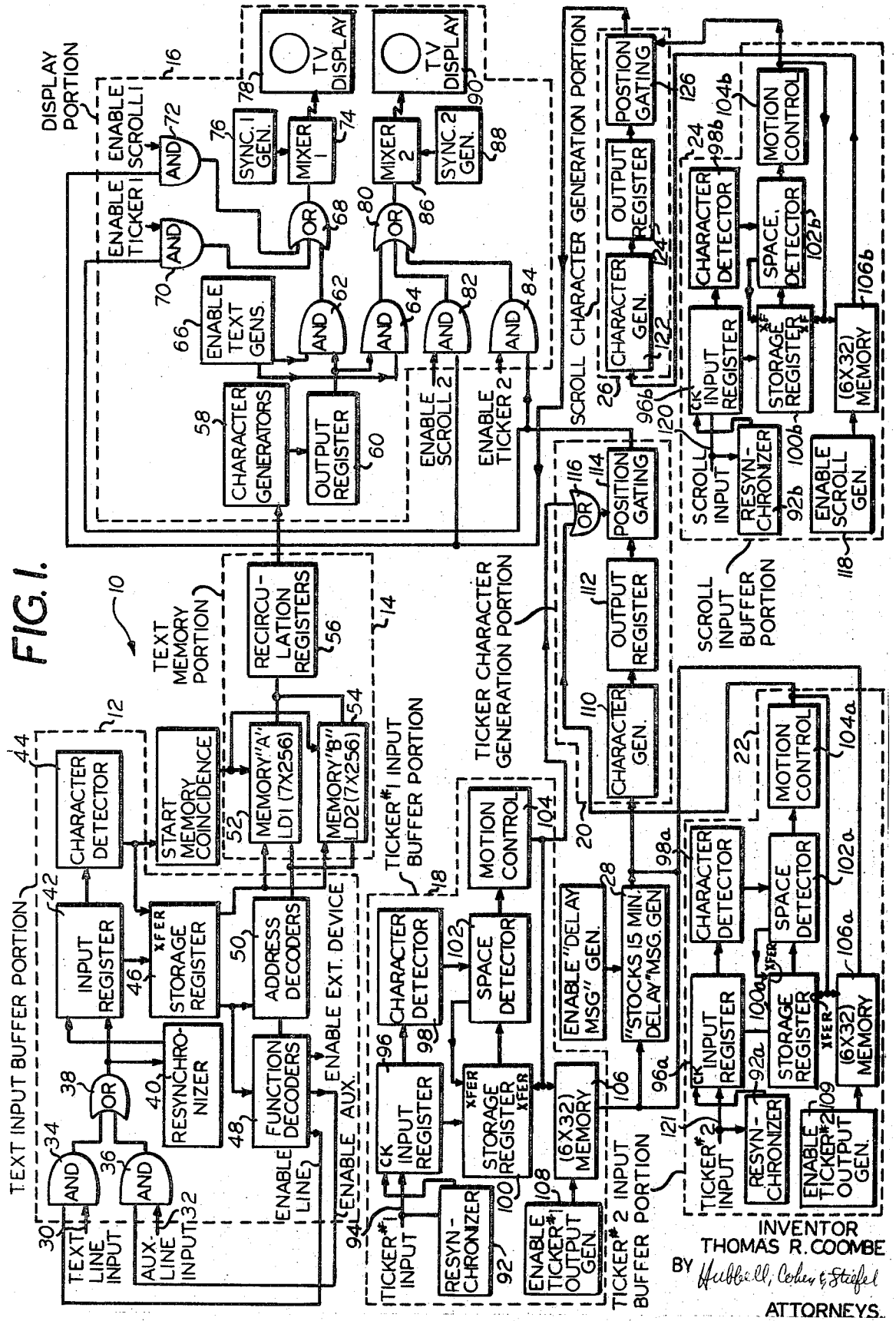


FIG. 1.

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FIG. 2.

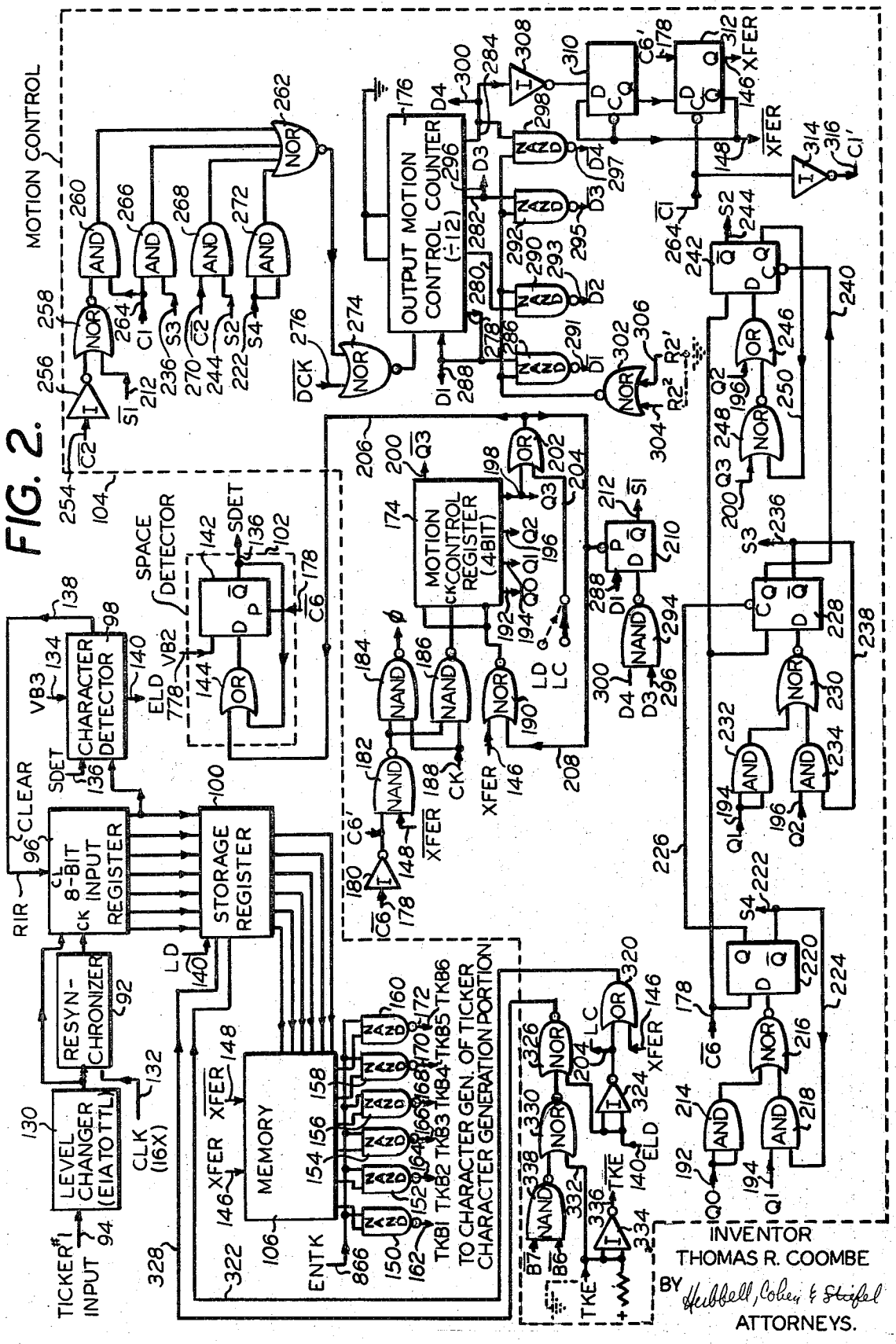
MOTION CONTROL
OUTPUT MOTION CONTROL COUNTER (÷12)
MOTION CONTROL REGISTER (4BIT)
SPACE DETECTOR
CHARACTER DETECTOR
8-BIT INPUT REGISTER
STORAGE REGISTER
RESYN-CHRONIZER
LEVEL CHANGER (EIA TO TTL)
MEMORY
TICKER INPUT
CLK (16X)
RIR
CLEAR
SDET
ELD
LD
LC
XFER
ENTK
TKE
TKB1 TKB2 TKB3 TKB4 TKB5 TKB6
TO CHARACTER GEN. OF TICKER CHARACTER GENERATION PORTION
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FIG. 3.

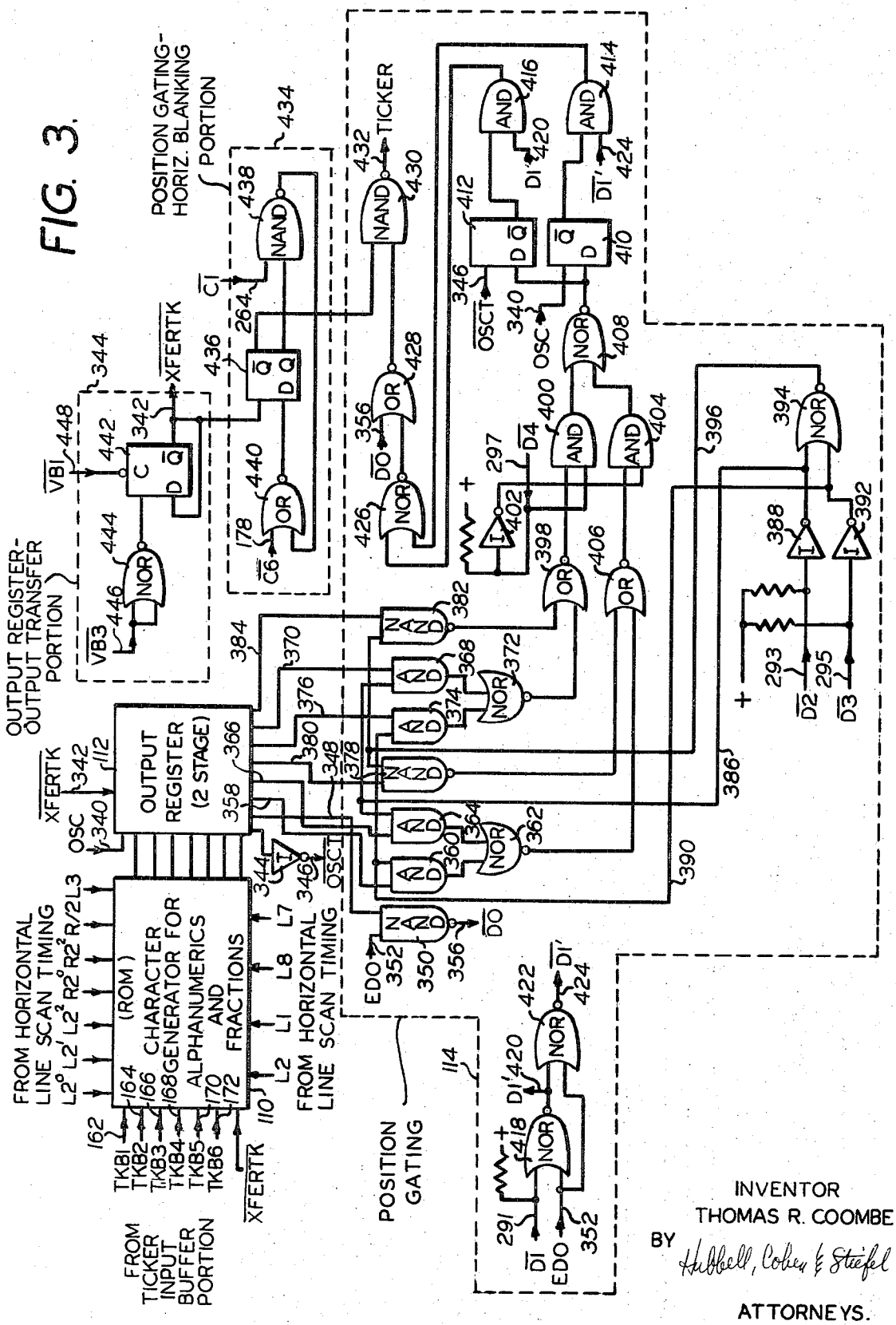

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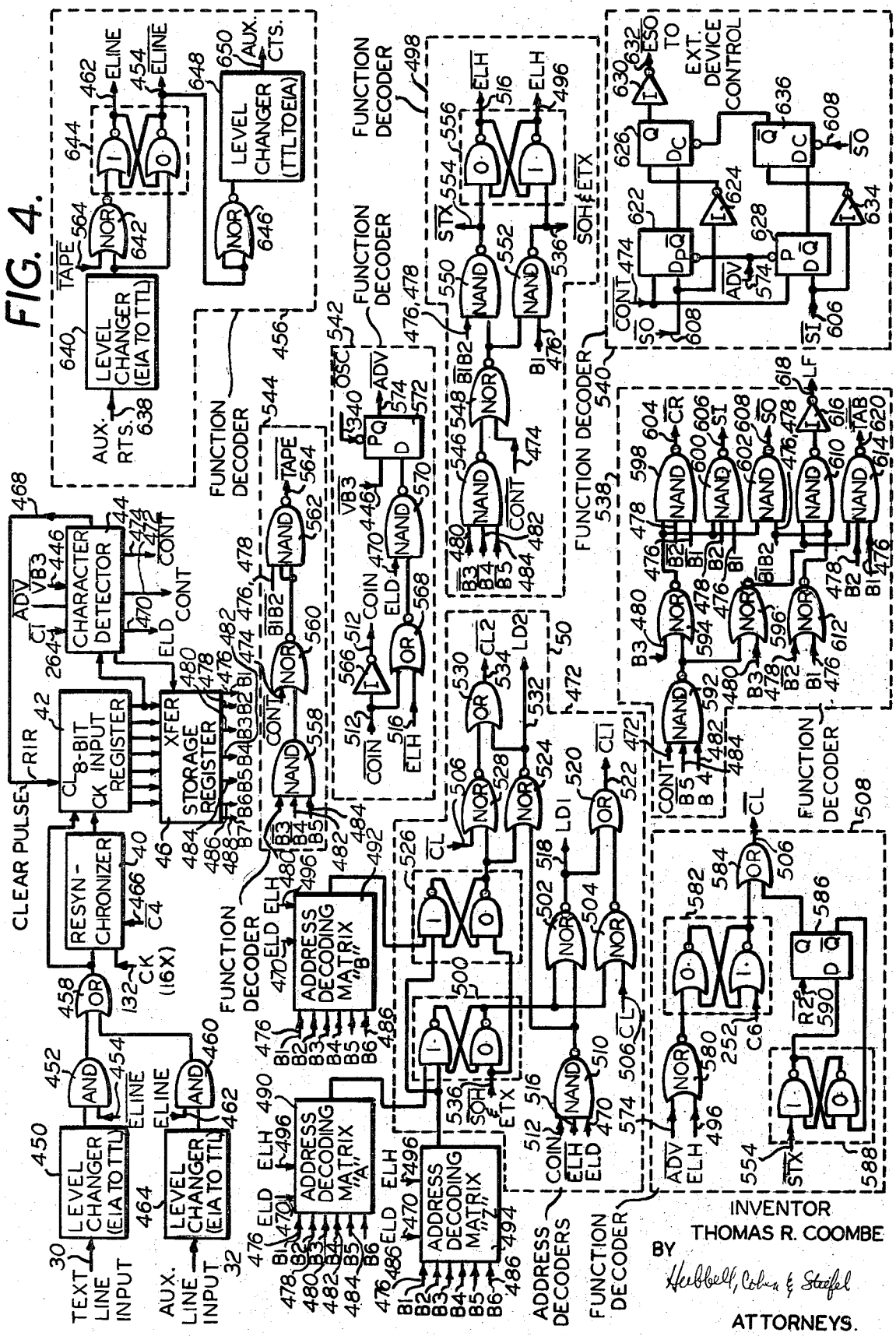
FIG. 4.


TEXT LINE INPUT
AUX. LINE INPUT
LEVEL CHANGER (EIA TO TTL)
RESYN-CHRONIZER
8-BIT INPUT REGISTER
STORAGE REGISTER
CHARACTER DETECTOR
ADDRESS DECODING MATRIX "A"
ADDRESS DECODING MATRIX "B"
ADDRESS DECODING MATRIX "Z"
ADDRESS DECODERS
FUNCTION DECODER
LEVEL CHANGER (TTL TO EIA)
AUX. RTS.
AUX. CTS.
TO EXT. DEVICE CONTROL
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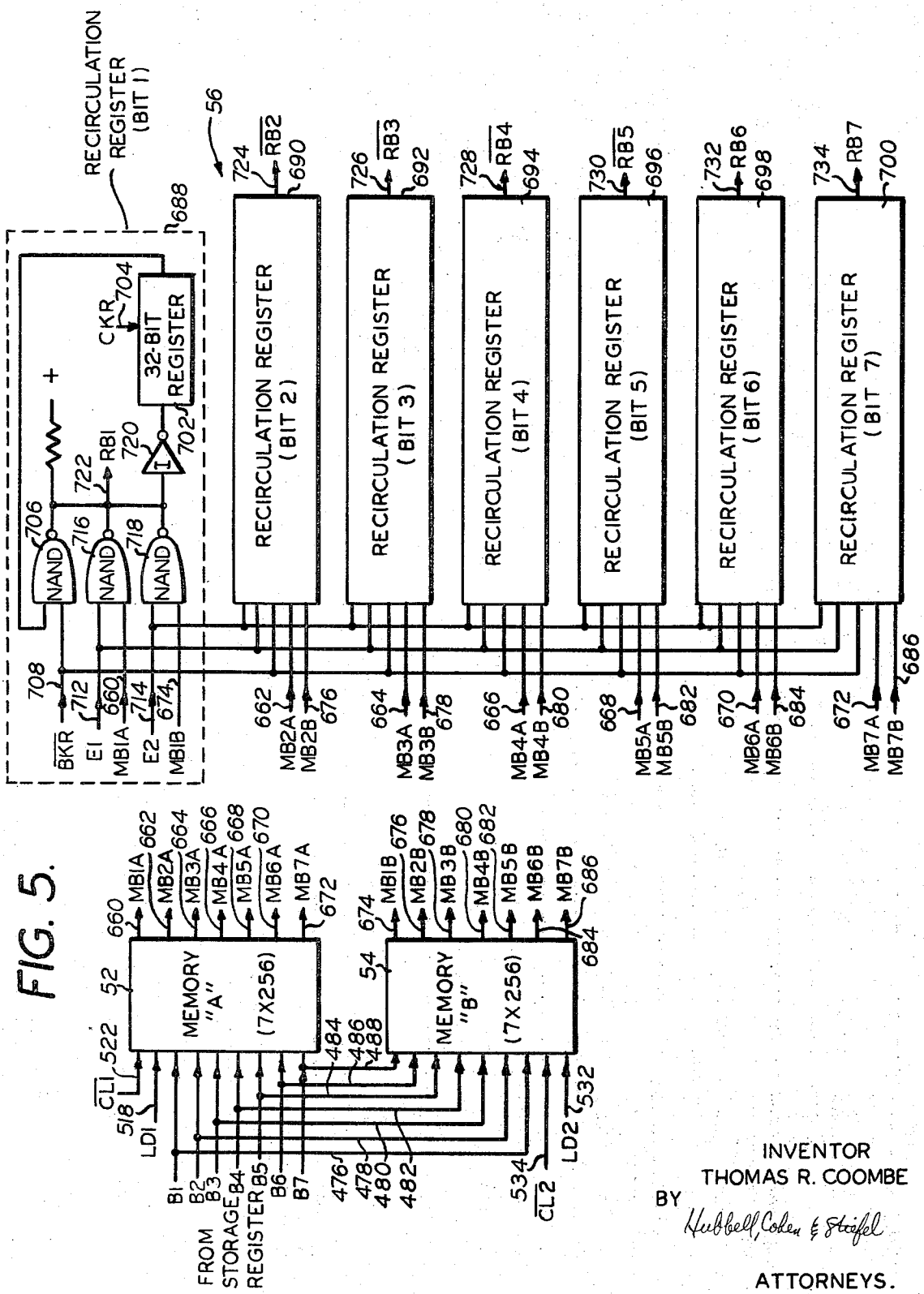

FIG. 5.

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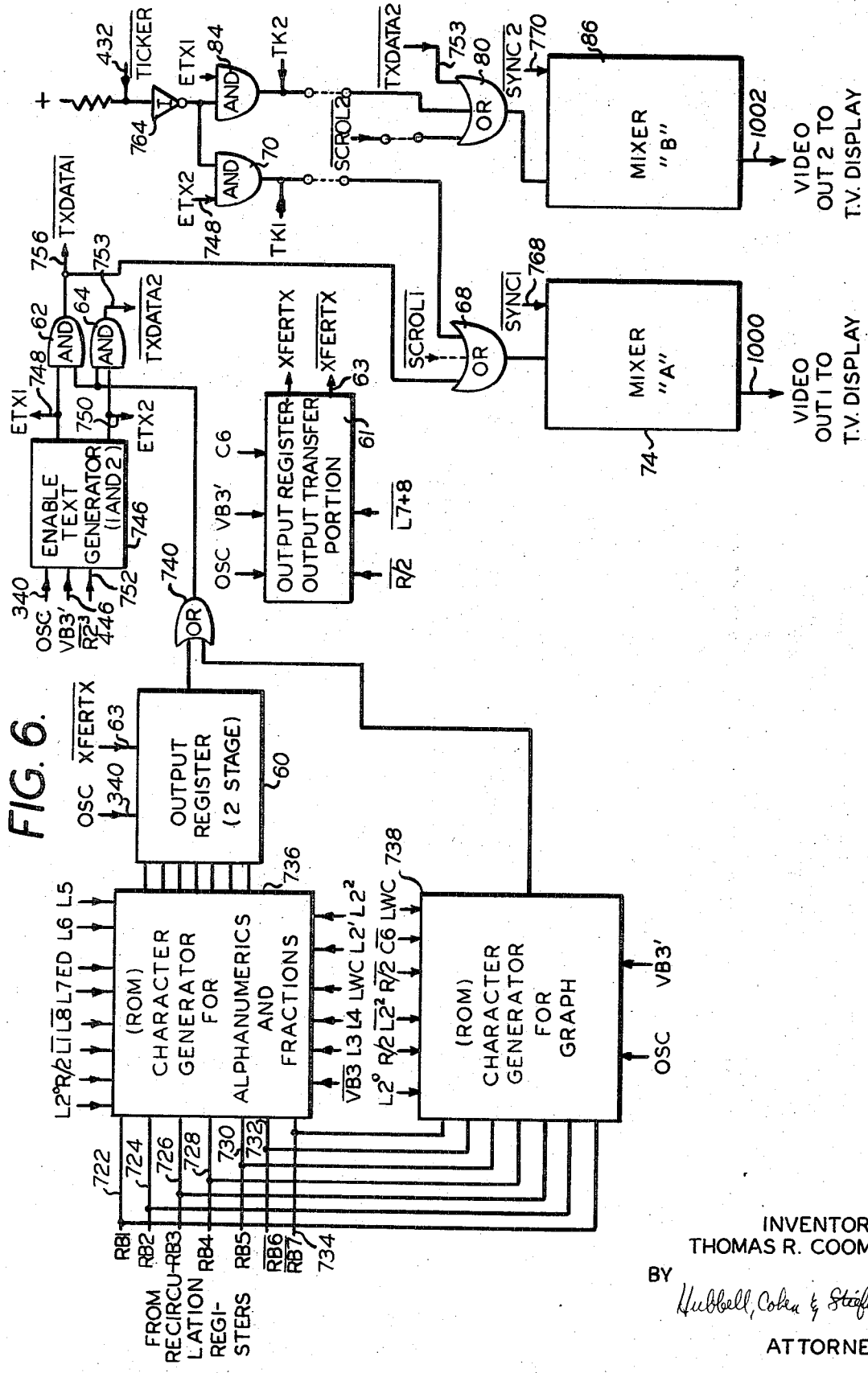
FIG. 6.
OUTPUT REGISTER (2 STAGE)
(ROM) CHARACTER GENERATOR FOR ALPHANUMERICS AND FRACTIONS
(ROM) CHARACTER GENERATOR FOR GRAPH
OUTPUT REGISTER OUTPUT TRANSFER PORTION
ENABLE TEXT GENERATOR (I AND 2)
MIXER "A"
MIXER "B"
VIDEO OUT 1 TO T.V. DISPLAY
VIDEO OUT 2 TO T.V. DISPLAY
FROM RECIRCULATION REGISTERS
TICKER
AND
OR
XFERTX
SCROL1
SCROL2
SYNC1
SYNC2
TXDATA1
TXDATA2
ETX1
ETX2
TK1
TK2
OSC
VB3'
C6
R/2
L7+8
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FIG. 7.

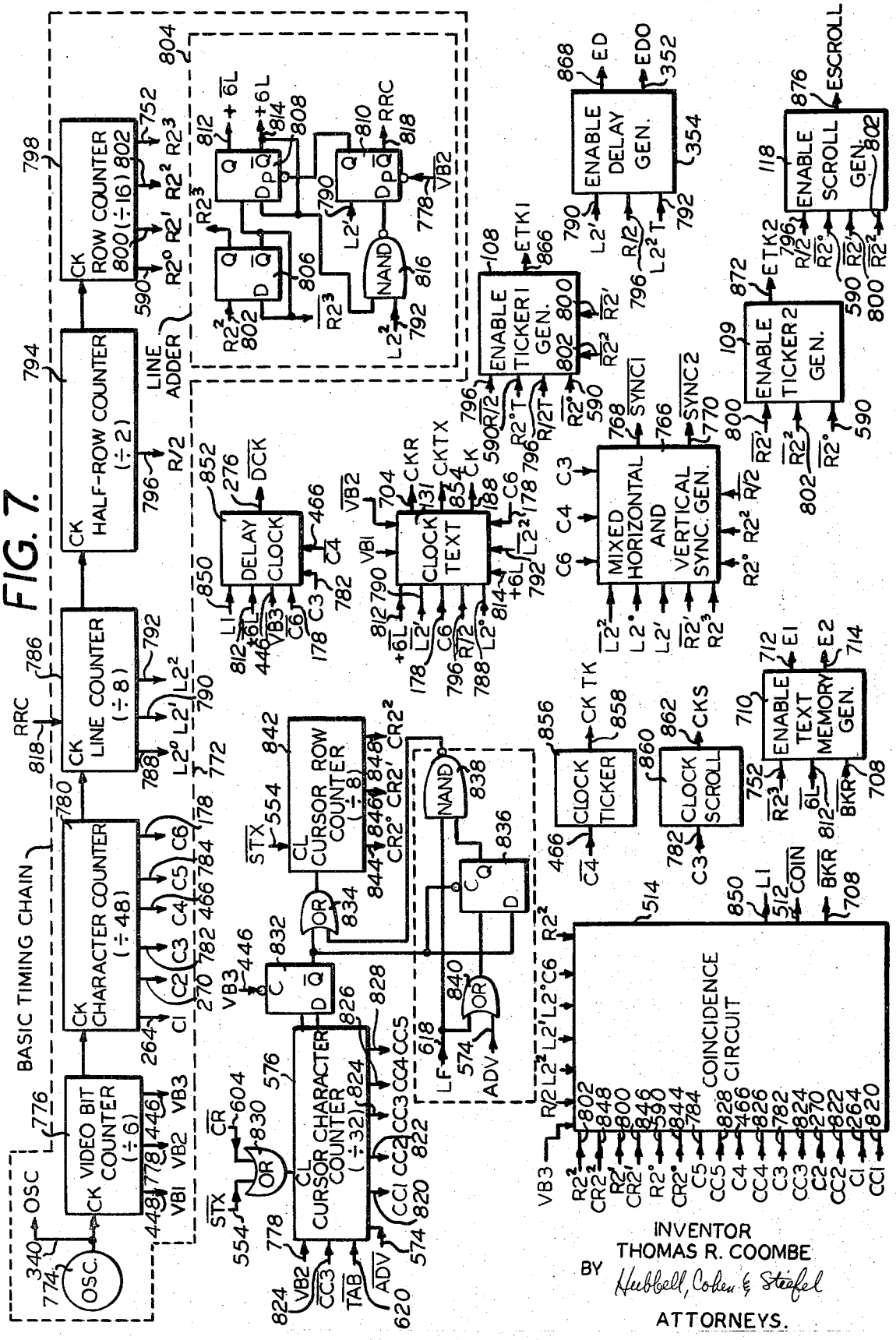
BASIC TIMING CHAIN
OSC
VIDEO BIT COUNTER (÷6)
CHARACTER COUNTER (÷48)
LINE COUNTER (÷8)
HALF-ROW COUNTER (÷2)
ROW COUNTER 800 (÷16) 802
LINE ADDER
CURSOR CHARACTER COUNTER (÷32)
CURSOR ROW COUNTER (÷8)
DELAY CLOCK
CLOCK TEXT
MIXED HORIZONTAL AND VERTICAL SYNC. GEN.
ENABLE TICKER1 GEN.
ENABLE TICKER2 GEN.
ENABLE DELAY GEN.
ENABLE SCROLL GEN. 802
ENABLE TEXT MEMORY GEN.
CLOCK TICKER
CLOCK SCROLL
COINCIDENCE CIRCUIT
NAND
OR
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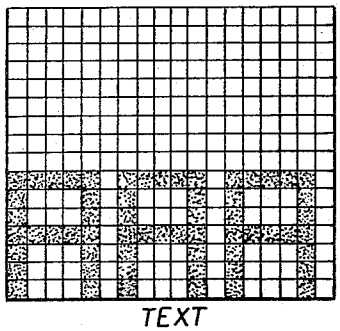
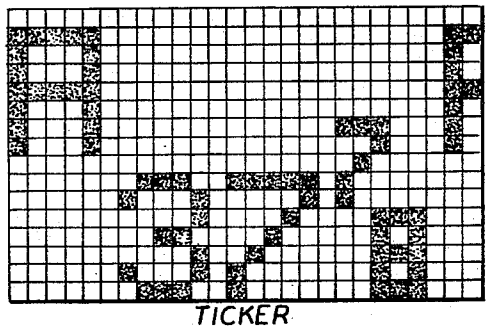
FIG. 8A.



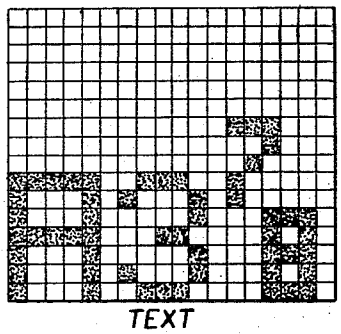
TEXT

FIG. 8B.



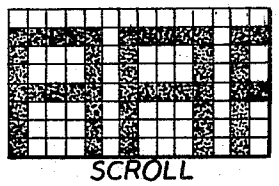
TICKER

FIG. 8C.



TEXT

FIG 8F.



SCROLL

FIG. 8E.

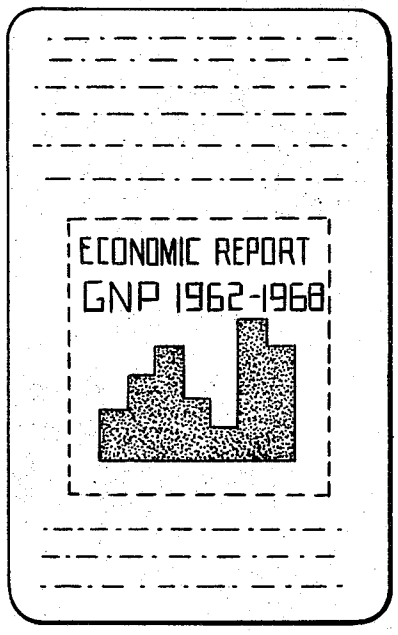
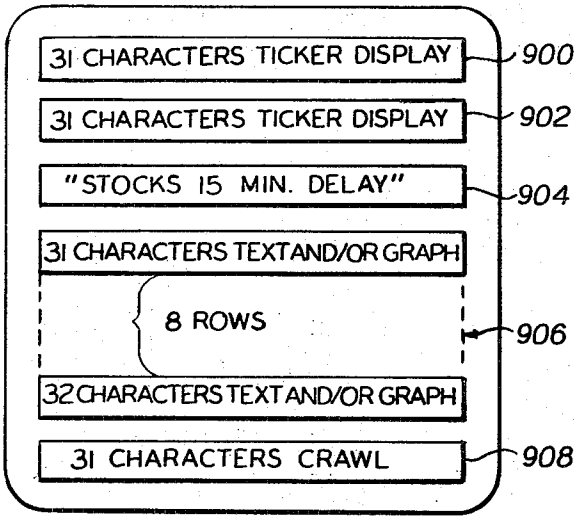


FIG. 8D.



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SYSTEM FOR PROVIDING A VIDEO DISPLAY HAVING DIFFERING VIDEO DISPLAY FORMATS

BACKGROUND OF INVENTION

1. Field of the Invention

The present invention relates to systems capable of providing a video display containing at least two different types of video display formats.

Description of the Prior Art

There are several prior art video display systems. Prior art systems, however, are normally of the type which utilize a television camera in order to provide the information to be displayed on the screen. In such a system, at least one television camera is provided for each display area on the screen to which different information is to be supplied. Furthermore, in such systems, the television cameras are slaved to each other and the various display areas on the screen are, therefore, not independently controllable with respect to each other. These systems are not capable of displaying different types of display formats on the video display screen so that if it is desired to display two types of information which each lend themselves to a different type of display format, such as a display of a news report for a predetermined interval of time, and a display of stock ticker information in a continuously moving format, these prior art systems cannot accomplish this. In an attempt to overcome this problem, prior art systems have utilized a separate television camera for scanning a moving tape containing the stock ticker information. However, such a system is inefficient and costly as it requires an additional television camera to scan the tape rather than directly utilizing the signals which cause the tape to be printed.

Prior art video display systems are also available of the type in which a selected one of a plurality of digitally stored messages may be displayed either as a message page or in a moving format across the video display screen. In such prior art systems, a combination of a given sequence of dot signals and a given sequence of line signals is utilized to define a character space area. Such systems are disclosed in U.S. Pat. Nos. 3,426,344; 3,422,420 and 3,345,458. These prior art systems, however, are not capable of providing different types of display formats on the common video display screen; rather, only one type of display format is displayed. Thus, as was previously mentioned, when it is desired to display two different types of display formats these systems cannot be utilized. In addition, such prior art systems which utilize a moving character display across the video display screen are not able to compensate for variations in the input rate of data to the system when such variations occur. Thus, if the device feeding information data to the system is such as a keyboard, as the rate of input of information by the keyboard operator varies, the moving character display on the screen will appear discontinuous or jerky so that a smooth display will not be provided as the data input rate varies. Thus, the display provided is undesirable as it is annoying to the viewer. Furthermore, such prior art video display systems capable of converting stored digital signals into a video display do not have sufficient flexibility in order to display alphanumeric information and fractions as well as graphic information simultaneously on the video display screen, such as for providing a video display of a graph having notations thereon. Thus, although television display systems capable of converting binary input signals into video signals for displaying the data in readable form on a conventional television picture tube have been available, they have not been utilized to maximum efficiency in areas where it is desired to display different types of information simultaneously, such as when it is desired to provide an up to data business forecast.

These disadvantages of the prior art are overcome by the present invention.

SUMMARY OF THE INVENTION

A system for providing a video character display containing at least two different types of video display formats is provided. These video display formats are independently self-generated digital-to-video scan signals which are provided in different areas of the television display screen. The display format displayed in each of the display areas is individually controllable. Conventional scanning techniques are utilized for display of the digital information in readable form on a conventional television picture tube. Preferably, at least one of the display formats provides a movable character display across the video display screen. Means are provided for controlling the motion of this character display across the screen by varying the rate of movement of the character display across the screen in accordance with the rate of information input to the system. In this manner, compensation for variations in input rate is provided so that a smooth moving display format is provided for all input rates. The system is capable of providing a character display composed of alphanumeric characters, fraction characters, and graph characters, so that a composite display of a graph having notational information thereon may be provided. Each display row is divided into a number of character spaces, a character space being defined by a predetermined sequence of lines and a predetermined sequence of dots.

The system determines the information to be displayed in each character space on a space-by-space basis so that one space may contain an alphanumeric character, another space in the row may contain a fraction character, and another space in the row may contain a graph character so that the composite graph display may be provided. In addition, the system is capable of providing a ticker type of display, which is normally a moving display format, a text type of display comprising a plurality of rows wherein the rows are painted on a row-by-row basis to form a message page which is held for a predetermined time, as well as a crawl type of display which is a moving display. In this manner different types of video display formats may be simultaneously displayed on the video display screen. If desired, any one or more of the plurality of display formats may be independently removed from the composite video display without altering the display of any of the other portions.

The system is also capable of controlling the display of one or more television display devices and may be utilized in conjunction with a remote computer which could be utilized to distribute different information through a plurality of television monitors on a time shared basis. In such instance, a particular channel is assigned to each television monitor and when the channel address associated therewith is transmitted from the

computer and decoded by the system, the particular channel will be accessed. In such instance, if desired, the text message page which has been painted on a given television monitor can be held until the channel associated with this monitor is addressed again by the remote computer.

BRIEF DESCRIPTION OF DRAWING

FIG. 1 is a functional block diagram of the preferred embodiment of the system of the present invention;

FIG. 2 is a block diagram, partially in schematic of the ticker input buffer portion of the system of FIG. 1;

FIG. 3 is a block diagram partially in schematic of the ticker character generation portion of the system of FIG. 1;

FIG. 4 is a block diagram, partially in schematic of the text input buffer portion of the system of FIG. 1;

FIG. 5 is a block diagram, partially in schematic of the text memory portion of the system of FIG. 1;

FIG. 6 is a block diagram, partially in schematic of the text display portion of the system of FIG. 1;

FIG. 7 is a block diagram, partially in schematic of the timing signals generation portions of the system of FIG. 1 which is omitted from FIG. 1 for purposes of clarity; and

FIGS. 8A through 8F are graphical illustrations exemplary of the various types of character displays which may be achieved with the system of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings in detail, and especially to FIG. 1 thereof which is a functional block diagram of the preferred embodiment of the system, generally referred to by the reference numeral **10**, of the present invention. For purposes of clarity, the portion of the system which generates the timing signals utilized for controlling operation throughout the system, as will described in greater detail hereinafter, has been omitted from FIG. 1, although the appropriate timing signals are shown throughout the figures. The timing signal generation network will be described in greater detail with reference to FIG. 7 hereinafter. The system **10** of the present invention preferably includes a text input buffer portion **12**, a text memory portion **14**, a display portion **16**, a ticker number 1 input buffer portion **18**, a ticker character generation portion **20**, a ticker number 2 input buffer portion **22**, a scroll input buffer portion **24**, a scroll character generation portion **26** and a stocks 15 min. delay message generation portion **28**. For purposes of illustration, and not by way of limitation, the system **10** of the present invention will be described with respect to provision of a composite plural display having a text and/or graph portion, two ticker portions, a delay message portion and a scroll portion. Any other desirable combination of plural display may be accomplished without departing from the spirit and scope of the present invention as will become apparent to one of ordinary skill in the art from the following description.

The text input buffer portion **12**, which is preferably capable of receiving either a text line input **30** and/or an auxiliary line input **32**, such as from an external digital system, includes an input gating circuit comprising AND gate **34** associated with the text line input **30** and AND gate **36** associated with the auxiliary line input **32**, both of which are fed to an OR gate **38**. The output of the OR gate **38** is connected in parallel to a conventional resynchronizer **40** and an input register **42**. As will be described in greater detail hereinafter, the resynchronizer **40** is connected to the clock terminal of the input register **42**. The input register **42** is connected to a character detector **44** which, as will be described in greater detail hereinafter, detects the presence of the start bit of the input signal. The output of the input register **42** is also connected to a storage register **46** which is in turn connected in parallel to a function decoder network **48**, to be described in greater detail hereinafter, which provides control functions for the system **10** of the present invention, and to an address decoder network **50** for detecting the appropriate channel to be addressed with the input information. The character detector **44** is also connected in parallel to the transfer terminal of the storage register **46** for controlling the transfer of data from the input register **42** to the storage register **46**, as will be described in greater detail hereinafter, and to the text memory portion **14**.

The output of the storage register **46** is connected in parallel to memory networks **52** and **54**, one such memory network being provided for each channel, only two channels A and B being shown for purposes of illustration. Each of the memories **52** and **54** is preferably a seven by 256 bit memory; that is, seven stages, one per bit, each having a capacity of 256 bits. The address decoder **50** is connected in parallel to the load terminal of memories **52** and **54**. The output of memories **52** and **54** are connected in parallel to the recirculation register network **56** which, as will be described in greater detail hereinafter, enables the scanning of one character row of data, which is preferably 16 horizontal lines.

The output of the recirculation registers **56** of the text memory portion **14** is connected to a conventional character generator **58** contained in the display portion **16**. The output of the character generator **58** is connected to a conventional output register **60** whose output is in turn connected to an output gating network which preferably includes a pair of AND gates **62** and **64** connected in parallel, one AND gate being provided for each channel, AND gates **62** and **64** being connected to an enable text signal generator **66**. The output of AND gate **62** is connected to a three input OR gate **68**. The other two inputs to OR gate **68** are provided from a pair of AND gates **70** and **72**, AND gate **70** being associated with the ticker character generation portion **20** output and AND gate **72** being associated with the scroll character generation portion **26** output, as will be described in greater detail hereinafter. The output of OR gate **68** is connected to a conventional video mixer **74** which is also connected to a sync signal generator **76** in order to provide a composite video signal which may be transmitted to a conventional television display **78** in order to provide a plural display of the text, ticker and scroll information, as will be described in greater detail hereinafter. Similarly, AND gate **64** associated with channel B, has its output connected to another three input OR gate **80** whose other two inputs are provided by a pair of AND gates **82** and **84**, AND gate **82** being associated with the scroll character generation portion **26** and AND gate

84 being associated with the ticker character generation portion **20.** The output of OR gate **80** is similarly connected to another conventional video mixer **86** which also has a sync signal generator **88** connected thereto in order to provide a composite video signal on channel B to a separate conventional television display device **90,** as will be described in greater detail hereinafter.

Now, generally describing the ticker number **1** input buffer portion **18,** the functional diagram except for the associated timing signals and input information signals, being preferably identical with that of the ticker number **2** input buffer portion **22** and the scroll input buffer portion **24,** the same reference numerals therefore being utilized for functionally identical components followed by the letters *a* and *b*, respectively, for input buffer portions **22** and **24.** The ticker number **1** input buffer portion **18** preferably includes a resynchronizer **92** connected to the ticker number **1** input **94.** The input **94** further being connected in parallel to an input register **96.** The output of the resynchronizer **92** is connected to the clock terminal of the input register **96** in the same manner as described with reference to a similar connection in the text input buffer portion **12.** The output of the input register **96** is connected to a character detector **98** which senses the start bit of the input signal, and to a storage register **100.** The output of the character detector is connected to a space detector **102** which, as will be described in greater detail hereinafter, has its output connected to a motion control network **104** so as to enable movement of the ticker character display across the video display screen of the display devices **78** and **90** in a smooth manner. The character detector circuit **98** via the space detector network **102** is connected to the transfer terminal of the storage register **100** to enable the loading of data, the output of the storage register **100** being connected to the space detector **102.** The output of the motion control network **104** is connected in parallel to the ticker number **1** input buffer memory **106,** which is preferably a six by 32 bit memory which is enabled by an enable ticker number **1** output signal **108,** and to the ticker character generation portion **20.**

The ticker character generation portion **20** includes a character generation **110** whose output is connected to an output register **112** which output, in turn, is connected to position gating circuitry **114,** to be described in greater detail hereinafter, the position gating network **114** being responsible for the movement of the ticker character display across the screen. The motion control **104** is connected to the position gating network **114** via an OR gate **116** which is provided with another input from the motion control **104***a* of the ticker number **2** input buffer portion **22.** The output of the position gating network **114** of the ticker character generation portion **20** is connected to AND gates **70** and **84** of the display portion **16.** The character generator **110** of the ticker character generation portion **20** is connected in parallel to the output of the memories **106** and **106***a* of the ticker number **1** input buffer portion **18** and the ticker number **2** input buffer portion **22,** respectively. In addition, the output of the "stocks 15 min. delay" message generator **28** is also connected in parallel with the memory **106** and **106***a* outputs to the character generator **110** of the ticker character generation portion **20.**

The functional description of the scroll input buffer portion **24,** as was previously mentioned, is identical with that previously described with reference to the ticker number **1** input buffer portion **18,** except that in place of the enable ticker number **1** output signal generator **108** there is an enable scroll signal generator **118,** the balance of the function diagram being identical except that in place of the ticker number **1** input **94** there is a scroll input **120** and, in the ticker number **2** input buffer portion **22,** in place of the ticker number **1** input **94** there is a ticker number **2** input **121.** Similarly, the functional portions of the scroll character generator portion **26** are identical with that previously described with reference to the ticker character generation portion **20,** the scroll character generation portion **26** including a character generator **122** whose output is connected to an output register **124** whose output is, in turn, connected to position gating network **126.** The motion control network **104***b* of the scroll input buffer portion **24** has its output connected also to the position gating network **126.** In addition, the output of the memory **106***b* of the scroll input buffer portion **24** is connected to the input of the character generator **122** of the scroll character generation portion **126.** The output of the position gating network **126** of the scroll character generation portion **26** is connected in parallel to AND gates **72** and **82** of display portion **16.**

TICKER NUMBER 1 INPUT BUFFER PORTION

Referring now to FIG. **2** and describing the ticker number **1** input buffer portion **18** in greater detail. As was previously mentioned, the ticker number **2** input buffer portion **22** and the scroll input buffer portion **24** are preferably identical in structure and operation, the only differences being in the nature of the input signal processed through the corresponding input buffer portion and the associated timing signals necessary to process this input signal. However, as will be explained in greater detail hereinafter, the ticker character generation portion **20** and the scroll character generation portion **26** provide different types of output signals through the display portion **16,** the ticker signal, whether it be from the ticker number **1** input buffer portion **18** or the ticker number **2** input buffer portion **22** ultimately providing a display of associated ticker information which is preferably sixteen lines high, the first eight lines being for display of the letter relating to the stock symbol, the bottom eight lines being for the display of alphanumeric characters associated with the symbol, and the bottom ten of these lines being for display of fraction characters associated with this symbol. The scroll character generation portion **26** ultimately provides a scroll display which is preferably only eight lines high. However, for purposes of explanation, since the circuitry associated with the input buffer portions **18, 22** and **24** are essentially the same, by way of example, only the associated circuitry of the ticker number **1** input buffer portion **18** will be described in greater detail hereinafter.

The ticker number input buffer portion **18,** as will be explained in greater detail hereinafter, receives the ticker number **1** input **94** from any conventional source of such information, such as a remote computer, teletype, or keyboard, the ticker number **1** input preferably being a conventional ticker code which is a nine unit code comprising a start bit, six information bits and two

stop marks, this code being similar to a teletype code. This ticker number 1 input **94** is normally at EIA compatible voltage levels and is, therefore, preferably fed through a conventional level changer **130** which changes the EIA compatible voltage level input to TTL compatible levels in a conventional manner. The output of this level changer **130** is connected in parallel to resynchronizer **92** and to the data input of input register **96** which is preferably an eight bit input register. As was previously mentioned, the output of the resynchronizer **92** is connected to the clock terminal of the input register **96.** The resynchronizer **92** also preferably receives a clock input via path **132,** the clock input preferably being sixteen times the frequency of the ticker input **94.** The resynchronizer **92,** which is preferably a conventional resynchronizer which functions in a conventional manner, resynchronizing on the leading edge of each new space pulse to insure center sampling of the input pulses and to minimize spurious noise pulses, may be any conventional type, such as one comprising a flip-flop arrangement connected in a conventional fashion to a divide-by-16 counter, which counter receives the clock input **132** such as through an inverter.

The eight bit input register **96** is preferably connected to the storage register **100** to provide a parallel transfer thereto. Preferably, one of the stages of the eight bit input register **96** is also connected in parallel to the conventional character detector circuit **98** which, as will be explained in greater detail hereinafter, senses the start bit. This character detector **98** may be any conventional character detector circuit such as one comprising a flip-flop network. As will be explained in greater detail hereinafter, the character detector **98** receives timing signals VB3 via path **134** and SDET via path **136** from the basic timing chain to be described in greater detail with reference to FIG. **7,** and from the space detector **102** associated with the input buffer portion **18,** respectively. The character detector **98** is connected to the clear-reset terminal of the input register **96** via path **138** so as to provide a reset pulse thereto. In addition, the character detector is connected to the load terminal of the storage register **100** via path **140.** The space detector **102** is preferably a conventional type of space detector network comprising a flip-flop **142,** and receives timing input signals VB2 and C6 from the basic timing chain (FIG. **7**). The data input terminal of the flip-flop **142** is preferably connected to the output of an OR gate **144** which has one input connected in a feedback path to the output of the flip-flop **142** and the other input connected to the motion control network **104** to be described in greater detail hereinafter.

The output of the storage register **100,** which conventional storage register **100** preferably comprises six four-bit-recirculation memories, one for each output bit, is connected to memory **106** so as to preferably supply a parallel transfer of data thereto. Memory **106** also preferably comprises six thirty-two-bit-recirculation memories. As will be explained in greater detail hereinafter, memory **106** preferably is connected to the motion control network **104** so as to receive transfer pulses labeled XFER and $\overline{\text{XFER}}$ via paths **146** and **148.** The output of memory **106,** is preferably also a parallel transfer of data, each of the six parallel transfer bits being connected as an input to an associated two input NAND gate **150, 152, 154, 156, 158** and **160.** These NAND gates **150** through **160** inclusive preferably have the other input thereto connected in parallel to a conventional enable ticker number 1 generator **108** (FIG. 7) to receive an enabling pulse therefrom via path **866** in order to provide a parallel transfer of ticker bits TKB1, TKB2, TKB3, TKB4, TKB5 and TKB6 via paths **162, 164, 166, 168, 170** and **172** respectively, to the ticker character generation portion **20** which will be described in greater detail hereinafter.

Now describing the motion control network **104** of the ticker number 1 input buffer portion **18,** the motion control network **104** providing a character incrementing function, as will be described in greater detail hereinafter in the discussion of the operation of the input buffer portion **18.** As will be described in greater detail hereinafter, the motion control network **104** cooperates with the position gating network **114** of the ticker character generation portion **20** to control the movement or motion of the resultant ticker display across the video display screen. The resultant motion is dependent on the rate of loading the data into the storage register **100;** that is, whether 1, 2, 3 or 4 bits of data are loaded into the storage register **100** for a given associated bit, before the associated recirculating memory is able to transfer the data from the storage register to the memory **106.** The motion control network **104** preferably includes a motion control register **174,** which is preferably a conventional four bit register, and an output motion control counter **176,** which is preferably a conventional divide-by-12 counter, and associated gating circuitry so as to provide the appropriate control signals to the position gating network **114** in order to control the motion of the ticker display. The C6 timing pulse provided from the basic timing chain shown in FIG. **7** is fed via path **178** through an inverter **180** to one input of a NAND gate **182** whose other input is the transfer pulse $\overline{\text{XFER}}$ which is also fed via path **148** to the memory **106.** The output of the NAND gate **182** is connected in parallel to a pair of NAND gates **184** and **186** which also have their other inputs connected in parallel to a clock input CK provided via path **188** from a conventional clock generator as shown in FIG. **7.**

The output of NAND gate **186** is connected to the clock terminal of the motion control register **174.** The data input terminal of the motion control register **174** is connected to the output of a two input NOR gate **190,** one input of which is the transfer pulse XFER which is also provided via path **146** to the memory **106.** The output of the motion control register **174** preferably comprises four parallel bits Q0, Q1, Q2, Q3 and, in addition, the complement of Q3 which is $\overline{\text{Q3}}$, provided via paths **192, 194, 196, 198** and **200,** respectively. The Q3 output bit via path **198** is connected in parallel to one input of a two input OR gate **202,** the outer input of gate **202** being a timing signal LC (load character) via path **204.** The output of OR gate **202** is provided in parallel as one input to OR gate **144** of space detector **102** via path **206,** and as an input to NOR gate **190** via path **208.** The output of OR gate **202** via path **208** is also provided in parallel to the preset input of a flip-flop **210** whose output in the set state is $\overline{\text{S1}}$ via path **212.** The inputs to the flip-flop **210,** as will be described in greater detail hereinafter, are provided from the output motion control counter **176.**

The Q0 bit via path **192** from motion control register **174** is provided as an input to an AND gate **214** whose output is connected to one input of a two input NOR gate **216.** The Q1 output bit of motion control register **174** via path **194** is provided as an input to another AND gate **218** whose output is connected to the other input of the NOR gate **216.** The output of NOR gate **260** is connected to the data input terminal of a flip-flop **220** which provides an output S4 via path **222** in the $\overline{Q}$ state. The output in the $\overline{Q}$ state is also provided via a feedback path **224** as an input to AND gate **218.** The Q state output of flip-flop **220** is connected via path **226** to the clock input of a flip-flop **228.**

The input to the data terminal of the flip-flop **228** is connected to the output of a two input NOR gate **230,** one input to NOR gate **230** being connected to the output of an AND gate **232,** the other input to the NOR gate **230** being connected to the output of AND gate **234.** The Q1 output bit of motion control register **174** bia path **194** is provided as an input to AND gate **232** and the Q2 output bit of motion control register **174** via path **196** is provided as an input to AND gate **234.** The $\overline{Q}$ state output of flip-flop **228** is a pulse S3 via path **236.** The $\overline{Q}$ state output is also connected via a feedback path **238** to an input to AND gate **234.** The Q state output of flip-flop **228** is connected via a path **240** to the clock terminal input of another flip-flop **242** whose $\overline{Q}$ state output is a pulse S2 via path **244.** The data input terminal of flip-flop **242** is connected to the output of a two input OR gate **246.** One input to OR gate **246** is the Q2 output bit from the motion control register **174** via path **196,** while the other input to OR gate **246** is connected to the output of a two input NOR gate **248.** One input to NOR gate **248** is the $\overline{Q3}$ output bit of motion control register **174** provided via path **200** while the other input to NOR gate **248** is connected to the Q state output of flip-flop **242** via path **250.** The signal $\overline{C6}$ provided from the basic timing chain of FIG. **7,** to be described in greater detail hereinafter, is connected in parallel as an input to flip-flops **220, 228** and **242** via path **178.**

Now describing the gating circuitry associated with the output motion control counter **176.** Another timing signal $\overline{C2}$ provided from the basic timing chain shown in FIG. **7** via path **254** is connected through an inverter **256** to one input of a two input NOR gate **258.** The other input to NOR gate **258** is the $\overline{S1}$ output of flip-flop **210** via path **212.** The output of NOR gate **258** is connected through one input of a two input AND gate **260** whose output is connected to one input of a four input NOR gate **262.** The other input to AND gate **260** is connected to the C1 timing signal output via path **264** of the basic timing chain shown in FIG. **7.** This signal is connected in parallel to one input of another AND gate **266,** the output of AND gate **266** being connected to a different input to NOR gate **262.** The other input to AND gate **266** is connected to the S3 output of flip-flop **228** via path **236.** A third input to NOR gate **262** is connected to the output of another two input AND gate **268** whose inputs are a timing signal $\overline{C2}$ provided from the basic timing chain shown in FIG. **7** via path **270,** and the S2 output of flip-flop **242** provided via path **244.** The fourth input of NOR gate **262** is connected to the output of another AND gate **272** whose input is connected to the S4 output of flip-flop **220** via path **222.** The output of NOR gate **262** is connected to one input of a two input NOR gate **274** whose other input is a timing signal delay clock ($\overline{DCK}$) supplied from the output of a conventional timing generator **852** shown in FIG. **7** via path **276.** The output of NOR gate **274** is connected to an input to the output motion control counter **176.**

The outputs of the output motion control counter **176** are parallel signals **D1, D2, D3** and **D4** provided via paths **278, 280, 282** and **284,** respectively. As will be explained in greater detail hereinafter, the D1 output via path **278** represents the output of the most rapid moving stage of counter **176** and the D4 output of counter **176** via path **284** represents the slowest moving stage of the counter **176.** The D1 output via path **278** is connected in parallel to one input of an NAND gate **286** and to associated circuitry, such as flip-flop **210,** via path **288.** The D2 output via path **280** is connected as one input to another NAND gate **290.** The D3 output via path **282** is connected in parallel to one input to another NAND gate **292** and to one input of another NAND gate **294** via path **296.** The D4 output via path **284** is connected in parallel to one input of a two input NAND gate **298** and to the other input of NAND gate **294** via path **300.** The other inputs of NAND gates **286, 290, 292** and **298** are connected in parallel to the output of an NOR gate **302** whose inputs, for purposes of ticker display, are timing signal $\overline{R2^2}$ amd $R2^1$ which are provided from the basic timing chain of FIG. **7** via paths **304** and **306** to provide an enable signal to gates **286, 290, 292** and **298.** The outputs of gates **286, 290, 292** and **298** are the complemeents $\overline{D1}$, $\overline{D2}$, $\overline{D3}$ and $\overline{D4}$ of the respective inputs D1, D2, D3 and D4 provided via paths **291, 293, 295** and **297,** respectively. When the network shown in FIG. **2** is utilized as a scroll input buffer, terminals **304** and **306** are grounded as shown by the dotted lines.

The D4 output via path **284** is also connected through an inverter **308** to a flip-flop **310.** The Q state output terminal of flip-flop **310** is connected to the data input terminal of another flip-flop **312** which receives the timing signal C6 from the basic timing chain of FIG. **7** as another input thereto. The $\overline{Q}$ state output terminal of flip-flop **312** is connected in parallel to the data terminal and clock terminal of flip-flop **310** to provide the transfer output pulse $\overline{XFER}$ via path **148.** The Q state output terminal of flip-flop **312** provides the transfer pulse XFER via path **146.** The timing signal $\overline{C1}$ provided from the basic timing chain of FIG. **7** via path **264** is connected in parallel through an inverter **314** to provide timing output signal $C1^1$ via path **316,** and to the clear input terminal of flip-flop **312.**

The motion control circuitry **104** is also connected to the storage register **100** to provide a transfer pulse thereto. The transfer pulse XFER provided via path **146** is connected to one input of a two input OR gate **320** whose output is connected via path **322** to the transfer input of storage register **100.** The other input to OR gate **320** is the enable load data (ELD) output signal from character detector **98** via path **140.** This signal via path **140** is fed through an inverter **324** to the input of OR gate **320** and also provides the signal LC (load character) via path **204** to OR gate **202.** The ELD signal via path **140** is also connected in parallel to one input of a two input NOR gate **326** whose output via path **328** is also connected to the transfer input of the storage register **100.** The other input to NOR gate **326** is connected to the output of another two input NOR gate **330.** One input to NOR gate **330** is con-

nected to timing signal TKE (ticker enable) via path **332,** which signal is preferably grounded when this input buffer network is utilized as a scroll input buffer, as shown by the dotted lines. The signal TKE (ticker enable) via path **332** is also connected in parallel to an inverter **334** whose output is the complement thereof $\overline{TKE}$ via path **336.** The other input to NOR gate **330** is connected to the output of an NAND gate **338** whose two inputs are two of the seven parallel bits provided as the output of input register **96,** preferably the sixth and seventh bits.

TICKER CHARACTER GENERATION PORTION

Now referring to FIG. **3** and describing the ticker character generation portion **20** in greater detail. As was previously mentioned, the circuitry associated with the ticker character generation portion **20** is preferably identical with that associated with the scroll character generation portion **26** with the exception of the type of signal input and the various timing signals utilized to control the processing of the signal through the character generation circuitry. In addition, the character generator **122** utilized for scroll character generation preferably differs from the character generator **110** utilized for ticker character generation in that the scroll character generator **122** is preferably not programmed to provide fraction characters, although, if desired, this could also be accomplished. As will be explained in a more detailed description of the operation of the system of the present invention, and as was previously mentioned, the timing signals associated with the scroll character generation portion **26** as compared to those associated with the ticker character generation portion **20** are such as to provide only eight horizontal scan lines for a scroll character space as opposed to sixteen horizontal scan lines for a ticker character space. Since, however, the ticker character generation portion **20** and the scroll character generation portion **26** are preferably identical but for the exceptions mentioned above, only the ticker character generation portion will be described in greater detail hereinafter.

The character generator portion **110** of the ticker character generation portion **20** is preferably a conventional character generator such as a read only memory (ROM) preprogrammed for a desired character generation function. Preferably, the character generator **110** is capable of generating both alphanumeric characters and fractions in response to the ticker bit outputs of memory **106** via paths **162, 164, 166, 168, 170** and **172** in the horizontal line scan signals. If desired, the conventional character generator could be a single metal-oxide semiconductor (MOS) read only memory chip preprogrammed for these functions, a pair of MOS read only memory chips wherein one is preprogrammed for alphanumeric characters and the other for fraction characters, or a single read only memory (MOS) chip which is preoprogrammed for alphanumeric characters in conjunction with supplementary TTL logic in order to generate the necessary fractions which are outside the range of the preprogrammed MOS chip. The horizontal line scan timing signals which are utilized to interrogate the read only memory character generator **110** in conjunction with the ticker bit input signal via paths **162** through **172** are provided from the basic timing chain of FIG. **7** in a manner to be described in greater detail hereinafter. Suffice it to say at this point that in response to these interrogation signals the character generator **110** provides an appropriate output character via a parallel transfer into the conventional output register **112** which is preferably a two stage register.

The output register is connected to a master oscillator associated with the basic timing chain of FIG. **7** via path **340** so that the register **112** will shift at the video dot frequency provided by the oscillator, as will be described in greater detail hereinafter. The output register **112** is also provided with a transfer pulse $\overline{XFERTK}$ via path **342** from an OUTPUT REGISTER-OUTPUT TRANSFER PORTION **344,** which will be described in greater detail hereinafter. Transfer pulse $\overline{XFERTK}$ permits the parallel loading of the output register **112** from the character generator **110.** The output of the output register **112** is transferred in parallel to the position gating network **114.** Oscillator timing pulse OSC via path **340** is also passed through an inverter **344** to provide a timing pulse $\overline{OSCT}$ which is the complement thereof via path **346.** One of the parallel output bits from output register **112** is connected via path **348** to one input of a two input NAND gate **350,** the other input to gate **350** being an enable delay output signal (EDO) provided via path **352** from a conventional timing generator **354** shown in FIG. **7,** and omitted from this figure for purposes of clarity. As will be described in greater detail hereinafter, the output of gate **350** is a timing signal delay output ($\overline{DO}$) via path **356** which signal enables a black on white display of the message (STOCK 15 MIN. DELAY) on the video display screen instead of the normal white on black display which is preferably provided for the ticker information.

Another parallel bit output of output register **112** is provided via path **358** to one input of a two input AND gate **360** whose output is provided as one input to a NOR gate **362.** The other input to NOR gate **362** is connected to the output of another two input AND gate **364** which has one input connected to another one of the parallel bit outputs of output register **112** via path **366.** The other input to AND gate **364** is connected in parallel to one input of another two input AND gate **368** whose other input is connected to another one of the parallel bit outputs of output register **112** via path **370.** The output of AND gate **368** is connected to one input of a two input NOR gate **372** whose other input is connected to the output of another AND gate **374.** One input of AND gate **374** is connected to another parallel bit output of output register **112** via path **376** and the other input to gate **374** is connected in parallel to one input of AND gate **360.**

Another one of the parallel bit outputs of output register **112** is connected to one input of another two input NAND gate **378** via path **380,** the other input to NAND gate **378** being connected in parallel to one input of another two input NAND gate **382.** The other input to NAND gate **382** is connected to another parallel bit output of output register **112** via path **384.** The parallel connected inputs of AND gates **364** and **368** are connected in parallel via path **386** to the output of an inverter **388** whose input is connected to the $\overline{D2}$ output associated with the output motion control counter **176** via path **293.** The parallel connected inputs of AND gates **360** and **374** are connected in parallel via path **390** to the output of an inverter **392** whose input is the $\overline{D3}$ output associated with output motion control counter **176** via path **295.** The outputs of inverters **388** and **392** are also connected in parallel to the inputs of

a two input NOR gate **394** whose output is connected in parallel to one input of NAND gates **378** and **382** via path **396.** The output of NOR gate **372** and the output of NAND gate **382** are respectively connected to the input of a two input OR gate **398** whose output is connected to the input of a two input AND gate **400.** The other input to AND gate **400** is connected to the $\overline{D4}$ output associated with motion control counter **176** via path **297,** this $\overline{D4}$ output being connected in parallel to the input of an inverter **402.**

The output of inverter **402** is connected to one input of a two input AND gate **404,** the other input to AND gate **404** being connected to the output of a two input OR gate **406.** The two inputs of OR gate **406** are connected to the outputs of NOR gate **362** and NAND gate **378,** respectively. The outputs of AND gates **400** and **404** are connected to the inputs of a two input NOR gate **408** whose output is connected in parallel to the data input terminal of a pair of flip-flops **410** and **412,** respectively. The clock terminal of flip-flop **410** is connected to the oscillator timing signal OSC via path **340,** and the clock terminal of flip-flop **412** is connected to the $\overline{OSCT}$ timing signal output of inverter **344** via path **346.** The $\overline{Q}$ state output of flip-flop **410** is connected to one input of a two input AND gate **414** and the $\overline{Q}$ state output of flip-flop **412** is connected to one input of another two input AND gate **416.**

The $\overline{D1}$ output associated with output motion control counter **176** via path **291** and the enable delay output signal (EDO) via path **352** of timing generator **354** (FIG. 7) are connected to the inputs of a two input NOR gate **418** whose output is a timing signal $D1^1$ via path **240** which is connected in parallel to one input of a two input NOR gate **422.** The other input to NOR gate **422** is connected in parallel to the EDO input to NOR gate **418,** the output of NOR gate **422** being a timing signal $\overline{D1}'$ via path **424.** Timing signal $D1^1$via path **420** is provided as the other input to AND gate **416** and timing signal $\overline{D1}'$ via path **424** is provided as the other input to AND gate **414.** The output of AND gates **416** and **414** are connected to the inputs of a two input NOR gate **426** whose output is connected to one input of a two input OR gate **428.** The other input to OR gate **428** is the timing signal $\overline{DO}$ via path **356** provided from NAND gate **350.** The output of OR gate **428** is connected to one input of the two input NAND gate **430** which provide a ticker position gating output signal TICKER to the display portion **16** via path **432.** The other input to NAND gate **430** is connected to a portion of the position gating network referred to as the position gating-horizontal blanking portion or window generation circuit **434.**

This horizontal blanking portion **434,** as will be described in greater detail hereinafter, provides a window which is thirty one characters long in order to provide a display of this length in this window. More particularly, the other input to NAND gate **430** is connected to the $\overline{Q}$ state output of a flip-flop **436** whose Q state output is connected to one input of a two input NAND gate **438,** the other input to NAND gate **438** being connected to the $\overline{C1}$ timing signal generated from the basic timing chain of FIG. 7 via path **264.** The output of NAND gate **438** is connected to one input of a two input OR gate **440** whose other input is connected to the $\overline{C6}$ output of the basic timing chain of FIG. 7 via path **178** and whose output is connected to the data input terminal of flip-flop **436.** Flip-flop **436** is connected to the output register-output transfer portion **344.** More particularly, flip-flop **436** is connected in parallel to the $\overline{Q}$ state output of a flip-flop **442** associated with the output transfer portion **344** and to the data input terminal of flip-flop **442,** the $\overline{Q}$ state output of flip-flop **442** being the transfer pulse $\overline{XFERTK}$ via path **342.** The output of an NOR gate **444** is also connected to the flip-flop **442,** the input to NOR gate **444** being connected to the timing signal output $\overline{VB3}$ of the basic timing chain of FIG. 7 via path **446.** The clock terminal of flip-flop **442** is connected to the timing signal output $\overline{VB1}$ of the basic timing chain of FIG. 7 via path **448.**

TEXT INPUT BUFFER PORTION

For purposes of clarity, before describing the display portion **16** in greater detail, the balance of the circuitry associated with providing the signal to the display portion **16** will now be described. Referring now to FIG. **4** and describing the text input buffer portion **12** in greater detail. The text line input via path **30,** which may be provided from a remotely located computer, keyboard, or teletype type of device, or any other conventional type of information input device, is connected to the input of a conventional level changer **450** which is capable of changing EIA compatible voltage levels to TTL compatible voltage levels. The output of level changer **450** is connected to one input of a two input AND gate **452** whose other input is connected to the enable line output signal $\overline{ELINE}$ provided via path **454** from a function decoder **456** of the function decoder network **48.** The output of AND gate **452** is connected to one input of a two input OR gate **458,** the other input to OR gate **458** being connected to the output of another two input AND gate **460.** One input to AND gate **460** is connected to the enable line output signal ELINE provided via path **462** from function decoder **456,** and the other input to AND gate **460** is connected to the output of another conventional level changer **464** capable of changing EIA compatible voltage levels to TTL compatible voltage levels. The input to level changer **464** is connected to the auxiliary line input AUX. LINE INPUT provided via path **32.**

The output of OR gate **458** is connected in parallel to conventional resynchronizer **40** and to the data input of input register **42,** which is preferably an eight bit input register. The output of resynchronizer **40,** as was previously mentioned, is preferably connected to the clock input terminal of input register **42.** The resynchronizer **40** is connected to the conventional clock signal generator shown in FIG. 7 via path **132,** the clock signal preferably being **16** times the input rate of the text line input signal provided via path **30** or the auxiliary line input signal provided via path **32.** Resynchronizer **40** is connected to the $\overline{C4}$ timing signal provided from the basic timing chain of FIG. 7 via path **466.** The input register **42** is connected to a conventional character detector **44** and to the storage register **46** in a manner similar to that previously described with reference to the interconnection of input register **96,** character detector **98** and storage register **100** of the ticker number **1** input buffer portion **18.** The input register **42** preferably provides a parallel output, character detector **44** preferably being connected to one of the parallel output bits of input register **42** to sense the occurrence of a start bit.

The character detector 44 is connected to the transfer terminal input of storage register 46 so as to cause a parallel transfer of the data present in input register 42 when the start bit is detected. In addition, the character detector 44 is connected to the clear-reset terminal of input register 42 via path 468 to provide a reset pulse RIR to the input register 42 after the transfer of the data from the input register 42 to the storage register 46. The character detector 44 is connected to the basic timing chain of FIG. 7 to receive timing pulses $\overline{C1}$ and $\overline{VB3}$ via paths 264 and 446, respectively. The character detector 44 operates in a conventional manner to sense the bits transferred to the storage register 46 to determine if the character is a displayable character in which instance an enable load data signal ELD will be sent via path 470 to address decoder 472, a displayable character being defined as one of the 64 ASCII characters including space plus the graph and fraction characters. If the character detected by the character detector 44 is not a displayable character, but rather is a control character such as line feed (LF), carriage return (CR), or start of text (STX), then the control signal CONT or $\overline{CONT}$ will be provided from the character detector 44 via paths 472 and 474, respectively.

Storage register 46 preferably provides a parallel output which is illustrated by parallel bits B1, B2, B3, B4, B5, B6 and B7 via paths 476, 478, 480, 482, 484, 486 and 488, respectively. The parallel output provided via paths 476 through 486 inclusive provides a parallel input to address decoding matrices A, B and Z, 490, 492 and 494, respectively. As will be described in greater detail hereinafter, these decoding matrices are conventional decoding matrices which provide a conventional output control pulse in response to the decoding of a given selected input signal code. For purposes of illustration, decoding matrix 490 is associated with channel 1 or A for video display device 78, decoding matrix 492 is associated with channel 2 or B for video display device 90 and decoding matrix 494 is associated with both devices 78 and 90 to simultaneously turn them both on, as opposed to only turning on one channel. Decoding matrices 490, 492 and 494 are connected in parallel to the enable load data signal output ELD provided via path 470 from character detector 44 and to an enable load header signal output ELH provided via path 496 from a function decoder 498 of function decoder network 48.

The output of decoding matrix 490 is connected to the input of a flip-flop 500 whose output is connectecd in parallel to one input of a pair of two input NOR gates 502 and 504 associated with the address decoder network 50. The other input to NOR gate 504 is a clear pulse $\overline{CL}$ provided via path 506 from a function decoder 508 of the function decoder network 48. Another input to NOR gate 502 is connected to the output of a three input NAND gate 510 whose inputs are a coincidence pulse COIN provided via path 512 from the conventional coincidence circuit 514 shown in FIG. 7, the enable load data pulse ELD provided via path 470 and the enable load header pulse $\overline{ELH}$ provided via path 516 from function decoder 498. The output of NOR gate 502, which is the load data signal LD1, is connected in parallel to the load input terminal of memory 52 via path 518 and to one input of a two input OR gate 520, the other input to OR gate 520 being connected to the output of NOR gate 504. The output of OR gate 520 is a clear plus $\overline{CL1}$ provided via path 522 to the clear terminal of memory 52. The output of NAND gate 510 is also connected in parallel to one input of a two input NOR gate 524.

Decoding matrix 492 has its output connected to a flip-flop 526 whose output is in turn connected in parallel to the other input of NOR gate 524 and to one input of another two input NOR gate 528. The other input to NOR gate 528 is the clear pulse $\overline{CL}$ provided via path 506. The output of NOR gate 528 is connected to one input of an OR gate 530. The output of NOR gate 524 is connected in parallel to the other input of OR gate 530 and to the load data terminal of memory 54 to provide a load data signal LD2 via path 532. The output of OR gate 530 is connected to the clear terminal of memory 54 to provide a clear pulse $\overline{CL2}$ via path 534 to memory 54. Control signals start of header ($\overline{SOH}$) and end of text (ETX) provided via path 536 from function decoder 498 are connected in parallel to flip-flops 500 and 526. Decoding matrix 494 is connected in parallel to flip-flops 500 and 526 for simultaneously controlling the operation of these flip-flop upon the decoding of the appropriate input signal.

The control signal inputs, as will be explained in greater detail hereinafter, are detected by means of the function decoder network 48 comprising function decoders 456, 498, 508, 538, 540, 542 and 544. By way of example, and not limitation, various parallel output bits from storage register 46 are illustrated as providing the various control vunction inputs to the function decoder network 48. Now describing function decoder 498. The parallel output bits provided via paths 480, 482 and 484 from storage register 46 are connected to the inputs of a three input NAND gate 546 whose output is connected to one input of a two input NOR gate 548. The othe input to NOR gate 548 is the control pulse output $\overline{CONT}$ from character detector 44 via path 474. The output of NOR gate 548 is connected in parallel to one input of a pair of two input NAND gates 550 and 552, respectively. The other input to NAND gate 550 is connected to parallel bit outputs 476 and 478 of storage register 46, and the other input to NAND gate 552 is connected to parallel output bit 476 of storage register 46. The output of NAND gate 550 is connected in parallel to function decoder 508 to provide a start of text signal ($\overline{STX}$) via path 554, and to the input to a flip-flop 556 which provides the enable load header signal $\overline{ELH}$ via path 516 in one state, and the enable load header signal ELH via path 496 in the other state. The output of NAND gate 552 is connected in parallel to flip-flop 500 to provide the start of header ($\overline{SOH}$) and end of text ($\overline{ETX}$) signals thereto via path 536, and to flip-flop 556.

Now describing function decoder 544. Parallel output bits 480, 482 and 484 from storage register 46 are connected to the inputs of a three input NAND gate 558 whose output is connected to one input of a two input NOR gate 560. The other input to NOR gate 560 is connected to the control pulse output $\overline{CONT}$ of character detector 44 via path 474. The output of NOR gate 560 is connected to an input of NAND gate 562 whose other input is connected to parallel output bits 476 and 478. The output of NAND gate 562 is a tape control signal $\overline{TAPE}$ provided via path 564 to function decoder 456.

Now describing function decoder 542. An output coincidence signal $\overline{COIN}$ provided via path 512 from coincidence circuit 514 is connected in parallel to the

input of an inverter **566** to provide the complement thereof, the coincidence signal COIN, and to one input of a two input OR gate **568.** The other input to OR gate **568** is connected to the enable load header signal output $\overline{ELH}$ of function decoder **498** via path **516.** The output of OR gate **568** is connected to one input of a two input NAND gate **570** whose other input is connected to the enable load data output ELD of character detector **44** via path **470.** The output of NAND gate **570** is connected to the data input terminal of a flip-flop **572.** The timing signal $\overline{VB3}$ from the basic timing chain of FIG. 7 is also connected to the flip-flop **572** via path **446.** In addition, the preset terminal of flip-flop **572** is connected to a master oscillator shown in FIG. 7 via path **340.** The output of flip-flop **572** in the Q state is the advance control pulse $\overline{ADV}$ provided via path **574** to function decoders **508** and **540** and, as will be described in greater detail hereinafter, to a cursor character counter **576** (FIG. 7).

Now describing function decoder **508.** The advance control pulse $\overline{ADV}$ provided via path **574** from function decoder **542,** and the enable load header pulse ELH via path **496** from function decoder **498,** are connected to the inputs of a two input NOR gate **580** whose output is connected to a flip-flop **582.** The timing signal C6 via path **252** is provided to flip-flop **582** from the basic timing chain of FIG. **7.** The output of flip-flop **582** is connected to one input of a two input OR gate **584** whose output is the clear pulse $\overline{CL}$ provided via path **506.** The other input of OR gate **584** is connected to the Q state output of a flip-flop **586.** The $\overline{Q}$ state output of flip-flop **586** is connected to the input of another flip-flop **588** whose output is connected to the data input terminal of flip-flop **586.** A timing signal $\overline{R2^0}$ is provided from the basic timing chain of FIG. 7 to flip-flop **586** via path **590.** Flip-flop **588** is also connected to the start of text ($\overline{STX}$) output of NAND gate **550** of function decoder **498** via path **554.**

Now describing function decoder **538.** Control signal CONT from character detector **44** via path **472** and parallel output bits **482** and **484** of storage register **46** are connected to the input of a three input NAND gate **592** whose output is connected in parallel to one input or NOR gates **594** and **596.** The other inputs to NOR gates **594** and **596** are connected to parallel output bit **480** of storage register **46.** The output of NOR gate **594** is connected in parallel to one input of NAND gates **598, 600** and **602.** The other inputs to NAND gate **598** are parallel output bits **476** and **478.** The output of NAND gate **598** is the control pulse or character carriage return $\overline{CR}$ provided via path **604** from function decoder **538.** The other inputs to NAND gate **600** are also parallel output bits **476** and **478,** more particularly the compliments thereof. The output of NAND gate **600** is the control character shift in $\overline{SI}$ provided via path **606** from function decoder **538.** The other input to NAND gate **602** is parallel output bits **476** and **478,** NAND gate **602** providing the control character shift out $\overline{SO}$ via path **608** from function decoder **538.** This input of NAND gate **602** is connected in parallel to one input of another NAND gate **610,** this input being connected to the output of an NOR gate **612** whose input is the parallel output bits **476** and **478,** from which the input to NAND gates **602** and **610** is derived. Another input to NAND gate **610** is connected to the output of NOR gate **596** which is also connected in parallel to one input of a three input NAND gate **614.** The output of NAND gate **610** is connected to the input of an inverter **616** whose output is the control character line feed LF provided via path **618** from function decoder **538.** The other inputs to NAND gate **614** are parallel output bits **476** and **478.** The output of NAND gate **614** is the control character tab $\overline{TAB}$ provided via path **620** from function decoder **538.**

Now describing function decoder **540.** The shift out $\overline{SO}$ character output of function deocder **538** via path **608** is connected in parallel to the data input terminal of a flip-flop **622** and to the input of an inverter **624** whose output is connected to another flip-flop **626.** The control signal $\overline{CONT}$ output of character detector **44** via path **474** is connected in parallel to flip-flop **622** and to another flip-flop **628.** The $\overline{Q}$ state output of flip-flop **622** is connected to the data input terminal of flip-flop **626** and the Q state output terminal of flip-flop **626** is connected to the input of an inverter **630** whose output is the control character enable shift out $\overline{ESO}$ which is preferably provided to an external device for control thereof via path **632** from function decoder **540.** The preset terminals of flip-flop **622** and **628** are connected together and in parallel to the advance control signal output $\overline{ADV}$ of function decoder **542** via path **574.** The shift in control character $\overline{SI}$ output of function decoder **538** via path **606** is connected in parallel to the data input terminal of flip-flop **626** and to the input of an inverter **634** whose output is connected to another flip-flop **636.** The $\overline{Q}$ state output of flip-flop **636** is connected to the clock terminal of flip-flop **626.** The clock terminal of flip-flop **636** is connected to the shift out control character output $\overline{SO}$ of function decoder **538** via path **608.**

Now describing function decoder **456.** Function decoder **456** is specifically related to the control of a video display of an auxiliary input from a remote source. The input control signal auxiliary ready to send AUX. RTS via path **638** is connected to the input of a conventional level changer **640** which changes EIA voltage compatible levels to TTL voltage compatible levels. The output of the level changer **640** is connected in parallel to one input of a two input NOR gate **642** and to a flip-flop **644.** The other input to NOR gate **642** is connected to the tape control signal output $\overline{TAPE}$ of function decoder **544** provided via path **564.** The output of NOR gate **642** is also connected to flip-flop **644** which provides the control signal enable line ELINE via path **462** in one state and the control signal enable line $\overline{ELINE}$ via path **454** in the other state. The enable line output $\overline{ELINE}$ of flip-flop **644** provided via path **454** is also connected in parallel to the input of a NOR gate **646** whose output is connected to the input of another conventional level changer **648** which changes TTL voltage compatible oevels to EIA voltage compatible signal levels and provides as an output the control signal auxiliary clear to send AUX. CTS via path **650.**

TEXT MEMORY PORTION

Referring now to FIG. 5 and describing in greater detail the text memory portion **14** associated with the text input buffer **12.** As was previously mentioned, the text memory portion **14** preferably includes memories **52** and **54** which are preferably each recirculating memories. Both memory **52** and **54** each preferably comprise seven stages, one for each input bit, each stage preferably being 256 bits. Each of these memories **52** and **54**

is a conventional recirculating memory network and is represented by the symbol labeled MEMORY (7X256) which is a symbol defined as meaning seven stages, 256 bits each. The parallel output bits from storage register **46** (FIG. **4**) are each connected in parallel to the parallel inputs to memory **52** and memory **54**, respectively, one bit per stage of each memory **52** and **54**. In addition, as was previously mentioned, the load input terminal of memory **52** is connected to the output of NOR gate **502** of address decoder **472** (FIG. **4**) via path **518** and the clear input terminal of memory **52** is connected to the output of OR gate **520** of address decoder **472** (FIG. **4**) via path **522**. Similarly, as was also previously mentioned, the load input terminal of memory **54** is connected to the output of NOR gate **524** of address decoders **472** (FIG. **4**) via path **532** and the clear input terminal of memory **54** is connected to the output of OR gate **530** of address decoder **472** (FIG. **4**) via path **534**. The parallel output bits of memory **52** are labeled respectively MB1A, MB2A, MB3A, MB4A, MB5A, MB6A and MB7A and are provided via paths **660, 662, 664, 666, 668, 670** and **672**, respectively, from memory **52**. Similarly, the parallel output bits of memory **54** are labeled, respectively, MB1B, MB2B, MB3B, MB4B, MB5B, MB6B and MB7B and are provided via paths **674, 676, 678, 680, 682, 684** and **686**, respectively, from memory **54**.

As was previously mentioned, memories **52** and **54** have their outputs connected in parallel to the recirculation register network **56** which preferably comprises seven recirculation registers **688, 690, 692, 694, 696, 698** and **700**, one register being provided for each bit, as will be explained in greater detail hereinafter. Recirculation registers **688** through **700** inclusive are preferably identical in structure and operation, and are preferably conventional. For purposes of explanation, a typical recirculation register **688** is shown in greater detail in FIG. **5**. Each recirculation register **688** to **700** inclusive preferably includes a **32** bit register **702**. Register **702** preferably has its clock input connected to a conventional clock generator shown in FIG. **7** via path **704** so as to receive the clock signal CKR via path **704**. A break recirculation control signal $\overline{BKR}$ from coincidence circuit **514** of FIG. **7** is connected in parallel to one input of a two input NAND gate **706** and to the corresponding inputs of recirculation registers **690** through **700** inclusive, via path **708**. The other input to NAND gate **706** is the recirculation output of register **702**.

Recirculation registers **688** through **700** inclusive are also provided with enable load signals E1 and E2, respectively, provided from a conventional clock generator **710** of FIG. **7** via paths **712** and **714**, respectively. The enable load signal E1 is connected in parallel to one input of a NAND gate **716** and to the corresponding inputs of recirculation registers **690** through **700** inclusive. The enable load signal E2 provided via path **714** is connected in parallel to one input of another NAND gate **718** and to the corresponding inputs of recirculation registers **690** through **700** inclusive. The other input to NAND gate **716** is the parallel output bit from memory **52** provided via path **660** and the other input bit to NAND gate **718** is the parallel output bit of memory **54** provided via path **674**. The outputs of NAND gate **706, 716** and **718** are connected in parallel. The output of NAND gate **718** is also connected to the input of an inverter **720** whose output is connected to the input of register **702**.

The output of NAND gate **716** is the recirculation register output bit RB1 provided via path **722** to the character generator network **58** of display portion **16**, shown in greater detail in FIG. **6**. Similarly, the parallel output bits from memories **52** and **54** provided via path **662** and **676**, respectively are connected to the input of recirculation register **690** whose output is recirculation bit RB2 provided via path **724** to the character generator network **58** of the display portion **16**; the parallel outputs of memories **52** and **54** provided via paths **664** and **678**, respectively, are connected to the input of recirculation register **692** whose output is recirculation bit RB3 provided via path **726** to the character generator network **48** of display portion **16**; the parallel output bits of memories **52** and **54** provided via paths **666** and **680** are connected to the input of recirculation register **694** whose output is recirculation bit RB4 provided via path **728** to the character generator network **58** of display portion **16**; the parallel output bits of memories **52** and **54** provided via paths **668** and **682** are connected to the inputs of recirculation register **696** whose output is recirculation bit RB5 provided via path **730** to the character generator network **58** of the display portion **16**; the parallel output bits of memories **52** and **54** provided via paths **670** and **684** are connected to the input of recirculation register **698** whose output is recirculation bit RB6 provided via path **732** to the character generator network **58** of display portion **16**; and the parallel output bits of memories **52** and **54** provided via paths **672** and **686** are connected to the input of recirculation register **700** whose output is recirculation bit RB7 provided via path **734** to the character generator network **58** of display portion **16**.

DISPLAY PORTION

Referring now to FIG. **6** and describing the display portion **16** in greater detail. Character generator network **58** preferably includes a pair of conventional character generators **736** and **738**. These conventional character generators are preferably MOS read only memories which are preprogrammed for the desired character generation functions. Preferably, character generator **736** is preprogrammed to provide alphanumeric characters and fraction characters in response to the recirculation bits and the horizontal line scanning signals, and character generator **738** is preferably preprogrammed to provide graph characters in response to the recirculation bits and the horizontal line scanning signals. The appropriate line scanning signals for triggering character generators **736** and **738** will be discussed in greater detail with reference to FIG. **7**. The output of character generator **736**, which is preferably a plurality of parallel output bits, is connected to the input of output register **60**, which is preferably a conventional two stage output register. The clock input of the output register **60** is connected via path **340** to the master oscillator associated with the basic timing chain of FIG. **7**. The transfer terminal input of output register **60** is connected to the transfer pulse output $\overline{XFERTK}$ of the output transfer portion **61** via path **63**, output transfer portion **61** preferably being similar in structure and operation to output transfer portion **344** (FIG. **3**).

The output of output register **60** is connected to one input of a two input OR gate **740**. The other input to

OR gate **740** is connected to the output of character generator **738.** The output of OR gate **740** is connected in parallel to one input of a pair of two input AND gates **62** and **64,** respectively. The other inputs of AND gates **62** and **64,** respectively, are connected to the output of a conventional timing generator **746** labeled ENABLE TEXT GENERATOR (**1** AND **2**) which generator **746** provides the timing pulse enable text **1** (ETX1) via path **748** to AND gate **62,** and the timing pulse enable text **2** (ETX2) via path **750** to AND gate **64.** The timing signals utilized to control the operation of enable text generator **746** are provided from the basic timing chain of FIG. **7** and are, respectively, the timing signal output of the master oscillator OSC provided via path **340,** the VB3′ timing signal output of the basic timing chain provided via path **446** and the $\overline{R2^3}$ timing signal output provided via path **752.**

The output of AND gate **62,** which is the information signal text data **1** ($\overline{TXDATA1}$), is connected in parallel to the input of the three input OR gate **68.** Another input to OR gate **68** is the scroll data output $\overline{SCROL1}$ provided from the scroll character generation portion **26.** The third input to OR gate **68** is connected in parallel to the ticker data output TK1 of the ticker character generation portion **20** and to the output of a two input AND gate **70.** One input of AND gate **70** is the enable text signal ETX2 provided via path **748.** The other input to AND gate **70** is connected in parallel to one input of another two input AND gate **84** and to the output of an inverter **764** whose input is connected to the TICKER output of position gating circuit **114** provided via path **432.** The output of AND gate **84** is connected in parallel to the ticker data input TK2 associated with the ticker number **2** input buffer portion **22** to one input of the three input OR gate **80.** The other inputs to OR gate **80** are the text data information $\overline{TXDATA2}$ provided via path **753** from AND gate **64,** and the scroll data input $\overline{SCROL2}$, if a second scroll data display is utilized.

As was previously mentioned, the output of OR gate **68** is connected to the input of a conventional video mixer **74** together with the composite sync signal output of the conventional mixed horizontal and vertical sync pulse generator **766** of FIG. **7** labeled $\overline{SYNC1}$ (represented by sync generator **76** in FIG. **1**), provided via path **768.** The output of mixer **74,** which is associated with channel A is a composite video signal output to television display device **78** which output is preferably a video display similar to that illustrated in FIG. **8**D, and which will be described in greater detail in the discussion of the operation of the circuit. Similarly, the output of OR gate **80** is connected to the input of another conventional video mixer **86** together with the sync signal output $\overline{SYNC2}$ (represented by sync generator **88** in FIG. **1**) from sync generator **766** of FIG. **7** provided via path **770.** The output of mixer **86,** which is associated with channel B is a composite video signal to TV display device **90,** similarly resulting in a video display preferably similar to that illustrated in FIG. **8**D. As will be discussed in the operation of the circuit, the video displays provided from mixers **74** and **86** need not be the same and are preferably different.

TIMING SIGNAL GENERATION PORTION

Referring now to FIG. **7** and describing in greater detail the timing signal generation portion which is the source of the timing signals which control the operation of the various portion of the system **10** and which has previously been referred to in the detailed discussion of the other portions of system **10.** The timing generator network shown in FIG. **7** includes the basic timing chain network **772** which provides the horizontal line scanning timing signals and the character counter timing signals utilized for controlling the timing of the various portions of the system **10** in a manner to be discussed in greater detail in the discussion of the operation of the system **10.**

The basic timing chain **772** includes a master oscillator **774** of a predetermined frequency, such as 4.5 megahertz, which provides the oscillator clock signal OSC via path **340** and which is connected in parallel to the clock input of the video bit counter **776,** which is a conventional divide-by-six counter whose outputs are the timing signals VB1, VB2 and VB3 provided on paths **448, 778** and **446,** respectively. Preferably, counter **776** is a two stage counter consisting of a divide-by-two stage between output bits provided via paths **448** and **778,** and a divide-by-three stage between output bits provided via paths **778** and **446** so that timing signal VB1 is equivalent to OSC/**2,** and VB2 and VB3 are each equivalent to OSC/**6.** The output of video bit counter **776** is connected to the clock input of a character counter **780** which is preferably a conventional divide-by-48 counter which provides the timing signal outputs C1, C2, C3, C4, C5 and C6 along paths **264, 270, 782, 466, 784** and **178,** respectively. Preferably, these timing signals are such that C1 is equivalent to VB3/2, C2 is equivalent to VB3/4, C3 is equivalent to VB3/8, C4 is equivalent to VB3/16, and C5 and C6 are each equivalent to VB3/48. The output of character counter **780** is connected to the clock input of a line counter **786** which is preferably a conventional divide-by-eight counter whose outputs are $L2^0$, $L2^1$ and $L2^2$ provided from counter **786** via paths **788, 790** and **792,** respectively. Preferably, the timing signals $L2^0$, $L2^1$ and $L2^2$ are such that $L2^0$ is equivalent to C6/2, $L2^1$ is equivalent to C6/4 and $L2^2$ is equivalent to C6/8. The output of line counter **786** is connected to the clock input of a half-row counter **794** which is preferably a conventional divide-by-two flip-flop whose output is the timing signal R/2 provided via path **796.** Preferably, the timing signal R/2 is equivalent to $L2^2/2$. The output of half-row counter **794** is connected to the clock input of a row counter **798** which is preferably a conventional divide-by-16 counter **798** whose outputs are $R2^0$, $R2^1$, $R2^2$ and $R2^3$ provided via paths **590, 800, 802** and **752,** respectively.

The reset terminal of row counter **798** is connected to a line adder network **804** which provides a reset pulse RRC to row counter **798** at the end of six additional horizontal scan lines provided by line adder **804,** as will be explained in greater detail hereinafter. Line adder **804** includes flip-flops **806, 808** and **810.** The $R2^2$ output of row counter **798** provided via path **802** is connected to flip-flop **806.** Flip-flop **806** provides the timing signal $R2^3$ in the Q state and $\overline{R2^3}$ in the $\overline{Q}$ state. The $\overline{Q}$ output of flip-flop **806** is connected in parallel to the data terminal input of flip-flop **806** and to flip-flop **808.** The Q state output of flip-flop **808** provides a signal which adds six horizontal scan lines labeled $\overline{+6L}$ provided via path **812.** In the $\overline{Q}$ state, flip-flop **808** also provides a signal which adds six horizontal scan lines labeled +6L provided via path **814.** The $\overline{Q}$ state output of flip-flop **808** is connected in parallel to the

data input terminal of flip-flop **808** and to one input of a two input NAND gate **816.** The other input to NAND gate **816** is the timing signal $L2^2$ provided via path **792** from line counter **786.** The output of NAND gate **816** is connected to the data terminal input of flip-flop **810** which is also connected to the timing signal $L2^1$ output of line counter **786** provided via path **790.** The preset terminal of flip-flop **810** is connected to the $\overline{VB2}$ output of video bit counter **776** provided via path **778.** The Q state output of flip-flop **810** is connected to the preset terminal of flip-flop **808** and the $\overline{Q}$ state output of flip-flop **810** is connected to the reset terminal of row counter **798** to provide the reset pulse RRC to clear row counter **798** via path **818.**

The cursor character counter **576** is preferably a conventional divide-by-32 counter which provide cursor character signal outputs CC1, CC2, CC3, CC4 and CC5 via paths **820, 822, 824, 826** and **828,** respectively, to the coincidence circuit **514.** The clear input terminals of the cursor character counter **576** is connected to the output of a two input OR gate **830** whose inputs are the control character outputs carriage return ($\overline{CR}$) provided via path **604** from function decoder **538** (FIG. 4) and start of text ($\overline{STX}$) provided via path **554** from function decoder **498** (FIG. 4). The inputs to cursor character counter **576** are the timing signals VB2 provided via path **778** from video bit counter **776,** the complement $\overline{CC3}$ of the cursor character output CC3 provided path **824,** the control character tab ($\overline{TAB}$) provided via path **620** from function decoder **538** (FIG. 4) and the control character advance $\overline{ADV}$ provided via path **574** from function decoder **542** (FIG. 4). The output of the cursor character counter **576** is connected to a flip-flop **832.** The clear input terminal of flip-flop **832** is connected to the VB3 output of video bit counter **776** via path **446.** The $\overline{Q}$ state output of flip-flop **832** is connected in parallel to one input of a two input OR gate **834,** and to the clear input terminal and the data input terminal of another flip-flop **836.** The other input to OR gate **834** is connected to the output of a two input NAND gate **838.** One input and NAND gate **838** is connected to the Q state output of flip-flop **836** and the other input to NAND gate **838** is connected to the control character output line feed LF provided via path **618** from function decoder **538** (FIG. 4). The line feed LF input is connected in parallel to one input of a two input OR gate **840** whose other input is connected to the control character output advance ADV of function decoder **542** provided via path **574** (FIG. 4). The output of OR gate **840** is connected to flip-flop **836.** Referring once again to OR gate **834,** the output of this gate is connected to the input of a cursor row counter **842** which is preferably a conventional divide-by-eight counter whose outputs are the signals $CR2^0$, $CR2^1$, $CR2^2$ provided via paths **844, 846** and **848,** respectively, to the coincidence circuit **514.** The clear input of the cursor row counter **842** is connected to the start of text ($\overline{STX}$) output of function decoder **498** provided via path **554** (FIG. 4).

As was previously mentioned, the coincidence circuit **514** is a conventional coincidence circuit which compares the cursor character counter **576** outputs against the respective character counter **780** outputs, and the cursor row counter **842** outputs against the respective row counter **798** outputs to provide the output coincidence signal $\overline{COIN}$ preferably at line **1** of the appropriate **16** line row of the video display for one character time. In addition, the coincidence circuit **514** preferably provides the break recirculation signal $\overline{BKR}$ via path **708** from timing signals $L2^2$, $L2^1$, and $L2^0$, providing the timing signal L1 via path **850** and together with the half-row counter timing signal R/2 provided via path **796** providing the break recirculation signal $\overline{BKR}$. This signal preferably occurs at line 1 of each 16 line row for the entire line time except for character time C6.

The balance of the timing signal generation network shown in FIG. 7 provides the various enable and clock signals for the previously discussed portions of the system **10** as well as the sync signals for the mixer portions **74** and **86** (FIG. 6) of the system **10** in a conventional manner. The delay clock generator **852** which is a conventional clock generator provides a clock output signal delay clock $\overline{DCK}$ via path **276** through NOR gate **274** of motion control network **104** (FIG. 2) in response to timing signal inputs L1, $\overline{+6L}$, $\overline{VB3}$, $\overline{C6}$, $\overline{C3}$ and $\overline{C4}$. The clock text signal generator **131** provides the clock signal output CKR, CKTX and CK via paths **704, 854** and **188,** respectively, in response to input signals $\overline{VB2}$, VB1, $\overline{+6L}$, $\overline{L2^1}$, C6, $\overline{R/2}$, $L2^0$, +6L and $\overline{L2^2}$. The clock ticker signal generator **856** provides the clock output signal CKTK via path **858** in response to the input signal $\overline{C4}$. The clock scroll signal generator **860** provides the clock scroll signal CKS via path **862** in response to the input signal C3. Enable test memory signal generator **710** provides the enable memory output signals E1 and E2 via paths **712** and **714,** respectively, in response to the input timing signals $\overline{R2^3}$, $\overline{+6L}$ and $\overline{BKR}$. The enable ticker number **1** signal generator **108** provides the enable ticker number **1** output signal ETK1 via path **866** in response to input timing signals $\overline{R/2}$, $R2^0$, R/2, $\overline{R2^0}$, $\overline{R2^2}$ and $\overline{R2^1}$. The enable delay signal generator **354** provides the enable delay output signal EDO via path **352** and the enable delay signal ED via path **868** in response to the input timing signals $L2^1$, R/2 and $L2^2$. The enable ticker number **2** signal generator **109** provides the enable ticker number **2** output signal ETK2 via path **872** in response to input timing signals $\overline{R2^1}$, $\overline{R2^2}$ and $\overline{R2^0}$. The enable scroll signal generator **118** provides the enable scroll output signal ESCROLL via path **876** in response to input timing signals R/2, $\overline{R2^0}$, $\overline{R2^1}$ and $\overline{R2^2}$. Lastly, the mixed horizontal and vertical sync signal generator **766** provides the mixed sync signal output $\overline{SYNC1}$ and $\overline{SYNC2}$ via paths **768** and **770,** respectively, in response to input timing signals C3, $\overline{C4}$, C6, $\overline{L2^2}$, $L2^0$, $L2^1$, $\overline{R2^1}$, $R2^3$, $R2^0$, $R2^2$ and $\overline{R/2}$.

OPERATION

Now describing the operation of the system **10** in response to the timing signals so as to provide a video display including at least two different independent video display formats. However, before describing the operation of the system **10** of the present invention in greater detail, the operation of the timing signal generation network shown in FIG. 7 will be summarized hereinafter. The basic timing chain **772** is clocked by the master oscillator **774,** which as was previously mentioned, is preferably a crystal controlled oscillator having a frequency such as 4.5 megahertz. This oscillator **774** clocks the video bit counter **776** which provides the timing signals VB1, VB2 and VB3 at the respective frequencies discussed above. The video bit counter **776,** in turn, clocks the character counter **780** which pro-

vides the timing signal outputs C1, C2, C3, C4, C5 and C6 at the respective frequencies discussed above. The timing signal C6, which is preferably at a frequency of VB3/48, which is equivalent to OSC/288, is utilized for horizontal blanking in the position gating horizontal blanking portion 434 (FIG. 3). The output of character counter 780 triggers the line counter 786 which provides output signals $L2^0$, $L2^1$ and $L2^2$ with the respective frequencies of C6/2, C6/4 and C6/8. The line counter 786, in turn, triggers the half-row counter 794 which provides a timing signal R/2 which is equivalent to $L2^2/2$, which is also equal to C6/16. This half-row counter 794, in turn, triggers the row counter 798 to provide the timing signals $R2^0$, $R2^1$, $R2^2$ and $R2^3$ which are equivalent, respectively, to $L2^2/4$, $L2^2/8$, $L2^2/16$ and $L2^2/32$. At the end of the row counter 798 the line adder 804 is triggered to add six horizontal lines of scan in order to preferably generate 262 lines per frame. At the end of the sixth line from the line adder 804, the reset pulse RRC is provided to the line counter 786 which is thereby reset to zero, all other counters 776, 780, 798 and 794 being in the zero state at this time. The coincidence circuit 514, which is preferably a conventional coincidence circuit has been previously discussed and its operation will not be discussed in further detail.

The cursor character counter 576 and cursor row counter 842 comprise what may be collectively termed the cursor counter. When the cursor character counter 576 is incremented by the control pulse advance $\overline{ADV}$ provided via path 574, or by the control pulse tab $\overline{TAB}$ provided via path 620, it will be incremented to the next group of eight characters. For example, if seven characters have been loaded and the control pulse $\overline{TAB}$ occurs, the cursor character counter 576 will increment to the seventeenth character instead of the ninth character, similar to the operation of a conventional typewriter. When the cursor character counter 576 recycles from the 32 character (32) to the first character (1), the cursor row counter 842 will automatically be incremented. If directly after, the control pulse line feed LF is received via path 618, that particular line feed will be suppressed unless the control pulse advance ADV via path 574 has occurred prior to the occurrence of the line feed control pulse, or unless a subsequent line feed control pulse occurs via path 618. If a subsequent line feed control pulse occurs via path 618, then that line feed control pulse will activate the system in a normal manner and will increment the cursor row counter 842 one increment. It should be noted that in discussing the various timing signals, the video bit counter 776 controls the number of bits per character, the character counter 780 controls the number of characters per line, the line counter 786 controls the number of lines per row and the half-row counter and row counter 794 and 798, respectively, control the number of rows per frame. It should be further noted, that although the character counter 780 is preferably a divide-by-48 counter, only 32 of the 48 characters are preferably utilized.

As was previously mentioned, the timing signal generation circuit shown in FIG. 7 also provides the break recirculation signal $\overline{BKR}$ which occurs at line 1 of each 16 line row of the entire character time except for character time C6, and the clock signals for the recirculation registers which signals are clock recirculation register CKR, clock CK, clock text memory CKTX, clock scroll CKS, clock ticker CKTK, the sync signals $\overline{SYNC1}$ and $\overline{SYNC2}$, the enable ticker signals ETK1 and ETK2, the enable scroll signal ESCROLL, the enable delay signals ED and EDO, the enable text memory signal E1 and E2 and the clock signals for the motion control delay clock DCK, these signals being provided throughout various portions of the system 10 to control the operation in the manner to be described in greater detail hereinafter.

DESCRIPTION OF SYSTEM OPERATION

The system 10 of the present invention preferably provides a video character display containing at least two different types of video display formats, such as those illustrated in FIGS. 8A through 8F, which are independently self-generated digital-to-video scan signals. These video display formats or character displays are provided in different areas on a common display screen, such as shown in FIG. 8D. Particularly, the signals that are generated preferably include two ticker display type of signals which are vertically spaced apart from each other and may be either continuously moving across the display screen or momentarily stationary, the rate of movement of the ticker type display across the screen varying with the rate of data input to the system 10. As will be described in greater detail hereinafter, the movement of the ticker display across the screen is continually smooth with variations in the rate of the data input due to the acceleration and deceleration of the movement or motion of the data by means of the motion control network 104, 104a and 104b, and the associated position gating networks 114 and 126, as will be explained in greater detail hereinafter.

In addition to the two ticker displays, which are each preferably 31 characters in length and are represented in FIG. 8D as displays 900 and 902, respectively, a stationary or static display of the message "STOCKS 15 MIN. DELAYED," display 904 of FIG. 8D, is preferably vertically spaced apart from the lowermost ticker display 902 and has the same character length. This display 904 is optional and is only utilized in accordance with the requirement of the Stock Exchanges. This message can therefore be removed, independently of the ticker displays 900 and 902 if desired, such as when the tickers are in real time displayed "live." In addition, this message which is provided from the STOCKS 15 MIN. DELAYED message generator 28, may also be removed in conjunction with the removal of the portions of the displays of FIG. 8D corresponding to the ticker displays 900 and 902.

In addition to the display 900, 902 and 904 a text display is also preferably provided which comprises a maximum of eight rows having 32 characters each, each row of text having a maximum height of 16 horizontal scan lines for each character. The text display 906 (FIG. 8D) is preferably vertically spaced from the delay message display 904 which has a 31 character length per row as do displays 900 and 902. In addition, a scroll or crawl display 908 is provided at the bottom portion of the screen vertically spaced from the last row of the text display 906, the scroll display 908 preferably being a display having a movement across the screen similar to that of ticker displays 900 and 902 under the control of motion control network 104*b* and position gating network 126. A typical scroll type display is shown in FIG. 8F wherein the scroll display is provided in a plurality of character spaces which are

each eight horizontal scan lines high and six dots wide. The height of the scroll display of FIG. 8F is, therefore, half the height of a row of the text display **906** which is illustrated in FIGS. 8A and 8C, one text row being divided into character spaces which are 16 horizontal scan lines high by six dots wide.

The ticker displays **900** and **902**, however, are preferably comprised of character spaces which although 16 horizontal scan lines high, utilize only the uppermost eight lines to display an alpha character such as relating to a stock symbol only seven of these lines being utilized for the symbol, the lowermost line providing a space, and the bottommost eight lines of the **16** being utilized for the display of alphanumeric characters associated with the stock symbol, such as the price of the stock as well as a symbol such as B for bid, or C for close if such a symbol is transmitted with the price. In this instance only seven of the lower most eight lines are utilized for this alphamumeric display. Preferably, in the ticker display **900** or **902**, which display is illustrated in FIG. 8B, the alphanumeric lower portion cannot be displayed directly under the stock symbol portion but must be displayed in its own separate character space of 16 horizontal scan lines, only utilizing the bottom eight scan lines. As also illustrated in FIG. 8B, when fraction characters are displayed in the ticker display **900** or **902**, the lowermost 10 lines of the **16** line character space area are utilized for display of the fractions; the top five lines of these 10 are utilized for the display of the numerator of the fraction and the bottom five lines being utilized for the display of the denominator of the fraction. The numerator and denominator are displaced from each other, preferably, so that they do not appear underneath each other but rather the denominator appears to the side of the numerator as shown in FIG. 8B. Furthermore, in displaying fraction characters, the entire composite fraction, both numerator and denominator, are displayed in a character space six dots wide. However, both the numerator and the denominator utilize only half the character space width for display; that is, three dots in width. Except for the numerator and the denominator of fraction characters, the alphanumeric characters displayed on the lowermost portion of the ticker display are each preferably displayed in character spaces six dots wide.

In addition, as shown in FIG. 8E, a simplified graph character display may also be provided on the video display screen in place of or in conjunction with the text display **906**. In such instance, the graph characters, which preferably utilize the standard ASCII code, are preferably at least four horizontal scan lines high by six dots wide and may go as high as 16 scan lines high by six dots wide, in which instance they would occupy the entire height of the character space area. When a graph display is desired, various combinations of graph characters are utilized to provide a composite block type of graph picture on the video display screen, such as illustrated in FIG. 8E, or may be utilized to provide a step type of graph. In addition, alphanumeric characters may appear at any desired location in the graph area as the scanning of the graph and alphanumeric characters in display portion **906** is determined on a character space-by-character space basis, as will be explained in greater detail hereinafter, so that the system **10** interrogates or determines what character is to be placed in a particular character space as the video system scans across the display screen in the text and/or graph display area **906**. It should be noted that, if desired, any one or more of displays **900, 902, 904, 906** or **908** can be independently removed from the video display screen without affecting the other displays on the screen.

Now describing the operation of the ticker number **1** input buffer portion **18** shown in greater detail in FIG. **2**, the operation of this portion being similar to that of the ticker number **2** input buffer portion **22** and the scroll input buffer portion **24**, whose operations will therefore, not be described in greater detail hereinafter. The ticker number **1** input buffer **18** receives the ticker number **1** input signal, which is a conventional nine bit ticker code comprising a start bit, six information bits and two stop marks, via path **94** through level changer **130** which changes the EIA compatible voltage level input to TTL compatible levels. This signal is then supplied to the resynchronizer **92** to ensure center sampling of the input pulses and to minimize spurious noise pulses. The resynchronizer **92** functions in a conventional manner, resyncronizing on the leading edge of each new space pulse. The output of resynchronizer **92** is provided to the input register **96**. The character supplied to register **96** shifts through the stages of the input register **96** in order to provide an output from each of the stages of the register, the output being a parallel bit output. The output bit from one of the stages of register **96** is supplied to the character detector **98** which senses the start bit. The character detector **98** upon sensing the start bit provides a load signal to load the data into storage register **100** and, at the completion of the loading of the data, a reset clear pulse is provided via path **138** to the input register **96** in anticipation of receipt of the next character. Preferably, at the same time as the character is loaded into the storage register **100** a mark is loaded into the motion control register **174**. The motion control register **174** provides the output Q3 via path **206** which is sensed by the spaced detector register **142**, which space detector **102** senses the next available portion of the storage register **100** immediately behind the previous character so that the next character will be loaded into this portion.

Now describing the motion control network **104** in greater detail. Flip-flop **210** becomes preset anytime there is data present in the storage register **100**. This data present conditon provides an output for the motion control register **174** to preset flip-flop **210**. Each time an $\overline{S1}$ ouput pulse is provided from flip-flop **210**, it is fed to the gating circuitry associated with the input of the output motion control counter **176** via path **212** which allows the counter **176** to increment once each frame. Anytime output motion control counter **176** returns to zero, an output is provided via path **284** which output causes a transfer pulse to be provided via paths **148** and **146**. This transfer pulse causes the data which is in the storage register **100** to be transferred to the memory **106**. The transfer of the character from the storage register **100** to the memory **106** removes that character from the storage register **100** and places it in the memory **106**. Character **1** of the storage register **100** thereby becomes character **32**, the last character, of the memory **106** and is off-line at transfer time. This character is then no longer stored in storage register **100** but is deleted therefrom after transfer. The next character is then advanced in position in the storage register **100** and, similarly, is advanced in position in

the memory **106** upon transfer so that, for example, character 2 in the storage register **100** becomes character 1 in position in the storage register **100,** and character 32 in position in the memory **106** becomes character 31 in position in the memory **106,** and so forth. In this manner the characters are incremented as they are transferred. This character incrementing function is similar to that described in U.S. Pat. Nos. 3,426,344 and 3,422,420. If the character present in the storage register **100** is the last character then, on transfer, the motion control register **174** will become empty and flip-flop **210** will stay on providing pulse $\overline{S1}$ until the output motion control counter **176** increments 11 times, which moves the new character on to the video display screen while moving the oldest character off the screen or, in other words, deleting this old character from the screen.

During normal operation, as the first character is loaded flip-flop **210** is set and $\overline{S1}$ is provided; as two characters are loaded flip-flop **242** is set and S2 and is provided; as three characters are loaded flip-flop **228** is set and S3 is provided and as four characters are loaded, the preferred capacity of the motion control register **174,** flip-flop **220** is set and S4 is provided. In other words, if on character is present in the storage register **100** then $\overline{S1}$ is provided; if two characters are present in the storage register **100** then S2 is provided; if three characters are present in the storage register **100** and then S3 is provided and if four characters are present in the storage register **100, S4** is provided. Once flip-flop **220** is set and S4 is provided, it will remain set until there are only two characters present in storage register **100.** Once flip-flop **228** is set and S3 is provided, it will remain set until only one character is left in the storage register **100.** Once flip-flop **242** is set and S2 is provided, it will remain set until there are no characters left in the storage register **100.** Once flip-flop **210** is set and S1 is provided, it will remain set until the last character loaded into the memory **106** is brought out onto the display in the manner previously discussed with respect to the last character condition.

Preferably, the recirculating memories which comprise the storage register **100** are preferably each four bit memories, the storage register configuration **100** preferably being a four-by-six memory configuration, one memory being provided for each bit. The outputs of memory **106** which are the ticker bit signals, are gated with the appropriate ticker enabling signal to provide ticker bit signals TKB1 through TKB6, which are provided to the character generator **110** of the ticker character generation portion **20.**

Now describing the operation of the ticker character generation portion **20** shown in FIG. **3.** As was previously mentioned, the ticker character generator **110** is a preprogrammed read only memory which provides alphanumeric characters and fraction characters in response to the ticker input bit signals TKB1 through TKB6 and the horizontal line scan signals L1, L2, L3, L7, L8, $L2^0$, $L2^1$, $L2^2$, $R2^0$, $R2^2$ and R/2. The output of character generator **110** is supplied to output register **112** which is provided with a transfer pulse from output transfer portion **344** via path **342** at the start of each character. This transfer pulse permits the parallel loading of data from the character generator **110** to the output register **112.** Output register **112** then shifts at the video dot frequency provided by the master oscillator **774** via path **340.** The output of output register **112** is provided to the position gating network, which senses the appropriate motion control counter output when more than one ticker input is provided, as in the example utilized in the description of the present invention where two ticker inputs one from the ticker number **1** input buffer portion **18** and from the ticker number **2** input buffer portion **22,** respectively, are provided, in order to provide the proper readout from the output register **112** so as to provide a ticker output signal to the appropriate mixer **74** or **86.** This signal represents the proper motion or rate of movement of the ticker display to be provided on the video display screen.

In describing the motion control counter **176** (FIG. **2**), whose outputs are D1 through D4, D1 is the most rapid moving stage and D4 the slowest moving stage. Motion control counter output signal D1 provided via path **288** causes the movement of the data in half dot increments. When the first half is present, $\overline{D4}$ is high, allowing the last three bits of the output register **112** to be sensed. When D4 is present it will allow the next to the last three bits of the output register **112** to be sensed. When D2 and D3 are not present, the last bit and the fourth from the last bit of output register **112** are allowed to be sensed. When D2 is present, the second from the last and the fifth from the last bit of output register **112** are allowed to be sensed. When D3 is present the third from the last and the sixth from the last bit of output register **112** are allowed to be sensed. Since the output motion control counter **176** is preferably composed of a divide-by-two, divide-by-three and divide-by-two counter configuration, both D2 and D3 cannot be present simultaneously. In this manner, the ouput moves closer to the horizontal sync pulse of the appropriate horizontal scan line. The output register **112** preferably delays the data by six bit times. It should be noted that the ticker input can normally only load three characters of data into the storage register **100** at its normal rate, the fourth character of each of the memories comprising storage register **100** accounting for a one percent deviation in the ticker rate.

In the manner described above, as data is input to the storage register **100** at the normal ticker rate, then flip-flop **228** will remain set and S3 will be provided. In the event ticker data is input to the storage register **100** at greater than the normal rate, flip-flop **220** will become set and S4 will be provided; however, the rate will in all probability return to the normal input rate and flip-flop **220** will change state so that S4 will no longer be provided, although flip-flop **228** will remain set and S3 will be provided. In the event that the data is input at less than the normal ticker rate, flip-flop **228** will change state and S3 will no longer be provided; however, flip-flop **242** will remain set and S2 will be provided or, if teh rate is even slower, flip-flop **242** will change state and S2 will no longer be provided, although flip-flop **210** will remain set and $\overline{S1}$ will be provided. The rate of movement of the data across the video display screen will accordingly be reduced as the data input rate is reduced and increased as the data input rate is increased. It should be noted that the number of characters present in the storage register **100** is preferably equivalent to the number of bits present in the motion control register **174,** the motion control register being synchronous with the storage register. Summarizing the operation of the motion control register **174,** when the data input and the corresponding movement of the dis-

play is accelerating in speed, Q3 will place you at $\overline{S1}$, Q2 will place you at S2, Q1 will place you at S3 and Q0 will place you at S4, the maximum speed. When the rate of input data and the corresponding movement of the display is decelerating in speed, S4 will stay set until Q1 has been cleared, S3 will stay set until Q2 has been cleared, S2 will stay set until Q3 has been cleared and $\overline{S1}$ will stay set until the last character has been cleared and displayed from memory **106.** In this manner the electronic flywheel function of the motion control network **104** occurs.

Now describing the operation of the horizontal blanking portion **434** (FIG. 3) of the ticker character generation portion **20.** The horizontal blanking portion **434** provides the length of window in which the character display is to appear on the screen, this window preferably being **31** characters long. Since the character counter **780** is capable of providing a total character length of **48** characters between horizontal sync pulses, the horizontal blanking portion **434** enables the character display for **31** characters while blanking **17** characters of the total **48** character length between the horizontal sync pulses. This provides a visual effect of the characters sliding onto and off the screen as the character display moves across the screen, as illustrated in FIGS. **8**A and 8F. The horizontal blanking pulse $\overline{C6}$ provided via path **178** is the non-display time of this data, the $\overline{C6}$ disabling pulse being delayed by one bit time by being fed through flip-flop **436** and by being triggered with the trailing edge of the transfer pulse. The disabling pulse output of flip-flop **436** will not be released until one bit time after character one time. Character one is the character which slides off the screen and is hidden. At this point a new character is loaded in for subsequent sliding onto the screen at the entry portion which is at the beginning of the corresponding row. The enable ticker number **1** signal, the enable ticker number 2 signal and the enable delay signal allow the data to be gated from the respective portions of the ticker generation circuitry to the character generator **110,** the time being determined by the output of the master clock oscillator **774** which provides the necessary row and line time of the gating in a conventional manner. The enable delay output provided to NAND gate **350** causes an inversion of the data so that a black on white display of the message "STOCK 15 MIN. DELAYED" is provided instead of the normal white on black display provided for the ticker display, text display and scroll display. In addition, the enable delay output provided to the position gating portion **114** via path **356** to OR gate **428** disables the position gating network **114** so that no output is provided which would interfere with the output of message generator **28,** otherwise this message would be repeated with a delay introduced into the message which would create a distorted message on the screen. It should be noted that no such signal is required for scroll character generation since no such message is introduced in this portion and, therefore, no such enable delay pulse is present.

Now describing the generation of the text display **906.** First describing the operation of the text input buffer portion **12** (FIG. 4). The text input signal is provided via path **30** to level changer **450** which changes EIA compatible voltage levels to TTL compatible voltage levels, this signal being provided to the resynchronizer **40** as well as to the input register **42.** Input register **42** functions in a conventional manner to shift the input character through the register **42** to the character detector **44.** The character detector **44** transfers the data into the storage register **46** when a start bit is detected. After the transfer of the data from the input register **42** to the storage register **46,** the transfer pulse from character detector **44** is removed and both the character detector **44** and the input register **42** are cleared for receipt of the next character. This operation is similar to that previously described with reference to the operation of the ticker input buffer portion **18.** When input register **42** is reset, the bias present in the storage register **46** are sensed to determine if the character is a displayable character, that is, if it is one of the 64 ASCII characters including space, graph or function characters. If the character is a displayable character, then the enable load data signal ELD will be sent from character detector **44** via path **470.** If this character is not a displayable character, but rather is a control character such as line feed LF, carriage return CR or start of text STX, the control signal CONT will become present on path **472** and the particular control function will occur assuming, of course, that it is one of the functions to be performed by the system **10.** When the enable load data signal is sent via path **470** is will be gated with the coincidence signal COIN provided from coincidence circuit **514** via path **512** in address decoder **50** to generate the load signals LD1 and LD2 to load the data into any memory or memories which are addressed. Naturally, if these memories are not addressed, they are not loaded. At the trailing edge of both the coincidence COIN and enable load data ELD signals, an advance pulse $\overline{ADV}$ will be provided from flip-flop **572** of function decoder **542** removing the enable load data signal from the character detector **44.** This advance pulse will then be cleared by generation of any output pulse from the oscillator **774.** This loading continues as each character is received until the control signal start of header SOH or end of text ETX is received.

In the addressing sequence, the first character received will normally be the control character start of header SOH via path **536** which will set enable load header which will, in turn, enable the address decoding matrices **490, 492** and **494.** As was previously mentioned, decoding matrices **490** and **492** will be programmed for any of the ASCII characters whereas coding matrix **494** is preprogrammed for the character "Z," the presence of which cause the generation of an output pulse which will turn on all channels. After start of header SOH is received, one or more alphabetic characters will be received. If this or these alphabetic characters correspond to the programming of matrix **490** and/or matrix **492,** the associated channel will be enabled. As previously mentioned, if that alphabetic character happens to be a "Z", then both channels will be enabled due to the detection of this character by matrix **494.** The next character which will be received to end the addressing sequence will be start of text STX which will reset enable load header, which will also clear the appropriate memory or memories. Each time enable load data ELD occurs and enable load header is set, an advance pulse $\overline{ADV}$ will be set without necessity of the presence of the coincidence pulse COIN. After start of text STX is received, which clears the memory, the data will be loaded into memories **52** and **54** in the manner previously described. When data is

loaded into the appropriate memory, as the first character is loaded into a line of memory, any data present on that line will be cleared from that character on so that the character will be loaded into a cleared line of memory, the loaded character only clearing the line into which it is being loaded. Accordingly, if the memory, as is preferred, is only eight lines long, after eight lines of data have been loaded in the memory, when the ninth line of data, if a ninth line is present, is loaded into the memory at line **1** of the memory, the data previously present on line **1** will be erased when the first character of line **9** is loaded onto line **1**; at this point nothing happens to lines **2** through **8** of the memory unless new data is specifically loaded into any one or more of these given lines.

When the control character tape $\overline{\text{TAPE}}$ is received and the auxiliary ready to send pulse RTS is present (FIG. **4**), the enable line ELINE pulse will be reset causing the occurrence of an auxiliary clear to send pulse CTS. This will, in turn, allow the data from the auxiliary line input to be entered into the input register **42**, which will operate on this data in the same manner as previously discussed with respect to the text line input. The auxiliary ready to send pulse will remain present on path **638** until all auxiliary supplied data has been received, at which time the auxiliary unit, such as an external computer, or teletype input, will remove its ready to send pulse. At this time enable line ELINE will be set and the clear to send signal will be removed from path **650**. After this occurrence, the ready to send pulse may be brought up again to await the occurrence of another control signal tape $\overline{\text{TAPE}}$ at a subsequent time. As soon as the auxiliary input removes the ready to send signal from path **638**, the enable line is set allowing the text line input via path **30** to be inserted into the system **10**.

When the control character shift out $\overline{\text{SO}}$ is received two times in succession by function decoder **540**, the signal enable shift out $\overline{\text{ESO}}$ will be set, activating an external device, such as a coaxial switch, in order to permit display of advertising on the screen in place of information generated from the system **10**. When the control character shift in $\overline{\text{SI}}$ is received two times in succession by function decoder **540**, the enable shift out signal will be removed from path **632**.

When the control character carriage return $\overline{\text{CR}}$ is received via path **604** (FIG. **7**), the cursor character counter **576** will be reset. When the control character start of text $\overline{\text{STX}}$ is received via path **554**, it will reset both the cursor character counter **576** and the cursor row counter **842**. When the control character line feed LF is received via path **618** it will increment the cursor row counter **842**, with the exception previously discussed. When the control character tab $\overline{\text{TAB}}$ is received via path **620**, it will increment the cursor character counter **576** at the start of the next increment of eight characters, except when it is present in the seventh count of a group of eight, in which instance it will advance to the start of the following group of eight characters.

Now describing the operation of the text memory portion **14** (FIG. **5**) of the system **10**. The loading of data into memories **52** and **54** has been previously described above in the discussion of the operation of the text input buffer portion **12**. The outputs of memories **52** and **54** are gated into the recirculation registers **688** through **700** inclusive by the enable signals E1 and E2 provided via paths **712** and **714**. When enable pulses E1 and E2 are enabling the loading of data into the recirculation registers **688** through **700**, inclusive, the break recirculation signal $\overline{\text{BKR}}$ provided via path **708** is breaking the associated recirculation paths of the recirculation registers **688** through **700**, inclusive, so that the data may be loaded into these registers. The break recirculation signal $\overline{\text{BKR}}$ breaks the recirculation path every line one of each **16** lines whether or not enable signals E1 and/or E2 are present; in other words, whether or not the data is being loaded into these registers. Memory **52** and memory **54** are each, as was previously mentioned, preferably both recirculating memories, operated in response to clear signals $\overline{\text{CL1}}$ and $\overline{\text{CL2}}$, respectively, which signals break the associated recirculation paths when data is being loaded into memories **52** and **54** due to the presence of the load data signals LD1 and LD2, respectively, in the same manner as previously discussed with reference to the break recirculation signal $\overline{\text{BKR}}$ associated with the recirculation registers **688** through **700** inclusive. The clear signals $\overline{\text{CL1}}$ and $\overline{\text{CL2}}$ also act independently to clear memories **52** and **54** at the appropriate times independent of the presence of load data signals LD1 and LD2.

The outputs of recirculation registers **688** through **700** which are recirculation bits RB1 through RB7, inclusive, provided via paths **722** through **734**, inclusive, are fed to character generators **736** and **738** respectively (FIG. **6**). Character generator **736** is preprogrammed to provide alphanumeric characters and fractions in response to the recirculation bit input and scanning signals $L2^0$, R/2, $\overline{\text{L1}}$, $\overline{\text{L8}}$, L7, L6, L5, $\overline{\text{VB3}}$, L3, L4, LWC, $L2^1$ and $L2^2$, as well as the enable delay message signal ED. Character generator **738** is preprogrammed to provide various graph characters in response to the recirculation bit input and timing signal $L2^2$, R/2, $\overline{L2^2}$, $\overline{\text{R/2}}$, $\overline{\text{C6}}$, LWC, VB3 and OSC. The output of character generator **736**, which is preferably a parallel bit output, is transferred into output register **60** at the occurrence of the transfer pulse $\overline{\text{XFERTX}}$ from output register output transfer portion **61** via path **63**. This transfer pulse occurs at VB3 time except during C6 time. The output of character generator **738** is transferred to OR gate **740** at VB3 time except during C6 time. The output of either output register **60** or character generator **738** passes through OR gate **740** and is then gated with the enable text 1 ETX1 or enable text 2 ETX2 signals to provide the text data information signals $\overline{\text{TXDATA1}}$ and $\overline{\text{TXDATA2}}$ for the character display. These text data information signals are OR'd with the appropriate scroll and ticker data signals in gates **68** and **80**, respectively, the output of OR gates **68** and **80** being fed to mixers **74** and **86**, respectively, together with the respective mixed horizontal and vertical sync signals $\overline{\text{SYNC1}}$ and $\overline{\text{SYNC2}}$, wherein the vertical sync pulse is preferably equal to three horizontal line times, to provide a video composite output signal via paths **1000** and **1002**, respectively, to video display devices **78** and **90**, respectively. It should be noted that the output transfer portion **61** is preferably disabled both when graph characters are being generated, on a character spaced-by-character space basis, and during the first eight of the 16 lines in a row when a text type display is being provided, except when fractions are being generated, in which instance it is disabled for the first six of the 16 lines.

During the operation of the system **10** of the present invention, when a text display **906** is provided to the display screen, this display will preferably remain on the screen until the appropriate channel is again addressed via the appropriate decoding matrix so that new information may be displayed in its place. Furthermore, the channel associated with decoding matrix **490** may be addressed with one text message while the channel associated with decoding matrix **492** may be addressed with another text message so that two different text messages may be simultaneously displayed on different video display screens. In this manner, if desired, several display screens may time share a remotely located computer.

It is to be understood that the above described embodiment of the invention is merely illustrative of the principles thereof and that numerous modifications and embodiments of the invention may be derived within the spirit and scope thereof, such as splitting the video display screen vertically instead of horizontally, or vertically as well as horizontally.

What is claimed is:

1. A system for providing character patterns for display on a display device screen that utilizes a television raster scan-line pattern to provide a composite video display, each character pattern being displayed in one character space, said system comprising means for generating a first video display format of character patterns in response to a first digital signal; means for generating a second video display format of character patterns in response to a second digital signal, said second format being different from said first format, said first and second generated video display formats being independent from each other; and means for combining said first and second video display formats to provide said composite video display for said display device in which said first and second display formats occupy different scan-line areas of said scan-line pattern on said screen; said character spaces associated with said character patterns each being defined by a predetermined number of scan lines in said scan-line pattern and a predetermined number of elemental dots; said scan lines having a given direction of scan with respect to said screen; said first video display format generating means including means for generating a plurality of dot signals in repetitive sequences during said scan lines to correspond to elemental dots on said display device to divide said device in said first video display format area in a first direction into a plurality of said character spaces, and means for generating a plurality of line signals in repetitive sequences in synchronism with said scan lines to divide said device in said first video display format area in a second direction into at least one row, the combination of a plurality of said dot signals and a plurality of sequences of said line signals defining a character space; said first digital signal having an associated information input rate to said first generating means, said first video display format generating means further including means for controllably periodically shifting each of said character spaces in said row an incremental distance in a given direction parallel to said direction of scan across said screen at a rate dependent on said information input rate to controllably move the character patterns displayed in said character spaces in said given direction across said screen in accordance with said input rate; said shifting means comprising means for varying said shifting rate in accordance with variations in said information input rate for accelerating said character movement in accordance with an acceleration in said information input rate and for decelerating said character movement in accordance with a deceleration in said information input rate; said first video display format generating means further comprising recirculating register storage means for receiving said first digital signal and loading therein said characters in response thereto at an associated data loading rate corresponding to said input rate, said storage register means having a character storage capacity of a plurality of said characters in length, and memory means operatively connected to said storage register means for receiving said characters therefrom upon transfer therefrom, said shifting means comprising motion control means for providing a transfer signal to said storage register for incrementally transferring said characters therefrom to said memory, said first video display format being provided in response to an output from said memory, said motion control means comprising means responsive to changes in said data loading rate from providing a different motion control signal in response to a different quantity of characters being loaded into said storage register for a given character prior to said transfer, and position gating means responsive to said motion control signals for controlling a change in incremental dot position of said given character in said display in accordance with said change in said data loading rate whereby the relative movement of said character patterns across said screen in said direction parallel to said direction of scan may be controlled in accordance with said information input rate.

2. A system in accordance with claim **1** wherein each of said video display formats is independently controllable.

3. A system in accordance with claim **1** wherein said line signal generating means generates said plurality of line signals in repetitive sequences in synchronism with said scan lines to divide said device in said first video display format area in a second direction into a plurality of rows, the combination of a plurality of said dot signals and a plurality of sequences of said line signals defining a character space in a given one of said rows, the character spaces in each of said rows being equal.

4. A system in accordance with claim **3** wherein said first video display format generating means includes means for providing a complete character pattern in at least a portion of said character space which is less than said total plurality of line signals.

5. A system in accordance with claim **4** wherein said first video display format generating means includes means for generating at least complete graph character patterns, a complete graph character pattern being provided in at least said character space portion.

6. A system in accordance with claim **4** wherein said first video display format generating means includes means for generating at least complete graph character patterns and alphanumeric character patterns, a complete graph character pattern being provided in at least said character space portion, and means for controlling which particular character pattern is to be displayed in a given character space for each of said character spaces.

7. A system in accordance with claim **6** wherein said character pattern generating means includes means for generating fraction character patterns, said fraction

character patterns including a complete numerator character pattern and a complete denominator character pattern, said complete numerator character pattern being provided in a portion of a given character space which is less than said total plurality of lines and dots, said complete denominator character pattern being provided in a different dot portion of said character space which is adjacent to said numerator character space dot portion, said denominator character pattern space line portion being lower than said numerator character pattern space line portion in said first video display format, whereby a complete fraction character pattern is provided in said adjacent character space portions.

8. A system in accordance with claim **1** wherein said first video display format generating means includes means for providing a complete character pattern in a portion of said character space which is less than said total plurality of line signals.

9. A system in accordance with claim **8** wherein said first video display format generating means includes means for generating at least alphabetic character patterns, a complete alphabetic character pattern being provided in said character space portion.

10. A system in accordance with claim **8** wherein said first video display format generating means includes means for generating at least alphanumeric character patterns, a complete alphanumeric character pattern being provided in said character space portion.

11. A system in accordance with claim **10** wherein each of said character spaces has an upper portion comprising a portion of said total plurality of line signals and a lower portion comprising the balance of said total plurality of line signals, said first video display format generating means providing a ticker video display format wherein said upper portions are utilized for providing complete alphabetic character patterns relating to a given stock ticker symbol and said lower portions are utilized for providing at least complete numeric character patterns relating to a given price associated with said symbol, only said upper portion or said lower portion of a given ticker video display format character space being utilized dependent on the type of stock ticker information to be displayed in a given character space.

12. A system in accordance with claim **8** wherein said first video display format generating means includes means for generating at least fraction character patterns, said fraction character patterns including a complete numerator character pattern and a complete denominator character pattern, said complete numerator character pattern being provided in a portion of a given character space which is less than said total plurality of lines and dots, said complete denominator character pattern being provided in a different dot portion of said character space which is adjacent to said numerator character space dot portion, said denominator character pattern space line portion being lower than said numerator character pattern space line portion in said first video display format, whereby a complete fraction character pattern is provided in said adjacent character space portions.

13. A system in accordance with claim **8** wherein said first video display format generating means includes means for generating at least complete alphanumeric character patterns for said character space portions and fraction character patterns, said fraction character patterns including a complete numerator character pattern and a complete denominator character pattern, said complete numerator character pattern being provided in a portion of a given character space which is less than said total plurality of lines and dots, said complete denominator character pattern being provided in a different dot portion of said character space which is adjacent to said numerator character space dot portion, said denominator character pattern space line portion being lower than said numerator character pattern space line portion in said first video display format, whereby a complete fraction character pattern is provided in said adjacent character space portions, said character space comprising 16 of said scan lines, said first video display format generating means generating an alphabetic character pattern in a character space portion comprising the uppermost eight scan lines of said 16 and a numeric character in a character space portion comprising the lowermost eight scan lines of said 16.

14. A system in accordance with claim **13** wherein said first video display format generating means generates a denominator fraction character pattern in a character space portion comprising the lowermost five scan lines of said 16 and a numerator fraction character pattern in said character space portion comprising the five scan lines of said 16 immediately above said lowermost five scan lines.

15. A system in accordance with claim **14** wherein said numerator character space dot portion and said denominator character space dot portion each comprise at least half the total plurality of dots.

16. A system in accordance with claim **1** wherein said system further includes means for controlling which character pattern is to be displayed in a given character space for each character space of said first and second video display formats.

17. A system in accordance with claim **1** wherein said movement controlling means includes means for controlling the total number of character spaces across said screen in said parallel direction in which said character patterns can be displayed.

18. A system in accordance with claim **1** wherein said system includes means for inhibiting the generation of said second video display format without affecting the generation of said first video display format, said combining means including means for enabling only said first video display format for said display device when said second video display format is inhibited.

19. A system in accordance with claim **1** wherein said motion control signal providing means comprises means having a different associated motion control signal corresponding to an incrementally different quantity of said characters, said motion control signal being initially provided in accordance with said initial loading rate and changing to incrementally increase said dot position change to a final initial value in accordance with an incremental increase in said initial loading rate as said character movement accelerate.

20. A system in accordance with claim **19** wherein said motion control signal providing means further comprises means for maintaining said motion control signal final initial value until the quantity of characters stored in said storage register decreases to a predetermined lower level, said motion control signal changing to a control signal indicative of said lower level quantity to decelerate said character movement.

21. A system for providing character patterns for display on a display device screen that utilizes a television raster scan-line pattern to provide a composite video display, each character pattern being displayed in one character space, said system comprising means for generating at least a first video display format of character patterns in response to a first digital signal; and means for providing said composite video display for said display device from said first video display format in which said first display format occupies a given scan-line area of said scan-line pattern on said screen; said character spaces associated with said character patterns each being defined by a predetermined number of scan lines in said scan-line pattern and a predetermined number of elemental dots; said scan lines having a given direction of scan with respect to said screen; said first video display format generating means including means for generating a plurality of dot signals in repetitive sequences during said scan lines to correspond to elemental dots on said display device to divide said device to said first video display format area in a first direction into a plurality of said character spaces, and means for generating a plurality of line signals in repetitive sequences in synchronism with said scan lines to divide said device in said first video display format area in a second direction into at least one row, the combination of a plurality of said dot signals and a plurality of sequences of said line signals defining a character space; said first digital signal having an associated information input rate to said first generating means, said first video display format generating means further including means for controllably periodically shifting each of said character spaces in said row an incremental distance in a given direction parallel to said direction of scan across said screen at a rate dependent on said information input rate to controllably move the character patterns displayed in said character spaces in said given direction across said screen in accordance with said input rate; said shifting means comprising means for varying said shifting rate in accordance with variations in said information input rate for accelerating said character movement in accordance with an acceleration in said information input rate and for decelerating said character movement in accordance with a deceleration in said information input rate; said first video display format generating means further comprising recirculating register storage means for receiving said first digital signal and loading therein said characters in response thereto at an associated data loading rate corresponding to said input rate, said storage register means having a character storage capacity of a plurality of said characters in length, and memory means operatively connected to said storage register means for receiving said characters therefrom upon transfer therefrom, said shifting means comprising motion control means for providing a transfer signal to said storage register for incrementally transferring said characters therefrom to said memory, said first video display format being provided in response to an output from said memory, said motion control means comprising means responsive to changes in said data loading rate for providing a different motion control signal in response to a different quantity of characters being loaded into said storage register for a given character prior to said transfer, and position gating means responsive to said motion control signals for controlling a change in incremental dot position of said given character in said display in accordance with said change in said data loading rate whereby the relative movement of said character patterns across said screen in said direction parallel to said direction of scan may be controlled in accordance with said information input rate.

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