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Maringer et al.

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[45] **July 15, 1975**

[54] **DIGITAL COMPUTER TO DETERMINE THE IGNITION ANGLE IN A PISTON ENGINE**

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[73] Assignee: **Siemens Aktiengesellschaft,** Munich, Germany

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[21] Appl. No.: **468,573**

[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.** **235/151.3;** 235/156; 235/164; 235/196; G06f/7/52

[51] **Int. Cl.** **G06f 15/20**

[58] **Field of Search** 235/151.3, 156, 159, 164, 235/196; 307/220; 328/161

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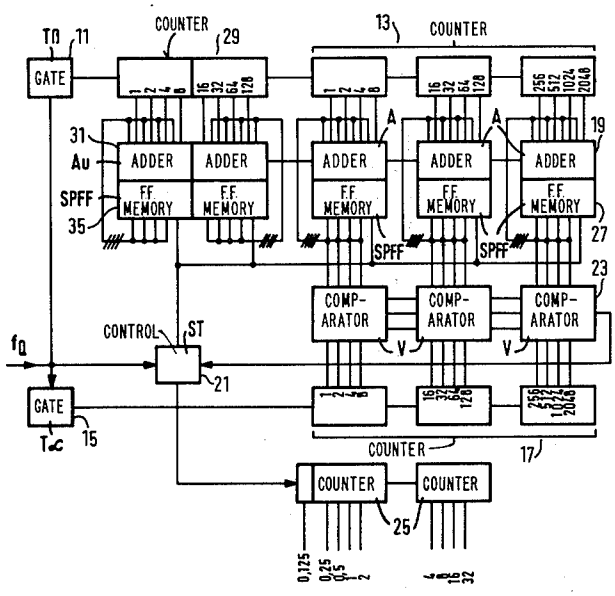
Assistant Examiner—Jerry Smith
Attorney, Agent, or Firm—Kenyon & Kenyon Reilly Carr & Chapin

[57] **ABSTRACT**

A digital computer for determining the ignition angle in a piston engine using the ratio of two pulse counts with a step-down counter preceding the counter for the denominator of the ratio to further include a multiplication factor corresponding to an additional factor in the ratio. The ratio is determined using adders and flip-flop memories coupled in parallel to both the step down counter and the denominator counter with a carry pulse connection between the step down counter adder and the denominator counter adder. A counter is provided for the numerator of the ratio and a comparator used to compare the outputs of the memories and the numerator counter with operation controlled by a control circuit and the result of the division stored in a result counter.

12 Claims, 6 Drawing Figures



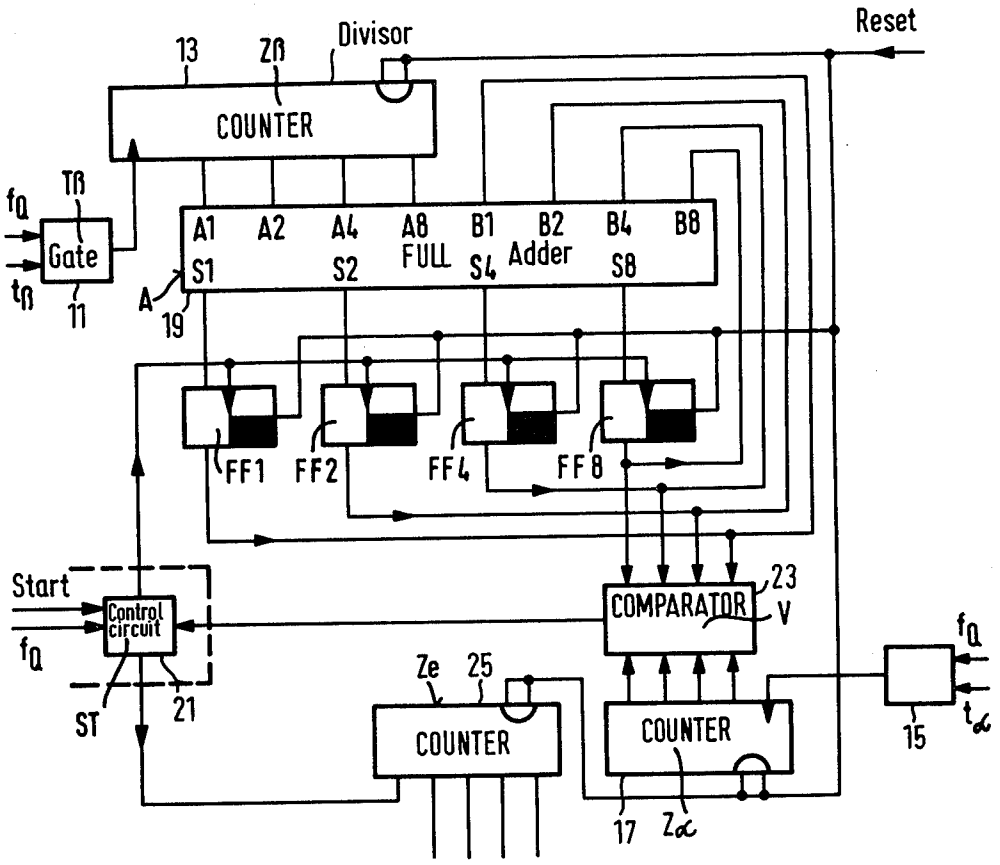

Reset
13
Zß
Divisor
COUNTER
fQ
Tß
Gate
tß
11
A1 A2 A4 A8 B1 B2 B4 B8
S1 S2 FULL S4 Adder S8
A
19
FF1 FF2 FF4 FF8
Start
Control circuit
fQ
ST
21
COMPARATOR
23
V
Ze
25
COUNTER
COUNTER
17
Zα
fQ
15
tα

Fig. 1

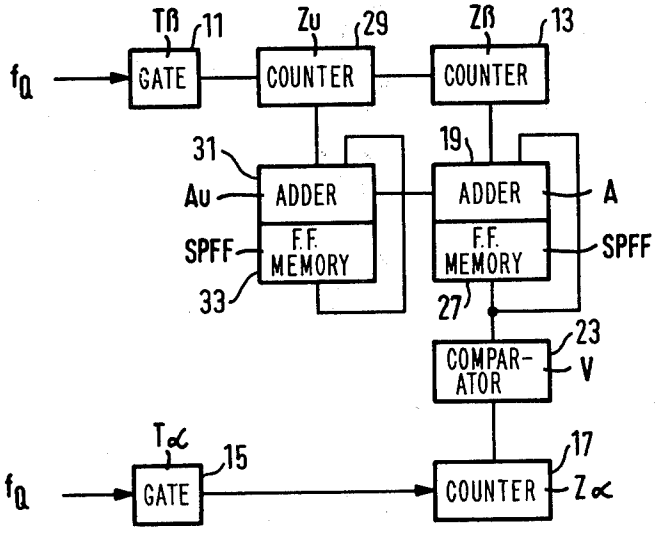

Tß
11
Zu
29
Zß
13
fQ
GATE
COUNTER
COUNTER
31
19
Au
ADDER
ADDER
A
SPFF
F.F. MEMORY
F.F. MEMORY
SPFF
33
27
23
COMPAR-ATOR
V
Tα
15
17
fQ
GATE
COUNTER
Zα

Fig. 2

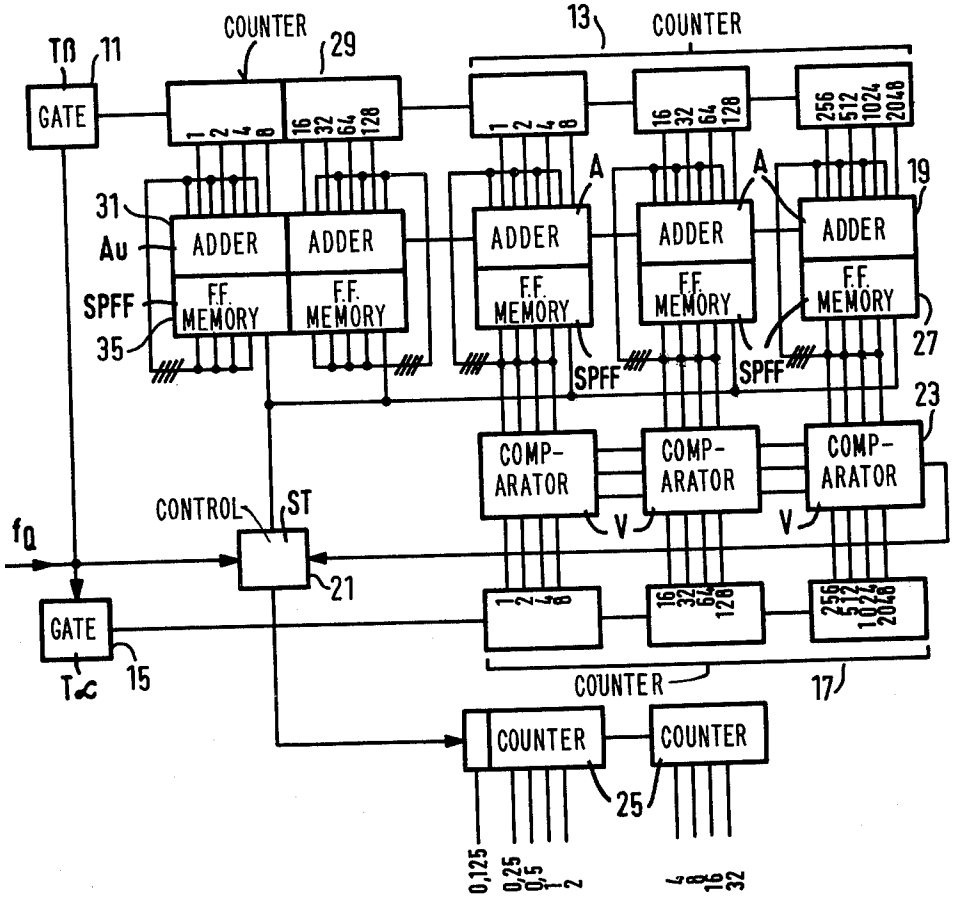
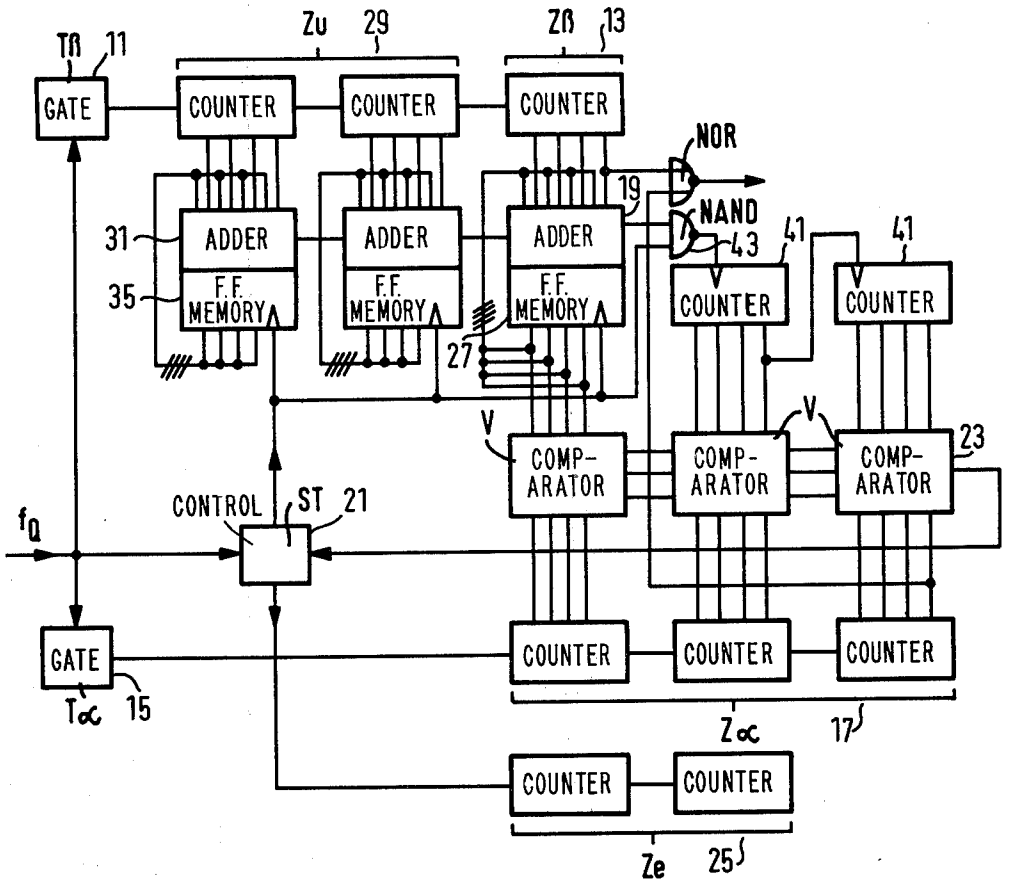

Tß
11
GATE
COUNTER
29
1 2 4 8
16 32 64 128
13
COUNTER
1 2 4 8
16 32 64 128
256 512 1024 2048
31
Au
SPFF
35
ADDER
F.F. MEMORY
A
19
27
SPFF
23
COMP-ARATOR
V
CONTROL
ST
fa
21
GATE
Tc
15
17
COUNTER
25
0,125
0,25
0,5
1
2
4
8
16
32

Fig. 3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Zu 29
ZB 13
GATE
COUNTER
COUNTER
COUNTER
NOR
19
NAND
43
41
41
31
ADDER
ADDER
ADDER
35
F.F. MEMORY
F.F. MEMORY
F.F. MEMORY
COUNTER
COUNTER
27
V
V
COMP-ARATOR
COMP-ARATOR
COMP-ARATOR
23
CONTROL
ST 21
fQ
GATE
Tα 15
COUNTER
COUNTER
COUNTER
Zα 17
COUNTER
COUNTER
Ze 25

Fig. 4

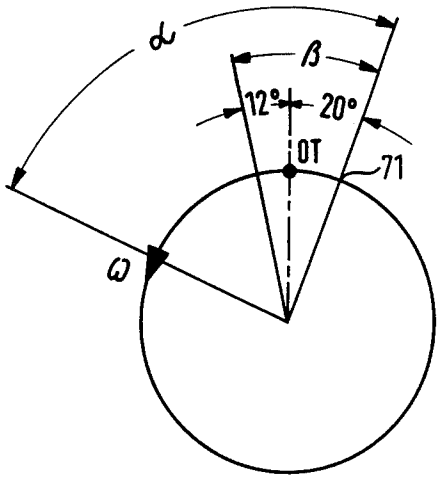
α
β
12°
20°
OT
71
ω

Fig. 5

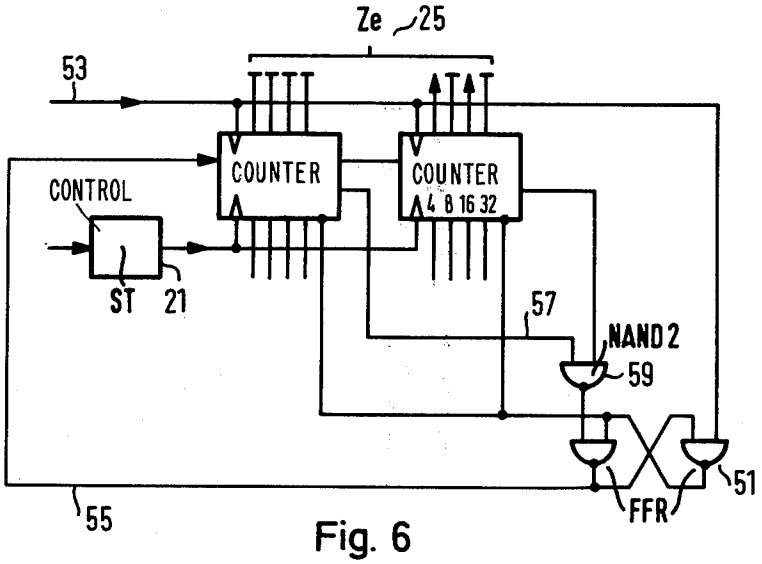
Ze
25
53
COUNTER
COUNTER
4 8 16 32
CONTROL
ST
21
57
NAND 2
59
51
FFR
55

Fig. 6

DIGITAL COMPUTER TO DETERMINE THE IGNITION ANGLE IN A PISTON ENGINE

BACKGROUND OF THE INVENTION

This invention relates to computing apparatus in general, and more particularly to a digital computer for determining the ignition angle in a piston engine. The ignition angle α in a piston engine can be determined by comparing the two time spans t_β and t_α where the time span t_β is the time required for the crankshaft to rotate through an angle β as defined by two marks and the time t_α the time required to rotate through an angle α defined by one of the two marks and the moment of ignition. This can be seen with reference to FIG. 5, illustrating a crank shaft rotating at an angular rotation ω. The time t_β is the time to rotate through the angle β as defined by marks on the crank shaft at the edges of that angle. The time t_α is the time to rotate through the angle α defined by one of the marks and the point of ignition. One simple way of determining these time periods t_β and t_α is by counting a clock output of constant frequency f_Q. The times t_β and t_α are then represented by pulse counts z and z_α respectively. With reference to FIG. 5, it can be seen that if the second mark 71 is assumed as a reference point, the angle α is equal to $\alpha = t\alpha \times \omega$. Similarly, the reference angle β is $+\beta = t_\beta \times \omega$. It then follows that:

$$\frac{\alpha}{\beta} = \frac{t_\alpha \times \omega}{t_\beta \times \omega} = \frac{t_\alpha \times f_Q}{t_\beta \times f_Q} = \frac{z_\alpha}{z_\beta}.$$

From this, the ignition angle α can be calculated as follows:

$$\alpha = \frac{z_\alpha}{z_\beta} \times \beta .$$

From this form of equation, it becomes clear that a computer used to determine the ignition angle must perform a division of two variable pulse counts along with a multiplication of the quotient by a constant number. One commonly known manner of digital dividing is that of adding the divisor until the sum is equal to or greater than the dividend. The number of additions performed is then the result of the division. In terms of the present equation to be solved, a further multiplication by a constant factor is then required.

It is thus, an object of the present invention to provide a digital computing circuit for solving the above equation to thereby determine the ignition angle in a piston engine. Furthermore, it is the object to do this in such a way that the resolution error resulting from the multiplication by the constant factor is compensated for.

SUMMARY OF THE INVENTION

Such a device is provided according to the present invention. Two pulse counts proportional to times t_β and t_α are obtained and stored in digital counters, one being provided for the divisor and dividend. Associated with the divisor counter is an adder and sum memory connected in parallel thereto. A comparator is provided for comparing the output of the sum memory and the output of the dividend counter. A control circuit is included along with a result counter for controlling and counting the multiple additions required in order to accomplish division. Multiplication by a constant factor is obtained through the use of a step down counter preceding the divisor counter, the step down counter dividing by the number which is the additional constant factor in the ratio, i.e., the quantity β in the above noted equation. In order to avoid a resolution error due to this multiplication, adders and sum memories are also provided in parallel with the step down counter with carry pulses from the additional adder provided to the least significant bit of the adder associated with the divisor counter. The result counter is accordingly expanded by a number of least significant bits corresponding to the division in the step down counter.

In the preferred embodiment, optimization is achieved by shortening the divisor counter by as many bits as the number of bits contained in the step down counter and by replacing the adders and sum memories associated with the portion of the counter eliminated with simple binary counters. In this arrangement, the carry output of the adder associated with the remaining divisor counter bits is coupled to the second least significant bit of the counter replacing the eliminated adders and sum memories. In this arrangement, the least significant bits of the result counter is also omitted. In this embodiment, the most significant divisor counter bit and most significant dividend counter bit are connected as two inputs to a NOR gate whose outputs is coupled as disabling inputs to gate circuits at the input to the dividend and divisor counters to block count pulses. The second least significant bit of the counter replacing the eliminated adders and sum memories is coupled through an NAND gate, one input of which is connected to the carry pulse output of the adder and the other to the adding pulse output of the control circuit.

Also illustrated is a result counter which is a presettable by-directional counter set to a 20° crank value prior to the start of computation.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block-logic diagram of a division circuit of the type used in the present invention.

FIG. 2 is a block diagram of a first embodiment according to the present invention.

FIG. 3 is an expanded block diagram illustrating in more detail the block diagram of FIG. 2.

FIG. 4 is a similar block diagram illustrating a optimized version of the embodiment of FIG. 3.

FIG. 5 is a diagram illustrating the angles α and β and the measuring range of the apparatus of the present invention with respect to top dead center.

FIG. 6 is a logic-block diagram of a preferred type of result counter.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a block-logic diagram helpful in understanding the computing apparatus of the present invention. Shown is a first gate circuit 11 having as inputs the output of a clock designated f_Q and a gating pulse t_β representing the time required to rotate through the angle β shown on FIG. 5. For this period of time, the gate 11 will be enabled and provide clock pulses at its output. These clock pulses are counted and stored in a counter 13. In similar fashion, a gate 15 is enabled by a pulse t_α representing the time to rotate through the angle α of FIG. 5 permitting the clock pulses f_Q to be gated

into a counter 17. As a result, after a rotation through the angle β a count will be stored in counter 13 proportional to the time t_β the count being designated z_β and a count will be stored in counter 17 proportional to t_α , the count being designated z_α . In accordance with the equation

$$\alpha = \frac{z_\alpha}{z_\beta} \times \beta$$

it is desired that z_α be divided by z_β. In the present invention, this is carried out by adding the value stored in counter 13 to itself until the sum reaches or exceeds the value stored in counter 17. For the purpose of adding, a full adder 19 is provided. In the embodiment of FIG. 1, both counters 13 and 17 are four bit counters and thus, adder 19 is a four bit full adder. The sum outputs of the adder are coupled respectively as data inputs to storage flip-flops designated FF1, FF2, FF4, FF8. The numbers associated with the flip-flops correspond to the value of their corresponding bit inputs. In similar fashion, the counter outputs are designated A1, A2, A4 and A8 and the second inputs to the adder B1, B2, B4 and B8. In conventional fashion, the adder 19 will add the values present at its two inputs and provide their sum in binary form at its outputs designated S1, S2, S4 and S8. As shown, the second inputs B1 through B8 of the adder are provided respectively, by the outputs of the flip-flops FF1 through FF8. These flip-flops are D type flip-flops with the input from the adders being the data input. The clock input to these flip-flops is provided from a control circuit 21 having as inputs a start command and the clock output f_Q. The flip-flop outputs are also coupled as inputs to a comparator 23. Comparator 23 has as its second inputs the outputs of counter 17. Comparator 23 will provide an output when the value at its input from the flip-flops is equal to or greater than the count stored in counter 17. A line from the control circuit 21 is also provided as an input to a counter 25 which is the result counter.

Operation of this division circuit will best be understood by an example. Prior to starting, all counters are reset by a reset command which is coupled as indicated. The crank shaft rotates through the angles β and α during which time counts are stored in counters 13 and 17. After these counts are gated into the counters, a start command is provided into the control circuit 21. This start command might, for example, set a flip-flop therein to enable a gate permitting the clock pulses f_Q to be provided as outputs to the clock inputs of flip-flops FF1 through FF8 and to the counter 25. For sake of a simple example, assume that the count stored in counter 17 is 8. This means that it will have an output at its most significant bit, i.e., the bit furthest to the left. In order for comparator 23 to have an output indicating equality, the corresponding bit from flip-flop FF8 must also be present. Assume that the count stored in counter 13 is 2. All flip-flops will be reset and up to this point, since no clock-pulses have appeared, any data appearing at their inputs cannot be loaded therein. However, as soon as clock pulses start in response to a start command, any data at the inputs to the flip-flops will be gated into them. In addition prior to the first clock pulse, all the second inputs to the adder, i.e., B1 through B8 will be 0 and only the input A2 from counter 13 will be a 1. As a result, the adder will be providing a 0 output at the sum terminal S1, a 1 output at the sum terminal S2 and 0 outputs on the sum terminals S4 and S8. Thus, when the first clock pulse appears, the 1 appearing at the output of the sum output S2 will be loaded into flip-flop FF2 causing its output to become a 1. The adder will now have an input at A2 and an input at B2. This addition will result in a 0 at S2 and a carry to S4. As a result, when the second clock pulse appears, 0 at the input to FF2 will cause it to be reset and the 1 at the output S4 will cause flip-flop FF4 to be set. Now at the input to full adder 2, there is a 1 on the A2 input and a 1 on the B4 input. As a result, on the third clock pulse, flip-flop FF2 will again be set and FF4 will continue to be set. Now at the input to adder 19 there will be a 1 on the A2 input, a 1 on the B2 input and a 1 on the B4 input. The resulting addition will cause an 0 at the S2 output and a carry to the next stage. This carry, when combined with the 1 on the B4 input will result in a 0 output at S4 and a carry to S8. Thus, on the fourth clock pulse, flip-flops FF2 and FF4 will be reset and flip-flop FF8 set, to have a 1 output which will be in agreement with the 1 input from counter 17 resulting in an output from comparator 23. This output disables the control circuit 21 from outputting further pulses. If a flip-flop is used therein, this pulse may be used to reset that flip-flop. The clock pulses were also provided to the counter 25 which is the result counter. Four pulses occured and the count stored in this counter is now four, the correct answer for a division of eight by two.

However, all that has been accomplished is a division. In accordance with the equations given above, a multiplication by the angle β is also required. Before describing the manner in which this is done, it should be noted that although only four bits are illustrated herein, the dividing unit can be expanded to as many bits as are required. In the embodiments to be described above, 12 bit counters are chosen so that the pulse counts z_β and z_α can reach a maximum of 4096. The clock frequency f_Q is selected so that even at the highest crank shaft speed, the resolution is no lower than 16 pulses per degree of crank angle.

It will be noted that multiplication by the constant reference β can be accomplished by dividing the divisor by rather than multiplying the quotient thereby. Since β is a constant number, this division can be carried out in a simple manner by a step down or dividing counter placed ahead of the divisor counter 13. However, simply providing a step down counter prior to the counter 13 will result in a loss of resolution with the resolution reduced to z_β / $_\beta$.

A circuit which avoids this resolution error is shown in block diagram form on FIG. 2. As in the embodiment of FIG. 1, gates 11 and 15 are provided as are counters 13 and 17 along with the adder 19, an associated flip-flop memory designated 27 and the comparator 23. However, there is provided in addition, a step down counter 29 to perform the multiplication by β by division of the divisor by β. Associated with the step down counter is a further adder 31 and associated flip-flop memory 33 arranged in similar manner to the adder 19 and memory 27 shown on FIG. 1. The carry output of the most significant bit of the adder 31 is coupled to the carry input of the least significant bit of the adder 19. Consider first the case where this additional adder and flip-flop memory 31 and 33 are not present. Assume that the count z_α is 15, that z_β is 5 and that β is 4. The counter 29 would then be arranged to divide by 4.

Thus, it would comprise two binary stages. After four pulses, a carry output would be generated by counter **29** setting the least significant bit in the counter **13.** The fifth bit would remain in the least significant bit of the step down counter **29.** Now, the addition cycles would be carried out as described in connection with FIG. **1.** Fifteen addition cycles would be required before coincidence was found between the count in the counter **17** and that in the flip-flop memory **27.** Thus, the result is **15.** However, the correct answer is **12** and thus, there is a significant error. An even greater error would result where, for example, z_α was 14, z_β was 7 and β again 4. Now, counting 7 pulses through the step down counter, would again result in only the least significant bit of z_β of counter **13** being set with both of the step down stages in counter **29** set. Now **14** additions would be carried out and that result stored before equality was reached. The correct answer in this case, however, is **8** rather than **14.** Thus, it can be seen that the resolution is greatly reduced. However, with the additional adder **31** and flip-flop memory **33,** this does not occur. Now, considering the last example given, additions will take place in the loop between the adder **31** and memory **33** with appropriate carries generated to the adder **19.** As a result of these carries which are added in with the numbers existing at the inputs to the adder **19,** a correct answer will be obtained. This will be better seen in conjunction with the discussion of a more detailed FIG. **3** below.

As alluded to above, β should be selected to be a number which is of power of **2.** In this way, the division within the binary counter can easily be accomplished. In other words, β should be selected to be a number such as 2, 4, 8, 16, 32, 64, 128 etc. It is known from experience that the total ignition angle range in a motor vehicle does not exceed 60° of crank angle. Since it is known that the measuring process will yield the smallest error when $\alpha = \beta$, it makes sense to put the one mark for the reference angle β in the middle of the ignition angle range, assuming that the angle α will probably vary mainly about a mean angle. Based on this, an angle $\beta = 32°$ crank angle is chosen.

If the function of angular speed ω vs. time is quadratic, the selected position of the reference angle relative to the entire ignition angle variation range has a particularly favorable effect. If, however ω is linear, the error is always zero.

Applying this to the example of FIG. **2,** counter **29** would be required to accomplish a division by **32.** With this assumption and assuming the counters **13** and **17** to be **12** bit counters, a 1° crank angle resolution in the result is possible. Consider the following example: The pulse number corresponding to the ignition angle is assumed to be $z_\alpha = 3011$. The pulse number corresponding to the reference angle is assumed to be $z_\beta = 3010$. The pulse number for the reference angle is divided by 32 in the step down counter Z_u with the following result:

$$\frac{3010}{32} = 94.0625$$

When calculated by conventional methods, the resultant crank angle value would be $\alpha = 32.101653°$ crank angle. The result counter of the dividing unit, however, will show a crank angle value of $\alpha = 33°$ crank angle. Thus, the error present is approximately 1° crank angle. This error can be reduced by a higher resolution of the result, i.e., by multiplying by a resolution factor G. The crank angle equation then reads as follows:

$$\alpha = \frac{z_\alpha}{z_\beta} \times \beta \times G.$$

Since this number must also be handled in a binary divider, it is expedient to select a factor of G = 4 since 4 is a power of 2. Again, the factor G is treated the same as the factor β. That is, instead of multiplying the quotient by the factor, the division of the divisor is accomplished by stepping it down. Since these two factors act the same, for the purpose of simplicity, the factor $\beta \times G$ will be referred to as β'. Thus $\beta' = 32 \times 4 = 128$. Therefore, the step down counter such as step down counter **29** of FIG. **2** must divide by 128. Two four bit binary counters in series will divide by 256. Counters are readily available in this form. If two such counters are used, the result counter **25** of FIG. **1** would have to be expanded by three bits to handle the values of 0.5° crank angle, 0.25° and 0.125°. The resolution error would then be 0.125° crank angle. However, only a ¼° crank angle resolution, i.e., a division of 128 is required to determine the ignition angle. As will be seen from the discussion of FIG. **3** below, a resolution of ¼° crank angle is possible through the selection of the economical combination of two 4-bit binary counters for the step down counter.

FIG. **3** shows a computing unit such as that of FIG. **2** in more detail. In this figure, the counters are labelled with the decimal values corresponding to their binary outputs. As shown, the step down counter **29** comprises two four bit counters and the value of its most significant bit is **128.** Both the dividend and divisor counters **17** and **13** respectively are 12-bit counters made up of three four bit counters and have a most significant bit value of 2048. The result counter **25** comprises two four bit counters preceded by an additional stage which may simply comprise a flip-flop and as illustrated it has a bit value of ⅛° crank angle. In all other aspects, the arrangement of FIG. **3** is identical to that shown on FIGS. **1** and **2,** with identical parts given identical reference numerals. As with the previous embodiments, the apparatus of FIG. **3** solves the following equation:

$$\alpha = \frac{t_\alpha \times f_u}{t_\beta \times f_u} \times \beta'$$

During the time periods t_α and t_β, the pulse count z_α and z_β are loaded into the counters **17** and **13** respectively with the content of the counter **13** stepped down or divided by the counter **29.** Thus, the crank angle can be expressed as

$$\alpha = \frac{z_{\alpha'}}{z_{\beta'}} \text{ where } z_{\beta'} = \frac{z_\beta}{\beta \times G}.$$

With the selection of $\beta = 32°$, and an established maximum ignition angle of 64°, z_α cannot become greater than $2 \times z_{\beta'}$. What this means is that the number stored in the series counter made up of the counters **29** and **13** will never take up more than 12 bits and thus the counter stages representing the numbers 16 through 2048 on FIG. **3** are not required in the division operation. That is to say, with reference to FIG. **1,** these outputs of the counter will never be providing in-

puts to the adder. As a result, the circuit can be optimized by omitting the bits corresponding to these numbers. However, the adders and flip-flop memories associated with these bits cannot simply be omitted. Numbers will appear in these associated memories. However, numbers stored in the memories do not come from the adders 19 but come from carry pulses of preceding stages. Thus, all that is necessary is a counter to keep track of the number of carry pulses generated by the stages in which actual addition is taking place. This may be accomplished using a simple binary counter.

Such an optimized arrangement is illustrated on FIG. 4. The two four bit counters representing the most significant bits in the counter **13** of FIG. 3 are omitted. Similarly, their associated adders **19** and storage flip-flops **27** are omitted. In their place are two simple four bit counters **41**. The counter outputs **41** now provide the second inputs to the comparators **23**. The carry output of the adder **19** is coupled through a NAND gate to the first counter **41**. The NAND gate **43** is enabled by clock pulses from the control circuit **21**. Thus, each time a carry is generated, on the next clock pulse, that carry will be entered into the counter **41**. In addition, a NOR gate is provided having as inputs the outputs of the most significant bit of counter **13** and the output of the most significant bit of counter **17**. The output of the NOR gate is coupled as a disabling input to the gate circuits **11** and **15**. (This disabling input is not specifically shown in order to simplify the figure.) This permits the arrangement of the present invention to operate with optimum accuracy at all times. Measurement data is counted into the counters until either the divisor counter z_β i.e., the divisor counter **13** or the dividend counter **17** is full and the most significant bit thereby set. In this embodiment, the NOR gate signals the end of data entry.

Furthermore, in the illustrated arrangement, the carry output of adder **19** is coupled into the second bit of the first counter **41** with the least significant bit bypassed. As a result, only the proper number of stages required for ¼° crank resolution are used and the additional stage in result counter **25** is not required.

The discussion up to this point has been concerned with a relative ignition angle. However, the absolute ignition angle is of interest in an ignition angle measurement. As can be seen from FIG. **5**, the absolute ignition angle will depend on the relationship between the position of the markings defining the angle β with respect to top-dead center designated OT. By placing these marks as illustrated with the second mark **71** 20° after top dead center, a relative ignition angle which is always located in one quadrant is obtained. The selection of 20° after top dead center as a reference point is selected knowing that, in piston engines, timing is almost never retarded beyond 15° after top dead center. However, in order to get the absolute ignition angle, the 20° lead angle must be subtracted from the relative value obtained. On the figure, the angle β extends from 20° after to 12° before top dead center. The range over which ignition angle α can be measured extends 64° from the second mark which is 20° after top dead center, in the direction of angular travel ω. The absolute ignition angle is expressed by the following equation:

$$\alpha_{abs} = \frac{t_\alpha}{t_\beta} \times \beta' - 20°$$

crank angle.

FIG. **6** illustrates a simple manner of carrying out the required subtraction. The result counter **25** is made as a presettable bi-directional counter. A plurality of preset inputs are provided extending from the top, with an arrow indicating that that particular stage is preset to a 1 and a bar designating that that stage is preset to an 0. As illustrated, the 16° and 4° bits are preset so that the counter contains a count of 20°. When control circuit **21** is enabled to start counting, in the manner described above, i.e., in counting the number of successive additions required, the counter is first caused to count down until it reaches zero and then caused to count up so that the final count at the end will be the total angular count minus 20°. Associated with the counters is a count direction flip-flop made up of cross-coupled NAND gates and designated **51**. Prior to the beginning of counting, a reset pulse is provided on line **53** causing the presetting of the stages of the counter **25** representing 16° and 4°. This reset line also resets the flip-flop **51** causing it to have an output on line **55** enabling the counter **25** to count down. Counting down continues until zero is reached as detected by the two output lines **57** which are inputs to a NAND gate **59**. NAND gate **59** then sets the flip-flop **51** changing the signal to the counter **25** to direct it to count up. Thus, the final answer out of the result counter **25** will be an absolute ignition angle.

Thus, a computing arrangement for computing the ignition angle of a piston engine has been shown. Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from the spirit of the invention which is intended to be limited solely by the appended claims.

What is claimed is:

1. Digital computing apparatus to determine the ignition angle in a piston engine using a division circuit for finding the ratio of two pulse counts which division circuit comprises a divisor counter for storing a first pulse count, an adder and sum memory connected in parallel therewith with the outputs of the sum memory coupled as second inputs to the adder, a dividend counter for storing a second pulse count a comparator having as inputs the outputs of the sum memory and the dividend counter, a clock, a result counter, and a control circuit enabled by a start command to couple said clock to said adder and sum memory to cause successive additions to be carried out, said control circuit being disabled by an output from said comparator, said control circuit also coupling said clock to said result counter when enabled to cause said result counter to count the number of successive additions carried out, wherein the improvement comprises:

a. a step down counter in series with said divisor counter having its most significant bit output couled to the least significant bit input of said divisor counter to carry out a division by an additional factor of the ratio;

b. a further adder and sum memory connected in parallel with said step down counter, with the carry pulses from the last stage of said further adder provided as carry inputs to the least significant bit of the adder associated with said divisor counter.

2. Digital computing apparatus according to claim **1** and further including additional stages in said result counter corresponding to a percentage of said additional factor.

3. Digital computing apparatus according to claim 2 wherein said divisor counter has a number of stages omitted equal to the number of stages in said step down counter, with the adders and sum memories normally associated with said omitted stages replaced by a counter.

4. Digital computing apparatus according to claim 1 wherein said divisor counter has a number of stages omitted equal to the number of stages in said step down counter, with the adders and sum memories normally associated with said omitted stages replaced by an additional counter.

5. Digital computing apparatus according to claim 4 wherein the carry output of the last adder associated with said divisor counter is coupled to the second least significant bit of said additional counter.

6. Digital computing apparatus according to claim 5 wherein the second least significant bit of said additional counter is coupled to said carry output through an NAND gate having a second input coupled to the output of said control circuit.

7. Digital computing apparatus according to claim 4 wherein means are provided to gate pulses into said step down counter and said dividend counter and wherein the most significant bit output of said divisor counter and the most significant bit output of said dividend counter are inputs to a NOR gate having its output coupled to disable said means to gate.

8. Digital computing apparatus according to claim 1 wherein said result counter is a presettable bi-directional counter preset to a 20° crank angle prior to the start of the computation.

9. Digital computing apparatus according to claim 1 wherein said additional factor is an angle β corresponding to a 32° crank angle.

10. Digital computing apparatus to determine the ignition angle in a piston engine from the ratio of two pulse counts comprising:

a. a divisor counter;
b. a step down counter in series with said divisor counter;
c. a first adder and sum memory coupled in parallel with said divisor counter;
d. a dividend counter;
e. a comparator having as inputs the outputs of said sum memory and of said dividend counter and providing an output when the input from said sum memory equals or exceeds the input from said dividend counter;
f. a result counter;
g. a clock;
h. first gating means for gating pulses from said clock into said dividend counter;
i. second gating means for gating pulses from said clock into said step down counter;
j. a second adder and sum memory in parallel with said step down counter with the carry output of the most significant bit of said second adder coupled to the carry input of the least significant bit of said first adder;
k. control circuit means responsive to a start command to couple said clock to said first and second adders and sum memories to load the adder outputs into the sum memory inputs, said control circuit also coupling said clock pulses to said result counter, said control circuit being disabled by an output from said comparator.

11. Digital computing apparatus for determining the ignition angle α in a piston engine from the ratio of two pulse counts, a first pulse count z_β, being proportional to the time t_β for the crank shaft to rotate through an angle β as defined by two reference marks, and a second pulse count z_α proportional to the time t_α required for the crank shaft to rotate through the angle α as defined by one of said reference marks and the point of ignition, the count z_β being the divisor of said ratio and the count z_β the dividend, said ratio being multipled by the angle β to obtain said angle comprising:

a. a clock;
b. a step down counter having a modulus equal to said angle β;
c. a divisor counter in series with said step down counter, the most significant bit output of said step down counter being the input to the least significant bit of said divisor counter;
d. a dividend counter;
e. first gating means for gating clock pulses into said step down counter for a time t_β to store in said step down counter and said divisor counter the count z_β ;
f. second gating means for coupling said clock to said dividend counter for a time t_α to thereby store a count z_α ; and
g. means for dividing the count stored in said step down counter and divisor counter into the count stored in said dividend counter by carrying out successive additions of the number in said step down counter and divisor counter to itself until it equals the number in said dividend counter, while counting and storing the number of successive additions required to reach said number in said dividend counter.

12. Digital computing apparatus according to claim 11 wherein the number of stages in divisor counter is less by the number of stages in said step down counter than the stages in said dividend counter, and wherein said means for dividing comprise:

a. a full adder having as many stages as said step down counter and divisor counter combined having first inputs coupled to the outputs of said step down and divisor counters;
b. a sum memory coupled to each output of said full adder with the outputs of said sum memories coupled back as the second input to respect stages of said adder;
c. a further counter having its input coupled to the carry output of said adder, the number of stages in said further counter being equal to the number of stages in said step down counter;
d. a comparator having as first inputs the outputs of said dividend counter and as second inputs the outputs of said further counter and as many stages of said sum memory as required to provide a number of second inputs equal to the number of first inputs;
e. a result counter;
f. a control circuit responsive to a start command for coupling clock pulses to said sum memories to carry out successive additions in said adders, said control circuit further coupling said clock pulses to said result counter, said control circuit being disabled from providing further pulses by an output from said comparator indicating that its second inputs represent a number equal to or greater than that represented by its first input.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 3,895,222

DATED : July 15, 1975

INVENTOR(S) : Albert Maringer et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In column 1, line 23 change "z and z_{α}" to --z_{β} and z_{α}--

Signed and Sealed this

twenty-fifth Day of *November 1975*

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks