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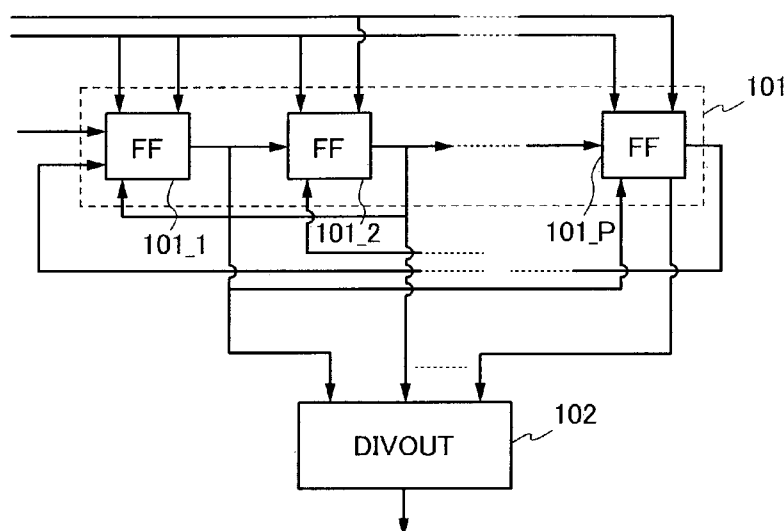
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(54) Title: DIVIDER CIRCUIT

FIG. 1



(57) Abstract: A divider circuit includes a shift register which generates $2X$ (X is a natural number greater than or equal to 2) pulse signals in accordance with a first clock signal or a second clock signal and outputs them, and a divided signal output circuit which generates a signal to be a third clock signal with a cycle X times longer than a cycle of the first clock signal in accordance with the $2X$ pulse signals and outputs it. The divided signal output circuit includes X first transistors which control whether voltage of the signal to be the third clock signal is set to first voltage; and X second transistors which control whether voltage of the signal to be the third clock signal is set to second voltage.

DESCRIPTION

DIVIDER CIRCUIT

5 TECHNICAL FIELD

[0001]

One embodiment of the present invention relates to a divider circuit.

BACKGROUND ART

10 [0002]

In recent years, a divider circuit has been used for driving a digital circuit with the use of a plurality of clock signals each with a different cycle from each other.

[0003]

As an example of a conventional divider circuit, a divider circuit including a
15 flip-flop can be given (e.g., Patent Document 1).

[Reference]

[Patent Document]

[0004]

[Patent Document 1] Japanese Published Patent Application No. H05-048432

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DISCLOSURE OF INVENTION

[0005]

For example, although the conventional divider circuit including a flip-flop, which is disclosed in Patent Document 1, can have a simple circuit configuration, a
25 malfunction might occur in the case where a clock signal with a short cycle is divided. For example, since the conventional divider circuit including a flip-flop generates an output signal by selectively outputting power supply voltage, operation speed is slow, and in the case where a clock signal with a short cycle is generated by the divider circuit, a malfunction might occur and a clock signal is not generated in some cases.

30 [0006]

One embodiment of the present invention is to prevent a malfunction in dividing operation of a divider circuit.

[0007]

According to one embodiment of the present invention, generated is a plurality of pulse signals which are voltage signals each having a value set in accordance with voltage of an input clock signal, and generated is a clock signal with a cycle N times (N is a natural number greater than or equal to 2) longer than a cycle of the input clock signal, with the use of the plurality of generated pulse signals.

[0008]

One embodiment of the present invention is a divider circuit including a shift register which is supplied with a first clock signal and a second clock signal, generates $2X$ (X is a natural number greater than or equal to 2) pulse signals sequentially outputting pulses, in accordance with the first clock signal and the second clock signal, and outputs the generated $2X$ pulse signals; and a divided signal output circuit which generates a signal to be a third clock signal with a cycle X times longer than a cycle of the first clock signal, in accordance with the $2X$ pulse signals, and outputs the generated signal to be the third clock signal. The divided signal output circuit includes X first transistors each having a source, a drain, and a gate, in which different pulse signal among the first to X -th pulse signals of the $2X$ pulse signals is input to the respective gates of the X first transistors. In other words, the first to X -th pulse signals among the $2X$ pulse signals are separately input to the respective gates of the X first transistors. The X first transistors control whether voltage of a signal to be the third clock signal is set to first voltage; and X second transistors each having a source, a drain, and a gate, in which different pulse signal among the $(X + 1)$ -th to $2X$ -th pulse signals of the $2X$ pulse signals is input to the respective gates of the X second transistors. In other words, the $(X + 1)$ -th to $2X$ -th pulse signals of the $2X$ pulse signals are separately input to the respective gates of the X second transistors. The X second transistors control whether voltage of the signal to be the third clock signal is set to second voltage.

[0009]

One embodiment of the present invention is a divider circuit including a first unit divider circuit which is supplied with a first clock signal and a second clock signal and generates a third clock signal with a cycle X times (X is a natural number greater than or equal to 2) longer than a cycle of the first clock signal; and a second unit divider

circuit which is supplied with the third clock signal and generates a fourth clock signal with a cycle K times (K is a natural number greater than or equal to 2) longer than the cycle of the third clock signal in accordance with the third clock signal. The first unit divider circuit includes a shift register which generates $2X$ (X is a natural number greater than or equal to 2) pulse signals sequentially outputting pulses, in accordance with the first clock signal and the second clock signal, and outputs the generated $2X$ pulse signals; and a divided signal output circuit which generates a voltage signal in accordance with the $(2 \times X)$ pulse signals, and outputs the generated voltage signal as the third clock signal. The divided signal output circuit includes X first transistors each having a source, a drain, and a gate, in which different pulse signal among the first to X -th pulse signals of the $2X$ pulse signals is input to the respective gates of the X first transistors. In other words, the first to X -th pulse signals among the $2X$ pulse signals are separately input to the respective gates of the X first transistors. The X first transistors control whether voltage of the voltage signal is set to first voltage, and X second transistors each having a source, a drain, and a gate, in which different pulse signal among the $(X + 1)$ -th to $2X$ -th pulse signals of the $2X$ pulse signals is input to the respective gates of the X second transistors. In other words, the $(X + 1)$ -th to $2X$ -th pulse signals of the $2X$ pulse signals are separately input to the respective gates of the X second transistors. The X second transistors control whether voltage of the voltage signal is set to second voltage.

[0010]

According to one embodiment of the present invention, a malfunction can be prevented even in operation of dividing a clock signal with a short cycle.

25 BRIEF DESCRIPTION OF DRAWINGS

[0011]

In the accompanying drawings:

FIG. 1 is a block diagram illustrating an example of a structure of a divider circuit in Embodiment 1;

30 FIGS. 2A to 2C each illustrate an example of a structure of a shift register in a divider circuit in Embodiment 2;

FIGS. 3A and 3B each illustrate an example of a structure of a divided signal output circuit in a divider circuit in Embodiment 2;

FIGS. 4A to 4 C are timing charts each showing an example of operation of a shift register in a divider circuit in Embodiment 2;

5 FIG. 5 is a timing chart showing an example of operation of a divided signal output circuit in a divider circuit in Embodiment 2;

FIG. 6 is a timing chart showing an example of operation of a divided signal output circuit in a divider circuit in Embodiment 2;

10 FIG. 7 is a block diagram illustrating an example of a structure of a divider circuit in Embodiment 3;

FIGS. 8A to 8D are cross-sectional schematic views each illustrating an example of a structure of a transistor in Embodiment 4;

FIGS. 9A to 9C are cross-sectional schematic views illustrating a method for manufacturing the transistor illustrated in FIG. 8A;

15 FIGS. 10A and 10B are cross-sectional schematic views illustrating a method for manufacturing the transistor illustrated in FIG. 8A; and

FIG. 11 is a block diagram illustrating an example of a structure of a semiconductor device in Embodiment 5.

20 BEST MODE FOR CARRYING OUT THE INVENTION

[0012]

Hereinafter, examples of embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description and it will be easily understood by those skilled in the art
25 that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be interpreted as being limited to the description of the embodiments to be given below.

[0013]

30 Note that contents of the embodiments can be combined with or replaced with each other as appropriate.

[0014]

(Embodiment 1)

In this embodiment, a divider circuit including a shift register will be described.

[0015]

5 A structure of the divider circuit of this embodiment will be described with reference to FIG. 1. FIG. 1 is a block diagram illustrating an example of the structure of the divider circuit of this embodiment.

[0016]

10 The divider circuit illustrated in FIG. 1 includes a shift register 101 and a divided signal output circuit (also referred to as DIVOUT) 102.

[0017]

15 A clock signal is input to the shift register 101. For example, a clock signal CLK1 (also referred to as a signal CLK1) and a clock signal CLK2 (also referred to as a signal CLK2) are input to the shift register 101 as the clock signal. Further, the shift register 101 outputs $2X$ (X is a natural number greater than or equal to 2) pulse signals.

[0018]

20 As a signal in the divider circuit of this embodiment, for example, a signal with voltage can be used. As the signal with voltage (also referred to as a voltage signal), an analog signal or a digital signal, which has at least first voltage and second voltage, can be used. For example, a binary digital signal such as a clock signal becomes at a low level and a high level, thereby having the first voltage (low-level voltage) and the second voltage (high-level voltage). Further, each of the high-level voltage and the low-level voltage preferably has a fixed value. However, since noise or the like has an influence on an electronic circuit, each of the high-level voltage and the low-level voltage does not necessarily have a fixed value and may have a value within a fixed range where a value can be seen as substantially equivalent. Further, as the signal in the divider circuit of this embodiment, a signal having first to third voltages may be used. As the third voltage, for example, voltage higher than or equal to the second voltage can be used.

30 [0019]

Note that voltage generally refers to a difference between potentials at two points (also referred to as a potential difference). However, values of both a voltage

and a potential are represented using volt (V) in a circuit diagram or the like in some cases, so that it is difficult to discriminate between them. Thus, in this specification, a potential difference between a potential at one point and a reference potential is sometimes used as a voltage at the point unless otherwise specified.

5 [0020]

The signal CLK1 and the signal CLK2 are clock signals whose waveforms are different from each other by a 1/2 cycle.

[0021]

The shift register 101 includes sequential circuits (also referred to as FFs)
10 (sequential circuits 101_1 to 101_P) of P ($P = 2 \times X$) stages, which includes P sequential circuits.

[0022]

The signal CLK1 or the signal CLK2 is input to the sequential circuits. Further, the sequential circuits output a signal having voltage set in accordance with the
15 input clock signal as an output signal. The sequential circuit includes a transistor for controlling voltage of the output signal, for example.

[0023]

Note in the divider circuit, the transistor includes at least a source, a drain, and a gate unless otherwise specified.

20 [0024]

A source refers to a source region, part of or the whole of a source electrode, or part of or the whole of a source wiring. A conductive layer having a function of both a source electrode and a source wiring is referred to as a source in some cases without distinction between a source electrode and a source wiring.

25 [0025]

A drain refers to a drain region, part of or the whole of a drain electrode, or part of or the whole of a drain wiring. A conductive layer having a function of both a drain electrode and a drain wiring is referred to as a drain in some cases without distinction between a drain electrode and a drain wiring.

30 [0026]

A gate refers to part of or the whole of a gate electrode, or part of or the whole of a gate wiring. A conductive layer having a function of both a gate electrode and a

gate wiring is referred to as a gate in some cases without distinction between a gate electrode and a gate wiring.

[0027]

5 A source and a drain of a transistor interchange with each other depending on a structure, an operation condition, or the like of a transistor in some cases.

[0028]

10 As a transistor in the divider circuit, a transistor having a semiconductor layer including a semiconductor (e.g., silicon) belonging to Group 14 of the periodic table or an oxide semiconductor layer can be used, for example. The semiconductor layer including a semiconductor belonging to Group 14 or the oxide semiconductor layer has a function of a channel formation layer of a transistor. The oxide semiconductor layer is highly purified to be an intrinsic (also referred to as I-type) or substantially intrinsic semiconductor layer. Note that the high purification means at least one of the following concepts: removal of hydrogen from an oxide semiconductor layer as much as possible; and reduction of defects, which are caused by oxygen deficiency in an oxide semiconductor layer, by supply of oxygen to the oxide semiconductor layer. Further, all transistors included in the divider circuit can have the same conductivity type. When all the transistors have the same conductivity type, a manufacturing process can be simplified as compared to the case where transistors with different conductivity types are used.

[0029]

25 The sequential circuit sets the voltage of the output signal in accordance with the voltage of the clock signal in such a manner that a transistor for controlling the voltage of the output signal of the sequential circuit is turned on. For example, in the sequential circuit in the odd-numbered stage, the transistor for controlling the voltage of the output signal sets the voltage of the output signal in accordance with the signal CLK1. In the sequential circuit in the even-numbered stage, the transistor for controlling the voltage of the output signal sets the voltage of the output signal in accordance with the signal CLK2. In the transistor for controlling the voltage of the output signal, capacitance is between the gate and either the source or the drain. Therefore, in the sequential circuit, the voltage of the gate of the transistor can be set higher than or equal to power supply voltage. Accordingly, it takes shorter time to set

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the voltage of the output signal to a desired value, and at least part of the voltage of the output signal can be higher than or equal to the power supply voltage. As the capacitance between the gate and either the source or the drain, parasitic capacitance, a capacitor which is additionally provided, or the like can be used.

5 [0030]

The $2X$ pulse signals are input to the divided signal output circuit 102. The divided signal output circuit 102 has a function of generating a signal to be a signal CLK3 with a cycle X times longer than the cycle of the signal CLK1 in accordance with the input $2X$ pulse signals, and outputting the generated signal to be the signal CLK3 as
10 an output signal. Note that generation of a signal with a cycle X times longer than the cycle of the signal CLK1 is also referred to as frequency division.

[0031]

The divided signal output circuit 102 includes at least X transistors Tr1 and X transistors Tr2.

15 [0032]

Different pulse signal among the first to X -th pulse signals is input to the respective gates of the X transistors Tr1. In other words, the first to X -th pulse signals among the $2X$ pulse signals are separately input to the respective gates of the X transistors Tr1. The transistors Tr1 have a function of controlling whether the voltage
20 of the signal to be the signal CLK3 in a predetermined period is set to the first voltage.

[0033]

Different pulse signal among the $(X + 1)$ -th to $2X$ -th pulse signals is input to the respective gates of the X transistors Tr2. In other words, the $(X + 1)$ -th to $2X$ -th pulse signals of the $2X$ pulse signals are separately input to the respective gates of the X
25 transistors Tr2. The transistors Tr2 have a function of controlling whether the voltage of the signal to be the signal CLK3 in a predetermined period is set to the second voltage.

[0034]

An example of the divider circuit of this embodiment includes a shift register
30 and a divided signal output circuit. The shift register has a function of outputting $2X$ pulse signals in accordance with a first clock signal and a second clock signal. The

divided signal output circuit sets voltage of a signal to be a third clock signal in such a manner that X first transistors and X second transistors are sequentially turned on in accordance with the $2X$ pulse signals, and thus outputs the third clock signal with a cycle X times longer than a cycle of the first clock signal. In the shift register in the divider circuit of this embodiment, it takes shorter time to set the voltage of the pulse signal to a desired value. This is because the voltage of the pulse signal to be an output signal is set in accordance with the voltage of the clock signal, for example. Accordingly, with the use of the shift register, operation speed of the divider circuit can be improved, and a malfunction in dividing operation can be prevented.

[0035]

(Embodiment 2)

In this embodiment, an example of a structure of the divider circuit in the above Embodiment 1 will be described.

[0036]

First, an example of a structure of each sequential circuit in the shift register of the divider circuit of the above embodiment will be described with reference to FIGS. 2A to 2C. FIGS. 2A to 2C each illustrate an example of a structure of the sequential circuit in the shift register of the divider circuit of this embodiment.

[0037]

A set signal ST11 (also referred to as a signal ST11), a reset signal RS11 (also referred to as a signal RS11), a reset signal RS12 (also referred to as a signal RS12), a clock signal CK11 (also referred to as a signal CK11), a clock signal CK12 (also referred to as a signal CK12), and power supply voltage V_p are input to each sequential circuit. Further, each sequential circuit outputs an output signal OUT11 (also referred to as a signal OUT11).

[0038]

FIG. 2A illustrates an example of a structure of a sequential circuit in the first stage. The sequential circuit illustrated in FIG. 2A includes transistors 101a to 101k.

[0039]

Voltage V_a is input to one of a source and a drain of the transistor 101a, and the signal ST11 is input to a gate of the transistor 101a.

[0040]

The voltage Va is input to one of a source and a drain of the transistor 101b, and the signal RS11 is input to a gate of the transistor 101b.

[0041]

One of a source and a drain of the transistor 101c is electrically connected to the other of the source and the drain of the transistor 101b, voltage Vb is input to the other of the source and the drain of the transistor 101c, and the signal ST11 is input to a gate of the transistor 101c.

[0042]

Note that one of the voltage Va and the voltage Vb is to be high power supply voltage Vdd and the other of the voltage Va and the voltage Vb is to be low power supply voltage Vss. The high power supply voltage Vdd is relatively higher than the low power supply voltage Vss, and the low power supply voltage Vss is relatively lower than the high power supply voltage Vdd. Values of the voltage Va and the voltage Vb interchange depending on polarity of a transistor or the like in some cases. A potential difference between the voltage Va and the voltage Vb is power supply voltage Vp.

[0043]

The voltage Va is input to one of a source and a drain of the transistor 101d, and the signal CK12 is input to a gate of the transistor 101d.

[0044]

One of a source and a drain of the transistor 101e is electrically connected to the other of the source and the drain of the transistor 101d, the other of the source and the drain of the transistor 101e is electrically connected to the other of the source and the drain of the transistor 101b, and the signal RS12 is input to a gate of the transistor 101e.

[0045]

One of a source and a drain of the transistor 101f is electrically connected to the other of the source and the drain of the transistor 101a, and the voltage Va is input to a gate of the transistor 101f. Note that a portion where the one of the source and the drain of the transistor 101f is connected to the other of the source and the drain of the transistor 101a is also referred to as a node NA1.

[0046]

One of a source and a drain of the transistor 101g is electrically connected to

the other of the source and the drain of the transistor 101a, the voltage Vb is input to the other of the source and the drain of the transistor 101g, and a gate of the transistor 101g is electrically connected to the other of the source and the drain of the transistor 101e.

[0047]

5 The signal CK11 is input to one of a source and a drain of the transistor 101h, and a gate of the transistor 101h is electrically connected to the other of the source and the drain of the transistor 101f. Note that a portion where the gate of the transistor 101h is connected to the other of the source and the drain of the transistor 101f is also referred to as a node NB1.

10 [0048]

One of a source and a drain of the transistor 101i is electrically connected to the other of the source and the drain of the transistor 101h, the voltage Vb is input to the other of the source and the drain of the transistor 101i, and a gate of the transistor 101i is electrically connected to the other of the source and the drain of the transistor 101e.

15 Note that a portion where the gate of the transistor 101i, the other of the source and the drain of the transistor 101b, the one of the source and the drain of the transistor 101c, the other of the source and the drain of the transistor 101e, the gate of the transistor 101g, and one of a source and a drain of the transistor 101k are connected to one another is also referred to as a node NC1.

20 [0049]

The voltage Va is input to one of a source and a drain of the transistor 101j, the other of the source and the drain of the transistor 101j is electrically connected to the other of the source and the drain of the transistor 101a, and a signal FB is input to a gate of the transistor 101j. The signal FB is a feedback signal, which is a signal OUT11 (also referred to as a signal OUT11(101_P)) of the sequential circuit 101_P in the P-th stage.

25 [0050]

The one of the source and the drain of the transistor 101k is electrically connected to the other of the source and the drain of the transistor 101b, the voltage Vb is input to the other of the source and the drain of the transistor 101k, and the signal FB is input to a gate of the transistor 101k.

30 [0051]

FIG. 2B illustrates an example of a structure of the sequential circuits in the second to $((P/2) + 1)$ -th stages.

[0052]

The sequential circuit illustrated in FIG. 2B has a structure, in which the transistor 101j and the transistor 101k are omitted from the structure of the sequential circuit illustrated in FIG. 2A. Therefore, the description of the example of the structure of the sequential circuit illustrated in FIG. 2A is employed as appropriate.

[0053]

FIG. 2C illustrates an example of a structure of the sequential circuits in the $((P/2) + 2)$ -th to P -th stages.

[0054]

The sequential circuit illustrated in FIG. 2C has a structure in which voltage of the node NB1 is output as a signal OUT12, in addition to the structure of the sequential circuit illustrated in FIG. 2B. Therefore, the description of the sequential circuit illustrated in FIG. 2A is employed as appropriate for a portion having the structure same as the structure of the sequential circuit illustrated in FIG. 2B.

[0055]

A start signal SP (also referred to as a signal SP) is input to the sequential circuit in the first stage as the signal ST11. The signal SP is a pulse signal.

[0056]

The signal OUT11 of the sequential circuit in the Q -th (Q is a natural number greater than or equal to 1 and less than or equal to $(P - 1)$) stage is input to the sequential circuit in the $(Q + 1)$ -th stage as the signal ST11.

[0057]

The signal OUT11 of the sequential circuit in the $(U + 1)$ -th (U is a natural number greater than or equal to 1 and less than or equal to $(P - 1)$) stage is input to the sequential circuit in the U -th stage as the signal RS11.

[0058]

The signal OUT11 of the sequential circuit in the first stage is input to the sequential circuit in the P -th stage as the signal RS11.

[0059]

To the sequential circuit in the even-numbered stage, the signal CLK2 is input as the signal CK11 and the signal CLK1 is input as the signal CK12.

[0060]

To the sequential circuit in the odd-numbered stage, the signal CLK1 is input as the signal CK11 and the signal CK12.

[0061]

A signal RST is input to each of the sequential circuits as the signal RS12. The signal RST is a pulse signal. Note that the signal SP can be generated with the use of the signal RST.

[0062]

Next, an example of a structure of a divided signal output circuit in the divider circuit of this embodiment will be described with reference to FIGS. 3A and 3B. FIGS. 3A and 3B each illustrate an example of the structure of the divided signal output circuit in the divider circuit of this embodiment.

[0063]

The divided signal output circuit illustrated in FIG. 3A is a divided signal output circuit in which a shift register includes sequential circuits of four stages. The divided signal output circuit illustrated in FIG. 3A includes transistors 102a to 102m, a delay circuit 102DL1, and a delay circuit 102DL2.

[0064]

A signal S1A, a signal S1B, a signal S2A, a signal S2B, a clock signal CK21 (also referred to as a signal CK21), a reset signal RS21 (also referred to as a signal RS21), and power supply voltage V_p are input to the divided signal output circuit illustrated in FIG. 3A. Further, the divided signal output circuit illustrated in FIG. 3A outputs an output signal OUT21 (also referred to as a signal OUT21). The signal OUT21 is a clock signal in which frequency of the clock signal CLK1 is divided by N . That is, a cycle of the signal OUT21 is N times longer than a cycle of the clock signal CLK1.

[0065]

Voltage V_a is input to one of a source and a drain of the transistor 102a, and the signal S1B is input to a gate of the transistor 102a.

[0066]

The voltage Va is input to one of a source and a drain of the transistor 102b, and the signal S2B is input to a gate of the transistor 102b.

[0067]

One of a source and a drain of the transistor 102c is electrically connected to the other of the source and the drain of the transistor 102b, voltage Vb is input to the other of the source and the drain of the transistor 102c, and the signal S1B is input to a gate of the transistor 102c.

[0068]

The voltage Va is input to one of a source and a drain of the transistor 102d, and the signal CK21 is input to a gate of the transistor 102d.

[0069]

One of a source and a drain of the transistor 102e is electrically connected to the other of the source and the drain of the transistor 102d, and the other of the source and the drain of the transistor 102e is electrically connected to the other of the source and the drain of the transistor 102b, and the signal RS21 is input to a gate of the transistor 102e.

[0070]

One of a source and a drain of the transistor 102f is electrically connected to the other of the source and the drain of the transistor 102a, and the voltage Va is input to a gate of the transistor 102f. Note that a portion where the one of the source and the drain of the transistor 102f is connected to the other of the source and the drain of the transistor 102a is also referred to as a node NA2.

[0071]

One of a source and a drain of the transistor 102g is electrically connected to the other of the source and the drain of the transistor 102a, the voltage Vb is input to the other of the source and the drain of the transistor 102g, and a gate of the transistor 102g is electrically connected to the other of the source and the drain of the transistor 102b. Note that a portion where the gate of the transistor 102g, the other of the source and the drain of the transistor 102b, the one of the source and the drain of the transistor 102c, and the other of the source and the drain of the transistor 102e are connected to one another is also referred to as a node NC2.

[0072]

The signal CK21 is input to one of a source and a drain of the transistor 102h, and a gate of the transistor 102h is electrically connected to the other of the source and the drain of the transistor 102f. Note that a portion where the gate of the transistor 102h is connected to the other of the source and the drain of the transistor 102f is also referred to as a node NB2.

[0073]

The voltage Va is input to one of a source and a drain of the transistor 102i, the other of the source and the drain of the transistor 102i is electrically connected to the other of the source and the drain of the transistor 102h, and the signal S2A is input to a gate of the transistor 102i through the delay circuit 102DL1.

[0074]

One of a source and a drain of the transistor 102j is electrically connected to the other of the source and the drain of the transistor 102h, the voltage Vb is input to the other of the source and the drain of the transistor 102j, and the signal S1B is input to a gate of the transistor 102j.

[0075]

The voltage Va is input to one of a source and a drain of the transistor 102k, the other of the source and the drain of the transistor 102k is electrically connected to the other of the source and the drain of the transistor 102h, and the signal S2B is input to a gate of the transistor 102k.

[0076]

One of a source and a drain of the transistor 102l is electrically connected to the other of the source and the drain of the transistor 102h, the voltage Vb is input to the other of the source and the drain of the transistor 102l, and the signal S1A is input to a gate of the transistor 102l.

[0077]

One of a source and a drain of the transistor 102m is electrically connected to the other of the source and the drain of the transistor 102f, the voltage Vb is input to the other of the source and the drain of the transistor 102m, and the signal S2A is input to a gate of the transistor 102m through the delay circuit 102DL1 and the delay circuit 102DL2.

[0078]

To the sequential circuit illustrated in FIG. 3A, the signal CLK1 is input as the signal CK21, the signal RST is input as the signal RS21, the signal OUT11 of the sequential circuit in the first stage in the shift register 101 (also referred to as a signal OUT11(101_1)) is input as the signal S1A, the signal OUT11 of the sequential circuit in the second stage in the shift register 101 (also referred to as a signal OUT11(101_2)) is input as the signal S1B, the signal OUT11 of the sequential circuit in the third stage in the shift register 101 (also referred to as a signal OUT11(101_3)) is input as the signal S2A, and the signal OUT12 of the sequential circuit 101_4 in the fourth stage in the shift register 101 (also referred to as a signal OUT12(101_4)) is input as the signal S2B.

10 [0079]

The divided signal output circuit illustrated in FIG. 3B is a divided signal output circuit in which the shift register 101 includes sequential circuits of eight stages. The divided signal output circuit illustrated in FIG. 3B includes transistors 102n to 102q in addition to the structure of the divided signal output circuit illustrated in FIG. 3A, and a signal S1C, a signal S1D, a signal S2C, and a signal S2D are further input.

15 [0080]

The voltage Va is input to one of a source and a drain of the transistor 102n, the other of the source and the drain of the transistor 102n is electrically connected to the other of the source and the drain of the transistor 102h, and the signal S2C is input to a gate of the transistor 102n.

20 [0081]

One of a source and a drain of the transistor 102o is electrically connected to the other of the source and the drain of the transistor 102h, the voltage Vb is input to the other of the source and the drain of the transistor 102o, and the signal S1C is input to a gate of the transistor 102o.

25 [0082]

The voltage Va is input to one of a source and a drain of the transistor 102p, the other of the source and the drain of the transistor 102p is electrically connected to the other of the source and the drain of the transistor 102h, and the signal S2D is input to a gate of the transistor 102p.

30 [0083]

One of a source and a drain of the transistor 102q is electrically connected to the other of the source and the drain of the transistor 102h, the voltage Vb is input to the other of the source and the drain of the transistor 102q, and the signal S1D is input to a gate of the transistor 102q.

5 [0084]

Further, to the divided signal output circuit illustrated in FIG. 3B, the signal CLK1 is input as the signal CK21, the signal RST is input as the signal RS21, the signal OUT11 of the sequential circuit in the first stage in the shift register 101 is input as the signal S1A, the signal OUT11 of the sequential circuit in the second stage in the shift register 101 is input as the signal S1B, the signal OUT11 of the sequential circuit in the third stage in the shift register 101 is input as the signal S1C, the signal OUT12 of the sequential circuit in the fourth stage in the shift register 101 is input as the signal S1D, the signal OUT11 of the sequential circuit in the fifth stage in the shift register 101 (also referred to as a signal OUT11(101_5)) is input as the signal S2A, the signal OUT12 of the sequential circuit in the sixth stage in the shift register 101 (also referred to as a signal OUT12(101_6)) is input as the signal S2B, the signal OUT12 of the sequential circuit in the seventh stage in the shift register 101 (also referred to as a signal OUT12(101_7)) is input as the signal S2C, and the signal OUT12 of the sequential circuit in the eighth stage in the shift register 101 (also referred to as a signal OUT12(101_8)) is input as the signal S2D.

20 [0085]

Note that the delay circuit 102DL1 and the delay circuit 102DL2 are each formed using $2N$ (N is a natural number) invertors which are electrically connected in parallel, for example.

25 [0086]

Next, an example of operation of the divider circuit of this embodiment will be described.

[0087]

First, an example of operation of the shift register 101 in the divider circuit will be described with reference to FIGS. 4A to 4C. FIGS. 4A to 4C are timing charts each showing an example of operation of the shift register in the divider circuit of this

30

embodiment. Note that here, as an example, all the transistors 101a to 101i have N-type conductivity, the high power supply voltage Vdd is input as the voltage Va, and the low power supply voltage Vss is input as the voltage Vb.

[0088]

5 FIG. 4A is a timing chart showing an example of operation of the sequential circuit in the odd-numbered stage. In FIG. 4A, at a time T11, the signal CK11 and the signal CK12 are each set to a high level, the signal ST11 is at a low level, the signal RS11 is at a low level, and the signal RS12 is set to a high level.

[0089]

10 At this time, the sequential circuit is set to a reset state. Further, the transistor 101b and the transistor 101c are turned off and the transistor 101d and the transistor 101e are turned on; therefore, voltage of the node NC1 (also referred to as V_{NC1}) becomes equivalent to the value of the voltage Va and the transistor 101g and the transistor 101i are turned on. In addition, the transistor 101a is turned off and the transistor 101g is in an on state; therefore, voltage of the node NA1 (also referred to as V_{NA1}) becomes equivalent to the value of the voltage Vb. Moreover, since the transistor 101f is in an on state, voltage of the node NB1 (also referred to as V_{NB1}) becomes equivalent to the value of the voltage Vb, and the transistor 101h is turned off. The transistor 101h is turned off and the transistor 101i is turned on, so that the signal
15 OUT11 is set to a low level.

[0090]

 Next, at a time T12, the signal CK11 and the signal CK12 are each set to a low level, the signal ST11 is set to a high level, the signal RS11 remains at a low level, and the signal RS12 remains at a high level.

25 [0091]

 At this time, the sequential circuit is set to a set state. The transistor 101b remains off, the transistor 101c is turned on, the transistor 101d is turned off, and the transistor 101e remains on; therefore, the voltage of the node NC1 remains equivalent to the value of the voltage Vb and the transistor 101g and the transistor 101i are turned off.
30 Further, the transistor 101a is turned on and the transistor 101g is turned off; therefore, the voltage of the node NA1 becomes equivalent to the value of the voltage Va. Moreover, since the transistor 101f is in an on state, the voltage of the node NB1

becomes equivalent to the value of the voltage V_a , the transistor 101h is turned on, the voltage of the node NA1 and the voltage of the node NB1 become equivalent to the value of the voltage V_a ; accordingly, the transistor 101f is turned off. The transistor 101h is turned on and the transistor 101i is turned off, so that the signal OUT11 remains at a low level.

[0092]

Next, at a time T13, the signal CK11 and the signal CK12 are each set to a high level, the signal ST11 is set to a low level, the signal RS11 remains at a low level, and the signal RS12 is set to a low level.

[0093]

At this time, the transistor 101b remains off, the transistor 101c is turned off, the transistor 101d is turned on, and the transistor 101e is turned off; therefore, the voltage of the node NC1 remains equivalent to the value of the voltage V_b , and the transistor 101g and the transistor 101i remain off. Further, the transistor 101a is turned off and the transistor 101g remains off; therefore, the voltage of the node NA1 remains equivalent to the value of the voltage V_a . The transistor 101f remains off and the node NB1 enters a floating state. The transistor 101h remains on and the transistor 101i remains off, so that the voltage of the other of the source and the drain of the transistor 101h is increased. Then, the voltage of the node NB1 is increased because of capacitive coupling due to parasitic capacitance generated between the gate of the transistor 101h and the other of the source and the drain of the transistor 101h. This is so-called bootstrap operation. The voltage of the node NB1 is increased to a value which is larger than the sum of the voltage V_a and the threshold voltage of the transistor 101h (also referred to as $V_{th_{101h}}$), that is, $V_a + V_{th_{101h}} + V_x$. At this time, the transistor 101h remains on. Further, the signal OUT11 is set to a high level.

[0094]

Next, at a time T14, the signal CK11 and the signal CK12 are each set to a low level, the signal ST11 remains at a low level, the signal RS11 is set to a high level, and the signal RS12 remains at a low level.

[0095]

At this time, the transistor 101b is turned on, the transistor 101c and the transistor 101e remain off, and the transistor 101d is turned off; therefore, the voltage of

the node NC1 becomes equivalent to the value of the voltage Va, and the transistor 101g and the transistor 101i are turned on. Further, the transistor 101a remains off and the transistor 101g is turned on; therefore, the voltage of the node NA1 becomes equivalent to the value of the voltage Vb and the transistor 101f is turned on. Since transistor 101f is turned on, the voltage of the node NB1 becomes equivalent to the value of the voltage Vb and the transistor 101h is turned off. Since the transistor 101h is turned off and the transistor 101i is turned on, the signal OUT11 is set to a low level.

[0096]

Thus, the sequential circuit in the odd-numbered stage outputs a pulse of the signal OUT11.

[0097]

FIG. 4B is a timing chart showing an example of operation of the sequential circuit in the even-numbered stage. In FIG. 4B, at the time T11, the signal CK11 is set to a low level, the signal CK12 is set to a high level, the signal ST11 is set to a low level, the signal RS11 is set to a low level, and the signal RS12 is set to a high level.

[0098]

At this time, the sequential circuit is set to a reset state. The transistor 101b and the transistor 101c are turned off, and the transistor 101d and the transistor 101e are turned on; therefore, the voltage of the node NC1 becomes equivalent to the value of the voltage Va, and the transistor 101g and the transistor 101i are turned on. Further, the transistor 101a is turned off and the transistor 101g is turned on; therefore, the voltage of the node NA1 becomes equivalent to the value of the voltage Vb. Since the transistor 101f is in an on state, the voltage of the node NB1 becomes equivalent to the value of the voltage Vb and the transistor 101h is turned off. The transistor 101h is turned off and the transistor 101i is turned on, so that the signal OUT11 is set to a low level.

[0099]

Next, at the time T12, the signal CK11 is set to a high level, the signal CK12 is set to a low level, the signal ST11 remains at a low level, the signal RS11 remains at a low level, and the signal RS12 remains at a high level.

[0100]

At this time, the transistor 101b and the transistor 101c remain off, the

transistor 101e remains on, and the transistor 101d is turned off; therefore, the voltage of the node NC1 remains equivalent to the value of the voltage Va, and the transistor 101g and the transistor 101i remain on. Further, the transistor 101a remains off and the transistor 101g remains on; therefore, the voltage of the node NA1 remains equivalent to the value of the voltage Vb. Since the transistor 101f remains on, the voltage of the node NB1 remains equivalent to the value of the voltage Vb and the transistor 101h remains off. The transistor 101h remains off and the transistor 101i remains on, so that the signal OUT11 remains at a low level.

[0101]

Next, at the time T13, the signal CK11 is set to a low level, the signal CK12 is set to a high level, the signal ST11 is set to a high level, the signal RS11 remains at a low level, and the signal RS12 is set to a low level.

[0102]

At this time, the sequential circuit is set to a set state. The transistor 101b remains off, the transistor 101c is turned on, the transistor 101d is turned on, and the transistor 101e is turned off; therefore, the voltage of the node NC1 becomes equivalent to the value of the voltage Vb and the transistor 101g and the transistor 101i are turned off. Further, the transistor 101a is turned on and the transistor 101g is turned off; therefore, the voltage of the node NA1 becomes equivalent to the value of the voltage Va. Since the transistor 101f remains on, the voltage of the node NB1 becomes equivalent to the value of the voltage Va and the transistor 101h is turned on. When the voltage of the node NA1 and the voltage of the node NB1 become equivalent to the value of the voltage Va, the transistor 101f is turned off. The transistor 101h is turned on and the transistor 101i is turned off, so that the signal OUT11 remains at a low level.

[0103]

Next, at the time T14, the signal CK11 is set to a high level, the signal CK12 is set to a low level, the signal ST11 is set to a low level, the signal RS11 remains at a low level, and the signal RS12 remains at a low level.

[0104]

At this time, the transistor 101b and the transistor 101e remain off, and the transistor 101c and the transistor 101d are turned off; therefore, the voltage of the node NC1 remains equivalent to the value of the voltage Vb and the transistor 101g and the

transistor 101i remain off. Further, the transistor 101a is turned off and the transistor 101g remains off; therefore, the voltage of the node NA1 remains equivalent to the value of the voltage Va. The transistor 101f remains off, the node NB1 enters a floating state, the transistor 101h remains on, and the transistor 101i remains off; therefore, the voltage of the other of the source and the drain of the transistor 101h is increased. Then, the voltage of the node NB1 is increased because of capacitive coupling due to parasitic capacitance generated between the gate of the transistor 101h and the other of the source and the drain of the transistor 101h. The voltage of the node NB1 is increased to a value which is larger than the sum of the voltage Va and the threshold voltage of the transistor 101h (also referred to as V_{th101h}), that is, $V_a + V_{th101h} + V_x$. At this time, the transistor 101h remains on, and the transistor 101i remains off, so that the signal OUT11 is set to a high level.

[0105]

Next, at a time T15, the signal CK11 is set to a low level, the signal CK12 is set to a high level, the signal ST11 remains at a low level, the signal RS11 is set to a high level, and the signal RS12 remains at a low level.

[0106]

At this time, the transistor 101c and the transistor 101e remain off and the transistor 101b is turned on; therefore, the voltage of the node NC1 becomes equivalent to the value of the voltage Va, and the transistor 101g and the transistor 101i are turned on. Further, the transistor 101a remains off and the transistor 101g is turned on; therefore, the voltage of the node NA1 becomes equivalent to the value of the voltage Vb. Since the transistor 101f is turned on, the voltage of the node NB1 becomes equivalent to the value of the voltage Vb and the transistor 101h is turned off. The transistor 101h is turned off and the transistor 101i is turned on, so that the signal OUT11 is set to a low level.

[0107]

Thus, the sequential circuit outputs a pulse of the signal OUT11.

[0108]

Further, an example of operation of the sequential circuit illustrated in FIG. 2A will be described with the use of the description of the example of operation of the

sequential circuit described with reference to FIG. 4A.

[0109]

In the sequential circuit illustrated in FIG. 2A, in addition to the operation of the sequential circuit illustrated in FIG. 2B, the transistor 101j and the transistor 101k are turned on when a pulse of the signal FB is input. When the transistor 101j is turned on, the voltage of the node NA1 becomes equivalent to the value of the voltage Va and the transistor 101f is turned off. When the transistor 101k is turned on, the voltage of the node NB1 becomes equivalent to the value of the voltage Vb and the transistor 101g and the transistor 101i are turned off.

[0110]

Further, operation of the sequential circuit illustrated in FIG. 2C is the same as the operation of the sequential circuit illustrated in FIG. 2B described above; therefore, the description of the example of the operation of the sequential circuit illustrated in FIG. 2B is employed as appropriate.

[0111]

FIG. 4C is a timing chart showing an example of operation of the shift register illustrated in FIG. 1.

[0112]

In FIG. 4C, first, a pulse of the signal RST is input, so that each sequential circuit is set to a reset state. Then, a pulse of the signal SP is input, so that the sequential circuit 101_1 in the first stage is set to a set state. In the next period, the sequential circuit 101_1 in the first stage outputs the pulse of the signal OUT11. Further, the pulse of the signal OUT11 of the sequential circuit 101_1 in the first stage is input to the sequential circuit 101_2 in the second stage as the set signal ST11, so that the sequential circuit 101_2 in the second stage is set to a set state. The sequential circuit 101_2 in the second stage outputs the pulse of the signal OUT11 in the next period. The above operation is sequentially performed in up to and including the sequential circuit 101_P in the P-th stage. Thus, the pulses of the signals OUT11 of the sequential circuit 101_1 in the first stage to the sequential circuit 101_P in the P-th stage are sequentially output. The above is an example of operation of the shift register in the divider circuit of this embodiment.

[0113]

Further, as an example of operation of a divided signal output circuit in a divider circuit of this embodiment, an example of operation of the divided signal output circuit having the structure illustrated in FIG. 3A will be described with reference to FIG.

5 FIG. 5 is a timing chart showing an example of operation of the divided signal output circuit having the structure illustrated in FIG. 3A.

[0114]

In FIG. 5, at a time T21, the signal CK21 is set to a high level, the signal RS21 is set to a high level, the signal S1A is at a low level, the signal S1B is at a low level, the
10 signal S2A is at a low level, and voltage of the signal S2B is equivalent to the value of the voltage Vb.

[0115]

At this time, the divided signal output circuit is set to a reset state. The transistor 102b and the transistor 102c are turned off and the transistor 102d and the
15 transistor 102e are turned on; therefore, voltage of the node NC2 (also referred to as V_{NC2}) becomes equivalent to the value of the voltage Va and the transistor 102g is turned on. Further, the transistor 102g is turned on and the transistor 102a is turned off; therefore, voltage of the node NA2 (also referred to as V_{NA2}) becomes equivalent to the value of the voltage Vb. Since the transistor 102f is in an on state, voltage of the
20 node NB2 (also referred to as V_{NB2}) becomes equivalent to the value of the voltage Vb and the transistor 102h is turned off. Further, the transistor 102h, the transistor 102i, the transistor 102j, the transistor 102k, the transistor 102l, and the transistor 102m are turned off, so that the signal OUT21 maintains the state in the previous period.

[0116]

25 Next, at a time T22, the signal CK21 is set to a low level, the signal RS21 remains at a high level, the signal S1A remains at a low level, the signal S1B remains at a low level, the signal S2A remains at a low level, and the voltage of the signal S2B remains equivalent to the value of the voltage Vb.

[0117]

30 At this time, the transistor 102b and the transistor 102c remain off, the transistor 102d is turned off, and the transistor 102e remains on; therefore, the voltage of the node NC2 remains equivalent to the value of the voltage Va and the transistor

102g remains on. Further, the transistor 102a remains off and the transistor 102g remains on; therefore, the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2 remains equivalent to the value of the voltage Vb and the transistor 102h remains off.

5 Further, the transistor 102h, the transistor 102i, the transistor 102j, the transistor 102k, the transistor 102l, and the transistor 102m remain off, so that the signal OUT21 maintains the state in the previous period.

[0118]

Next, at a time T23, the signal CK21 is set to a high level, the signal RS21 is
10 set to a low level, the signal S1A is set to a high level, the signal S1B remains at a low level, the signal S2A remains at a low level, and the voltage of the signal S2B remains equivalent to the value of the voltage Vb.

[0119]

At this time, the transistor 102b and the transistor 102c remain off, the
15 transistor 102d is turned on, and the transistor 102e is turned off; therefore, the voltage of the node NC2 remains equivalent to the value of the voltage Va and the transistor 102g remains on. Further, the transistor 102a remains off and the transistor 102g remains on; therefore, the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2
20 remains equivalent to the value of the voltage Vb and the transistor 102h remains off. Further, the transistor 102l is turned on and the transistor 102h, the transistor 102i, the transistor 102j, the transistor 102k, and the transistor 102m remain off, so that the signal OUT21 is set to a low level.

[0120]

25 Next, at a time T24, the signal CK21 is set to a low level, the signal RS21 remains at a low level, the signal S1A is set to a low level, the signal S1B is set to a high level, the signal S2A remains at a low level, and the voltage of the signal S2B remains equivalent to the value of the voltage Vb.

[0121]

30 At this time, the transistor 102b and the transistor 102e remain off, the transistor 102c is turned on, and the transistor 102d is turned off; therefore, the voltage of the node NC2 becomes equivalent to the value of the voltage Vb and the transistor

102g is turned off. Further, the transistor 102a is turned on and the transistor 102g is turned off; therefore, the voltage of the node NA2 becomes equivalent to the value of the voltage V_a . Since the transistor 102f is in an on state, the voltage of the node NB2 becomes equivalent to the value of the voltage V_a , the transistor 102h is turned on, and the voltage of the node NA2 and the voltage of the node NB2 become equivalent to the value of the voltage V_a ; accordingly, the transistor 102f is turned off. Further, the transistor 102l is turned off, the transistor 102h and the transistor 102j are turned on, and the transistor 102i, the transistor 102k, and the transistor 102m remain off, so that the signal OUT21 remains at a low level.

10 [0122]

Next, at a time T25, the signal CK21 is set to a high level, the signal RS21 remains at a low level, the signal S1A remains at a low level, the signal S1B is set to a low level, the signal S2A is set to a high level, and the voltage of the signal S2B becomes equivalent to the value of the voltage V_a .

15 [0123]

At this time, the transistor 102a is turned off and the transistor 102f remains off; therefore, the node NB2 enters a floating state. Since the transistor 102h remains on, the voltage of the other of the source and the drain of the transistor 102h is increased. Then, the voltage of the node NB2 is increased because of capacitive coupling due to parasitic capacitance generated between the gate of the transistor 102h and the other of the source and the drain of the transistor 102h. This is so-called bootstrap operation. The voltage of the node NB2 is increased to a value which is larger than the sum of the voltage V_a and the threshold voltage of the transistor 102h (also referred to as $V_{th_{102h}}$), that is, $V_a + V_{th_{102h}} + V_x$. At this time, the transistor 102h remains on. Further, the transistor 102i and the transistor 102k are turned on, the transistor 102j is turned off, the transistor 102h remains on, and the transistor 102l remains off; therefore, the signal OUT21 is set to a high level. Further, the transistor 102b and the transistor 102d are turned on, the transistor 102c is turned off, and the transistor 102e remains off; therefore, the voltage of the node NC2 becomes equivalent to the value of the voltage V_a and the transistor 102g is turned on. Since the transistor 102g is in an on state and the transistor 102a is in an off state, the voltage of the node NB2 becomes equivalent to the value of the voltage V_b . Further, the transistor 102f is turned on and the transistor

102m is turned on, so that the voltage of the node NB2 becomes equivalent to the value of the voltage Vb and the transistor 102h is turned off.

[0124]

Next, at a time T26, the signal CK21 is set to a low level, the signal RS21
5 remains at a low level, the signal S1A remains at a low level, the signal S1B remains at a low level, the signal S2A is set to a low level, and the voltage of the signal S2B becomes $V_a + V_{th_{102h}} + V_x$.

[0125]

At this time, the transistor 102b remains on, the transistor 102c and the
10 transistor 102e remain off, and the transistor 102d is turned off; therefore, the voltage of the node NC2 remains equivalent to the value of the voltage Va and the transistor 102g remains on. Further, the transistor 102a remains off and the transistor 102g remains on; therefore, the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2 remains
15 equivalent to the value of the voltage Vb and the transistor 102h remains off. Further, the transistor 102i and the transistor 102m are turned off, the transistor 102h, the transistor 102j, and the transistor 102l remain off, and the transistor 102k remains on, so that the signal OUT21 remains at a high level.

[0126]

20 Thus, the divided signal output circuit outputs the signal CLK3 as the signal OUT21. The signal CLK3 is a clock signal, whose cycle is twice longer than the cycle of the signal CLK1.

[0127]

Further, an example of operation of the divided signal output circuit illustrated
25 in FIG. 3B will be described with the use of the above-described description of the example of operation of the divided signal output circuit illustrated in FIG. 3A.

[0128]

An example of operation of the divided signal output circuit illustrated in FIG.
3B will be described with reference to FIG. 6. FIG. 6 is a timing chart showing an
30 example of operation of the divided signal output circuit illustrated in FIG. 3B.

[0129]

As shown in FIG. 6, in the divided signal output circuit illustrated in FIG. 3B,

in addition to the operation of the divided signal output circuit illustrated in FIG. 3A, at a time T31 between the time T23 and the time T24, the signal CK21 is set to a low level, the signal RS21 remains at a low level, the signal S1A is set to a low level, the signal S1C is set to a high level, the signal S1D remains at a low level, the signal S1B remains at a low level, the signal S2A remains at a low level, the voltage of the signal S2B remains equivalent to the value of the voltage Vb, the voltage of the signal S2C remains equivalent to the value of the voltage Vb, and the signal S2D remains at a low level.

[0130]

At this time, the transistor 102b, the transistor 102c, and the transistor 102e remain off and the transistor 102d is turned off; therefore, the voltage of the node NC2 remains equivalent to the value of the voltage Va and the transistor 102g remains on. Further, the transistor 102a remains off and the transistor 102g remains on; therefore, the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2 remains equivalent to the value of the voltage Vb and the transistor 102h remains off. The transistor 102i is turned off, the transistor 102o is turned on, and the transistor 102h, the transistor 102i, the transistor 102j, the transistor 102k, the transistor 102m, the transistor 102n, the transistor 102p, and the transistor 102q remain off, so that the signal OUT21 remains at a low level.

[0131]

Next, at a time T32, the signal CK21 is set to a high level, the signal RS21 remains at a low level, the signal S1A remains at a low level, the signal S1C is set to a low level, the signal S1D is set to a high level, the signal S1B remains at a low level, the signal S2A remains at a low level, the voltage of the signal S2B remains equivalent to the value of the voltage Vb, the voltage of the signal S2C remains equivalent to the value of the voltage Vb, and the voltage of the signal S2D remains equivalent to the value of the voltage Vb.

[0132]

At this time, the transistor 102b, the transistor 102c, and the transistor 102e remain off, and the transistor 102d is turned on; therefore, the voltage of the node NC2 remains equivalent to the value of the voltage Va and the transistor 102g remains on. Further, the transistor 102a remains off and the transistor 102g remains on; therefore,

the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2 remains equivalent to the value of the voltage Vb and the transistor 102h remains off. Further, the transistor 102o is turned off, the transistor 102q is turned on, and the transistor 102h, the transistor 102i, the transistor 102j, the transistor 102k, the transistor 102l, the transistor 102m, the transistor 102n, and the transistor 102p remain off, so that the signal OUT21 remains at a low level.

[0133]

Further, at the time T25, the signal CK21 is set to a high level, the signal RS21 remains at a low level, the signal S1A remains at a low level, the signal S1C remains at a low level, the signal S1D remains at a low level, the signal S1B is set to a low level, the signal S2A is set to a high level, the voltage of the signal S2B becomes equivalent to the value of the voltage Va, the voltage of the signal S2C remains equivalent to the value of the voltage Vb, and the voltage of the signal S2D remains equivalent to the value of the voltage Vb.

[0134]

At this time, the transistor 102a is turned off and the transistor 102f remains off; therefore, the node NB2 enters a floating state. Since the transistor 102h remains on, the voltage of the other of the source and the drain of the transistor 102h is increased. Then, the voltage of the node NB2 is increased because of capacitive coupling due to parasitic capacitance generated between the gate of the transistor 102h and the other of the source and the drain of the transistor 102h. This is so-called bootstrap operation. The voltage of the node NB2 is increased to a value which is larger than the sum of the voltage Va and the threshold voltage of the transistor 102h (also referred to as $V_{th_{102h}}$), that is, $V_a + V_{th_{102h}} + V_X$. At this time, the transistor 102h remains on. Further, the transistor 102i and the transistor 102k are turned on, the transistor 102j is turned off, the transistor 102h remains on, and the transistor 102l, the transistor 102n, the transistor 102o, and the transistor 102q remain off; therefore, the signal OUT21 is set to a high level. The transistor 102b and the transistor 102d are turned on, the transistor 102c is turned off, and the transistor 102e remains off; therefore, the voltage of the node NC2 becomes equivalent to the value of the voltage Va and the transistor 102g is turned on. Since the transistor 102g is turned on and the transistor 102a is turned off, the voltage of

the node NB2 becomes equivalent to the value of the voltage Vb. Further, the transistor 102f is turned on and the transistor 102m is turned on, so that the voltage of the node NB2 becomes equivalent to the value of the voltage Vb and the transistor 102h is turned off.

5 [0135]

Next, at the time T26, the signal CK21 is set to a low level, the signal RS21 remains at a low level, the signal S1A remains at a low level, the signal S1C remains at a low level, the signal S1D remains at a low level, the signal S1B remains at a low level, the signal S2A is set to a low level, the voltage of the signal S2B becomes $V_a + V_{th_{102h}}$
10 + V_x , the voltage of the signal S2C becomes equivalent to the value of the voltage V_a , and the voltage of the signal S2D remains equivalent to the value of the voltage Vb.

[0136]

At this time, the transistor 102b remains on, the transistor 102c and the transistor 102e remain off, and the transistor 102d is turned off; therefore, the voltage of
15 the node NC2 remains equivalent to the value of the voltage V_a and the transistor 102g remains on. Further, the transistor 102a remains off and the transistor 102g remains on; therefore, the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2 remains equivalent to the value of the voltage Vb and the transistor 102h remains off. Further,
20 the transistor 102i and the transistor 102m are turned off, the transistor 102n is turned on, the transistor 102k remains on, and the transistor 102h, the transistor 102j, the transistor 102l, the transistor 102o, and the transistor 102q remain off, so that the signal OUT21 remains at a high level.

[0137]

25 Further, at a time T33 after the time T26, the signal CK21 is set to a high level, the signal RS21 remains at a low level, the signal S1A remains at a low level, the signal S1C remains at a low level, the signal S1D remains at a low level, the signal S1B remains at a low level, the signal S2A remains at a low level, the voltage of the signal S2B becomes equivalent to the value of the voltage Vb, the voltage of the signal S2C
30 becomes $V_a + V_{th_{101h}} + V_x$, and the voltage of the signal S2D becomes equivalent to the value of the voltage V_a .

[0138]

At this time, the transistor 102c remains off, the transistor 102b is turned off, the transistor 102d is turned on, and the transistor 102e remains off; therefore, the voltage of the node NC2 remains equivalent to the value of the voltage Va, and the transistor 102g remains on. Further, the transistor 102a remains off and the transistor 102g remains on; therefore, the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2 remains equivalent to the value of the voltage Vb and the transistor 102h remains off. Further, the transistor 102n remains on, the transistor 102k is turned off, the transistor 102p is turned on, and the transistor 102h, the transistor 102i, the transistor 102j, the transistor 102l, the transistor 102m, the transistor 102o, and the transistor 102q remain off, so that the signal OUT21 remains at a high level.

[0139]

Further, at a time T34, the signal CK21 is set to a low level, the signal RS21 remains at a low level, the signal S1A remains at a low level, the signal S1C remains at a low level, the signal S1D remains at a low level, the signal S1B remains at a low level, the signal S2A remains at a low level, the voltage of the signal S2B remains equivalent to the value of the voltage Vb, the voltage of the signal S2C becomes equivalent to the value of the voltage Vb, and the voltage of the signal S2D becomes $V_a + V_{th_{102h}} + V_x$.

[0140]

At this time, the transistor 102b, the transistor 102c, and the transistor 102e remain off and the transistor 102d is turned off; therefore, the voltage of the node NC2 remains equivalent to the value of the voltage Va and the transistor 102g remains on. The transistor 102a remains off and the transistor 102g remains on; therefore, the voltage of the node NA2 remains equivalent to the value of the voltage Vb. Since the transistor 102f remains on, the voltage of the node NB2 remains equivalent to the value of the voltage Vb and the transistor 102h remains off. Further, the transistor 102n is turned off, the transistor 102p remains on, and the transistor 102h, the transistor 102i, the transistor 102j, the transistor 102k, the transistor 102l, the transistor 102m, the transistor 102o, and the transistor 102q remain off, so that the signal OUT21 remains at a high level.

[0141]

Thus, the divided signal output circuit outputs the signal CLK3 as the signal OUT21. The signal CLK3 is a clock signal whose cycle is four times longer than the cycle of the signal CLK1.

[0142]

5 As described above, an example of the divider circuit of this embodiment includes a shift register and a divided signal output circuit. The shift register has a function of outputting $2X$ pulse signals in accordance with a first clock signal and a second clock signal. The divided signal output circuit sets voltage of a signal to be a third clock signal in such a manner that X first transistors and X second transistors are
10 sequentially turned on in accordance with the $2X$ pulse signals, and the divided signal output circuit outputs the third clock signal with a cycle X times longer than a cycle of the first clock signal. In the shift register in the divider circuit of this embodiment, it takes shorter time to set the voltage of the pulse signal to a desired value. This is because the voltage of the pulse signal to be an output signal is set in accordance with
15 the voltage of the clock signal. Accordingly, with the use of the shift register, operation speed of the divider circuit can be improved, and a malfunction in dividing operation can be prevented.

[0143]

In an example of the divider circuit of this embodiment, a voltage signal having
20 a value higher than power supply voltage is employed for setting voltage of a signal to be a third clock signal to a second voltage. With such a structure, the voltage of the third clock signal at a high level can be set higher than or equal to the power supply voltage.

[0144]

25 (Embodiment 3)

In this embodiment, a divider circuit in which a divider circuit including a shift register and a divider circuit having another structure are used in combination will be described.

[0145]

30 An example of a structure of the divider circuit of this embodiment will be described with reference to FIG. 7. FIG. 7 is a block diagram illustrating an example of a structure of the divider circuit of this embodiment.

[0146]

The divider circuit illustrated in FIG. 7 includes a unit divider circuit 201 (also referred to as DIV1) and a unit divider circuit 202 (also referred to as DIV2).

[0147]

5 A start signal SP31 (also referred to as a signal SP31) and a clock signal CK31 (also referred to as a signal CK31) are input to the unit divider circuit 201. The unit divider circuit 201 outputs a clock signal CK32 (also referred to as a signal CK32) with a cycle X times longer than a cycle of the signal CK31. Any of the divider circuits described in the above embodiments can be applied to the unit divider circuit 201. In
10 this case, the signal SP31 corresponds to the signal SP and the signal CK32 corresponds to the signal OUT21.

[0148]

 The signal SP31 and the signal CK32 are input to the unit divider circuit 202. The unit divider circuit 202 outputs a clock signal CK33 (also referred to as a signal
15 CK33) with a cycle K times (K is a natural number greater than or equal to 2) longer than a cycle of the signal CK32. A flip-flop can be used for the unit divider circuit 202, for example. Further, the unit divider circuit 202 may include a plurality of flip-flops. When a flip-flop is formed using transistors of the same conductivity type, the divider circuit 202 can be formed in the same process as the unit divider circuit 201. With
20 such a structure, clock signals which have cycles different from each other and K times longer than the cycle of the signal CK32 can be generated.

[0149]

 As described with reference to FIG. 7, an example of the divider circuit of this embodiment is provided with a first unit divider circuit and a second unit divider circuit.
25 The first unit divider circuit is the divider circuit described in any of the above embodiments, and a cycle of a clock signal which is an output signal of the second unit divider circuit is longer than a cycle of a clock signal which is an output signal of the first unit divider circuit. The second unit divider circuit can have a circuit configuration simpler than that of the first unit divider circuit. Further, the speed of
30 dividing operation is generally faster as a cycle of the clock signal at the time after frequency division is shorter. Therefore, when the first unit divider circuit and the second unit divider circuit are used in combination, clock signals with cycles different

from each other can be generated while increase in an area of a circuit is suppressed, and a malfunction is suppressed.

[0150]

(Embodiment 4)

5 In this embodiment, a transistor including an oxide semiconductor layer, which can be used in any of the divider circuits of the above embodiments, will be described.

[0151]

The transistor including an oxide semiconductor layer, which can be used in any of the divider circuits of the above embodiments, is a transistor including a semiconductor layer which is highly purified to be intrinsic (also referred to as I-type) or substantially intrinsic.

[0152]

Examples of an oxide semiconductor used in the oxide semiconductor layer are a four-component metal oxide, a three-component metal oxide, and a two-component metal oxide. As the four-component metal oxide, an In-Sn-Ga-Zn-O-based metal oxide or the like can be used, for example. As the three-component metal oxide, an In-Ga-Zn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, a Sn-Al-Zn-O-based metal oxide, or the like can be used, for example. As the two-component metal oxide, an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, an In-Mg-O-based metal oxide, an In-Sn-O-based metal oxide, or the like can be used, for example. In addition, an In-O-based metal oxide, a Sn-O-based metal oxide, a Zn-O-based metal oxide, or the like can also be used as the oxide semiconductor. Moreover, the metal oxide that can be used as the oxide semiconductor may contain SiO₂.

[0153]

As the oxide semiconductor, a material represented by InMO₃(ZnO)_m (*m* is larger than 0) can be used. Here, *M* represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, Ga, Ga and Al, Ga and Mn, Ga and Co, and the like can be given as *M*.

[0154]

The band gap of the oxide semiconductor layer is greater than or equal to 2 eV, preferably greater than or equal to 2.5 eV, more preferably greater than or equal to 3 eV, which reduces the number of carriers generated by thermal excitation to a negligible level. In addition, the amount of impurity such as hydrogen which might serve as a donor is reduced to a certain amount or less so that the carrier concentration is lower than $1 \times 10^{14}/\text{cm}^3$, preferably lower than or equal to $1 \times 10^{12}/\text{cm}^3$. That is, the carrier concentration of the oxide semiconductor layer is reduced to zero or substantially zero.

[0155]

In the aforementioned oxide semiconductor layer, the avalanche breakdown does not easily occur and the breakdown voltage is high. For example, the band gap of silicon is as narrow as 1.12 eV; thus, electrons are easily generated like an avalanche owing to the avalanche breakdown, and the number of electrons which are accelerated to high speed so as to go over an energy barrier to a gate insulating layer is increased. In contrast, since the oxide semiconductor used for the aforementioned oxide semiconductor layer has a band gap of as wide as 2 eV or more, the avalanche breakdown does not easily occur and resistance to hot-carrier degradation is higher than that of silicon, and the breakdown voltage is thus high.

[0156]

Hot-carrier degradation means, for example, degradation of transistor characteristics due to fixed charges caused by the fact that accelerated electrons are injected into a gate insulating layer in the vicinity of a drain in a channel; or degradation of transistor characteristics due to a trap level or the like formed by highly-accelerated electrons at the interface between an oxide semiconductor layer and a gate insulating layer. Examples of degradation of transistor characteristics due to hot carriers are variations in threshold voltage and gate leakage. The hot-carrier degradation is caused by channel-hot-electron injection (also referred to as CHE injection) or drain-avalanche-hot-carrier injection (also referred to as DAHC injection).

[0157]

Note that the band gap of silicon carbide, which is one of materials having high breakdown voltage, is substantially equal to that of an oxide semiconductor used for the oxide semiconductor layer, but electrons are less likely to be accelerated in an oxide semiconductor because the mobility of the oxide semiconductor is lower than that of

silicon carbide by approximately two orders of magnitude. Further, a barrier between a gate insulating layer and an oxide semiconductor is larger than a barrier between a gate insulating layer and silicon carbide, gallium nitride, or silicon; therefore, the number of electrons injected into the gate insulating layer is extremely small, whereby hot-carrier degradation is less likely to be caused and breakdown voltage is higher as compared to the case of silicon carbide, gallium nitride, or silicon. The oxide semiconductor has high breakdown voltage even in an amorphous state.

[0158]

Furthermore, the transistor including the oxide semiconductor layer can have an off-state current per micrometer of channel width of 10 aA (1×10^{-17} A) or smaller, 1 aA (1×10^{-18} A) or smaller, 10 zA (1×10^{-20} A) or smaller, and further 1 zA (1×10^{-21} A) or smaller.

[0159]

In the transistor including the above oxide semiconductor layer, degradation due to light (e.g., variations in the threshold voltage) is little.

[0160]

Examples of structures of the transistors including an oxide semiconductor layer, which is applicable to any of the divider circuits described in the above embodiments, will be described with reference to FIGS. 8A to 8D. FIGS. 8A to 8D are cross-sectional schematic views each illustrating an example of the structure of the transistor.

[0161]

The transistor illustrated in FIG. 8A is one of bottom-gate transistors, which is also referred to as an inverted staggered transistor.

[0162]

The transistor illustrated in FIG. 8A includes a conductive layer 401a serving as a gate electrode, an insulating layer 402a serving as a gate insulating layer, an oxide semiconductor layer 403a serving as a channel formation layer, and a conductive layer 405a and a conductive layer 406a serving as a source or drain electrode.

[0163]

The conductive layer 401a is formed over a substrate 400a, the insulating layer

402a is formed over the conductive layer 401a, the oxide semiconductor layer 403a is formed over the conductive layer 401a with the insulating layer 402a interposed therebetween, and the conductive layer 405a and the conductive layer 406a are each formed over part of the oxide semiconductor layer 403a.

5 [0164]

Further, in the transistor illustrated in FIG. 8A, an oxide insulating layer 407a is in contact with part of a top surface of the oxide semiconductor layer 403a (part of the oxide semiconductor layer 403a over which neither the conductive layer 405a nor the conductive layer 406a is provided). In addition, a protective insulating layer 409a is provided over the oxide insulating layer 407a.

[0165]

The transistor illustrated in FIG. 8B is a channel protective (also referred to as a channel stop) transistor which is one of the bottom-gate transistors, and is also referred to as an inverted staggered transistor.

15 [0166]

The transistor illustrated in FIG. 8B includes a conductive layer 401b serving as a gate electrode, an insulating layer 402b serving as a gate insulating layer, an oxide semiconductor layer 403b serving as a channel formation layer, an insulating layer 427 serving as a channel protective layer, and a conductive layer 405b and a conductive layer 406b serving as a source or drain electrode.

[0167]

The conductive layer 401b is formed over a substrate 400b, the insulating layer 402b is formed over the conductive layer 401b, the oxide semiconductor layer 403b is formed over the conductive layer 401b with the insulating layer 402b interposed therebetween, the insulating layer 427 is formed over the conductive layer 401b with the insulating layer 402b and the oxide semiconductor layer 403b interposed therebetween, and the conductive layer 405b and the conductive layer 406b are formed over part of the oxide semiconductor layer 403b with the insulating layer 427 interposed therebetween. Further, a structure can be employed in which the entire oxide semiconductor layer 403b overlaps with the conductive layer 401b. When the entire oxide semiconductor layer 403b overlaps with the conductive layer 401b, light can be prevented from entering the oxide semiconductor layer 403b. The structure which is employed is not

limited thereto, and a structure can be employed in which the conductive layer 401b overlaps with part of the oxide semiconductor layer 403b.

[0168]

Further, a protective insulating layer 409b is in contact with a top part of the transistor illustrated in FIG. 8B.

[0169]

The transistor illustrated in FIG. 8C is one of the bottom-gate transistors.

[0170]

The transistor illustrated in FIG. 8C includes a conductive layer 401c serving as a gate electrode, an insulating layer 402c serving as a gate insulating layer, an oxide semiconductor layer 403c serving as a channel formation layer, and a conductive layer 405c and a conductive layer 406c serving as a source or drain electrode.

[0171]

The conductive layer 401c is formed over a substrate 400c, the insulating layer 402c is formed over the conductive layer 401c, the conductive layer 405c and the conductive layer 406c are formed over part of the insulating layer 402c, and the oxide semiconductor layer 403c is formed over the conductive layer 401c with the insulating layer 402c, the conductive layer 405c, and the conductive layer 406c interposed therebetween. Further, a structure can be employed in which the entire oxide semiconductor layer 403c overlaps with the conductive layer 401c. When the entire oxide semiconductor layer 403c overlaps with the conductive layer 401c, light can be prevented from entering the oxide semiconductor layer 403c. The structure which is employed is not limited thereto, and a structure can be employed in which the conductive layer 401c overlaps with part of the oxide semiconductor layer 403c.

[0172]

Further, in the transistor illustrated in FIG. 8C, an oxide insulating layer 407c is in contact with an upper surface and a side surface of the oxide semiconductor layer 403c. In addition, a protective insulating layer 409c is provided over the oxide insulating layer 407c.

[0173]

The transistor illustrated in FIG. 8D is one of top-gate transistors.

[0174]

The transistor illustrated in FIG. 8D includes a conductive layer 401d serving as a gate electrode, an insulating layer 402d serving as a gate insulating layer, an oxide semiconductor layer 403d serving as a channel formation layer, and a conductive layer 405d and a conductive layer 406d serving as a source or drain electrode.

5 [0175]

The oxide semiconductor layer 403d is formed over a substrate 400d with an insulating layer 447 interposed therebetween, the conductive layer 405d and the conductive layer 406d are each formed over part of the oxide semiconductor layer 403d, the insulating layer 402d is formed over the oxide semiconductor layer 403d, the conductive layer 405d, and the conductive layer 406d, and the conductive layer 401d is formed over the oxide semiconductor layer 403d with the insulating layer 402d interposed therebetween.

[0176]

As the substrates 400a to 400d, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like can be used, for example.

[0177]

Alternatively, a substrate of an insulator, such as a ceramic substrate, a quartz substrate, or a sapphire substrate, can be used as the substrates 400a to 400d. Further alternatively, crystallized glass can be used for the substrates 400a to 400d. Still further alternatively, a plastic substrate or a semiconductor substrate of silicon or the like can be used as the substrates 400a to 400d.

[0178]

The insulating layer 447 has a function of a base layer which prevents diffusion of an impurity element from the substrate 400d. As the insulating layer 447, a silicon nitride layer, a silicon oxide layer, a silicon nitride oxide layer, a silicon oxynitride layer, an aluminum oxide layer, or an aluminum oxynitride layer can be used, for example. The insulating layer 447 can also be formed by stacking layers of materials which can be used for the insulating layer 447. Alternatively, as the insulating layer 447, a stack of a layer including a material having a light-blocking property and a layer including a material applicable to the insulating layer 447 can be used. When the insulating layer 447 includes a layer of a material having a light-blocking property, light can be prevented from entering the oxide semiconductor layer 403d.

[0179]

Note that in each of the transistors illustrated in FIGS. 8A to 8C, an insulating layer may be formed between the substrate and the conductive layer serving as a gate electrode, as in the transistor illustrated in FIG. 8D.

5 [0180]

As the conductive layers 401a to 401d, it is possible to use, for example, a layer of a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium or an alloy material containing any of these materials as a main component. The conductive layers 401a to 401d can also be
10 formed by stacking layers of materials which can be used for the conductive layers 401a to 401d.

[0181]

As the insulating layers 402a to 402d, a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer,
15 an aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, or a hafnium oxide layer can be used, for example. The insulating layers 402a to 402d can also be formed by stacking layers of materials which can be used for the insulating layers 402a to 402d. The layers of materials which can be used for the insulating layers 402a to 402d can be formed by a plasma CVD method, a sputtering
20 method, or the like. For example, the insulating layers 402a to 402d can be formed in such a manner that a silicon nitride layer is formed by a plasma CVD method and a silicon oxide layer is formed over the silicon nitride layer by a plasma CVD method.

[0182]

As an oxide semiconductor which can be used for the oxide semiconductor
25 layers 403a to 403d, a four-component metal oxide, a three-component metal oxide, and a two-component metal oxide can be given, for example. As the four-component metal oxide, an In-Sn-Ga-Zn-O-based metal oxide or the like can be given, for example. As the three-component metal oxide, an In-Ga-Zn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based
30 metal oxide, an Al-Ga-Zn-O-based metal oxide, a Sn-Al-Zn-O-based metal oxide, or the like can be given, for example. As the two-component metal oxide, an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a

Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, an In-Mg-O-based metal oxide, an In-Sn-O-based metal oxide, or the like can be given. Further, as the oxide semiconductor, an In-O-based metal oxide, a Sn-O-based metal oxide, a Zn-O-based metal oxide, or the like can be used. The metal oxide that can be used as the oxide semiconductor may contain SiO_2 . Here, for example, the In-Ga-Zn-O-based metal oxide means an oxide containing at least In, Ga, and Zn, and the composition ratio of the elements is not particularly limited. The In-Ga-Zn-O-based metal oxide may contain an element other than In, Ga, and Zn.

[0183]

In the case where an In-Zn-O-based material is used as an oxide semiconductor, a target to be used has a composition ratio of In:Zn = 50:1 to 1:2 in an atomic ratio (In_2O_3 : ZnO = 25:1 to 1:4 in a molar ratio), preferably, In:Zn = 20:1 to 1:1 in an atomic ratio (In_2O_3 : ZnO = 10:1 to 1:2 in a molar ratio), further preferably, In:Zn = 15:1 to 1.5:1 in an atomic ratio (In_2O_3 : ZnO = 15:2 to 3:4 in a molar ratio). For example, in a target used for formation of an In-Zn-O-based oxide semiconductor which has an atomic ratio of In:Zn:O = W : Y : Z , the relation of $Z > 1.5W + Y$ is satisfied.

[0184]

Further, as an oxide semiconductor which can be used for the oxide semiconductor layers 403a to 403d, a metal oxide represented by a chemical formula $\text{InMO}_3(\text{ZnO})_m$ (m is larger than 0) can be given. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, Ga, Ga and Al, Ga and Mn, Ga and Co, and the like can be given as M .

[0185]

As the conductive layers 405a to 405d and the conductive layers 406a to 406d, a layer of a metal material such as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten or an alloy material containing any of the metal materials as a main component can be used, for example. The conductive layers 405a to 405d and the conductive layers 406a to 406d can also be formed by stacking layers of materials which can be used for the conductive layers 405a to 405d and the conductive layers 406a to 406d.

[0186]

For example, the conductive layers 405a to 405d and the conductive layers 406a to 406d can be formed by stacking a metal layer of aluminum or copper and a high-melting-point metal layer of titanium, molybdenum, tungsten, or the like. The conductive layers 405a to 405d and the conductive layers 406a to 406d may have a structure in which a metal layer of aluminum or copper is provided between a plurality of high-melting-point metal layers. Further, when the conductive layers 405a to 405d and the conductive layers 406a to 406d are formed using an aluminum layer to which an element that prevents generation of hillocks or whiskers (e.g., Si, Nd, or Sc) is added, heat resistance can be increased.

10 [0187]

Alternatively, the conductive layers 405a to 405d and the conductive layers 406a to 406d can be formed using a layer containing a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an alloy of indium oxide and tin oxide ($\text{In}_2\text{O}_3\text{-SnO}_2$, abbreviated to ITO), an alloy of indium oxide and zinc oxide ($\text{In}_2\text{O}_3\text{-ZnO}$), or any of these metal oxide materials containing silicon oxide can be used, for example.

[0188]

In addition, another wiring may be formed using a material used to form the conductive layers 405a to 405d and the conductive layers 406a to 406d.

20 [0189]

As the insulating layer 427, a layer which can be applied to the insulating layer 447 can be used, for example. The insulating layer 427 can also be formed by stacking layers of materials which can be applied to the insulating layer 427.

[0190]

25 As the oxide insulating layer 407a and the oxide insulating layer 407c, an oxide insulating layer can be used and, for example, a silicon oxide layer or the like can be used. The oxide insulating layer 407a and the oxide insulating layer 407c can also be formed by stacking layers of materials which can be applied to the oxide insulating layer 407a and the oxide insulating layer 407c.

30 [0191]

As the protective insulating layers 409a to 409c, an inorganic insulating layer such as a silicon nitride layer, an aluminum nitride layer, a silicon nitride oxide layer, or

an aluminum nitride oxide layer can be used, for example. The protective insulating layers 409a to 409c can also be formed by stacking layers of materials which can be applied to the protective insulating layers 409a to 409c.

[0192]

5 In order to reduce surface unevenness due to the transistor of this embodiment, a planarization insulating layer can be formed over the transistor (over the transistor with the oxide insulating layer or the protective insulating layer interposed therebetween in the case where the transistor includes an oxide insulating layer or a protective insulating layer). As the planarization insulating layer, a layer of an organic material
10 such as polyimide, acrylic, or benzocyclobutene can be used. Alternatively, a layer of a low-dielectric constant material (a low-k material) can be used as the planarization insulating layer. The planarization insulating layer can also be formed by stacking layers of materials which can be applied to the planarization insulating layer.

[0193]

15 Next, as an example of a method for manufacturing the transistor including an oxide semiconductor layer, which can be applied to any of the divider circuits of the above embodiments, an example of a method for manufacturing the transistor illustrated in FIG. 8A will be described with reference to FIGS. 9A to 9C and FIGS. 10A and 10B. FIGS. 9A to 9C and FIGS. 10A and 10B are cross-sectional schematic views illustrating
20 an example of the method for manufacturing the transistor illustrated in FIG. 8A.

[0194]

First, the substrate 400a is prepared, and a first conductive film is formed over the substrate 400a.

[0195]

25 A glass substrate is used as an example of the substrate 400a.

[0196]

As the first conductive film, a film of a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which contains any of the metal materials as a main component can
30 be used. The first conductive film can also be formed by stacking layers of materials which can be applied to the first conductive film.

[0197]

Next, a first photolithography process is carried out: a first resist mask is formed over the first conductive film, the first conductive film is selectively etched with the use of the first resist mask to form the conductive layer 401a, and the first resist mask is removed.

5 [0198]

In this embodiment, the resist mask may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced.

[0199]

10 In order to reduce the number of photomasks and steps in the photolithography process, the etching step may be performed using a resist mask formed with a multi-tone mask. A multi-tone mask is a light-exposure mask through which light is transmitted to have a plurality of intensities. A resist mask formed using a multi-tone mask has a plurality of thicknesses and further can be changed in shape by being etched,
15 and thus can be used in a plurality of etching steps to provide different patterns. Therefore, a resist mask corresponding to at least two kinds or more of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography processes can also be reduced, whereby a manufacturing process can be simplified.

20 [0200]

Next, the insulating layer 402a is formed over the conductive layer 401a.

[0201]

For example, the insulating layer 402a can be formed by a high-density plasma CVD method. For example, a high-density plasma CVD method using microwaves
25 (e.g., microwaves with a frequency of 2.45 GHz) is preferable because an insulating layer can be dense and have high breakdown voltage and high quality. When the oxide semiconductor layer is in contact with the high-quality insulating layer formed by a high-density plasma CVD method, the interface state can be reduced and good interface characteristics can be obtained.

30 [0202]

The insulating layer 402a can also be formed by another method such as a sputtering method or a plasma CVD method. Further, heat treatment may be

performed after the formation of the insulating layer 402a. The heat treatment can improve the quality of the insulating layer 402a and the interface characteristics between the insulating layer 402a and the oxide semiconductor.

[0203]

5 Next, an oxide semiconductor film 530 having a thickness of greater than or equal to 2 nm and less than or equal to 200 nm, preferably greater than or equal to 5 nm and less than or equal to 30 nm is formed over the insulating layer 402a. For example, the oxide semiconductor film 530 can be formed by a sputtering method.

[0204]

10 Note that before the formation of the oxide semiconductor film 530, powdery substances (also referred to as particles or dust) attached on a surface of the insulating layer 402a are preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which, without application of voltage to a target side, an RF power source is used for
15 application of voltage to a substrate side in an argon atmosphere, so that plasma is generated to modify a surface of the substrate. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used.

[0205]

20 For example, the oxide semiconductor film 530 can be formed using an oxide semiconductor material which can be used as a material of the oxide semiconductor layer 403a. In this embodiment, as an example, the oxide semiconductor film 530 is formed by a sputtering method with the use of an In-Ga-Zn-O-based oxide target. A cross-sectional schematic view at this stage corresponds to FIG. 9A. Further, the oxide
25 semiconductor film 530 can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen.

[0206]

30 As a target for forming the oxide semiconductor film 530 by a sputtering method, for example, an oxide target having a composition ratio of In_2O_3 : Ga_2O_3 : ZnO = 1:1:1 [molar ratio] can be used. Without limitation to the above target, an oxide

target having a composition ratio of In_2O_3 : Ga_2O_3 : ZnO = 1:1:2 [molar ratio] may be used, for example. The proportion of the volume of a portion except for an area occupied by a space and the like with respect to the total volume of the oxide target (also referred to as the filling rate) is higher than or equal to 90 % and lower than or equal to 100 %, and preferably higher than or equal to 95 % and lower than or equal to 99.9 %. With the use of a metal oxide target with high filling rate, the formed oxide semiconductor film has high density.

[0207]

Note that as a sputtering gas used for forming the oxide semiconductor film 530, for example, a high-purity gas from which an impurity such as hydrogen, water, hydroxyl groups, or hydride is removed is preferably used.

[0208]

Before the formation of the oxide semiconductor film 530, it is preferable that the substrate 400a over which the conductive layer 401a is formed or the substrate 400a over which the conductive layer 401a and the insulating layer 402a are formed be heated in a preheating chamber of the sputtering apparatus, so that an impurity such as hydrogen or moisture adsorbed on the substrate 400a is eliminated and removed. The heating can prevent hydrogen, hydroxyl groups, and moisture from entering the insulating layer 402a and the oxide semiconductor film 530. Note that a cryopump is preferably used as an exhaustion unit provided in the preheating chamber, for example. The heating treatment in the preheating chamber may be omitted. The heating may be similarly performed, before the formation of the oxide insulating layer 407a, on the substrate 400a over which layers up to and including the conductive layer 405a and the conductive layer 406a have been formed.

[0209]

When the oxide semiconductor film 530 is formed by a sputtering method, the substrate 400a is held inside a film formation chamber which is kept in a reduced pressure state, and the substrate temperature is set to higher than or equal to 100 °C and lower than or equal to 600 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. By heating the substrate 400a, the concentration of an impurity contained in the oxide semiconductor film 530 can be reduced. Further, heating of the

substrate 400a can reduce damage on the oxide semiconductor film 530 due to sputtering. Then, a sputtering gas from which hydrogen and moisture are removed is introduced while remaining moisture in the film formation chamber is removed, and the above-described target is used; thus, the oxide semiconductor film 530 is formed over the insulating layer 402a.

[0210]

Note that in this embodiment, for example, an entrapment vacuum pump can be used as a means for removing moisture remaining in the film formation chamber in which sputtering is performed. As the entrapment vacuum pump, a cryopump, an ion pump, or a titanium sublimation pump can be used, for example. When a cryopump is used as an example, a compound including either or both of a hydrogen atom and a carbon atom, or the like can be evacuated, and thus the concentration of an impurity included in a film formed in the film formation chamber can be reduced. Further, in this embodiment, a turbo pump provided with a cold trap may be used as a means for removing moisture remaining in the film formation chamber in which sputtering is performed.

[0211]

As one example of the deposition condition, the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct-current (DC) power source is 0.5 kW, and the atmosphere is an oxygen atmosphere (the proportion of the oxygen flow rate is 100 %). Note that when a pulsed direct-current power source is used, powdery substances generated at the time of film formation can be reduced and the film thickness can be made uniform.

[0212]

Next, a second photolithography process is carried out: a second resist mask is formed over the oxide semiconductor film 530, the oxide semiconductor film 530 is selectively etched with the use of the second resist mask to process the oxide semiconductor film 530 into an island-shaped oxide semiconductor layer, and the second resist mask is removed.

[0213]

In the case of forming a contact hole in the insulating layer 402a, the contact hole can be formed at the time of processing the oxide semiconductor film 530 into the

island-shaped oxide semiconductor layer.

[0214]

For example, dry etching, wet etching, or both dry etching and wet etching can be employed for etching the oxide semiconductor film 530. As an etchant used for wet etching, for example, a mixed solution of phosphoric acid, acetic acid, and nitric acid, or the like can be used. Alternatively, ITO07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0215]

Next, the oxide semiconductor layer is subjected to first heat treatment. With the first heat treatment, dehydration or dehydrogenation of the oxide semiconductor layer can be conducted. The temperature of the first heat treatment is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is put in an electric furnace that is a kind of heat treatment apparatus and heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere at 450 °C for one hour, and then the oxide semiconductor layer is not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layer is prevented. In this manner, the oxide semiconductor layer 403a is obtained (see FIG. 9B).

[0216]

The heat treatment apparatus is not limited to the electric furnace and may be the one provided with a device for heating a process object using heat conduction or heat radiation from a heating element such as a resistance heating element. For example, an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used. An LRTA apparatus is an apparatus for heating a process object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the high-temperature gas, an inert gas which does not react with a process object by heat treatment, such as nitrogen or a rare gas like argon, can be used.

[0217]

For example, as the first heat treatment, GRTA may be performed in the following manner. The substrate is moved into an inert gas heated to 650 °C to 700 °C, heated for several minutes, and taken out of the heated inert gas.

5 [0218]

Note that in the first heat treatment, it is preferable that water, hydrogen, or the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. It is also preferable that nitrogen or a rare gas such as helium, neon, or argon introduced into the heat treatment apparatus have a purity of 6N (99.9999 %) or more, preferably, 7N
10 (99.99999 %) or more (that is, the impurity concentration is set to be lower than or equal to 1 ppm, preferably, lower than or equal to 0.1 ppm).

[0219]

After the oxide semiconductor layer is heated in the first heat treatment, a high-purity oxygen gas, a high-purity N₂O gas, or ultra-dry air (having a dew point of
15 -40 °C or lower, preferably -60 °C or lower) may be introduced into the same furnace that has been used in the first heat treatment. It is preferable that the oxygen gas or the N₂O gas do not contain water, hydrogen, and the like. The purity of the oxygen gas or the N₂O gas which is introduced into the heat treatment apparatus is preferably 6N or more, more preferably 7N or more (i.e., the impurity concentration of the oxygen gas or
20 the N₂O gas is preferably lower than or equal to 1 ppm, more preferably lower than or equal to 0.1 ppm). By the effect of the oxygen gas or the N₂O gas, oxygen that has been reduced through the step of eliminating an impurity by the dehydration or dehydrogenation treatment is supplied; thus, the oxide semiconductor layer 403a is highly purified.

25 [0220]

The first heat treatment may also be performed on the oxide semiconductor film 530 before being processed into the island-shaped oxide semiconductor layer. In such a case, the substrate is taken out of the heating apparatus after the first heat treatment and then the oxide semiconductor film 530 is processed into the island-shaped
30 oxide semiconductor layer.

[0221]

Other than the above-described timings, the first heat treatment may be performed, as long as it is performed after the formation of the oxide semiconductor layer, after the conductive layer 405a and the conductive layer 406a are formed over the oxide semiconductor layer 403a or after the oxide insulating layer 407a is formed over the conductive layer 405a and the conductive layer 406a

[0222]

In the case of forming a contact hole in the insulating layer 402a, the contact hole may be formed before the first heat treatment is performed.

[0223]

The oxide semiconductor layer may be formed using an oxide semiconductor film which is formed through two deposition steps and two heat treatments so as to be a thick film including a crystalline region (a single crystal region), that is, a crystalline region having the c-axes aligned in a direction perpendicular to a surface of the film, regardless of the material of a base component such as an oxide, a nitride, or a metal.

For example, a first oxide semiconductor film with a thickness of greater than or equal to 3 nm and less than or equal to 15 nm is formed and subjected to first heat treatment at a temperature higher than or equal to 450 °C and lower than or equal to 850 °C, preferably higher than or equal to 550 °C and lower than or equal to 750 °C under an atmosphere of nitrogen, oxygen, a rare gas, or dry air, so that the first oxide semiconductor film which includes a crystalline region (including a plate-like crystal) in a region including a surface is formed. Then, a second oxide semiconductor film which is thicker than the first oxide semiconductor film is formed, and second heat treatment is performed at a temperature higher than or equal to 450 °C and lower than or equal to 850 °C, preferably higher than or equal to 600 °C and lower than or equal to 700 °C, so that crystal growth proceeds upward from the first oxide semiconductor film to the second oxide semiconductor film using the first oxide semiconductor film as a seed of the crystal growth, and the entire region of the second oxide semiconductor film is crystallized. Thus, the oxide semiconductor layer 403a can be formed using an oxide semiconductor film including a crystalline region having a large thickness.

[0224]

Next, a second conductive film is formed over the insulating layer 402a and the

oxide semiconductor layer 403a.

[0225]

As the second conductive film, a film of a metal material such as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten, or an alloy material which contains any of the metal materials as a main component can be used, for example. The second conductive film can also be formed by stacking films of materials which can be applied to the second conductive film.

[0226]

Next, a third photolithography process is carried out: a third resist mask is formed over the second conductive film, the second conductive film is selectively etched with the use of the third resist mask to form the conductive layer 405a and the conductive layer 406a, and the third resist mask is removed (see FIG. 9C).

[0227]

Note that another wiring may be formed using the second conductive film at the time of forming the conductive layer 405a and the conductive layer 406a.

[0228]

In light exposure in forming the third resist mask, ultraviolet light, KrF laser light, or ArF laser light is preferably used. A channel length L of the transistor to be completed later depends on the width of an interval between bottom ends of the conductive layers 405a and 406a which are adjacent to each other over the oxide semiconductor layer 403a. In the case where the channel length L is less than 25 nm, the light exposure is preferably performed using extreme ultraviolet light having an extremely short wavelength of several nanometers to several tens of nanometers in forming the third resist mask. In the light exposure with extreme ultraviolet light, the resolution is high and the focus depth is large. Therefore, the channel length L of the transistor to be completed later can be made greater than or equal to 10 nm and less than or equal to 1000 nm, and the use of the transistor formed through such light exposure enables higher speed operation of a circuit. In addition, the off-state current of the transistor is extremely small, which results in a reduction in power consumption.

[0229]

In the case of etching the second conductive film, etching conditions are preferably optimized in order to prevent the oxide semiconductor layer 403a from being

divided by the etching. However, it is difficult to set conditions under which only the second conductive film can be etched and the oxide semiconductor layer 403a is not etched at all. In some cases, part of the oxide semiconductor layer 403a is etched at the time of etching the second conductive film, so that the oxide semiconductor layer 403a comes to include a groove portion (depression portion).

[0230]

In this embodiment, a titanium film is used as an example of the second conductive film, an In-Ga-Zn-O-based oxide semiconductor is used as an example of the oxide semiconductor layer 403a, and an ammonia hydrogen peroxide mixture (a mixed solution of ammonia, water, and hydrogen peroxide) is used as an etchant.

[0231]

Next, the oxide insulating layer 407a is formed over the oxide semiconductor layer 403a, the conductive layer 405a, and the conductive layer 406a. Here, the oxide insulating layer 407a is in contact with part of the upper surface of the oxide semiconductor layer 403a.

[0232]

The oxide insulating layer 407a can be formed to a thickness of at least 1 nm using a method by which impurities such as water or hydrogen are not introduced into the oxide insulating layer 407a, such as a sputtering method, as appropriate. When hydrogen is contained in the oxide insulating layer 407a, entry of the hydrogen to the oxide semiconductor layer, or extraction of oxygen in the oxide semiconductor layer by the hydrogen is caused, thereby causing the back channel of the oxide semiconductor layer to have lower resistance (to have an n-type conductivity), so that a parasitic channel might be formed. Therefore, in order to form the oxide insulating layer 407a containing as little hydrogen as possible, it is preferable that a method in which hydrogen is not used be employed as a method for forming the oxide insulating layer 407a.

[0233]

In this embodiment, as an example of the oxide insulating layer 407a, a silicon oxide film having a thickness of 200 nm is formed by a sputtering method. The substrate temperature at the time of the film formation may be higher than or equal to room temperature and lower than or equal to 300 °C; in this embodiment, the substrate

temperature is set to 100 °C as an example. The silicon oxide film can be formed by a sputtering method under a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen.

[0234]

5 Further, a silicon oxide target or a silicon target can be used as a target for forming the oxide insulating layer 407a. For example, with the use of a silicon target, a silicon oxide film can be formed by a sputtering method under an atmosphere containing oxygen.

[0235]

10 As a sputtering gas used for forming the oxide semiconductor layer 407a, for example, a high-purity gas from which an impurity such as hydrogen, water, hydroxyl groups, or hydride is removed is preferably used.

[0236]

15 Before formation of the oxide insulating layer 407a, plasma treatment with the use of a gas such as N₂O, N₂, or Ar may be performed to remove water or the like adsorbed on an exposed surface of the oxide semiconductor layer 403a. In the case where plasma treatment is performed, the oxide insulating layer 407a which is in contact with part of the upper surface of the oxide semiconductor layer 403a is preferably formed without exposure to the air.

20 [0237]

Then, second heat treatment (preferably, at a temperature higher than or equal to 200 °C and lower than or equal to 400 °C, for example, higher than or equal to 250 °C and lower than or equal to 350 °C) can be performed in an inert gas atmosphere or in an oxygen gas atmosphere. For example, the second heat treatment is performed at 25 °C in a nitrogen atmosphere for one hour. By the second heat treatment, heat is applied while part of the upper surface of the oxide semiconductor layer 403a is in contact with the oxide insulating layer 407a.

[0238]

30 Through the above-described process, an impurity such as hydrogen, moisture, hydroxyl groups, or hydride (also referred to as a hydrogen compound) can be intentionally removed from the oxide semiconductor layer, and in addition, oxygen can

be supplied to the oxide semiconductor layer. Therefore, the oxide semiconductor layer is highly purified.

[0239]

Through the above-described process, the transistor is formed (see FIG. 10A).

5 [0240]

When a silicon oxide layer having many defects is used as the oxide insulating layer 407a, the heat treatment after formation of the silicon oxide layer has an effect of diffusing an impurity such as hydrogen, moisture, hydroxyl groups, or hydride contained in the oxide semiconductor layer 403a to the oxide insulating layer 407a, so
10 that the impurity contained in the oxide semiconductor layer 403a can be further reduced.

[0241]

Further, the protective insulating layer 409a may be formed over the oxide insulating layer 407a. For example, a silicon nitride film is formed by an RF sputtering method. The RF sputtering method is preferably used as a formation
15 method of the protective insulating layer 409a because it achieves high mass productivity. In this embodiment, as an example, a silicon nitride film is formed as the protective insulating layer 409a (see FIG. 10B).

[0242]

20 In this embodiment, the protective insulating layer 409a is formed in such a manner that the substrate 400a over which layers up to the oxide insulating layer 407a are formed is heated at a temperature of 100 °C to 400 °C, a sputtering gas containing high-purity nitrogen from which hydrogen and moisture are removed is introduced, and a silicon nitride film is formed with the use of a target of a silicon semiconductor. In
25 this case also, the protective insulating layer 409a is preferably formed while moisture remaining in a treatment chamber is removed, similarly to the oxide insulating layer 407a.

[0243]

After formation of the protective insulating layer 409a, heat treatment may be
30 further performed at a temperature higher than or equal to 100 °C and lower than or equal to 200 °C under the air for longer than or equal to 1 hour and shorter than or equal

to 30 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then
5 decreased to room temperature. That is an example of the method for manufacturing the transistor illustrated in FIG. 8A.

[0244]

Although an example of the method for manufacturing the transistor illustrated in FIG. 8A is described, the present invention is not limited thereto. For example as for
10 the components of FIGS. 8B to 8D which have the same designations as the components of FIG. 8A and whose function is at least partly the same as that of the components of FIG. 8A, description of the example of the manufacturing method of the transistor illustrated in FIG. 8A can be referred to as appropriate.

[0245]

15 As described above, the transistor including an oxide semiconductor layer, which can be applied to any of the divider circuits described in the above embodiments, is a transistor including an oxide semiconductor layer as a channel formation layer. The oxide semiconductor layer used in the transistor is highly purified by heat treatment and thus becomes an i-type or substantially i-type oxide semiconductor layer.

20 [0246]

The highly-purified oxide semiconductor layer includes extremely few (close to 0) carriers. The carrier concentration of the oxide semiconductor layer is less than $1 \times 10^{14} / \text{cm}^3$, preferably less than $1 \times 10^{12} / \text{cm}^3$, and more preferably less than $1 \times 10^{11} / \text{cm}^3$. Accordingly, the off-state current per micrometer of channel width can be 10 aA
25 ($1 \times 10^{-17} \text{ A}$) or less, 1 aA ($1 \times 10^{-18} \text{ A}$) or less, 10 zA ($1 \times 10^{-20} \text{ A}$) or less, and further 1 zA ($1 \times 10^{-21} \text{ A}$) or less.

[0247]

Further, with the use of the above transistor, breakdown voltage of the divider circuit can be improved, for example. In the divider circuit of this embodiment,
30 voltage which is higher than or equal to power supply voltage is applied between a gate and a source of a transistor or between a gate and a drain of a transistor in some cases;

therefore, it is preferable to use the transistor of this embodiment, which has high breakdown voltage.

[0248]

(Embodiment 5)

5 In this embodiment, a semiconductor device including any of the divider circuits of the above embodiments will be described.

[0249]

As the semiconductor device of this embodiment, a display device, a wireless communication device, an integrated circuit, or the like can be given, for example. As
10 an example of a display device, a liquid crystal display device, an electroluminescent display device (also referred to as an EL display device), or the like can be given. As an example of a wireless communication device, an RFID (radio frequency identification) tag can be given. The RFID tag is also referred to as an RF tag, a wireless tag, an electronic tag, or a wireless chip.

15 [0250]

An example of a structure of the semiconductor device of this embodiment will be described with reference to FIG. 11. FIG. 11 is a block diagram showing an example of a structure of the semiconductor device of this embodiment.

[0251]

20 The semiconductor device illustrated in FIG. 11 includes a clock signal generation circuit (also referred to as CLKG) 501, a first digital circuit 502a (also referred to as DIG1), and a second digital circuit 502b (also referred to as DIG2).

[0252]

The clock signal generation circuit 501 has a function of outputting a first clock
25 signal and a second clock signal. The clock signal generation circuit 501 is provided with an oscillator circuit and a divider circuit. Any of the divider circuits of the above embodiments can be used as the divider circuit of this embodiment. Note that a cycle of the first clock signal and a cycle of the second clock signal are different from each other, and the cycle of the second clock signal is N times longer than the cycle of the
30 first clock signal.

[0253]

The first clock signal generated in the clock signal generation circuit 501 is

input to the first digital circuit 502a. The first digital circuit 502a has a function of performing arithmetic processing using the clock signal. A circuit including a shift register, a flip-flop, a logic circuit, or the like can be given as an example of the first digital circuit 502a.

5 [0254]

The second clock signal generated in the clock signal generation circuit 501 is input to the second digital circuit 502b. The second digital circuit 502b has a function of performing arithmetic processing using the clock signal. A circuit including a shift register, a flip-flop, a logic circuit, or the like can be given as an example of the second
10 digital circuit 502b.

[0255]

As described above, the semiconductor device of this embodiment includes a divider circuit in a clock signal generation circuit. With such a structure, even in the case where a plurality of digital circuits each of which is driven by a clock signal with a
15 different cycle is provided, each of the digital circuits can operate.

This application is based on Japanese Patent Application serial no. 2010-090296 filed with Japan Patent Office on April 9, 2010, the entire contents of which are hereby incorporated by reference.

20

CLAIMS

1. A divider circuit comprising:

5 a shift register configured to output $2X$ pulse signals in accordance with a first clock signal and a second clock signal, wherein X is a natural number greater than or equal to 2; and

a divided signal output circuit configured to output a third clock signal with a cycle X times longer than a cycle of the first clock signal in accordance with the $2X$ pulse signals,

10 wherein the divided signal output circuit comprises:

X first transistors each having a source, a drain, and a gate,

wherein the shift register is configured to separately supply the respective gates of the X first transistors with the first to X -th pulse signals among the $2X$ pulse signals, and

15 wherein the X first transistors are configured to control whether voltage of a signal to be the third clock signal is set to first voltage; and

X second transistors each having a source, a drain, and a gate,

wherein the shift register is configured to separately supply the respective gates of the X second transistors with $(X + 1)$ -th to $2X$ -th pulse signals among the $2X$ pulse signals, and

20 wherein the X second transistors are configured to control whether voltage of a signal to be the third clock signal is set to second voltage.

2. The divider circuit according to claim 1,

25 wherein the shift register comprises sequential circuits of $2X$ stages,

wherein sequential circuits of odd-numbered stage in the $2X$ stages each comprise a third transistor which controls whether voltage of a pulse signal is set to voltage having a value depending on the first clock signal, and

30 wherein sequential circuits of even-numbered stage in the $2X$ stages each comprise a fourth transistor which controls whether the voltage of a pulse signal is set to voltage having a value depending on the second clock signal.

3. The divider circuit according to claim 1,
wherein a value of voltage of at least part of the $2X$ pulse signals is higher than
or equal to power supply voltage.

5 4. The divider circuit according to claim 1,
wherein the X first transistors and the X second transistors each comprise an
oxide semiconductor layer serving as a channel formation layer, and
wherein a band gap of the oxide semiconductor layer is 2 eV or more.

10 5. The divider circuit according to claim 1,
wherein the first clock signal and the second clock signal are clock signals
whose waveforms are different from each other by a $1/2$ cycle.

6. A clock signal generation circuit comprising:

15 an oscillator; and

the divider circuit according to claim 1.

7. A divider circuit comprising:

20 a first unit divider circuit configured to generate a third clock signal in
accordance with a first clock signal and a second clock signal, wherein a cycle of the
third clock signal is X times longer than a cycle of the first clock signal, and wherein X
is a natural number greater than or equal to 2; and

25 a second unit divider circuit configured to generate a fourth clock signal in
accordance with the third clock signal, wherein a cycle of the fourth clock signal is a
cycle K times longer than the cycle of the third clock signal, and wherein K is a natural
number greater than or equal to 2,

wherein the first unit divider circuit comprises:

30 a shift register configured to output $2X$ pulse signals in accordance
with the first clock signal and the second clock signal; and

a divided signal output circuit configured to output the third clock
signal in accordance with the $2X$ pulse signals,

wherein the divided signal output circuit comprises:

X first transistors each having a source, a drain, and a gate,
wherein the shift register is configured to separately supply
the respective gates of the X first transistors with the first to X -th pulse signals among
the $2X$ pulse signals, and

5 wherein the X first transistors are configured to control
whether voltage of a signal to be the third clock signal is set to first voltage; and

X second transistors each having a source, a drain, and a gate,
wherein the shift register is configured to separately supply
the respective gates of the X second transistors with $(X + 1)$ -th to $2X$ -th pulse signals
10 among the $2X$ pulse signals, and

wherein the X second transistors are configured to control
whether voltage of a signal to be the third clock signal is set to second voltage.

8. The divider circuit according to claim 7,
15 wherein the shift register comprises sequential circuits of $2X$ stages,
wherein sequential circuits of odd-numbered stage in the $2X$ stages each
comprise a third transistor which controls whether voltage of a pulse signal is set to
voltage having a value depending on the first clock signal, and

wherein sequential circuits of even-numbered stage in the $2X$ stages each
20 comprise a fourth transistor which controls whether the voltage of a pulse signal is set to
voltage having a value depending on the second clock signal.

9. The divider circuit according to claim 7,
wherein a value of voltage of at least part of the $2X$ pulse signals is higher than
25 or equal to power supply voltage.

10. The divider circuit according to claim 7,
wherein the X first transistors and the X second transistors each comprise an
oxide semiconductor layer serving as a channel formation layer, and
30 wherein a band gap of the oxide semiconductor layer is 2 eV or more.

11. The divider circuit according to claim 7,

wherein the first clock signal and the second clock signal are clock signals whose waveforms are different from each other by a $1/2$ cycle.

12. A clock signal generation circuit comprising:

5 an oscillator; and
the divider circuit according to claim 7.

13. A divider circuit comprising:

a shift register configured to output a plurality of pulse signals comprising a
10 first pulse signal, a second pulse signal, a third pulse signal, and a fourth pulse signal in
accordance with a first clock signal and a second clock signal; and

a divided signal output circuit configured to output a third clock signal with a
cycle X times longer than a cycle of the first clock signal in accordance with the
plurality of pulse signals, wherein X is a natural number greater than or equal to 2,

15 wherein the divided signal output circuit comprises:

a plurality of first transistors configured to control whether voltage of
a signal to be the third clock signal is set to first voltage, the plurality of first transistors
comprising at least two transistors; and

a plurality of second transistors configured to control whether voltage
20 of a signal to be the third clock signal is set to second voltage, the plurality of second
transistors comprising at least two transistors,

wherein the shift register is configured to supply a gate of one of the
two transistors comprised in the plurality of first transistors with one of the first pulse
signal and the second pulse signal,

25 wherein the shift register is configured to supply a gate of the other of
the two transistors comprised in the plurality of first transistors with the other of the first
pulse signal and the second pulse signal,

wherein the shift register is configured to supply a gate of one of the
two transistors comprised in the plurality of second transistors with one of the third
30 pulse signal and the fourth pulse signal, and

wherein the shift register is configured to supply a gate of the other of
the two transistors comprised in the plurality of second transistors with the other of the

third pulse signal and the fourth pulse signal.

14. The divider circuit according to claim 13,
wherein the plurality of pulse signals comprise $2X$ pulse signals.

5

15. The divider circuit according to claim 14,
wherein the plurality of first transistors comprise X transistors, and
wherein the plurality of second transistors comprise X transistors.

10

16. The divider circuit according to claim 13,
wherein the plurality of first transistors and the plurality of second transistors
each comprise an oxide semiconductor layer serving as a channel formation layer, and
wherein a band gap of the oxide semiconductor layer is 2 eV or more.

15

17. The divider circuit according to claim 13,
wherein the shift register comprises sequential circuits of $2X$ stages,
wherein sequential circuits of odd-numbered stage in the $2X$ stages each
comprise a third transistor which controls whether voltage of a pulse signal is set to
voltage having a value depending on the first clock signal, and

20

wherein sequential circuits of even-numbered stage in the $2X$ stages each
comprise a fourth transistor which controls whether the voltage of a pulse signal is set to
voltage having a value depending on the second clock signal.

25

18. The divider circuit according to claim 13,
wherein a value of voltage of at least part of the $2X$ pulse signals is higher than
or equal to power supply voltage.

30

19. The divider circuit according to claim 13,
wherein the first clock signal and the second clock signal are clock signals
whose waveforms are different from each other by a $1/2$ cycle.

20. A clock signal generation circuit comprising:

an oscillator; and
the divider circuit according to claim 13.

FIG. 1

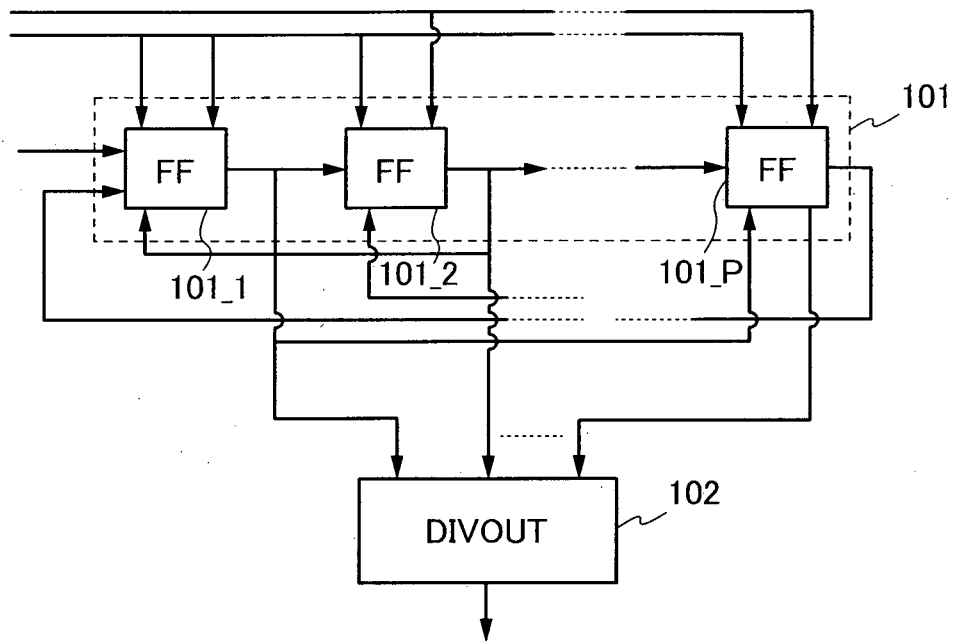


FIG. 2A

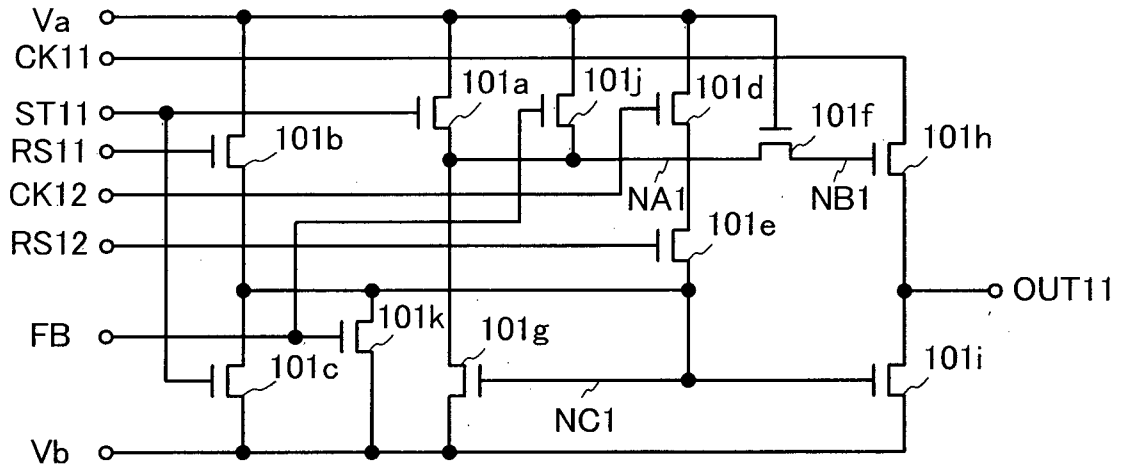


FIG. 2B

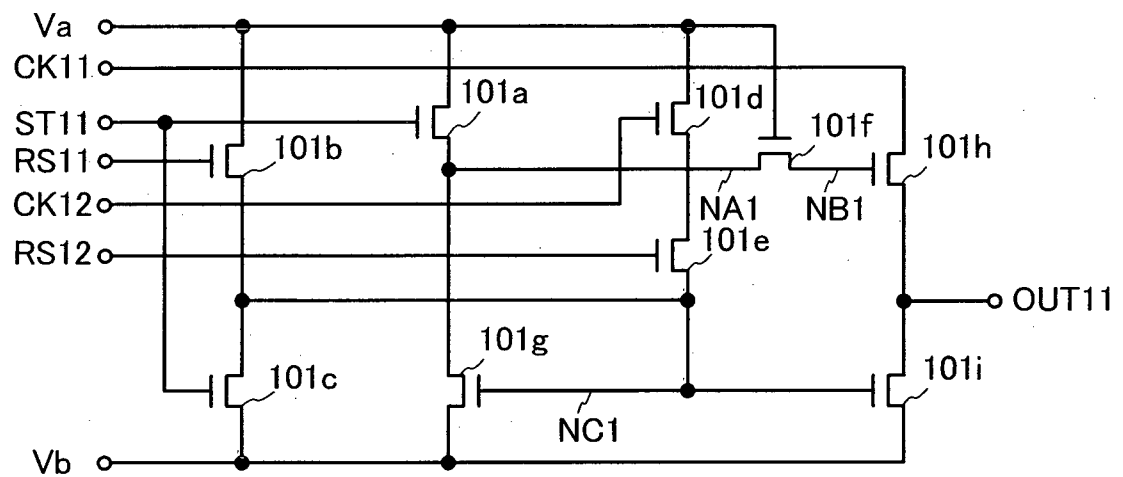


FIG. 2C

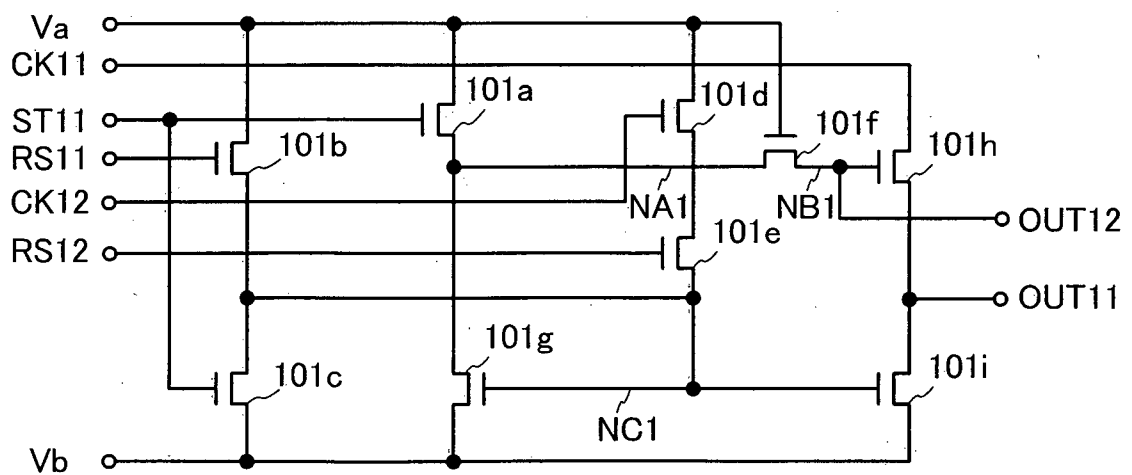


FIG. 3A

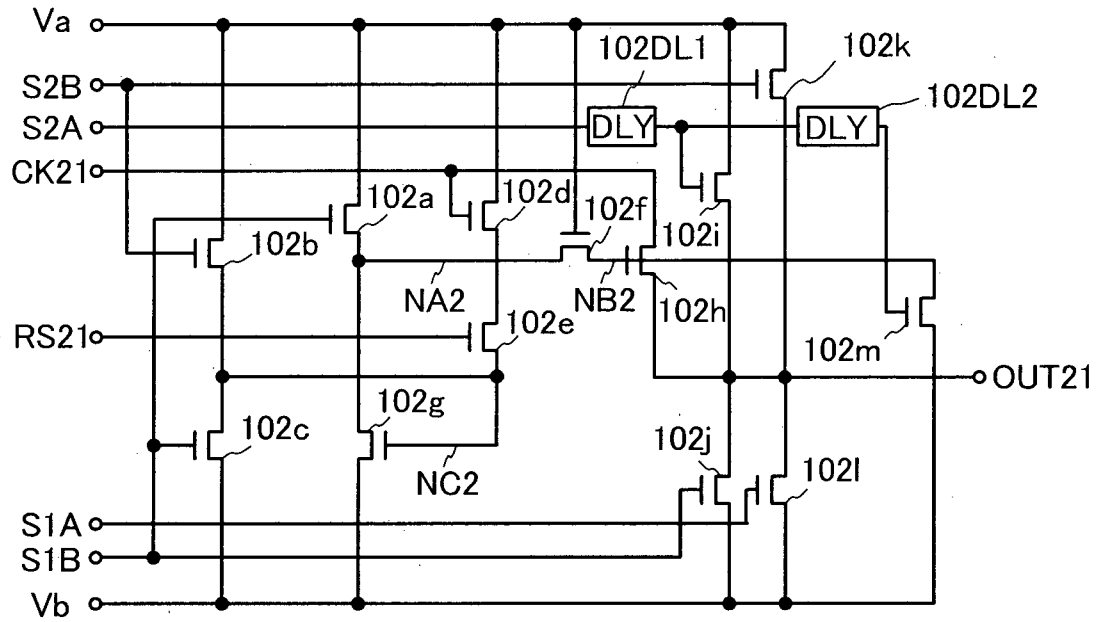


FIG. 3B

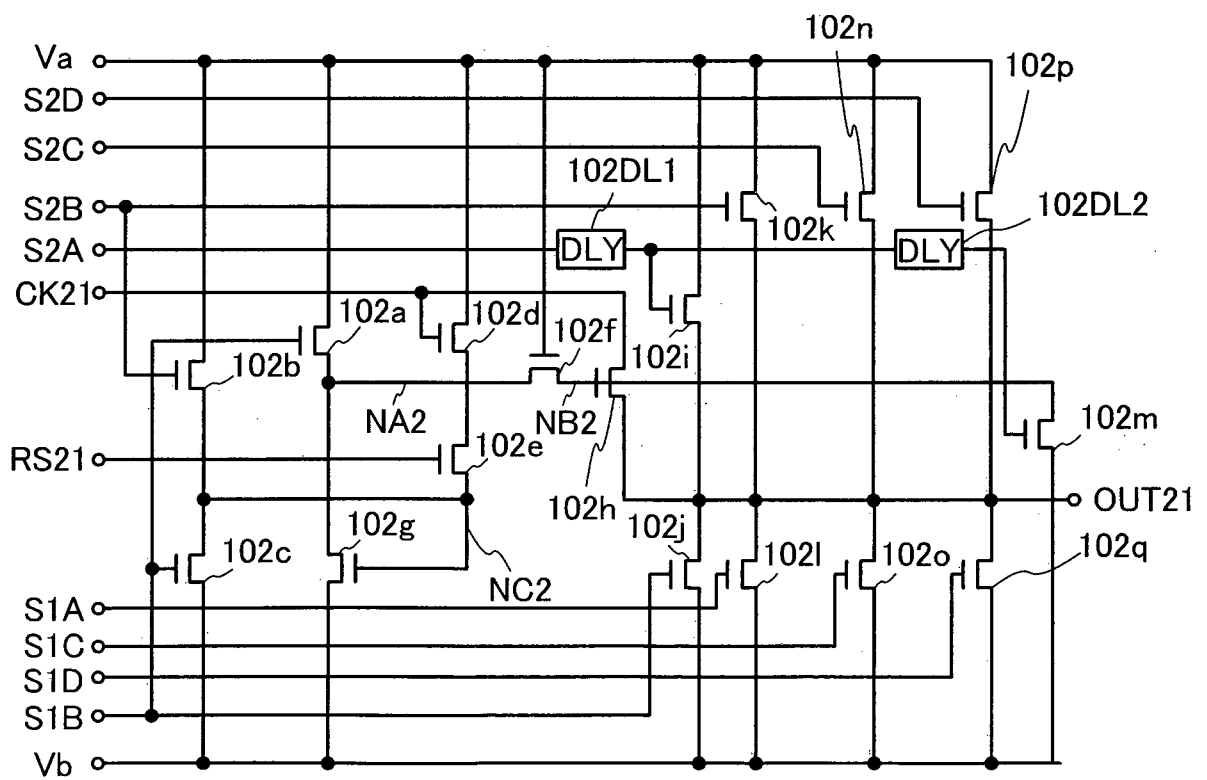


FIG. 4A

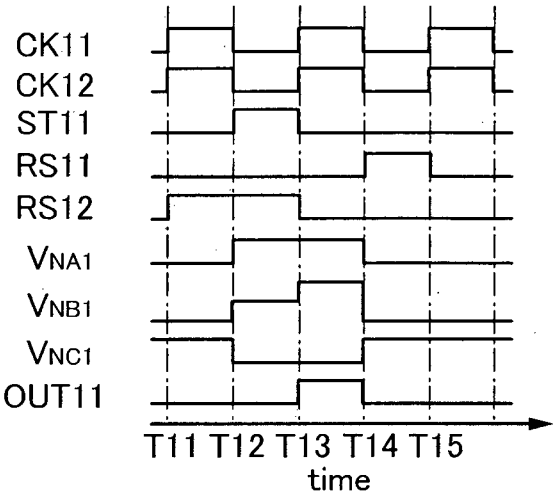


FIG. 4B

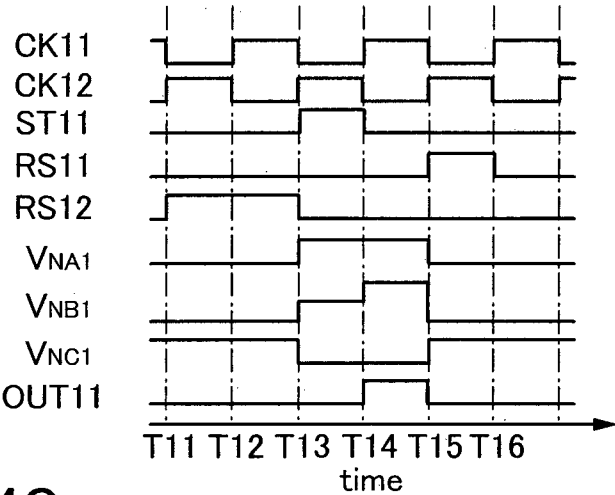


FIG. 4C

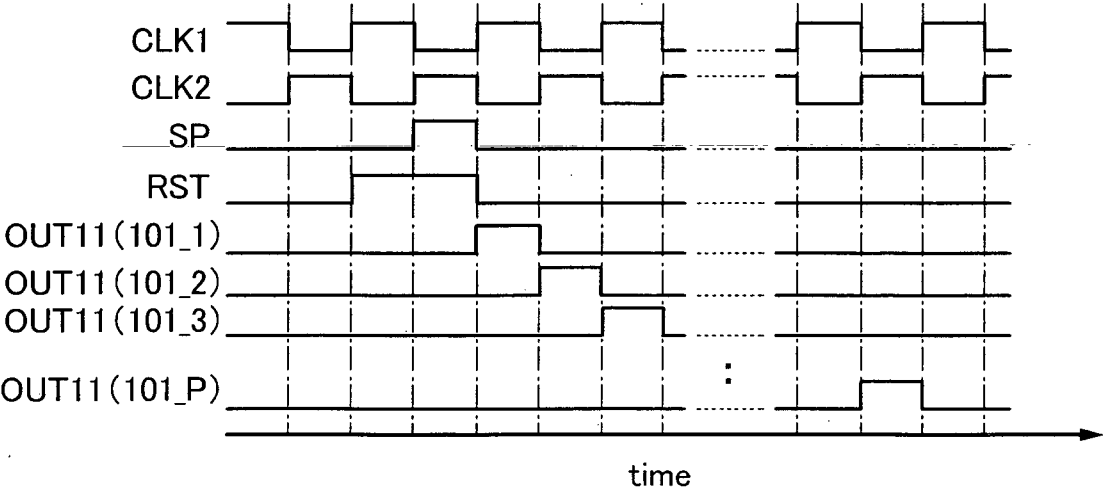


FIG. 5

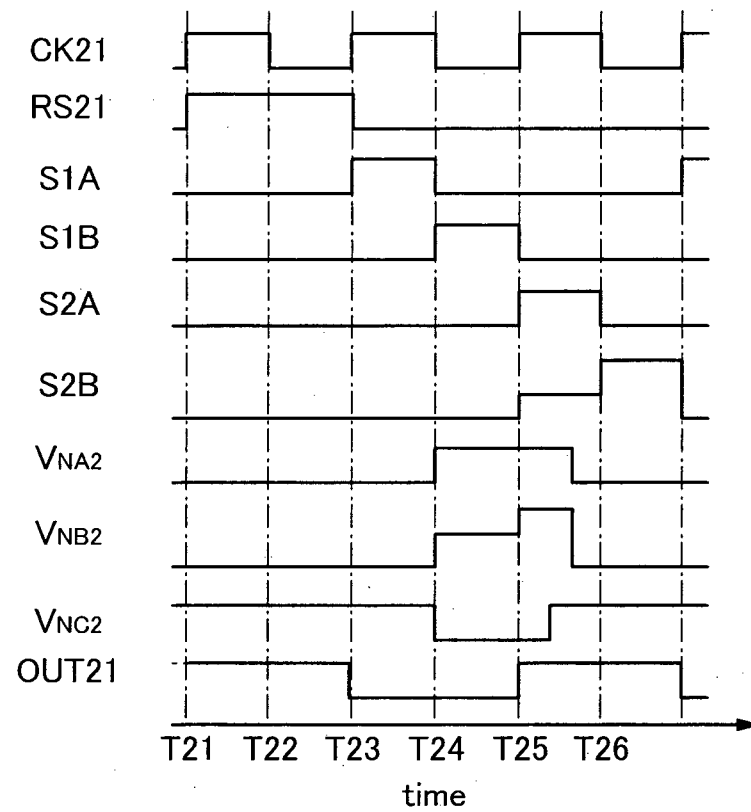


FIG. 6

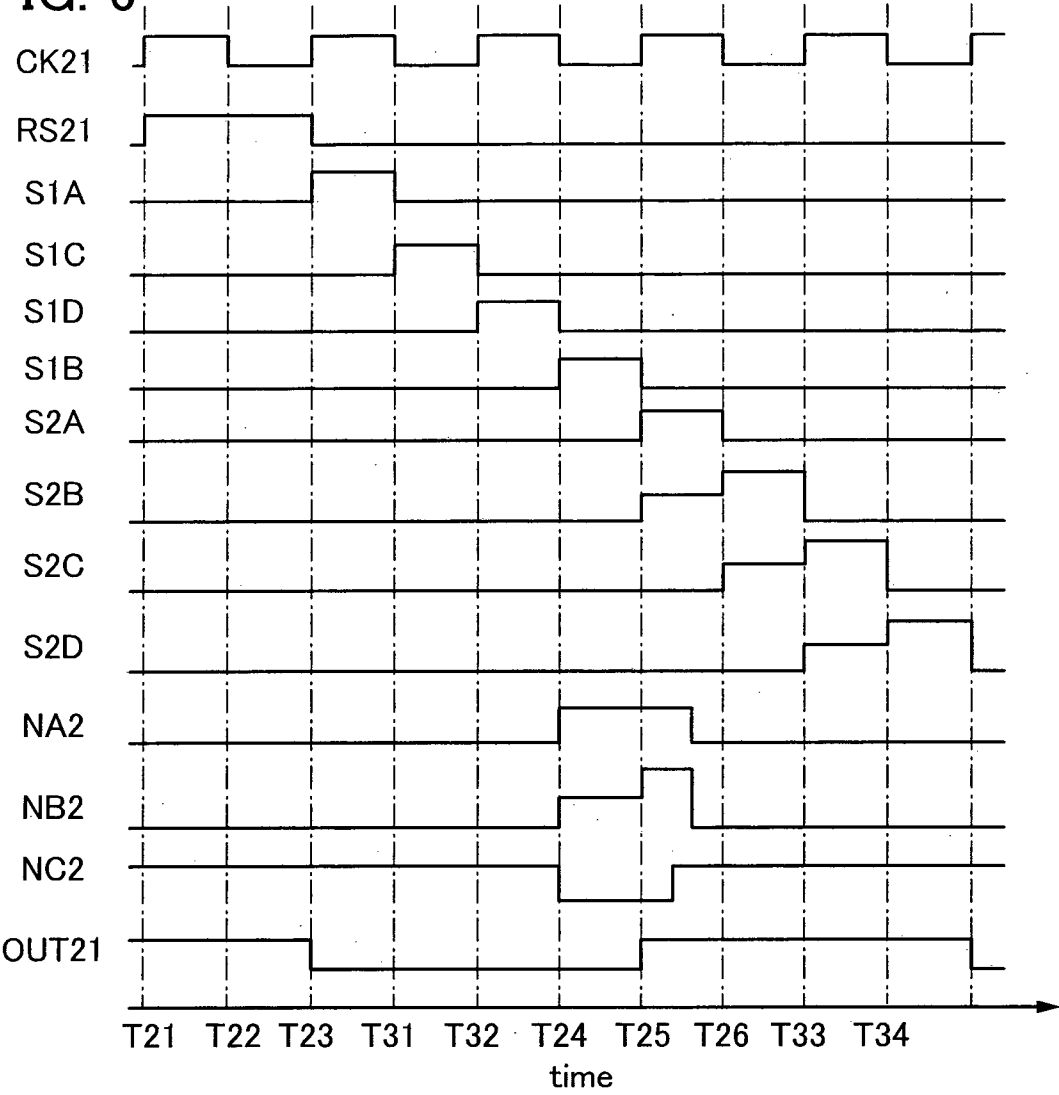


FIG. 7

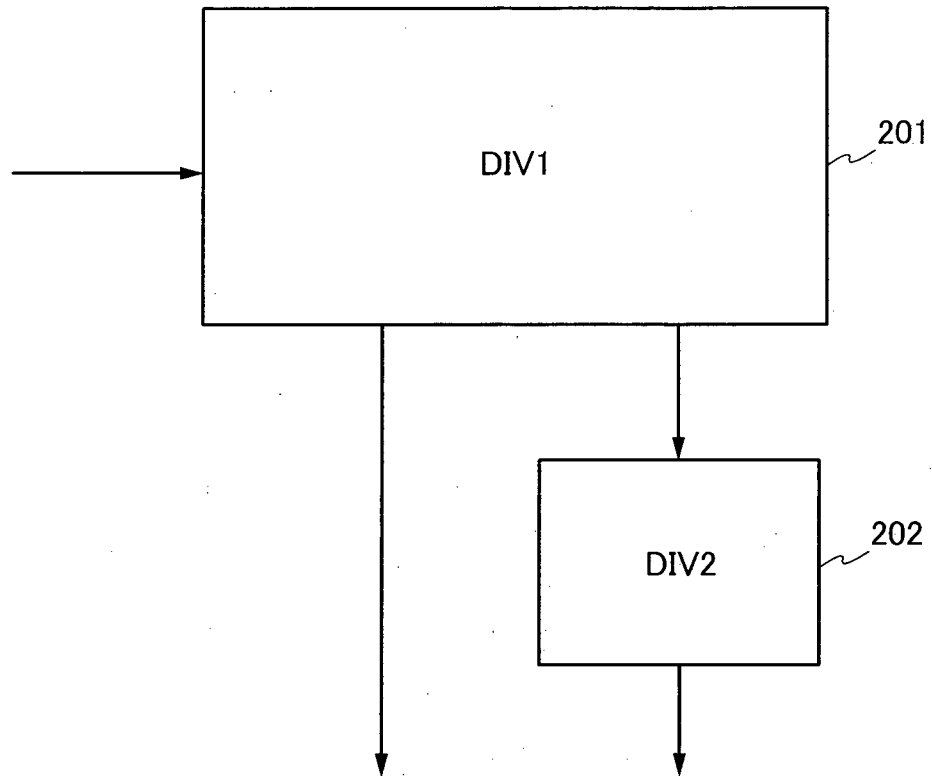


FIG. 8A

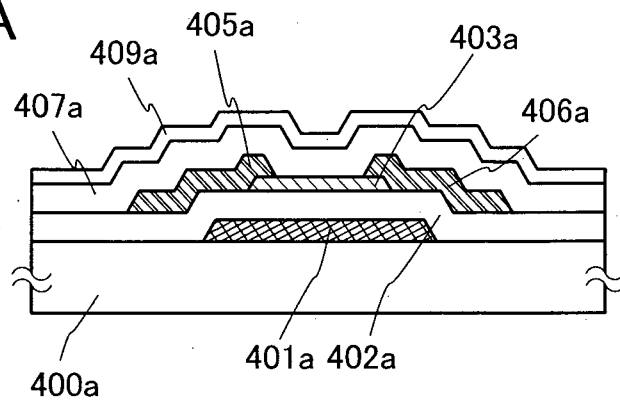


FIG. 8B

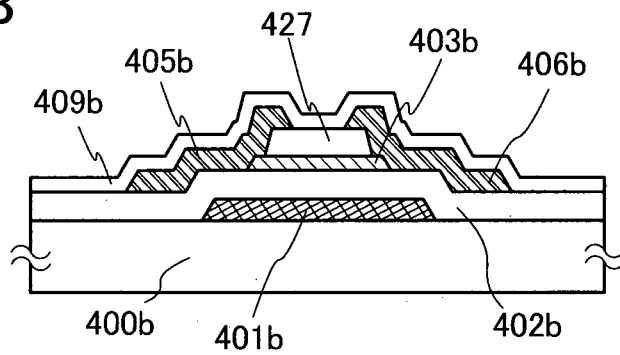


FIG. 8C

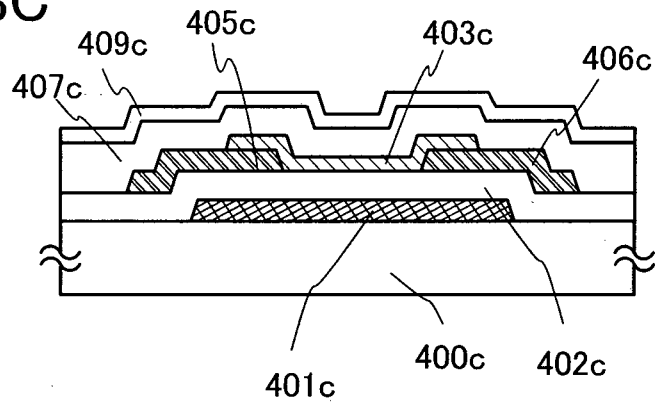


FIG. 8D

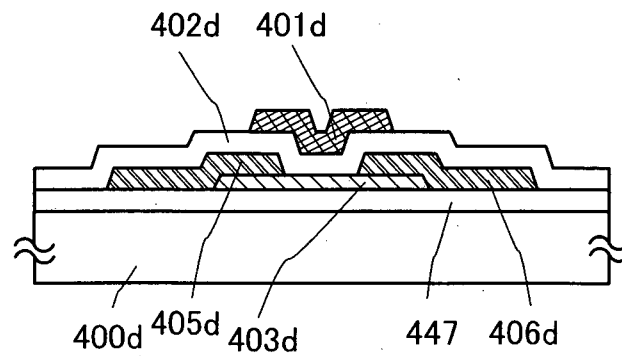


FIG. 9A

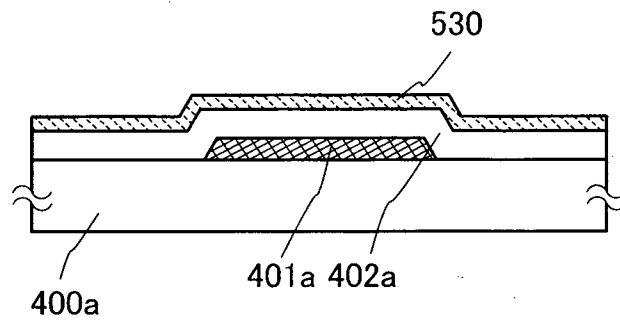


FIG. 9B

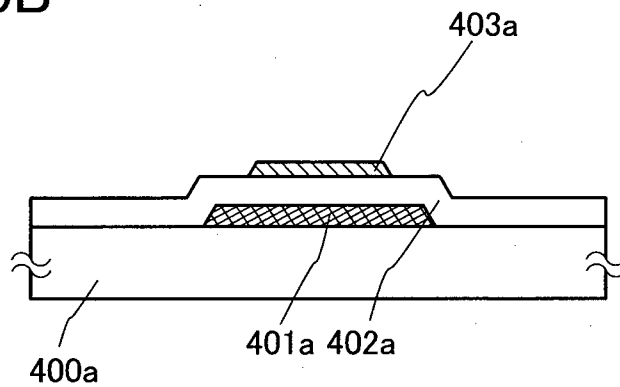


FIG. 9C

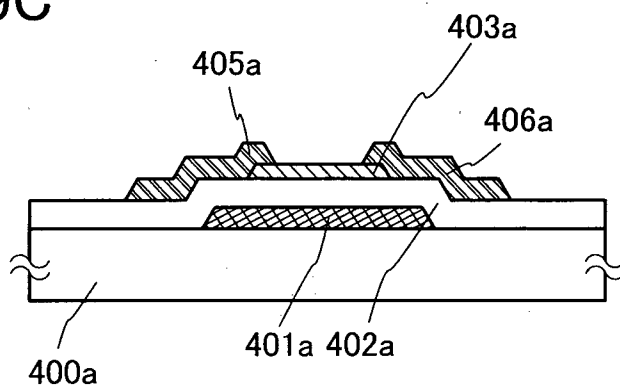


FIG. 10A

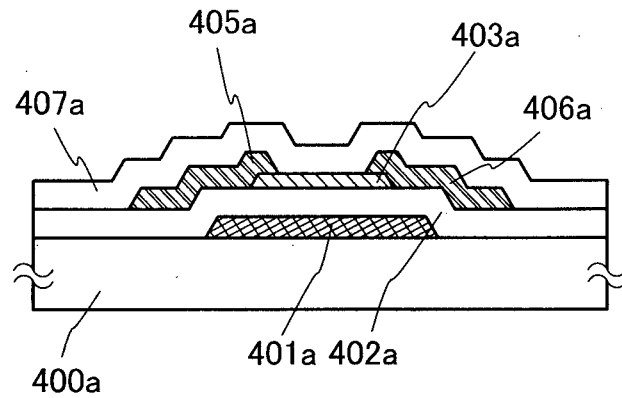


FIG. 10B

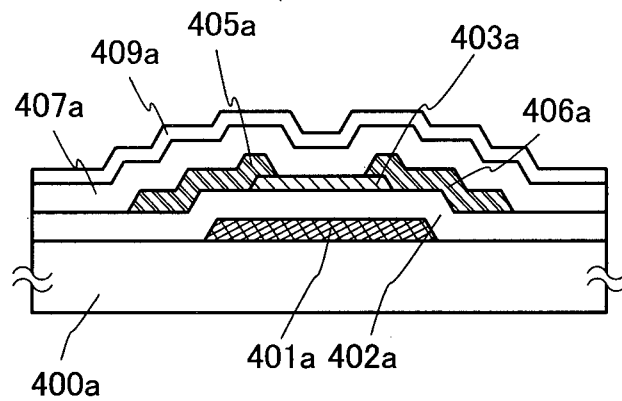
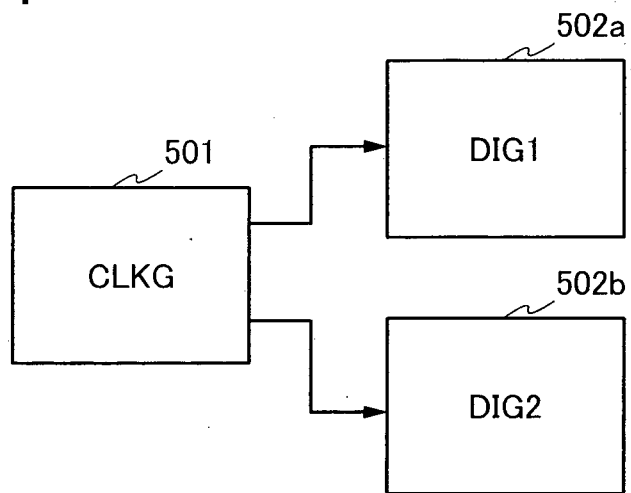


FIG. 11



EXPLANATION OF REFERENCE

101: shift register, 101a: transistor, 101b: transistor, 101c: transistor, 101d: transistor, 101e: transistor, 101f: transistor, 101g: transistor, 101h: transistor, 101i: transistor, 101j: transistor, 101k: transistor, 102: divided signal output circuit, 102a: transistor, 102b: transistor, 102c: transistor, 102d: transistor, 102e: transistor, 102f: transistor, 102g: transistor, 102h: transistor, 102i: transistor, 102j: transistor, 102k: transistor, 102l: transistor, 102m: transistor, 102n: transistor, 102o: transistor, 102p: transistor, 102q: transistor, 102DL1: delay circuit, 102DL2: delay circuit, 201: unit divider circuit, 202: unit divider circuit, 400a: substrate, 400b: substrate, 400c: substrate, 400d: substrate, 401a: conductive layer, 401b: conductive layer, 401c: conductive layer, 401d: conductive layer, 402a: insulating layer, 402b: insulating layer, 402c: insulating layer, 402d: insulating layer, 403a: oxide semiconductor layer, 403b: oxide semiconductor layer, 403c: oxide semiconductor layer, 403d: oxide semiconductor layer, 405a: conductive layer, 405b: conductive layer, 405c: conductive layer, 405d: conductive layer, 406a: conductive layer, 406b: conductive layer, 406c: conductive layer, 406d: conductive layer, 407a: oxide insulating layer, 407c: oxide insulating layer, 409a: protective insulating layer, 409b: protective insulating layer, 409c: protective insulating layer, 427: insulating layer, 447: insulating layer, 501: clock signal generation circuit, 502a: digital circuit, 502b: digital circuit, and 530: oxide semiconductor film.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/057496

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H03K3/356 (2006.01) i, H03K19/0175 (2006.01) i, H03K23/00 (2006.01) i,
H03K23/54 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H03K3/356, H03K19/0175, H03K23/00, H03K23/54

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2010-49791 A (KABUSHIKIKAISHA HANDOUTAI ENERUGI- KENKYUUSHO) 2010.03.04 Whole document, Figure4 and figure.9 (No Family)	1-20
A	JP 2008-122939 A (KABUSHIKIKAISHA HANDOUTAI ENERUGI- KENKYUUSHO) 2008.05.29 Whole document, Figure 8 & US 2008/0258998 A1	1-20
A	JP 2004-226429 A (KABUSHIKIKAISHA HANDOUTAI ENERUGI- KENKYUUSHO) 2004.08.12 Whole document, Figure4 and figure.9 & US 2004/0140839 A1 & US 2005/0062515 A1 & US 2006/0280279 A1	1-20



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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

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Date of mailing of the international search report

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