United States Patent

[11] 3,585,629

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[54] **DISPLAY UTILIZING DIMMED OR FLICKERING LAMPS TO INDICATE DIFFERENT DATA SETS**
5 Claims, 5 Drawing Figs.

[52] **U.S. Cl.** **340/324R,** 340/331, 340/332
[51] **Int. Cl.** **G08b 5/38**
[50] **Field of Search** ..... 340/324 R, 331, 276, 332

[56] **References Cited**

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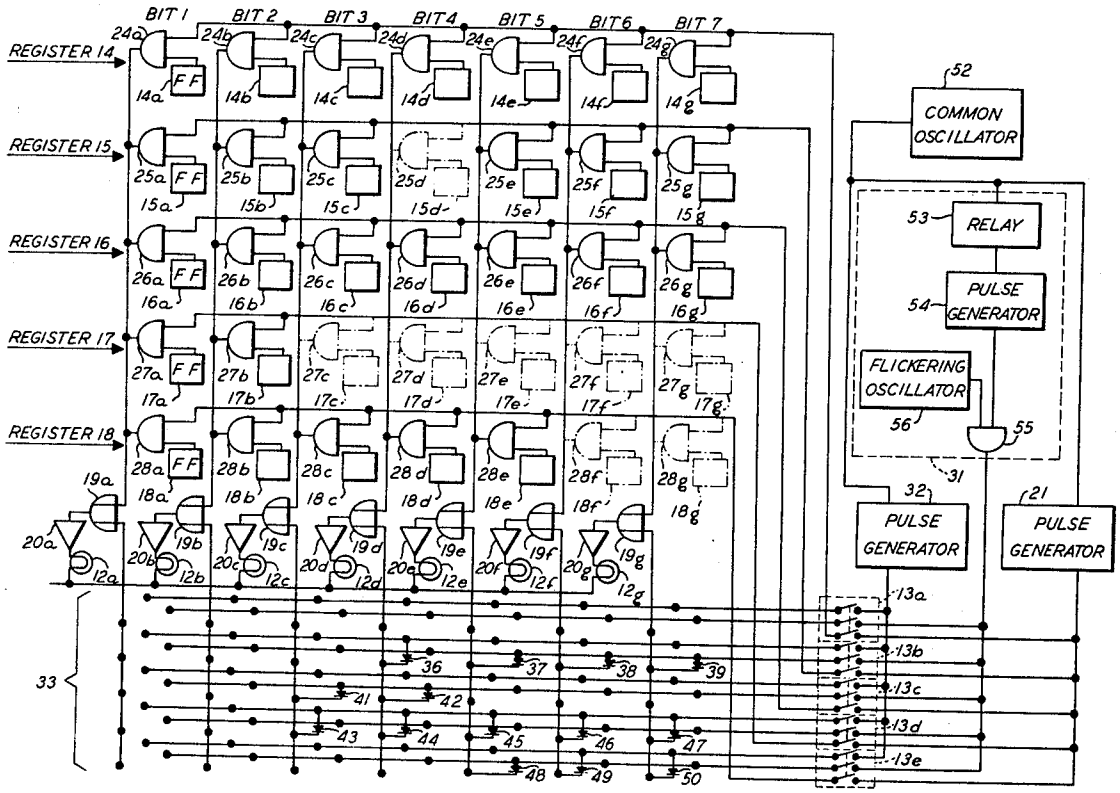
ABSTRACT: Different data sets displayed in a lamp array are distinguished by dimming or blinking the lamps associated with the different data sets. Pulse generators having different duty cycles and different frequencies of operation are used to illuminate the dimmed or flickering lamps.



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SHEET 1 OF 3

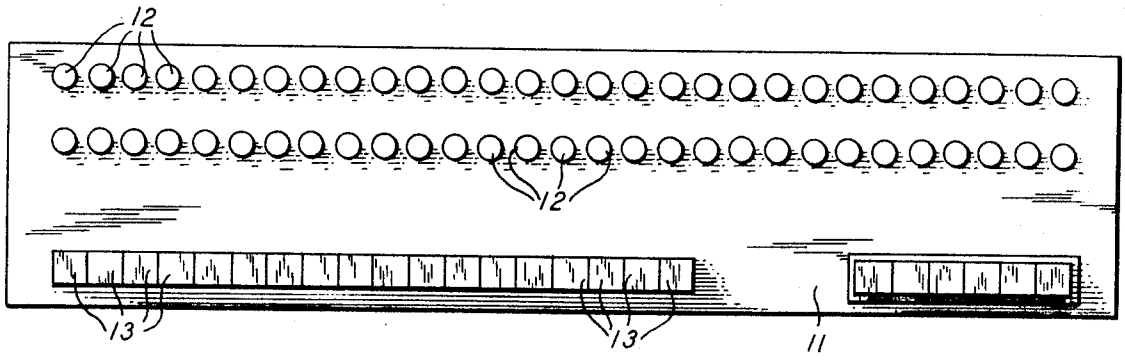

FIG-1

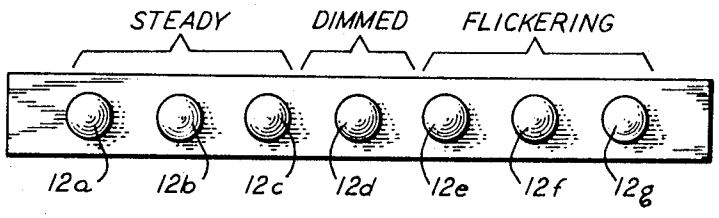

FIG-2

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FIG-3

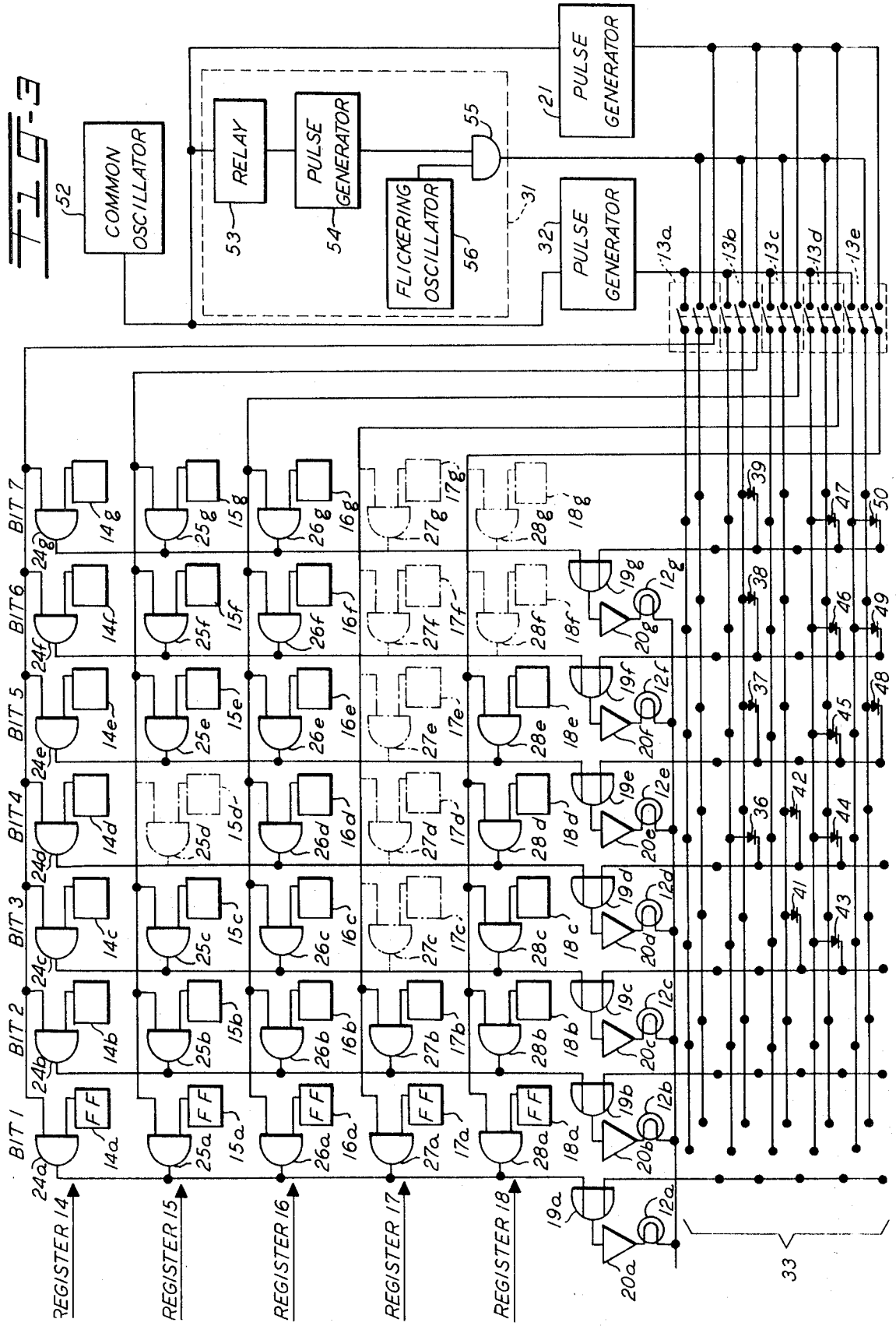
COMMON OSCILLATOR
52
RELAY
53
PULSE GENERATOR
54
FLICKERING OSCILLATOR
56
55
31
PULSE GENERATOR
32
PULSE GENERATOR
21
13a
13b
13c
13d
13e
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT6
BIT 7
REGISTER 14
REGISTER 15
REGISTER 16
REGISTER 17
REGISTER 18
33

FIG-4

	STATE OF APPLIED BINARY SIGNAL			
	0		1	
	DUTY CYCLE OF LAMP CURRENT	BRIGHTNESS OF LAMP	DUTY CYCLE OF LAMP CURRENT	BRIGHTNESS OF LAMP
STEADY	0 %	DARK	85 %	MEDIUM
FLICKERING	25 %	VERY DIM	100 %	BRIGHT
	0 %	DARK	85 %	MEDIUM
DIMMED	35 %	DIM		

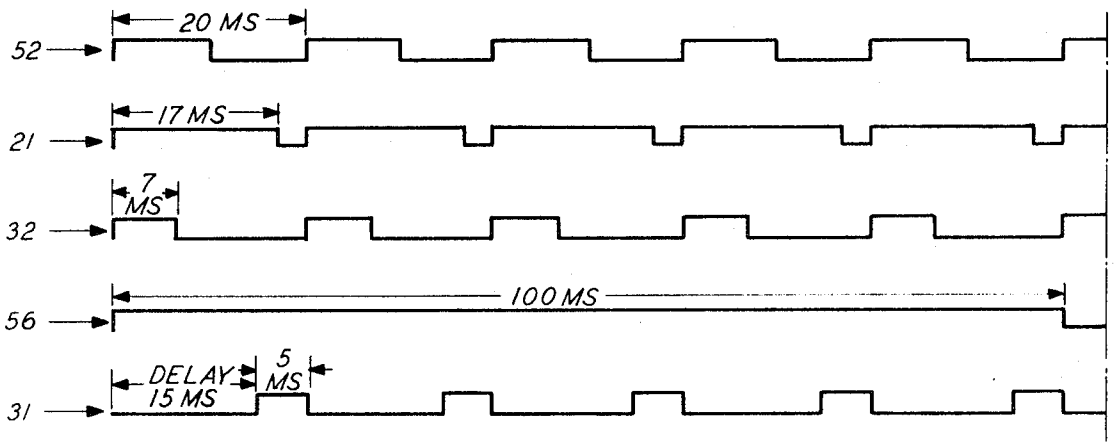

FIG-5

DISPLAY UTILIZING DIMMED OR FLICKERING LAMPS TO INDICATE DIFFERENT DATA SETS

GOVERNMENT CONTRACT

The invention herein claimed was made in the course of, or under contract with the United States Army.

BACKGROUND OF THE INVENTION

1. Field of the Invention

In various data storage and processing systems, such as digital computers, it is often necessary to display the contents of one or more storage registers of the system upon an operator's control panel for purposes of troubleshooting or data analysis. This may be done by providing a row or array of indicating lamps which may be selectively illuminated to display the contents of each bit position of a binary storage register. The information in the register, however, may consist of a plurality of different words, each of which has a particular significance and, further, there may be unused bit positions within the register. In order to enable an operator at the display console to distinguish the lamps which correspond to different words of a display and to be alerted to those bit positions which are unused in the selected register, the display must incorporate some means of dividing the display into word groups and used and unused bit positions.

2. Description of the Prior Art

One technique which has been used in the past to distinguish various word groups from one another is that of simply labeling the display lamps and marking off word groups on the face of the panel. However, if a single lamp display is used to selectively display different registers which contain words of different lengths and different word group arrangements, permanent labeling cannot be used. Flexible labeling arrangements, such as an optical screen above the display lamps upon which different labels may be selectively projected to correspond to the selected register being displayed have been proposed. Most of these arrangements, however, are very complicated and therefore very expensive to implement.

SUMMARY OF THE INVENTION

An object of the present invention is a display lamp system utilizing new and improved facilities for indicating different groups of the lamps.

In one embodiment of the invention, different modulation signals are superimposed upon the signals to respective groups of lamps to produce different illumination characteristics between different groups of lamps. More particularly, different lamps within a display are either brightly illuminated, blinked or dimly illuminated to distinguish adjacent word groups within the display and/or unused bit positions within the display

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a display panel for a data storage system;

FIg. 2 is a row of indicator lamps which may be selectively energized to display the contents of a given date register upon the face of the console shown in FIG. 1;

FIG. 3 is a schematic diagram of a lamp energizing circuit constructed in accordance with the invention;

FIG. 4 is a chart illustrating the various lamp illumination arrangements for various groups of data; and

FIG. 5 is a diagram of various voltage waveforms produced by pulse generators in FIG. 3 illustrating the timing relationship between the waveforms.

DETAILED DESCRIPTION

Referring to FIG. 1, there is shown a control panel upon which the contents of selected storage registers within the system may be displayed for purposes of troubleshooting or data analysis. The panel includes a face plate **11** upon which a plurality of adjacent display lamps **12–12** and a plurality of register selection buttons **13–13** are mounted. When a selected one of the register select buttons **13** is depressed, the contents of the selected register are automatically displayed, in binary form, by illuminating various lamps **12** within the lamp display.

Referring to FIG. **3**, a circuit is shown to provide a system for illuminating the lamps in a display, such as seven lamps **12***a*—*12g*, indicating different words and unused bit positions. FIG. **3** illustrates the invention by illustratively showing five different registers, **14**—**18**, which may be selectively displayed on the lamps **12***a*—*12g* by closing a respective one of the switches **13***a*—*13e*. The switches **13***a*—*13e* are mechanically coupled in a conventional manner to prevent operation of more than one switch at a time. Thus, only one of the registers **14**—**18** may be displayed on the lamps **12***a*—*12g* at one time. It is to be noted that registers or portions of registers having many more than seven-bit positions could be displayed using the technique of the present invention and the total number of registers which may be selectively displayed could be much greater.

Register **14** includes seven bistable storage devices, such as flip-flops **14***a*—*14g*. The state of each of the flip-flops **14***a*—*14g* determines whether a 1 or 0 is stored in that particular bit position of the register **14**. The flip-flops **14***a*—*14g* are set and reset by an associated computer or storage equipment (not shown) of a data system. Each of the flip-flops **14***a*—*14g* is connected to one input of one of the respective AND gates **24***a*—*24g*. The other input of each of the AND gates **24***a*—*24g* is connected by the register selector switch **13***a* to a pulse generator **21**. The outputs of each of the AND gates **24***a*—*24g* is connected by a respective OR gate **19***a*—*19g* and a respective amplifier **20***a*—*20g* to the respective lamp **12***a*—*12g*. Thus, the respective lamps **12***a*—*12g* are illuminated if the corresponding flip-flops **14***a*—*14g* have a 1 stored therein.

Similarly, the registers **15**—**18** have respective flip-flops **15***a*—*15g*, **16***a*—*16g*, **17***a*—*17g* and **18***a*—*18g* which are connected to first inputs of respective AND gates **25***a*—*25g*, **26***a*—*26g*, **27***a*—*27g* and **28***a*—*28g*. The second inputs of the AND gates **25***a*—*25g*, **26***a*—*26g*, **27***a*—*27g* and **28***a*—*28g* may be selectively connected to the pulse generator **21** by the switches **13***b*—*13e*. The outputs of the AND gates **25***a*—*25g*, **26***a*—*26g*, **27***a*—*27g* and **28***a*—*28g* are connected by respective OR gates **19***a*—*19g* and respective amplifiers **20***a*—*20g* to the respective lamps **12***a*—*12g*. Thus, when a respective one of the switches **13***b*—*13e* is closed the contents of a respective one of the registers **15**—**18** is displayed on the lamps **12***a*—*12g*.

The flip-flops **15***d*, **17***c*—*17g*, **18***f* and **18***g* are shown in phantom in FIG. **3** to indicate that these memory positions are unused. In an actual hardware arrangement they may be eliminated along with the AND gates **25***d*, **27***c*—*27g*, **28***f* and **28***g*, or if the flip-flops **15***d*, **17***c*—*17g*, **18***f* and **18***g* are present, they are maintained in a 0 state.

Signals from pulse generators **31** and **32** are selectively superimposed on the signals from the pulse generator **21** by the selected one of the switches **13***a*—*13e* connecting the generators **31** and **32** to a diode matrix **33** which in turn is designed to selectively apply to outputs of generators **31** and **32** to the OR gates **19***a*—*19g*. For example, operation of the switch **13***b* applies the output of the generator **32** through a diode **36** to the OR gate **19***d* and applies the output of the generator **31** through the diodes **37**, **38** and **39** to the OR gates **19***e*, **19***f* and **19***g*. Similarly, diodes **41**—**50** in the matrix **33** connect the respective pulse generators **31** and **32** to respective OR gates **19***c*—*19d* when a respective switch **13***c*—*13e* is closed.

The pulse generators **21**, **31** and **32** are driven by a common relaxation oscillator **52**, having a frequency which does not produce a discernable flicker of the lamps **12***a*—*12g*. Where the lamps **12***a*—*12g* are incandescent lamps, the oscillator **52** should have a frequency greater than about 40 Hz. while for gaseous discharge lamps the frequency must be somewhat greater or greater than about 45 Hz. The pulse generators **21** and **32** are designed to produce output pulses on every cycle

of the oscillator **52**. One suitable type of pulse generator is a monostable multivibrator. The duty cycle of the pulse generator **21** is designed to give a medium illumination to the lamps **12***a*—*12g*. A duty of about 70 to 90 percent of the cycle time of the pulse generator **21** has been found to give a medium illumination to incandescent lamps while a duty of about 45 to 60 percent gives a medium illumination to gaseous discharge lamps. The duty cycle of the pulse generator **32** is designed to give a dim illumination to the lamps **12***a*—*12g*. A duty of about 15 to 40 percent of the cycle time of the pulse generator **32** has been found to give a dim illumination to incandescent lamps while a duty of about 5 to 20 percent gives a dim illumination to gaseous discharge lamps. If lamps other than incandescent or gaseous discharge are used, the duty cycles and frequencies may be accordingly adjusted.

The pulse generator **31** includes a delay circuit **53** and a pulse generator **54** for applying a pulse to an input of an AND gate **55**. The pulse generator **54** has a duty time designed to give a dim illumination to the lamps **12***a*—*12g*. The delay circuit **53** delays the input signal to the pulse generator **54** such that the output pulse of the pulse generator **54** occurs during the off time of the pulse generator **21**. Thus, when the output of the pulse generator **54** is superimposed on the output of the pulse generator **21** to illuminate one of the lamps **12***a*—*12g*, the lamp will be brightly illuminated. A flickering oscillator **56** is connected to the other input of the AND gate **55** to modulate the signal from the pulse generator **54** at a frequency designed to produce a discernable flickering or blinking of the lamps **12***a*—*12g*. For incandescent lamps the frequency must be less than about 20 Hz. while for gaseous discharge lamps the frequency may go up to about 30 Hz. and still be discernable.

Referring now to FIG. **5**, there are shown typical output signals for the generators **21**, **31** and **32** to operate incandescent lamps. The oscillator **52** operates at 50 Hz. and the oscillator **56** operates at 5 Hz. The generator **21** is triggered by the oscillator **52** and produces a 17 ms. pulse. The generator **32** produces a 5 ms. pulse which is delayed by 15 ms. from the start of each cycle of the oscillator **52**. The 5 **ms.** pulses are produced only during the first half of the 0.2-second-cycle time of the oscillator **56** while no pulses are produced by the generator **31** during the last half of the 0.2-second-cycle time of the oscillator **56**.

Referring back to FIG. **3**, in operation with the switch **13***b* closed to display the contents of register **15** on the lamps **12***a*—*12g*, the 85 percent duty cycle pulse from the generator **21** is applied to the AND gates **25***a*, **25***b*, **25***c*, **25***e*, **25***f* and **25***g*. If any of the flip-flops **15***a*, **15***b*, **15***c*, **15***e*, **15***f* and **15***g* are in the 1 state, the pulses pass through the respective AND gate **25***a*—*25c*, and **25***e*—*25g* and OR gate **19***a*—*19c* and **19***e*—*19g* to the respective lamp **12***a*—*12c* and **12***e*—*12g*. The output of the generator **32** is applied through diode **36** in the matrix **33** to the OR gate **19***d* and the lamp **12***d* to dimly illuminate the lamp **12***d* to indicate that the flip-flop **15***d* is unused or absent. The output of the generator **31** is applied through diodes **37**, **38** and **39** to the respective OR gates **19***e*, **19***f* and **19***g* to superimpose the output of the generator **31** on the output of the AND gates **25***e*, **25***f* and **25***g* to produce a readily noticeable flickering or blinking of the lamps **12***e*, **12***f* and **12***g*.

Referring now to FIGS. **2** and **4**, the three lamps **12***a*, **12***b* and **12***c* are operated in the "steady" condition where the respective lamps are dark if the respective flip-flops **15***a*, **15***b* or **15***c* are in the 0 state or the respective lamps **12***a*, **12***b* and **12***c* have medium illumination of the respective flip-flop **15***a*, **15***b* and **15***c* are in the 1 state. The lamp **12***d* is dimly illuminated and is easily distinguished from any of the lamps **12***a*, **12***b* and **12***c* which may have medium illumination. The respective lamps **12***e*, **12***f* and **12***g* flicker or blink between dark and dim illumination if the respective flip-flop **15***e*, **15***f* or **15***g* is in the 0 state or the respective lamps **12***e*, **12***f* and **12***g* flicker between medium and bright illumination if the respective flip-flop **15***e*, **15***f* or **15***g* is in the 1 state. It is easy to distinguish the "flickering" lamps **12***e*, **12***f* and **12***g* from the "steady" lamps **12***a*, **12***b* and **12***c* and the "dimmed" lamp **12***d*.

The circuit shown in FIG. **1** is merely illustrative of the principles of the invention. Many other display systems could be devised which utilize the principles of the invention. For example, the circuit describes a particular AND and OR gate arrangement for superimposing the "flickering" signal on the "steady" signal. There are many other modulating arrangements of signal generating arrangements which could be adapted in accordance with the invention to produce the same result.

What I claim is:

1. A system for displaying the contents of a register wherein the contents represent first and second data sets comprising:

a plurality of lamps each of which is associated with a respective stage of the register;

a first signal generator for producing a first signal to illuminate the lamps;

a second signal generator for producing a second signal to illuminate the lamps wherein lamps illuminated by the second signal are distinguishable from lamps illuminated by the first signal; and

means responsive to the contents of the register for applying the first and second signals to respective first and second groups of said plurality of lamps to display the respective first and second data sets.

2. A system for displaying the contents of a register containing first and second data sets, comprising:

a plurality of lamps, each of which is associated with a respective stage of the register;

a first signal generator for producing a first signal to illuminate the lamps in a steady condition;

a second signal generator for generating a second signal to illuminate the lamps with a noticeable flickering condition; and

means responsive to the contents of the register for applying the respective first and second signals to respective first and second groups of said plurality of lamps to display the first and second data sets.

3. A system for displaying the contents of a register containing first and second data sets, comprising:

a plurality of lamps each of which is associated with a respective stage of the register;

a first signal generator for producing a first signal to illuminate the lamps in a steady condition;

means responsive to the contents of the register for selectively applying the first signal to first and second groups of the lamps to display the respective first and second data sets;

a second signal generator for producing a second signal to illuminate the lamps with a noticeable flickering condition; and

means for superimposing the second signal onto the signals applied to the second group of lamps to produce a noticeable flickering of the second groups of lamps.

4. A system for displaying the contents of a binary register containing first and second data sets, comprising:

a plurality of lamps each of which is associated with a respective stage of the binary register;

a first pulse generator for producing a pulse signal having a duty cycle of from 45 to 90 percent to illuminate the lamps and having a frequency sufficiently high to produce no noticeable flickering of the lamps;

a plurality of AND gates, one connected to each stage of the register and to the first generator for passing the first signal when the respective stage of the register is in a first state and for blocking the first signal when the respective register stage is in a second state;

a second pulse generator producing a pulse signal having a duty cycle from 5 to 40 percent to illuminate the lamps and having a frequency sufficiently low to produce a noticeable flickering of the lamps;

a plurality of OR gates, one associated with each AND gate for applying the output of each AND gate to the respective lamp; and

selective connecting means for connecting the output of the second pulse generator to the OR gates associated with the register stages containing the second data set for imposing the flickering signal on the first signal whereby the second data set displayed on the lamps is easily distinguished from the first data set.

5. A system for displaying the contents of a register containing first and second data sets, comprising:

a plurality of lamps each of which is associated with a respective stage of the register;

a first pulse generator for producing an output pulse having a duty cycle of from 5 to 40 percent for illuminating the lamps with a first intensity;

second pulse generator for producing pulses having a duty cycle of from 45 to 90 percent for illuminating the lamps with a second intensity which is distinguishable from the first intensity; and

means responsive to the contents of the register for applying the respective first and second signals to the respective lamps associated with the first and second data sets whereby the first and second data sets may be distinguished from each other.

L-566-PT
(6-69)

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,585,629 Dated June 15, 1971

Inventor(s) JOSEPH S. BAYNARD, JR.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, line 59 cancel "date" and insert --data--.

Column 2, line 29, after "each" insert --one--.

Column 3, line 37, after "a" insert --7 ms pulse. The generator 32 produces a--.

Signed and sealed this 12th day of September 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents