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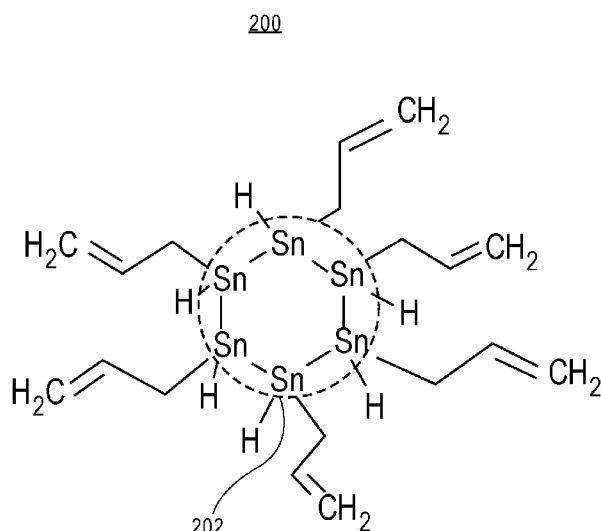


FIG. 2

(57) Abstract: Polysilane-, polygermane-, and polystannane-based resists for extreme ultraviolet or electron beam lithography are described. A discrete molecule for a resist formulation includes a closed central inorganic ring having only E-E bonds, where E is Si, Ge or Sn, or a combination thereof. Organic ligands are covalently bonded to the E atoms of the closed central inorganic ring. In another example, a discrete molecule for a resist formulation includes a central inorganic element E. Radiating E elements are bonded to the central element E to provide E-E bonds, where E is Si, Ge or Sn, or a combination thereof. Organic ligands are covalently bonded to the radiating E elements. In yet another example, a resist composition includes a solvent and a resist material selected from the group consisting of a polysilane material, a polygermane material, or a polystannane material, the resist material suspended or dissolved in the solvent.

**POLYSILANE-, POLYGERMANE-, AND POLYSTANNANE-BASED MATERIALS FOR EUV AND
EBEAM LITHOGRAPHY**

5 TECHNICAL FIELD

Embodiments of the invention are in the field of lithography and, in particular, lithography involving polysilane-, polygermane-, and polystannane-based resists.

BACKGROUND

10 For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips.

For example, shrinking transistor size allows for the incorporation of an increased
15 number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant. In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes,
20 tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and compatibility with the existing high-yielding bulk silicon substrate infrastructure. Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of
25 fundamental building blocks fabricated in a given region is increased, the constraints on the semiconductor processes used to fabricate these building blocks have become overwhelming.

Integrated circuits commonly include electrically conductive microelectronic structures, which are known in the arts as vias, to electrically connect metal lines or other interconnects

above the vias to metal lines or other interconnects below the vias. Vias are typically formed by a lithographic process. Representatively, a photoresist layer may be spin coated over a dielectric layer, the photoresist layer may be exposed to patterned actinic radiation through a patterned mask, and then the exposed layer may be developed in order to form an opening in the photoresist layer. Next, an opening for the via may be etched in the dielectric layer by using the opening in the photoresist layer as an etch mask. This opening is referred to as a via opening. Finally, the via opening may be filled with one or more metals or other conductive materials to form the via.

In the past, the sizes and the spacing of vias has progressively decreased, and it is expected that in the future the sizes and the spacing of the vias will continue to progressively decrease, for at least some types of integrated circuits (e.g., advanced microprocessors, chipset components, graphics chips, etc.). One measure of the size of the vias is the critical dimension of the via opening. One measure of the spacing of the vias is the via pitch. Via pitch represents the center-to-center distance between the closest adjacent vias. When patterning extremely small vias with extremely small pitches by such lithographic processes, several challenges present themselves, especially when the pitches are around 70 nanometers (nm) or less and/or when the critical dimensions of the via openings are around 35nm or less. One such challenge is that the overlay between the vias and the overlying interconnects, and the overlay between the vias and the underlying landing interconnects, generally need to be controlled to high tolerances on the order of a quarter of the via pitch. As via pitches scale ever smaller over time, the overlay tolerances tend to scale with them at an even greater rate than lithographic equipment is able to keep up.

Another such challenge is that the critical dimensions of the via openings generally tend to scale faster than the resolution capabilities of the lithographic scanners. Shrink technologies exist to shrink the critical dimensions of the via openings. However, the shrink amount tends to be limited by the minimum via pitch, as well as by the ability of the shrink process to be

sufficiently optical proximity correction (OPC) neutral, and to not significantly compromise line width roughness (LWR) and/or critical dimension uniformity (CDU).

Yet another such challenge is that the LWR and/or CDU characteristics of photoresists generally need to improve as the critical dimensions of features of an integrated circuit decrease in order to maintain the same overall fraction of the critical dimension budget. However, currently the LWR and/or CDU characteristics of most photoresists are not improving as rapidly as the critical dimensions of the via openings are decreasing.

Thus, improvements are needed in the area of resist technologies, e.g., for EUV and Ebeam based lithographic processing.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B illustrate chemical schematic representations of polystannane molecules having C=C bonds and Sn-H bonds, in accordance with an embodiment of the present invention.

Figure 2 illustrates a chemical schematic representation of a tin catenane molecule, in accordance with an embodiment of the present invention.

Figure 3 illustrates a chemical schematic representation of a molecular glass molecule, in accordance with an embodiment of the present invention.

Figure 4A is a cross-sectional schematic representation of an EUV lithographic process, in accordance with an embodiment of the present invention.

Figure 4B is a cross-sectional schematic representation of an ebeam column of an electron beam lithography apparatus and an associated sample, in accordance with an embodiment of the present invention.

Figure 5A illustrates a cross-sectional view of a starting structure following deposition, but prior to patterning, of a hardmask material layer formed on an interlayer dielectric (ILD) layer.

Figure 5B illustrates a cross-sectional view of the structure of Figure 1A following patterning of the hardmask layer by pitch halving.

Figure 6 illustrates cross-sectional views in a spacer-based-sextuple-patterning (SBSP) processing scheme which involves pitch division by a factor of six.

5 Figure 7 illustrates cross-sectional views in a spacer-based-nonuple-patterning (SBNP) processing scheme which involves pitch division by a factor of nine.

Figure 8 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present invention.

10 Figure 9A illustrates a cross-sectional view of a non-planar semiconductor device having fins, in accordance with an embodiment of the present invention.

Figure 9B illustrates a plan view taken along the a-a' axis of the semiconductor device of Figure 9A, in accordance with an embodiment of the present invention.

Figure 10 illustrates a computing device in accordance with one implementation of the invention.

15 Figure 11 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

Figure 12 is an interposer implementing one or more embodiments of the invention.

DESCRIPTION OF THE EMBODIMENTS

20 Polysilane-, polygermane-, and polystannane-based resists for extreme ultraviolet (EUV) or electron beam (Ebeam) lithography are described. In the following description, numerous specific details are set forth, such as specific material and tooling regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these
25 specific details. In other instances, well-known features, such as single or dual damascene processing, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the

Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, “below”, “bottom,” and “top” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

One or more embodiments described herein are directed to extreme ultraviolet (EUV) or electron beam (Ebeam) lithography using polymers based on polysilane, polygermane or polystannane materials containing chemically sensitive substituents. Such resist materials may be described as inorganic resists having high absorption.

In accordance with one or more embodiments of the present invention, polysilane, polygermane and polystannane resist materials are described as designed for use in EUV or Ebeam lithography. Such resist materials may be based on silicon (Si), germanium (Ge) or tin (Sn), with the latter two elements in particular having higher EUV absorbance than typical organic photoresists composed of C, H, O, and N. Such resist materials may be designed to possess (a) multiple radiation-sensitive Si-Si, Ge-Ge, or Sn-Sn bonds which are susceptible to ionization and electron-based chemistry and b) cross-linking functionality. In an embodiment, such resist materials provide potentially weak bonds for generating radical cations. In a specific embodiment, resists described herein are based on element to element bonds, e.g., Ge-Ge, which are much more absorbing for EUV. As such, implementation of resist materials described herein

may provide advantages such as lower power and lower dose requirements and, thus, possibly lower defects based on resulting reduction in stochastic error.

To provide context, in order for EUV lithography to be economically viable, resist materials may be needed which have ability for high resolution imaging at relatively low doses (e.g., less than $20\text{mJ}/\text{cm}^2$). In order for EUV lithography to be technologically viable, billions and billions of features need to be printed without defects. At the dimensions being printed (e.g., less than 20nm), however, resist uniformity in a given volume may need to be nearly mono-disperse to prevent stochastic patterning differences.

In accordance with an embodiment of the present invention, a new class of resist materials is described which have higher EUV absorbance (e.g., 2-5x) as compared with conventional resist materials. In one such embodiment, resist materials are described that are based on one component, e.g., a polygermane or polystannane, which contains both functionality designed to absorb and interact with EUV photons and high energy electrons, and functionality designed to react with the resulting chemical functionality and secondary electrons via catalytic reactions.

In accordance with more specific embodiments, polysilanes, polygermanes and/or polystannanes having polymer chain with repeating $-\text{SiR}_2-$, $-\text{GeR}_2-$ and $-\text{SnR}_2-$ units, respectively, are prepared from any of a number of methods including, but not limited to, dehydrocoupling from R_2SiH_2 , R_2GeH_2 or R_2SnH_2 , respectively, or dehalocoupling from R_2SiCl_2 , R_2GeCl_2 or R_2SnCl_2 , respectively. In one embodiment, copolymers are fabricated from a reaction of two or more of R_2SiX_2 , R_2GeX_2 or R_2SnX_2 species, allowing different functionality to be introduced in the polymers in defined amounts. In one embodiment, R represents an organic group such as al alkyl or aryl group.

In accordance with one or more embodiments described herein, resist materials have one or more of the following attributes: (1) multiple E-E bonds (e.g., $\text{E} = \text{Ge}$ or Sn) which are highly EUV absorbing and thermally stable but susceptible to ionization reactions and heterolytic and homolytic E-E bond cleavage reactions, (2) sidechain functionality designed to react with the Ge

or Sn based products of high energy ionization chemistry and/or (3) sidechain functionality designed to react with the products of the reaction of the first sidechain functionality either stoichiometrically or catalytically. In one embodiment, the net effect of such reaction cascades is a structural change in the polymeric material. Different types of structural changes can be elicited based on the sidechain groups chosen including cases where a polymer is cleaved from high molecular weight (MW) to low MW units leading to enhanced solubility (e.g., positive tone imaging) or where polymers are cross-linked to each other leading to very high (MW) insoluble matrix (e.g., negative tone imaging).

In a first aspect, a resist material is based on an inorganic backbone. For example, Figures 1A and 1B illustrate chemical schematic representations of polystannane molecules having C=C bonds and Sn-H bonds, in accordance with an embodiment of the present invention.

Referring to Figure 1A, in an embodiment, a copolymer of $\text{Ph}(\text{vinyl})\text{SnX}_2$ and $\text{Ph}(\text{H})\text{SnX}_2$ ($\text{X} = \text{H}, \text{Cl}, \text{Br}$) is used to form a polymer 100A. C=C double bonds are included in polymer 100A as radical traps which can react with Sn based radicals formed during initial ionization events. In one embodiment, the resulting alkyl radical which is ultimately formed can react with an additional C=C bond leading to a new alkyl radical. In another embodiment, the resulting alkyl radical which is ultimately formed can abstract H from an unreacted Sn-H site leading to another Sn-based radical which can initiate a new radical cascade by reacting with a C=C bond. In a specific embodiment, the combination of two radicals (e.g., two Sn radicals, two alkyl radicals or a Sn and alkyl radical) will stop the radical cascade. The extent of radical chemistry occurring may be dependent on several factors including the amount of reactive groups introduced, packing within the film and stabilities of the radicals. It is to be appreciated that other chain termination events can occur in the film through volatilization of small molecular weight (MW) radicals from the film. In a second example, referring to Figure 1B, a reactive Sn-H bond is also introduced as sidechain on the polymer of Figure 1A, providing an alternative source for cross-linking.

In accordance with an embodiment of the present invention, as depicted in Figures 1A and 1B, polystannanes are shown as a specific example. In another embodiment, the same general features apply to the synthesis and use of polygermane materials as well. And, in another embodiment, although not as highly absorbing, the above design approach is also suitable for polysilane resists which offer advantages in terms of costs of starting materials and lower toxicity.

In a second aspect, single discrete inorganic molecules are used as a resist material, as opposed to polymers. In a first example of the second aspect, Figure 2 illustrate a chemical schematic representation of a tin catenane molecule, in accordance with an embodiment of the present invention.

Referring to Figure 2, molecule 200 has a center ring 202, with E = Sn in the specific example illustrated. Cyclic polystannane, polygermane, or polysilane can be synthesized using similar chemistry to polymers but where cyclization (e.g., bite-back) occurs leading to chain termination. In the specific example shown, in one embodiment, $\text{allylSnH(X}_2\text{)}$ is cyclized to provide isomeric mixture of 6-membered rings of E atoms (E = Sn shown). In one embodiment, ionization chemistry ultimately leads to ring-opening and reaction with other cyclic or ring-opened molecules.

Referring more generically to Figure 2, in an embodiment, a discrete molecule for a resist formulation includes a closed central inorganic ring having only E-E bonds, where E is Si, Ge or Sn, or a combination thereof (other embodiments may include E = Te or E = Bi). Organic ligands are covalently bonded to the E atoms of the closed central inorganic ring. In one embodiment, the closed central inorganic ring is a homogeneous ring (all same E). In a specific such embodiment, the closed central inorganic ring includes only Sn or Ge, a former example being provided by molecule 200. In another embodiment, however, the closed central inorganic ring is a heterogeneous ring (more than one type of E in a same ring, i.e., a mixture of two or more of Si, Ge or Sn). In an embodiment, the discrete molecule is absorbing for extreme

ultraviolet (EUV) irradiation. In an embodiment, the discrete molecule is reactive to electron beam (Ebeam) irradiation.

In a second example of the second aspect, Figure 3 illustrates a chemical schematic representation of a molecular glass molecule, in accordance with an embodiment of the present invention.

Referring to Figure 3, molecule 300 has a center element E 302 and radiating E elements, with E = Sn in the specific example illustrated. In this example, in one embodiment, small MW polystannane molecules are synthesized through reaction of SnCl₄ and Sn-Li or other similar reagents. The resulting small molecules are analogous to organic molecular glass materials used as EUV resists; however molecules of the type 300 contain high absorption Sn (or Ge or Si) cores with reactive functionality distributed on periphery. It is to be appreciated that T_g or glass transition temperature of the resulting films may be a function of MW and nature of substituents used.

Referring more generically to Figure 3, in an embodiment, a discrete molecule for a resist formulation includes a central inorganic element E. Radiating E elements are bonded to the central element E to provide E-E bonds, where E is Si, Ge or Sn, or a combination thereof (other embodiments may include E = Te or E = Bi). Organic ligands are covalently bonded to the radiating E elements. In one embodiment, the E-E bonds are all homogeneous bonds (all same E). In a specific such embodiment, the E-E bonds are all only Sn-Sn bonds or Ge-Ge bonds, a former example being provided by molecule 300. In another embodiment, however, at least some of the E-E bonds are heterogeneous bonds (more than one type of E in a same discrete molecule, i.e., a mixture of two or more of Si, Ge or Sn as central and/or radiating elements). In an embodiment, the discrete molecule is absorbing for extreme ultraviolet (EUV) irradiation. In an embodiment, the discrete molecule is reactive to electron beam (Ebeam) irradiation.

In accordance with an embodiment of the present invention, in all of the above cases, the functionality responsible for patterning response are delivered in single component, either as a polymer or as a single molecule. In one such embodiment, this approach leads to greater

uniformity relative to multi-component resists including polymers/photoacid generators (PAGs)/quenchers etc., and, thus, addresses resist stochastic issues which are more and more important as smaller features are printed. In an embodiment, due to the similarity of Si, Ge, Sn elements and similarity of synthetic chemistry, homogeneous systems based on a single element or mixed systems containing two or three elements can be synthesized. In one embodiment, resist materials described herein have higher absorbance based on, e.g., high EUV absorbance of Sn and Ge.

In an embodiment, the exemplary resist materials described in association with Figures 1A, 1B, 2 and 3, are combined with a solvent in order to deliver the resist material onto a substrate or wafer. In one such embodiment, the solvent is one such as, but not limited to, propylene glycol monoethyl acetate (PGMEA), 2-heptanone, cyclohexanone, methyl isobutyl ketone, toluene, ethyl lactate, or mesitylene. In an embodiment, a resist composition including a resist material in a solvent is applied to a wafer or substrate by a spin-on process. The solvent may then be evaporated following the spin-on process. Bake operations may be performed prior to and/or subsequent to exposure of the resist composition to a lithographic process.

In an embodiment, the above described resist material or resist composition is subjected to a lithographic process as part of a patterning process. In one such embodiment, the resist material or resist composition is exposed to extreme ultraviolet (EUV) or e-beam radiation. In a specific embodiment, the resist material or resist composition is substantially absorbing at a wavelength of approximately 13.5 nanometers. In an embodiment, the resist material or resist composition is substantially absorbing at an energy approximately in the range of 5-150 keV.

In an embodiment, referring generally to Figures 1A, 1B, 2 and 3, a resist composition for EUV or Ebeam lithography includes a solvent and a resist material selected from the group consisting of a polysilane material, a polygermane material, or a polystannane material. The resist material suspended or dissolved in the solvent. In one embodiment, the resist material includes polystannane molecules having C=C bonds and Sn-H bonds, such as described in association with Figures 1A and 1B. In one embodiment, the resist material includes

polygermane molecules having C=C bonds and Ge-H bonds, such as is also described in association with Figures 1A and 1B.

In another embodiment, the resist material includes discrete molecules, each of the discrete molecules having a closed central inorganic ring including only E-E bonds, where E is Si, Ge or Sn, or a combination thereof, and organic ligands covalently bonded to the E atoms of the closed central inorganic ring, such as described in association with Figure 2. In another embodiment, the resist material includes discrete molecules, each of the discrete molecules having a central inorganic element E, radiating E elements bonded to the central element E to provide E-E bonds, where E is Si, Ge or Sn, or a combination thereof and organic ligands covalently bonded to the radiating E elements, such as described in association with Figure 3.

In an embodiment, the solvent is selected from the group consisting of propylene glycol monoethyl acetate (PGMEA), 2-heptanone, cyclohexanone, methyl isobutyl ketone, toluene, ethyl lactate, and mesitylene. In one embodiment, the resist composition is a positive tone resist composition. In one embodiment, the resist composition is a negative tone resist composition.

In an embodiment, subsequent to exposure, a development operation is performed. In any of the above described cases, in an embodiment, developing the exposed resist material or resist composition includes, in the case of positive tone development, immersion or coating with standard aqueous TMAH developer (e.g., in a concentration range from 0.1M – 1M) or other aqueous or alcoholic developer based on tetraalkylammonium hydroxides for 30-120 seconds followed by rinse with deionized (DI) water. In another embodiment, in the case of negative tone development, developing the resist material or resist composition includes immersion or coating with organic solvents such as cyclohexanone, 2-heptanone, propylene glycol methylethyl acetate or others followed by rinse with another organic solvent such as hexane, heptane, cyclohexane, or the like.

In an embodiment, a polysilane-, polygermane-, or polystannane-based resist may be used in a fabrication scheme involving photobuckets. The term “photobucket” as used herein may involve use of an ultrafast resist or ebeam resist, such as a polysilane-, polygermane-, or

polystannane-based resist described above, formed in etched openings. In one embodiment, lithography is used to expose the corresponding photobuckets that are selected for removal.

However, the lithographic constraints may be relaxed and misalignment tolerance may be high since the photobuckets are surrounded by non-photolyzable materials. Furthermore, in an

5 embodiment, instead of exposing at, e.g. 30mJ/cm², such photobuckets might be exposed at, e.g., 3mJ/cm². Normally this would result in very poor critical dimension (CD) control and roughness. But in this case, the CD and roughness control will be defined by the photobuckets, which can be very well controlled and defined. Thus, the photobucket approach may be used to circumvent imaging/dose tradeoff which limits the throughput of next generation lithographic
10 processes. In one embodiment, the photobuckets are subject to exposure of extreme ultraviolet (EUV) light or Ebeam irradiation in order to expose the photobuckets.

In an embodiment, extreme ultraviolet (EUV) light is used for lithographic exposure of the above described resists or resist compositions. In one embodiment, extreme ultraviolet radiation (EUV or XUV) or high-energy ultraviolet radiation refers to electromagnetic radiation

15 in the part of the electromagnetic spectrum spanning wavelengths from 124 nm down to 10 nm, and therefore (by the Planck–Einstein equation) having photons with energies from 10 eV up to 124 eV (corresponding to 124 nm to 10 nm respectively). EUV may be naturally generated by

the solar corona and artificially by plasma and synchrotron light sources. Extreme ultraviolet lithography (also known as EUV or EUVL) is a lithography technology using an extreme

20 ultraviolet (EUV) wavelength, e.g., 13.5 nm. It is to be appreciated that, as is the case for Ebeam lithography described below, EUV lithography may be used as a complementary lithographic process used to “cut” lines fabricated by another optical lithography approach. Alternatively, EUV may be used as the primary or “direct” approach.

Figure 4A is a cross-sectional schematic representation of an EUV lithographic process,
25 in accordance with an embodiment of the present invention.

Referring to Figure 4A, a system 400A is provided for image formation using EUV lithography. System 400A includes an EUV multilayer 402A and absorber 404A which is a

mask pattern for imaging a line. EUV radiation 406A is reflected from the mask pattern and is absorbed in a resist material 408A (such as a polysilane-, polygermane-, and polystannane-based resist material) and substrate 410A, producing photoelectrons and secondary electrons 412A.

These electrons increase the extent of chemical reactions in the resist material 408A. A

5 secondary electron pattern that is random in nature may be superimposed on the optical image, as is illustrated in Figure 4A.

In another aspect, direct ebeam lithography may be used to pattern polysilane-, polygermane-, and polystannane-based resists such as described herein. In yet another aspect, ebeam lithography is used as part of a broader complementary lithography approach.

10 Complementary lithography draws on the strengths of two lithography technologies, working hand-in-hand, to lower the cost of patterning critical layers in logic devices at 20nm half-pitch and below, in high-volume manufacturing (HVM). The most cost-effective way to implement complementary lithography is to combine optical lithography with e-beam lithography (EBL). The process of transferring integrated circuit (IC) designs to the wafer entails the following:

15 optical lithography to print unidirectional lines (either strictly unidirectional or predominantly unidirectional) in a pre-defined pitch, pitch division techniques to increase line density, and EBL to “cut” the lines. EBL is also used to pattern other critical layers, notably contact and via holes. Optical lithography can be used alone to pattern other layers. When used to complement optical lithography, EBL is referred to as CEBL, or complementary EBL. CEBL is directed to cutting

20 lines and holes. By not attempting to pattern all layers, CEBL plays a complementary but crucial role in meeting the industry’s patterning needs at advanced (smaller) technology nodes (e.g., 10nm or smaller such as 7nm or 5nm technology nodes). CEBL also extends the use of current optical lithography technology, tools and infrastructure. Alternatively, Ebeam lithography (EBL) may be used as the primary or “direct” approach.

25 An electron beam lithography tool may be used to perform such ebeam lithography. In an exemplary embodiment, Figure 4B is a cross-sectional schematic representation of an ebeam

column of an electron beam lithography apparatus and an associated sample, in accordance with an embodiment of the present invention.

Referring to Figure 4B, an ebeam column 400 includes an electron source 402 for providing a beam of electrons 404. The beam of electrons 404 is passed through a limiting aperture 406 and, subsequently, through high aspect ratio illumination optics 408. The outgoing beam 410 is then passed through a slit 412 and may be controlled by a slim lens 414, e.g., which may be magnetic. Ultimately, the beam 404 is passed through a shaping aperture 416 (which may be a one-dimensional (1-D) shaping aperture) and then through a blanker aperture array (BAA) 418. The BAA 418 includes a plurality of physical apertures therein, such as openings formed in a thin slice of silicon. It may be the case that only a portion of the BAA 418 is exposed to the ebeam at a given time. Alternatively, or in conjunction, only a portion 420 of the ebeam 404 that passes through the BAA 418 is allowed to pass through a final aperture 422 (e.g., beam portion 421 is shown as blocked) and, possibly, a stage feedback deflector 424.

Referring again to Figure 4B, the resulting ebeam 426 ultimately impinges as a spot 428 on a surface of a wafer 430, such as a silicon wafer used in IC manufacture. Specifically, the resulting ebeam may impinge on a photo-resist layer on the wafer, but embodiments are not so limited. A stage scan 432 moves the wafer 430 relative to the beam 426 along the direction of the arrow 434 shown in Figure 4B. It is to be appreciated that an ebeam tool in its entirety may include numerous columns 400 of the type depicted in Figure 4B. Also, as described in some embodiments below, the ebeam tool may have an associated base computer, and each column may further have a corresponding column computer. In accordance with an embodiment of the present invention, wafer 430 has layer of polysilane-, polygermane-, or polystannane-based resist thereon.

It is also to be appreciated that, in some embodiments, an ebeam column as described above may also include other features in addition to those described in association with Figure 4B. For example, in an embodiment, the sample stage can be rotated by 90 degrees to accommodate alternating metallization layers which may be printed orthogonally to one another

(e.g., rotated between X and Y scanning directions). In another embodiment, an e-beam tool is capable of rotating a wafer by 90 degrees prior to loading the wafer on the stage.

In another aspect, as alluded to above in discussions of complementary lithographic approaches, lithographic processing described herein may be implemented to complement a first performed pitch division technique (which may be initiated with optical lithography) used to increase a line density prior to using EUV lithography or Ebeam lithography to “cut” such lines. In a first example, pitch halving can be implemented to double the line density of a fabricated grating structure. Figure 5A illustrates a cross-sectional view of a starting structure following deposition, but prior to patterning, of a hardmask material layer formed on an interlayer dielectric (ILD) layer. Figure 5B illustrates a cross-sectional view of the structure of Figure 5A following patterning of the hardmask layer by pitch halving.

Referring to Figure 5A, a starting structure 500 has a hardmask material layer 504 formed on an interlayer dielectric (ILD) layer 502. A patterned mask 506 is disposed above the hardmask material layer 504. The patterned mask 506 has spacers 508 formed along sidewalls of features (lines) thereof, on the hardmask material layer 504.

Referring to Figure 5B, the hardmask material layer 504 is patterned in a pitch halving approach. Specifically, the patterned mask 506 is first removed. The resulting pattern of the spacers 508 has double the density, or half the pitch or the features of the mask 506. The pattern of the spacers 508 is transferred, e.g., by an etch process, to the hardmask material layer 504 to form a patterned hardmask 510, as is depicted in Figure 5B. In one such embodiment, the patterned hardmask 510 is formed with a grating pattern having unidirectional lines. The grating pattern of the patterned hardmask 510 may be a tight pitch grating structure. For example, the tight pitch may not be achievable directly through conventional lithography techniques. Even further, although not shown, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like pattern of the patterned hardmask 510 of Figure 5B may have hardmask lines spaced at a constant pitch and having a constant width relative to

one another. The dimensions achieved may be far smaller than the critical dimension of the lithographic technique employed.

Accordingly, as a first portion of a complementary EUV or Ebeam integration scheme, a blanket film may be patterned using optical lithography and etch processing which may involve, e.g., spacer-based-double-patterning (SBDP) or pitch halving, or spacer-based-quadruple-patterning (SBQP) or pitch quartering. It is to be appreciated that other pitch division approaches may also be implemented.

For example, Figure 6 illustrates cross-sectional views in a spacer-based-sextuple-patterning (SBSP) processing scheme which involves pitch division by a factor of six. Referring to Figure 6, at operation (a), a sacrificial pattern X is shown following litho, slim and etch processing. At operation (b), spacers A and B are shown following deposition and etching. At operation (c), the pattern of operation (b) is shown following spacer A removal. At operation (d), the pattern of operation (c) is shown following spacer C deposition. At operation (e), the pattern of operation (d) is shown following spacer C etch. At operation (f), a pitch/6 pattern is achieved following sacrificial pattern X removal and spacer B removal.

In another example, Figure 7 illustrates cross-sectional views in a spacer-based-nonuple-patterning (SBNP) processing scheme which involves pitch division by a factor of nine.

Referring to Figure 7, at operation (a), a sacrificial pattern X is shown following litho, slim and etch processing. At operation (b), spacers A and B are shown following deposition and etching. At operation (c), the pattern of operation (b) is shown following spacer A removal. At operation (d), the pattern of operation (c) is shown following spacer C and D deposition and etch. At operation (e), a pitch/9 pattern is achieved following spacer C removal.

In any case, in an embodiment, complementary lithography as described herein involves first fabricating a gridded layout by conventional or state-of the-art lithography, such as 193nm immersion lithography (193i). Pitch division may be implemented to increase the density of lines in the gridded layout by a factor of n. Gridded layout formation with 193i lithography plus pitch division by a factor of n can be designated as 193i + P/n Pitch Division. Patterning of the

pitch divided gridded layout may then be patterned using EUV or electron beam direct write (EBDW) “cuts,” which may involve use of a polysilane-, polygermane-, or polystannane-based resist. In one such embodiment, 193nm immersion scaling can be extended for many generations with cost effective pitch division. Complementary EUV lithography or EBL is used to break gratings continuity and to pattern, e.g., vias, line ends (plugs) or gate ends.

More specifically, embodiments described herein are directed to patterning features during the fabrication of an integrated circuit. In one embodiment, direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist is used to pattern openings for forming vias. Vias are metal structures used to electrically connect metal lines above the vias to metal lines below the vias. In another embodiment, direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist is used to form non-conductive spaces or interruptions along the metal lines. Conventionally, such interruptions have been referred to as “cuts” since the process involved removal or cutting away of portions of the metal lines. However, in a damascene approach, the interruptions may be referred to as “plugs” which are regions along a metal line trajectory that are actually not metal at any stage of the fabrication scheme, but are rather preserved regions where metal cannot be formed. In either case, however, use of the terms cuts or plugs may be done so interchangeably. Via opening and metal line cut or plug formation is commonly referred to as back end of line (BEOL) processing for an integrated circuit. In another embodiment, direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist is used for front end of line (FEOL) processing. For example, the scaling of active region dimensions (such as fin dimensions) and/or associated gate structures can be performed using direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist as described herein.

More generally, referring to all of the above aspects of embodiments of the present invention, it is to be appreciated that a metallization layer having lines with line cuts (or plugs) and having associated vias may be fabricated above a substrate and, in one embodiment, may be

fabricated above a previous metallization layer. As an example, Figure 8 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present invention. Referring to Figure 8, a starting structure 800 includes a pattern of metal lines 802 and interlayer dielectric (ILD) lines 804. The starting
5 structure 800 may be patterned in a grating-like pattern with metal lines spaced at a constant pitch and having a constant width, as is depicted in Figure 8. Although not shown, the lines 802 may have interruptions (i.e., cuts or plugs) at various locations along the lines. The pattern, for example, may be fabricated by a pitch halving or pitch quartering approach, as described above. Some of the lines may be associated with underlying vias, such as line 802' shown as an example
10 in the cross-sectional view.

In an embodiment, fabrication of a metallization layer on the previous metallization structure of Figure 8 begins with formation of an interlayer dielectric (ILD) material above the structure 800. A hardmask material layer may then be formed on the ILD layer. The hardmask material layer may be patterned to form a grating of unidirectional lines orthogonal to the lines
15 802 of 800. In one embodiment, the grating of unidirectional hardmask lines is fabricated using conventional lithography (e.g., photoresist and other associated layers) and may have a line density defined by a pitch-halving, pitch-quartering etc. approach as described above. The grating of hardmask lines leaves exposed a grating region of the underlying ILD layer. It is these exposed portions of the ILD layer that are ultimately patterned for metal line formation, via
20 formation, and plug formation. For example, in an embodiment, via locations are patterned in regions of the exposed ILD using direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist, as described above. The patterning may involve formation of a resist layer and patterning of the resist layer by EUV or Ebeam lithography to provide via opening locations which may be etched into the ILD
25 regions. The lines of overlying hardmask can be used to confine the vias to only regions of the exposed ILD, with overlap accommodated by the hardmask lines which can effectively be used as an etch stop. Plug (or cut) locations may also be patterned in exposed regions of the ILD, as

confined by the overlying hardmask lines, in a separate EUV or Ebeam lithography processing operation. The fabrication of cuts or plugs effectively preserve regions of ILD that will ultimately interrupt metal lines fabricated therein. Metal lines may then be fabricated using a damascene approach, where exposed portions of the ILD (those portions between the hardmask lines and not protected by a plug preservation layer, such as a resist layer patterned during “cutting”) are partially recessed. The recessing may further extend the via locations to open metal lines from the underlying metallization structure. The partially recessed ILD regions are then filled with metal (a process which may also involve filling the via locations), e.g., by plating and CMP processing, to provide metal lines between the overlying hardmask lines. The hardmask lines may ultimately be removed for completion of a metallization structure. It is to be appreciated that the above ordering of line cuts, via formation, and ultimate line formation is provided only as an example. A variety of processing schemes may be accommodated using EUV or Ebeam lithography cuts and vias, as described herein.

In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

In an embodiment, as is also used throughout the present description, interconnect material is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

In an embodiment, as is also used throughout the present description, hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In some embodiments, a hardmask layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other materials, such as oxygen, may be included in one or more of these layers. Alternatively, other hardmask layers known in the arts may be used depending upon the particular implementation. The hardmask layers maybe formed by CVD, PVD, or by other deposition methods.

It is to be appreciated that the layers and materials described in association with Figure 8 are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the structure depicted in Figure 8 may be fabricated on underlying lower level interconnect layers.

In another embodiment, direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist may be used to fabricate semiconductor devices, such as PMOS or NMOS devices of an integrated circuit. In one such embodiment, EUV or Ebeam lithography “cuts” are used to pattern a grating of active regions that are ultimately used to form fin-based or trigate structures. In another such embodiment, such

cuts are used to pattern a gate layer, such as a polycrystalline silicon layer, ultimately used for gate electrode fabrication. As an example of a completed device, Figures 9A and 9B illustrate a cross-sectional view and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device having a plurality of fins, in accordance with an embodiment of the present invention.

Referring to Figure 9A, a semiconductor structure or device 900 includes a non-planar active region (e.g., a fin structure including protruding fin portion 904 and sub-fin region 905) formed from substrate 902, and within isolation region 906. A gate line 908 is disposed over the protruding portions 904 of the non-planar active region as well as over a portion of the isolation region 906. As shown, gate line 908 includes a gate electrode 950 and a gate dielectric layer 952. In one embodiment, gate line 908 may also include a dielectric cap layer 954. A gate contact 914, and overlying gate contact via 916 are also seen from this perspective, along with an overlying metal interconnect 960, all of which are disposed in inter-layer dielectric stacks or layers 970. Also seen from the perspective of Figure 9A, the gate contact 914 is, in one embodiment, disposed over isolation region 906, but not over the non-planar active regions.

Referring to Figure 9B, the gate line 908 is shown as disposed over the protruding fin portions 904. Source and drain regions 904A and 904B of the protruding fin portions 904 can be seen from this perspective. In one embodiment, the source and drain regions 904A and 904B are doped portions of original material of the protruding fin portions 904. In another embodiment, the material of the protruding fin portions 904 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 904A and 904B may extend below the height of dielectric layer 906, i.e., into the sub-fin region 905.

In an embodiment, the semiconductor structure or device 900 is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one

such embodiment, the gate electrode stacks of gate lines 908 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

Figure 10 illustrates a computing device 1000 in accordance with one implementation of the invention. The computing device 1000 houses a board 1002. The board 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006. The processor 1004 is physically and electrically coupled to the board 1002. In some implementations the at least one communication chip 1006 is also physically and electrically coupled to the board 1002. In further implementations, the communication chip 1006 is part of the processor 1004.

Depending on its applications, computing device 1000 may include other components that may or may not be physically and electrically coupled to the board 1002. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some implementations of the invention, the integrated circuit die of the processor includes one or more structures fabricated using direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist, in accordance with implementations of embodiments of the invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also includes an integrated circuit die packaged within the communication chip 1006. In accordance with another implementation of embodiments of the invention, the integrated circuit die of the communication chip includes one or more structures fabricated using direct or complementary EUV lithography or EBL in conjunction with a

polysilane-, polygermane- or polystannane-based resist, in accordance with implementations of embodiments of the invention.

In further implementations, another component housed within the computing device 1000 may contain an integrated circuit die that includes one or more structures fabricated using direct or complementary EUV lithography or EBL in conjunction with a polysilane-, polygermane- or polystannane-based resist, in accordance with implementations of embodiments of the invention.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1000 may be any other electronic device that processes data.

Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present invention. In one embodiment, the computer system is coupled with an EUV system or ebeam tool such as described in association with Figures 4A and 4B, respectively. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

Figure 11 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 1100 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein (such as end-point detection), may be

executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

The exemplary computer system 1100 includes a processor 1102, a main memory 1104 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 1106 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 1118 (e.g., a data storage device), which communicate with each other via a bus 1130.

Processor 1102 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 1102 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 1102 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 1102 is configured to execute the processing logic 1126 for performing the operations described herein.

The computer system 1100 may further include a network interface device 1108. The computer system 1100 also may include a video display unit 1110 (e.g., a liquid crystal display

(LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 1112 (e.g., a keyboard), a cursor control device 1114 (e.g., a mouse), and a signal generation device 1116 (e.g., a speaker).

The secondary memory 1118 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 1132 on which is stored one or more sets of instructions (e.g., software 1122) embodying any one or more of the methodologies or functions described herein. The software 1122 may also reside, completely or at least partially, within the main memory 1104 and/or within the processor 1102 during execution thereof by the computer system 1100, the main memory 1104 and the processor 1102 also constituting machine-readable storage media. The software 1122 may further be transmitted or received over a network 1120 via the network interface device 1108.

While the machine-accessible storage medium 1132 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term “machine-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

Implementations of embodiments of the invention may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group

III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the invention, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may refer only to planar transistors, it should be noted that the invention may also be carried out using nonplanar transistors.

Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode

layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g.,

5 ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide.

10 An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another

15 implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the invention, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of
20 one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In some implementations of the invention, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art
25 and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

Figure 12 illustrates an interposer 1200 that includes one or more embodiments of the invention. The interposer 1200 is an intervening substrate used to bridge a first substrate 1202 to a second substrate 1204. The first substrate 1202 may be, for instance, an integrated circuit die. The second substrate 1204 may be, for instance, a memory module, a computer motherboard, or

another integrated circuit die. Generally, the purpose of an interposer 1200 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1200 may couple an integrated circuit die to a ball grid array (BGA) 1206 that can subsequently be coupled to the second substrate 1204. In some embodiments, the first and second substrates 1202/1204 are attached to opposing sides of the interposer 1200. In other embodiments, the first and second substrates 1202/1204 are attached to the same side of the interposer 1200. And in further embodiments, three or more substrates are interconnected by way of the interposer 1200.

The interposer 1200 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 1208 and vias 1210, including but not limited to through-silicon vias (TSVs) 1212. The interposer 1200 may further include embedded devices 1214, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1200. In accordance with embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 1200.

The above description of illustrated implementations of embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

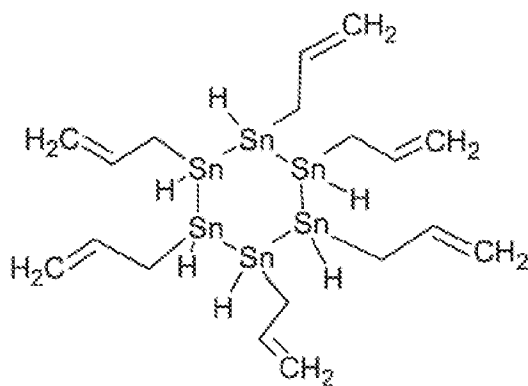
These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

In an example, a discrete molecule for a resist formulation includes a closed central inorganic ring having only E-E bonds, where E is Si, Ge or Sn, or a combination thereof. Organic ligands are covalently bonded to the E atoms of the closed central inorganic ring.

In one example, the closed central inorganic ring is a homogeneous ring.

In one example, the closed central inorganic ring includes only Sn or Ge.

In one example, the chemical formula of the discrete molecule is represented by:



In one example, the closed central inorganic ring is a heterogeneous ring.

In one example, the discrete molecule is absorbing for extreme ultraviolet (EUV) irradiation.

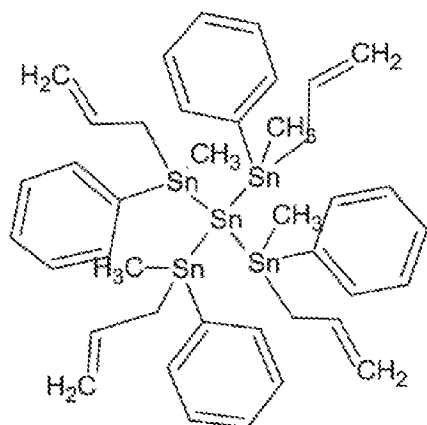
In one example, the discrete molecule is reactive to electron beam (Ebeam) irradiation.

In an example, a discrete molecule for a resist formulation includes a central inorganic element E. Radiating E elements are bonded to the central element E to provide E-E bonds, where E is Si, Ge or Sn, or a combination thereof. Organic ligands are covalently bonded to the radiating E elements.

In one example, the E-E bonds are all homogeneous bonds.

In one example, the E-E bonds are all only Sn-Sn bonds or Ge-Ge bonds.

In one example, the chemical formula of the discrete molecule is represented by:



In one example, at least some of the E-E bonds are heterogeneous bonds.

- 5 In one example, the discrete molecule is absorbing for extreme ultraviolet (EUV) irradiation.

In one example, the discrete molecule is reactive to electron beam (Ebeam) irradiation.

- In an example, a resist composition for EUV or Ebeam lithography includes a solvent and a resist material selected from the group consisting of a polysilane material, a polygermane
10 material, or a polystannane material, the resist material suspended or dissolved in the solvent.

In one example, the resist material includes polystannane molecules having C=C bonds and Sn-H bonds.

In one example, the resist material includes polygermane molecules having C=C bonds and Ge-H bonds.

- 15 In one example, the resist material includes discrete molecules, each of the discrete molecules having a closed central inorganic ring including only E-E bonds, where E is Si, Ge or Sn, or a combination thereof, and organic ligands covalently bonded to the E atoms of the closed central inorganic ring.

- In one example, the resist material includes discrete molecules, each of the discrete
20 molecules having a central inorganic element E, radiating E elements bonded to the central

element E to provide E-E bonds, where E is Si, Ge or Sn, or a combination thereof and organic ligands covalently bonded to the radiating E elements.

In one example, the solvent is selected from the group consisting of propylene glycol monoethyl acetate (PGMEA), 2-heptanone, cyclohexanone, methyl isobutyl ketone, toluene,
5 ethyl lactate, and mesitylene.

In one example, the resist composition is a positive tone resist composition.

In one example, the resist composition is a negative tone resist composition.

CLAIMS

What is claimed is:

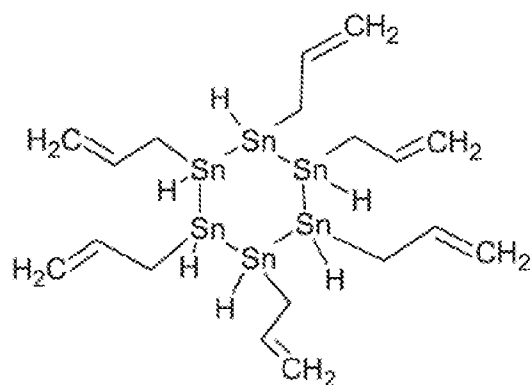
1. A discrete molecule for a resist formulation, the discrete molecule comprising:

5 a closed central inorganic ring including only E-E bonds, where E is Si, Ge or Sn, or a combination thereof; and
organic ligands covalently bonded to the E atoms of the closed central inorganic ring.

2. The discrete molecule of claim 1, wherein the closed central inorganic ring is a homogeneous
10 ring.

3. The discrete molecule of claim 1, wherein the closed central inorganic ring includes only Sn or Ge.

15 4. The discrete molecule of claim 1, wherein the chemical formula of the discrete molecule is represented by:



5. The discrete molecule of claim 1, wherein the closed central inorganic ring is a heterogeneous
20 ring.

6. The discrete molecule of claim 1, wherein the discrete molecule is absorbing for extreme ultraviolet (EUV) irradiation.

7. The discrete molecule of claim 1, wherein the discrete molecule is reactive to electron beam (Ebeam) irradiation.

8. A discrete molecule for a resist formulation, the discrete molecule comprising:

a central inorganic element E;

radiating E elements bonded to the central element E to provide E-E bonds, where E is Si, Ge

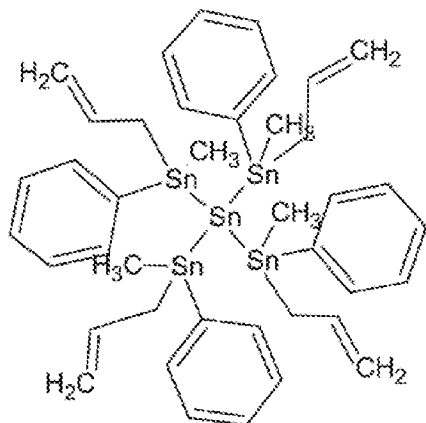
or Sn, or a combination thereof; and

organic ligands covalently bonded to the radiating E elements.

9. The discrete molecule of claim 8, wherein the E-E bonds are all homogeneous bonds.

10. The discrete molecule of claim 8, wherein the E-E bonds are all only Sn-Sn bonds or Ge-Ge bonds.

11. The discrete molecule of claim 8, wherein the chemical formula of the discrete molecule is represented by:



12. The discrete molecule of claim 8, wherein at least some of the E-E bonds are heterogeneous bonds.

13. The discrete molecule of claim 8, wherein the discrete molecule is absorbing for extreme ultraviolet (EUV) irradiation.

14. The discrete molecule of claim 8, wherein the discrete molecule is reactive to electron beam (Ebeam) irradiation.

15. A resist composition for EUV or Ebeam lithography, the resist composition comprising:
a solvent; and
a resist material selected from the group consisting of a polysilane material, a polygermane material, or a polystannane material, the resist material suspended or dissolved in the solvent.

16. The resist composition of claim 15, wherein the resist material comprises polystannane molecules having C=C bonds and Sn-H bonds.

17. The resist composition of claim 15, wherein the resist material comprises polygermane molecules having C=C bonds and Ge-H bonds.

18. The resist composition of claim 15, wherein the resist material comprises discrete molecules, each of the discrete molecules comprising a closed central inorganic ring including only E-E bonds, where E is Si, Ge or Sn, or a combination thereof, and organic ligands covalently bonded to the E atoms of the closed central inorganic ring.

19. The resist composition of claim 15, wherein the resist material comprises discrete molecules, each of the discrete molecules comprising a central inorganic element E, radiating E elements bonded to the central element E to provide E-E bonds, where E is Si, Ge or Sn, or a combination thereof and organic ligands covalently bonded to the radiating E elements.

5

20. The resist composition of claim 15, wherein the solvent is selected from the group consisting of propylene glycol monoethyl acetate (PGMEA), 2-heptanone, cyclohexanone, methyl isobutyl ketone, toluene, ethyl lactate, and mesitylene.

10 21. The resist composition of claim 15, wherein the resist composition is a positive tone resist composition.

22. The resist composition of claim 15, wherein the resist composition is a negative tone resist composition.

15

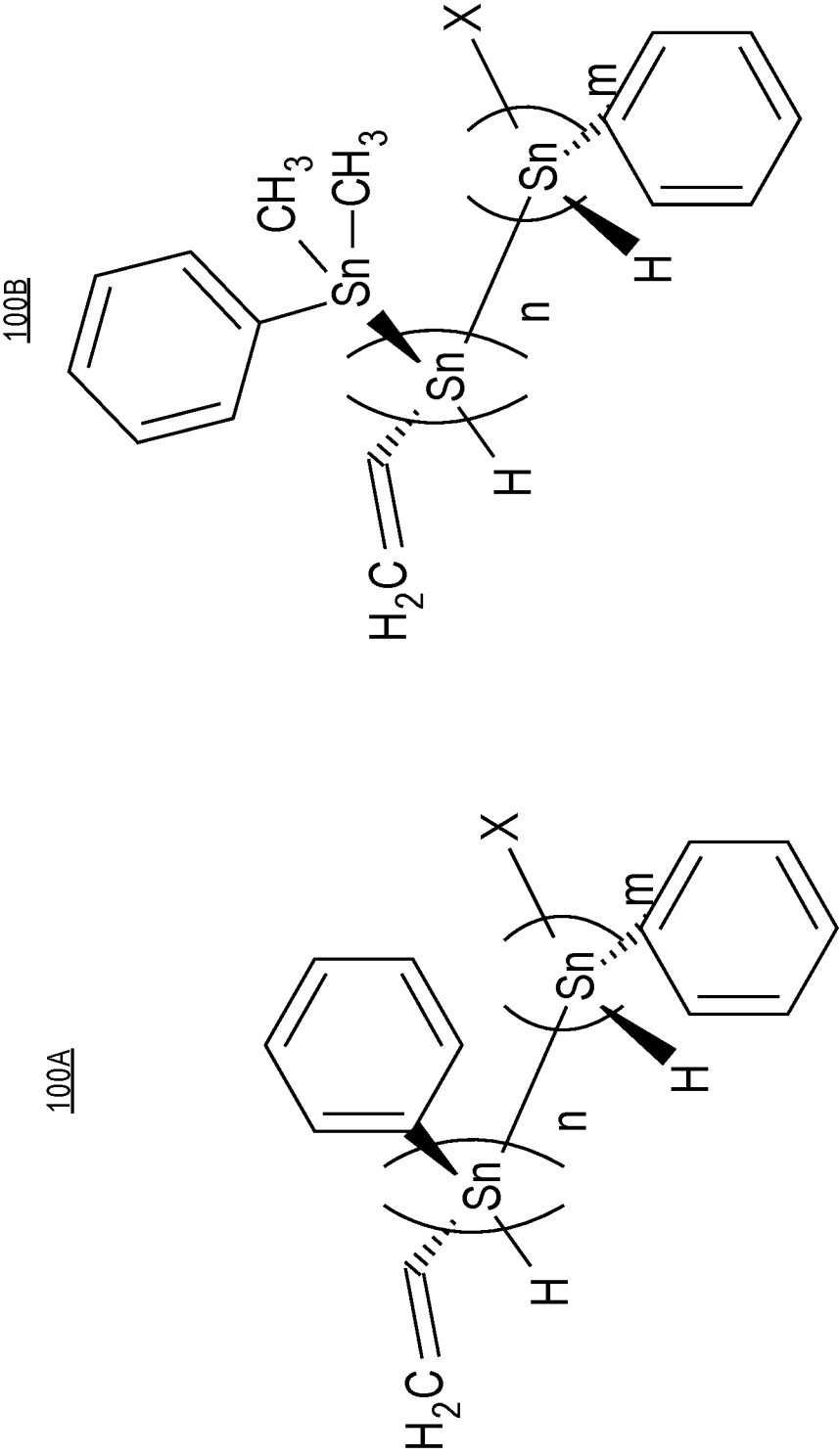


FIG. 1A

FIG. 1B

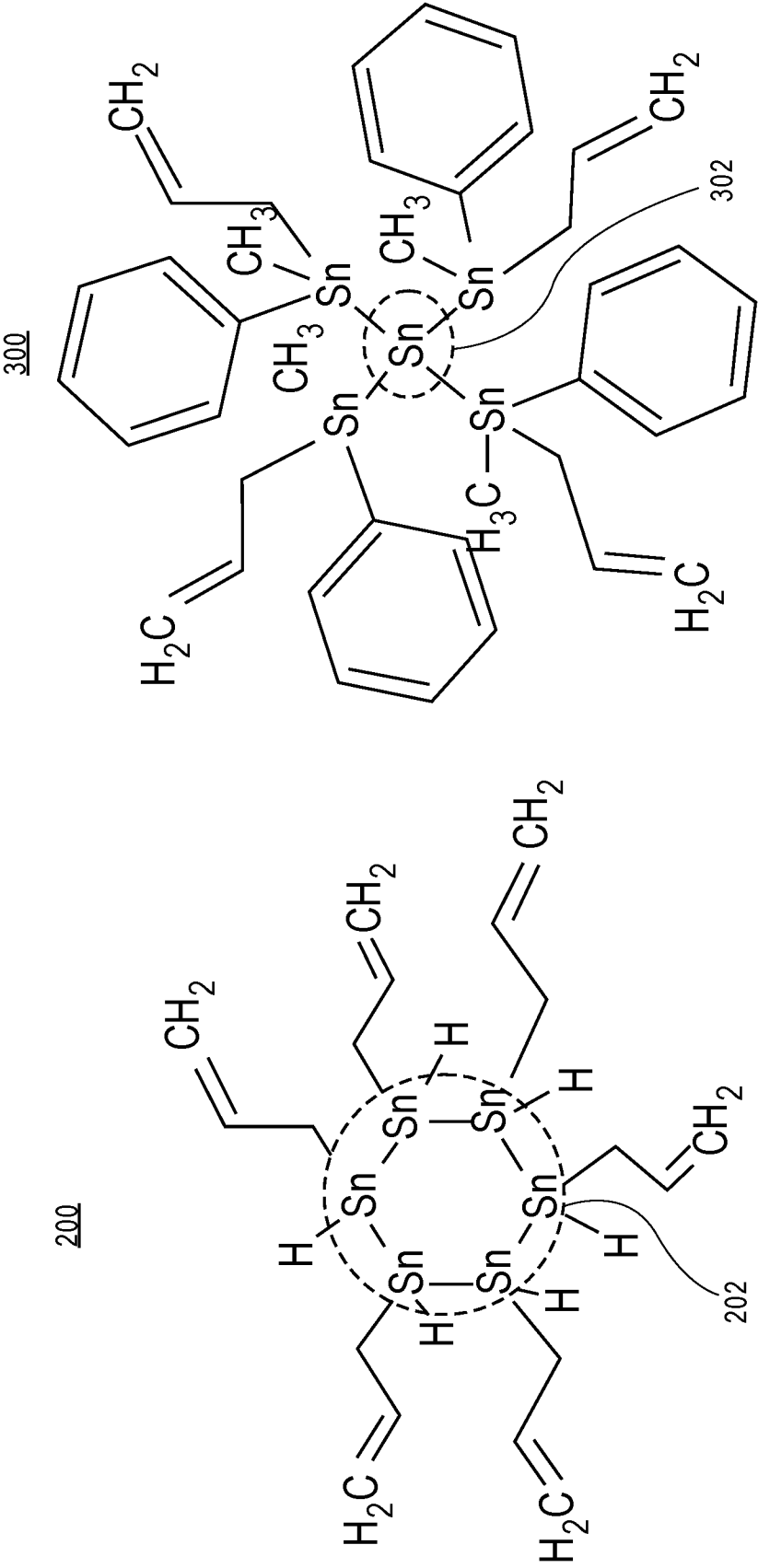


FIG. 2

FIG. 3

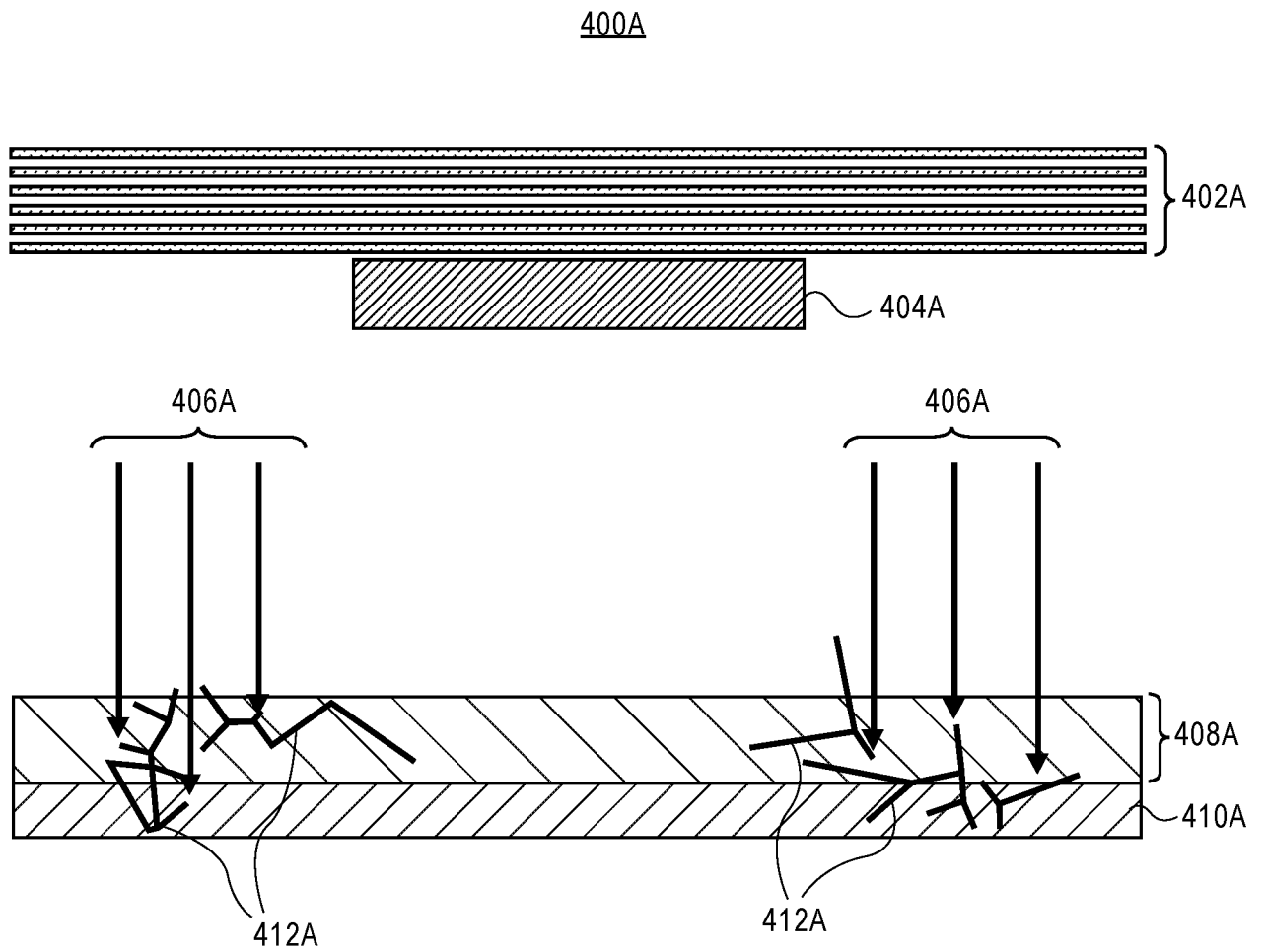
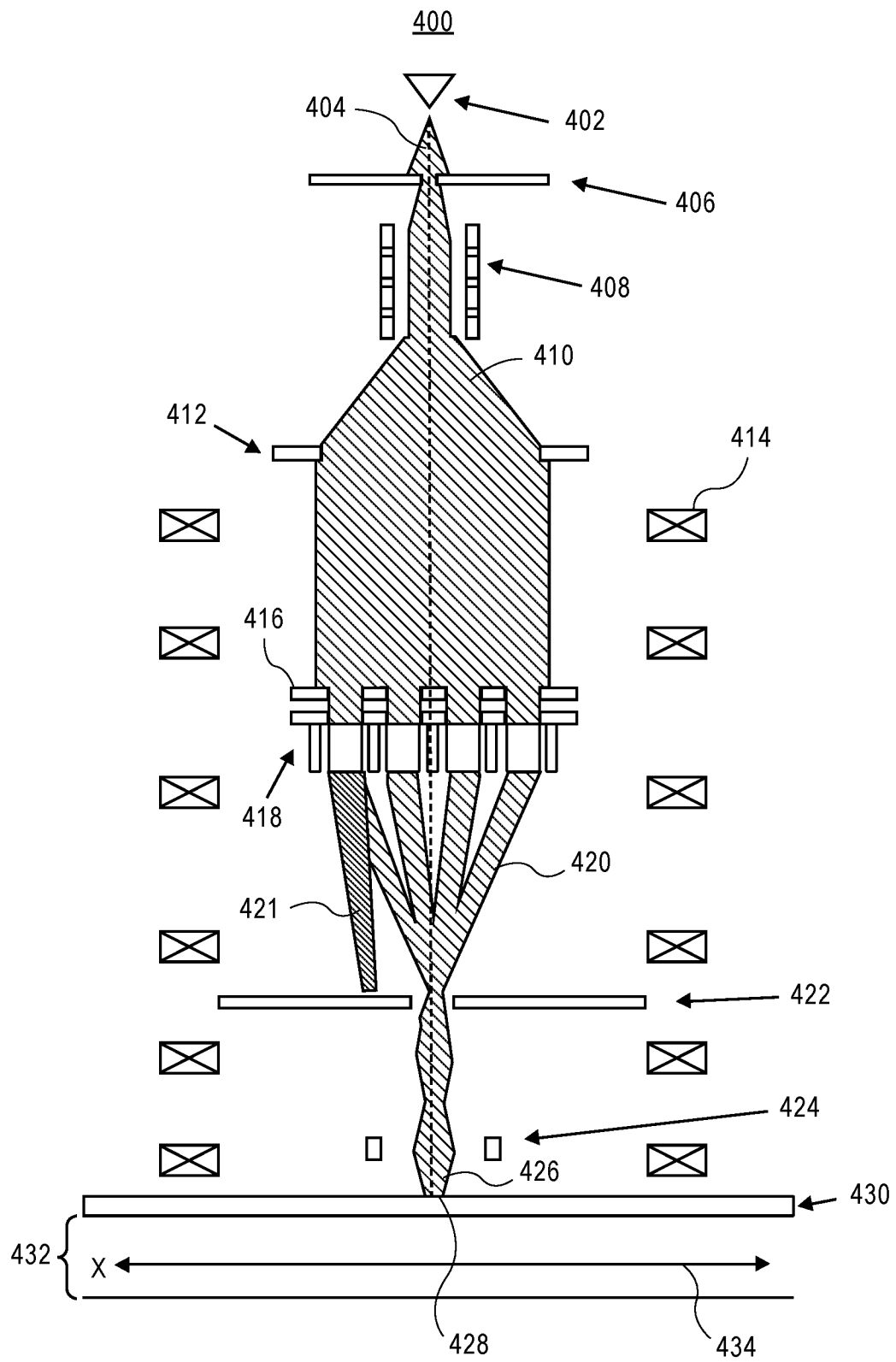


FIG. 4A

**FIG. 4B**

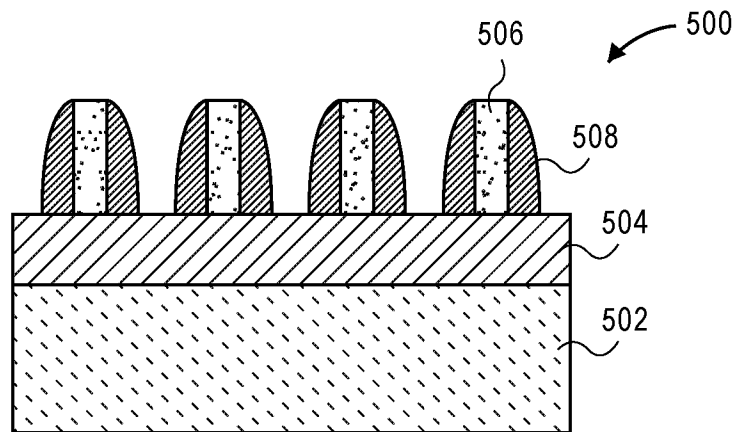


FIG. 5A

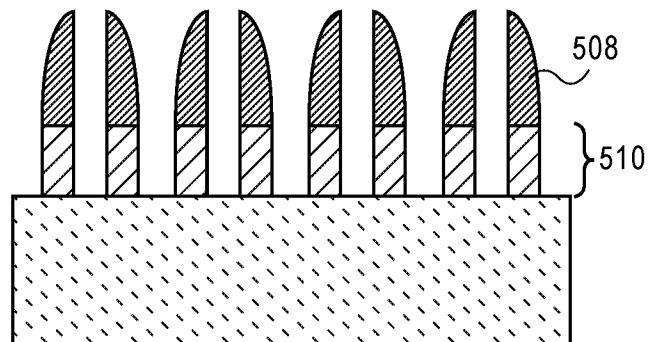


FIG. 5B

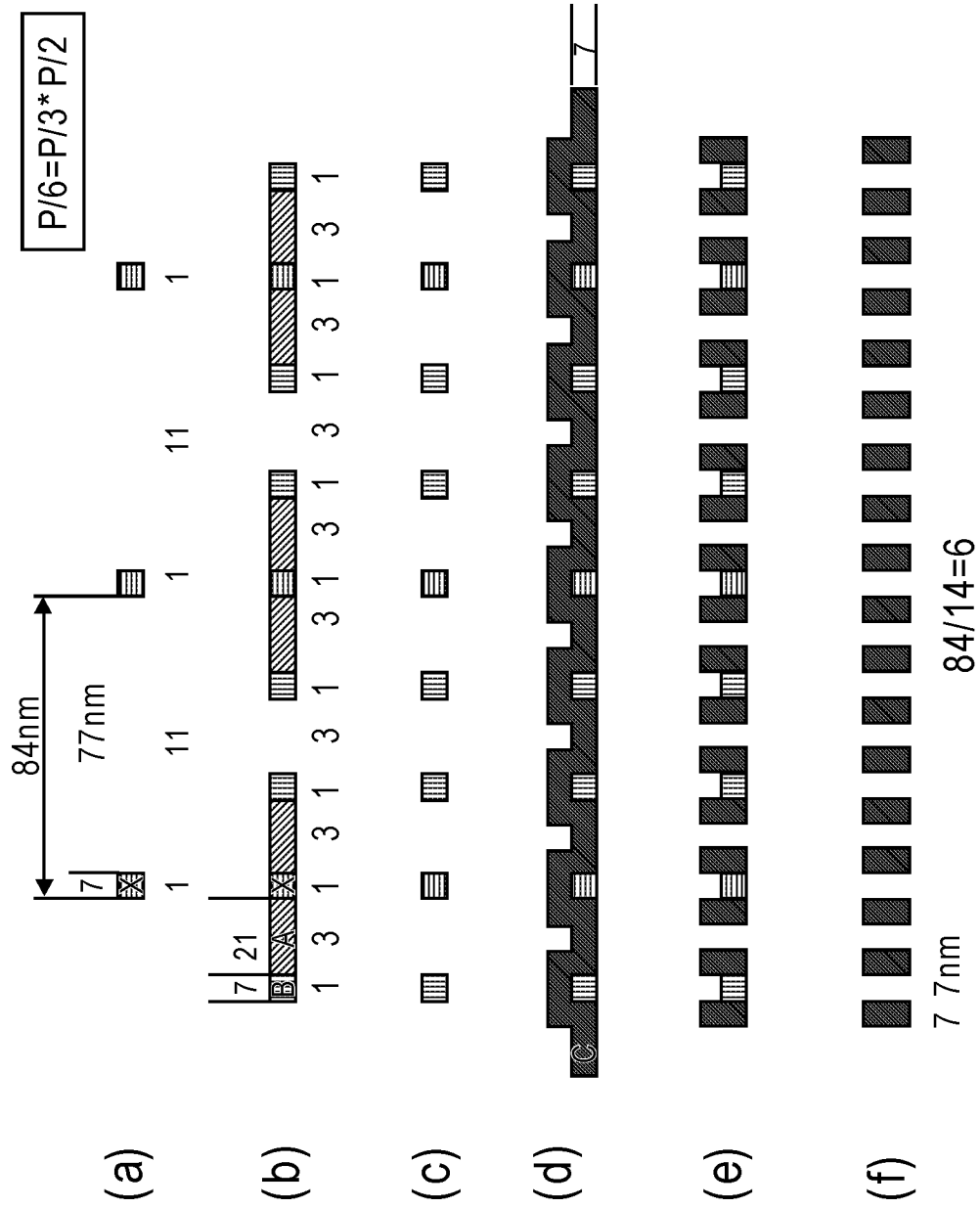


FIG. 6

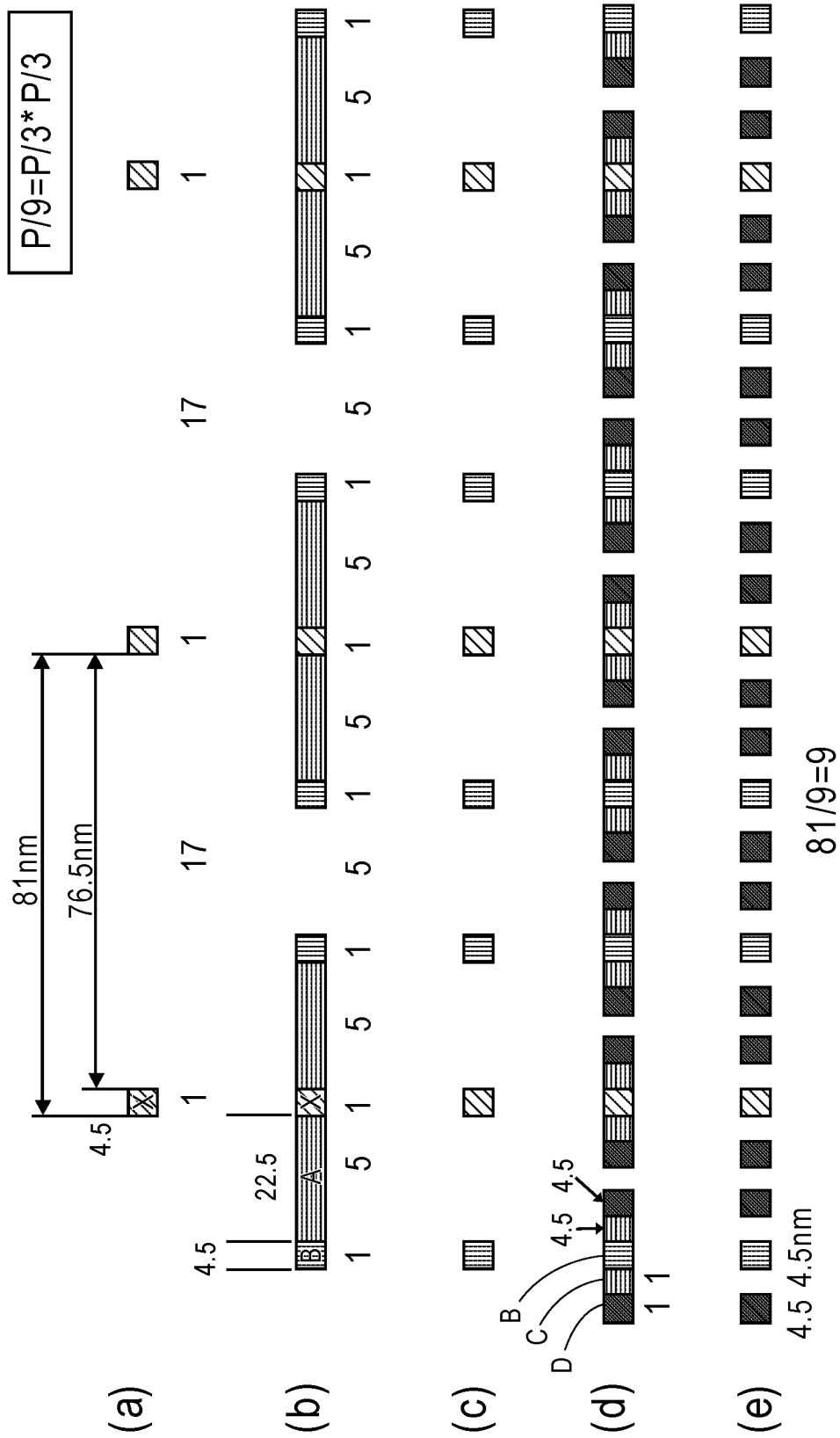


FIG. 7

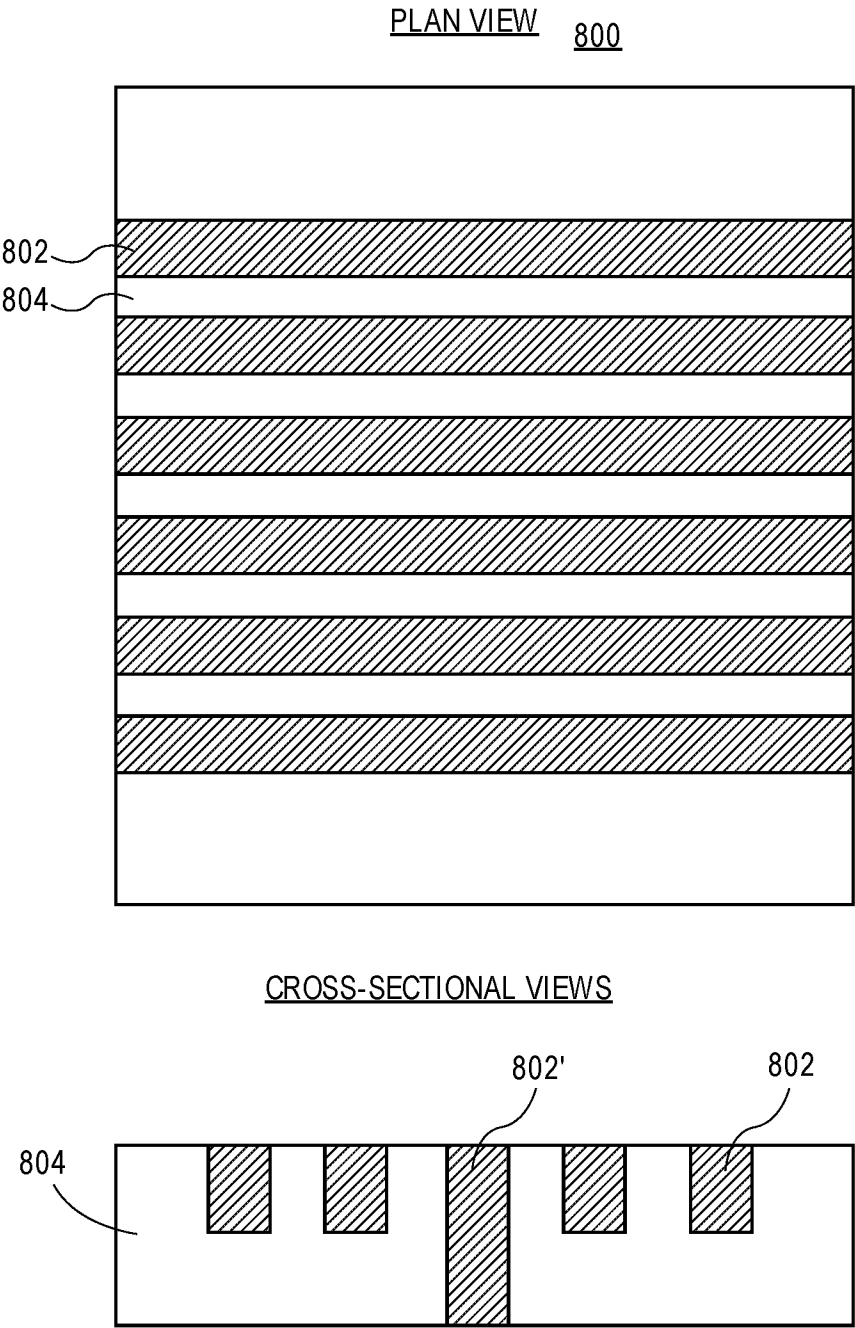
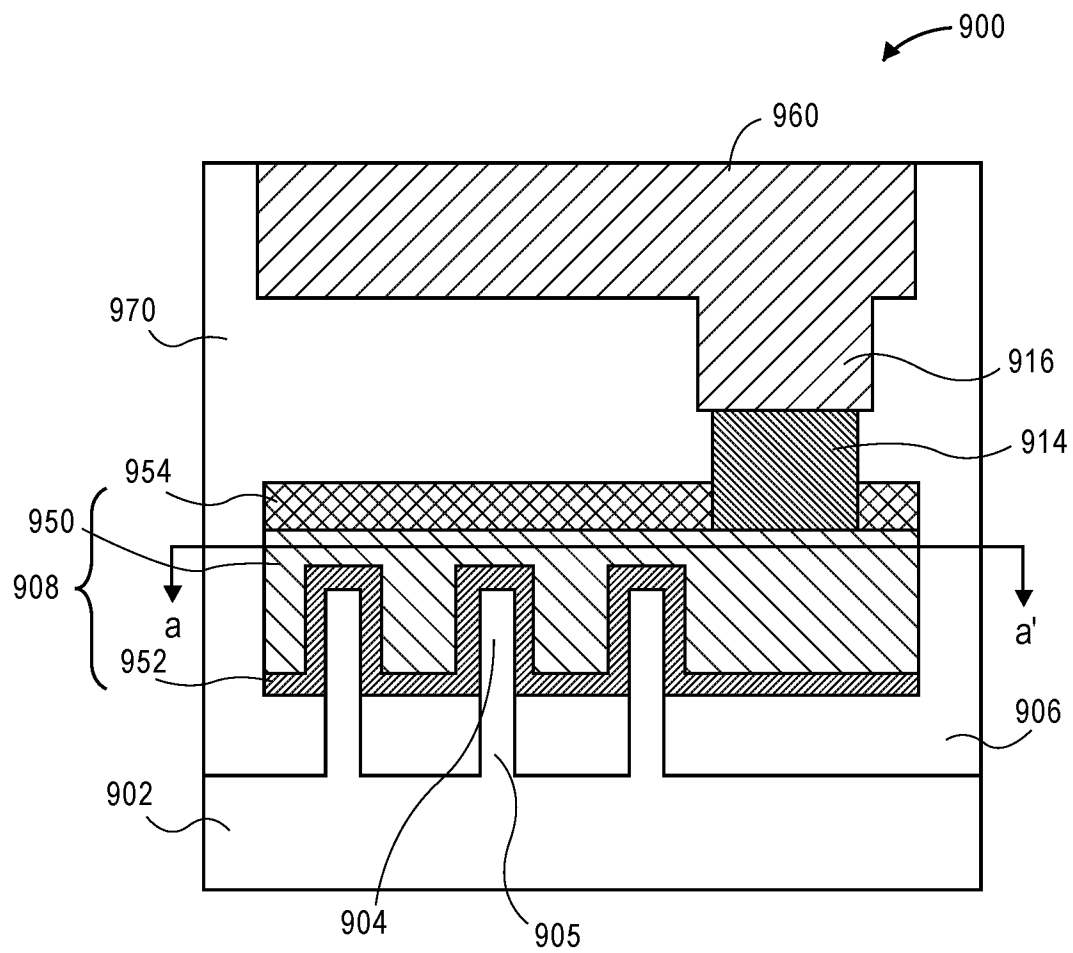
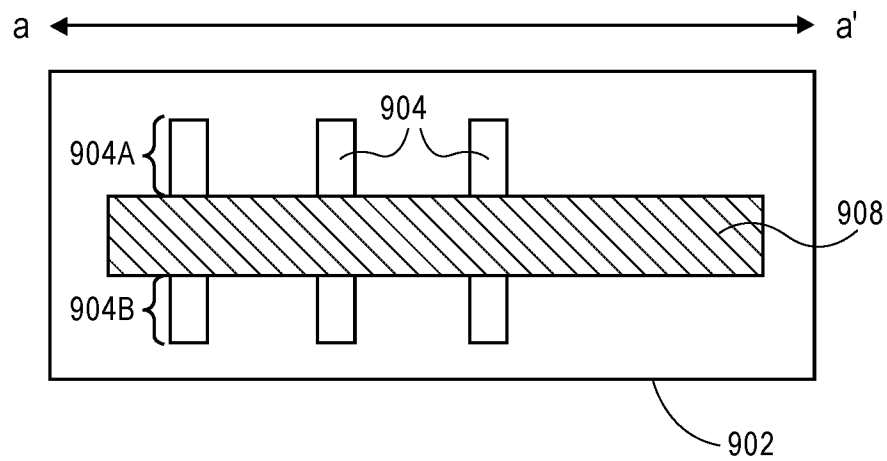


FIG. 8

**FIG. 9A****FIG. 9B**

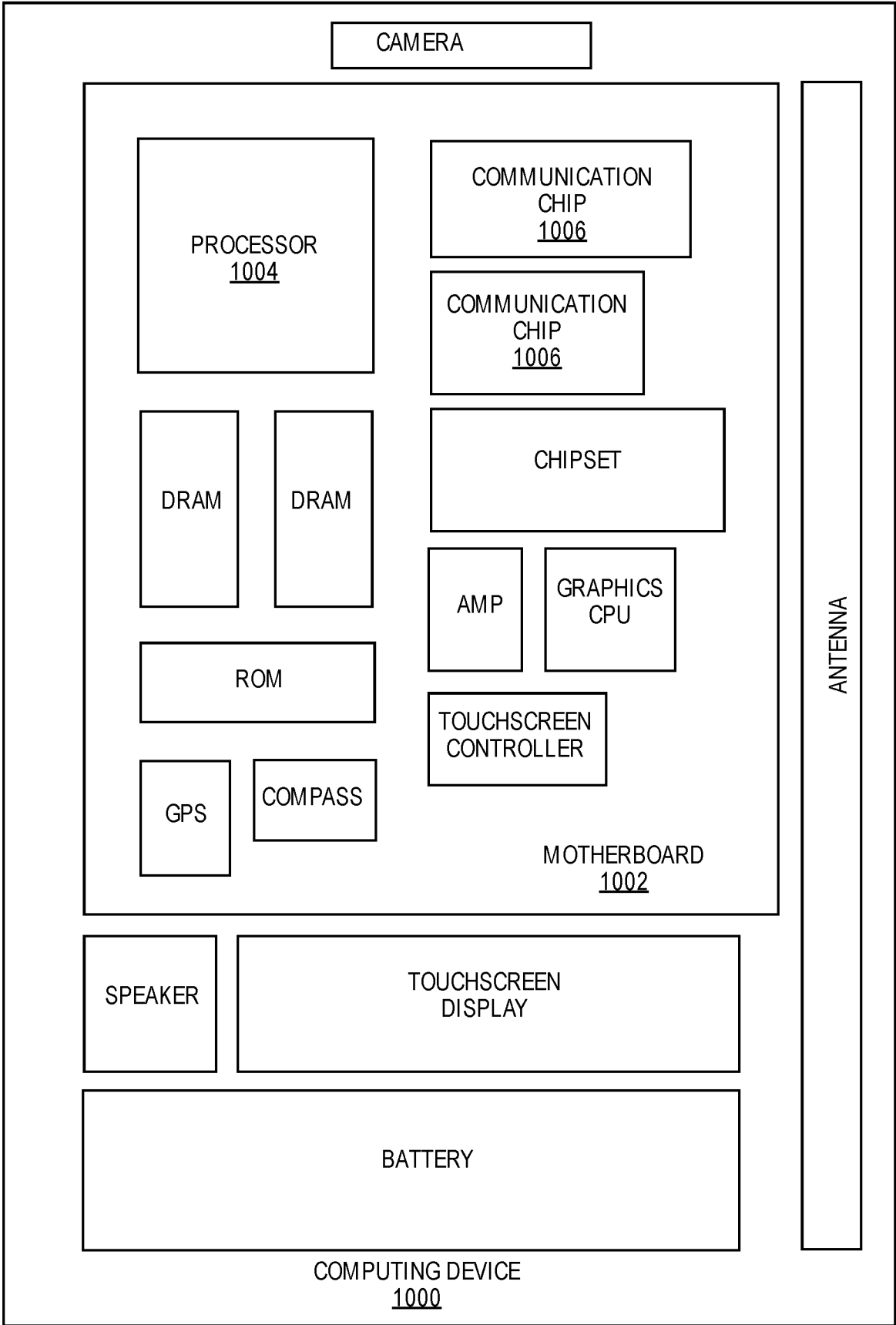
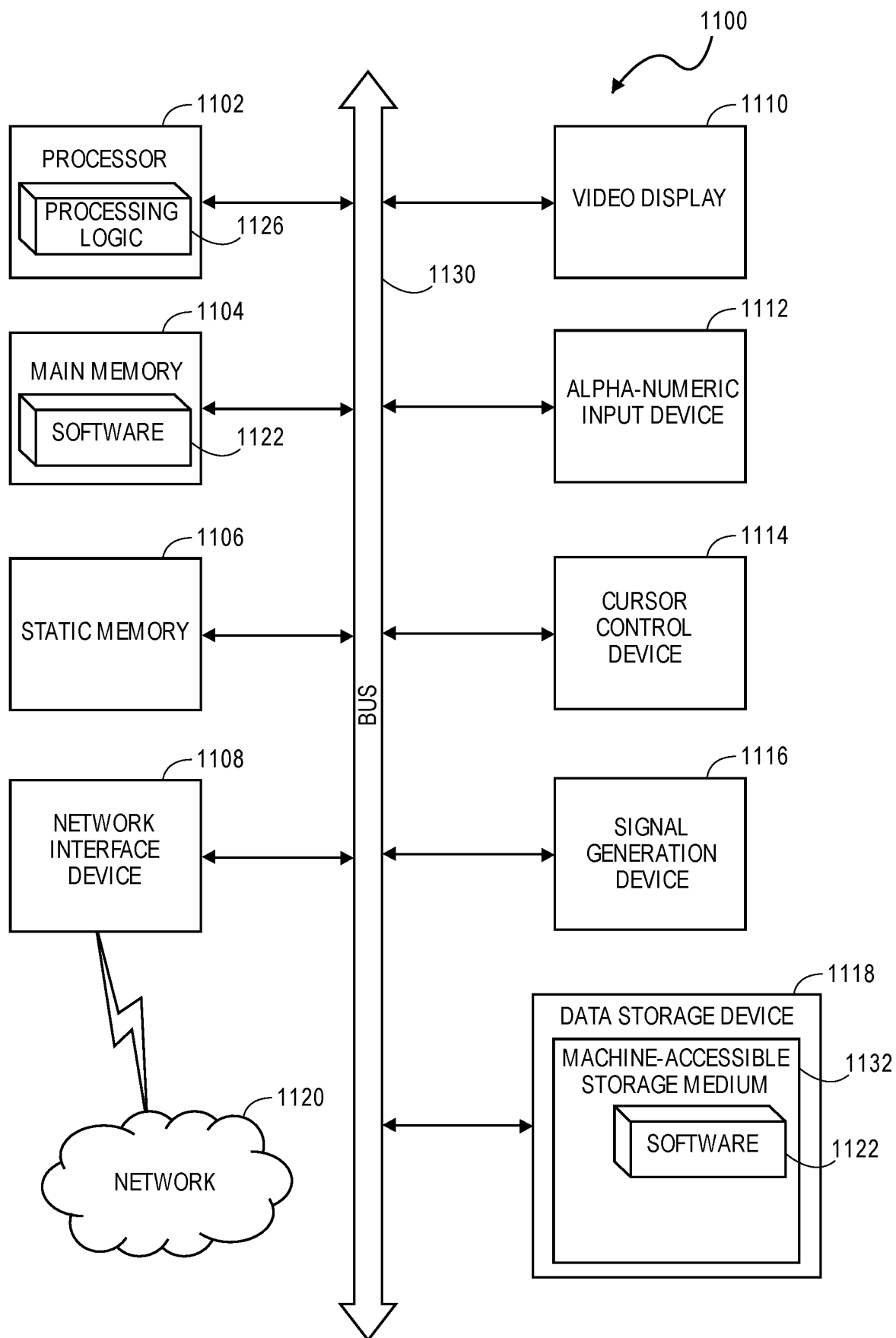


FIG. 10

**FIG. 11**

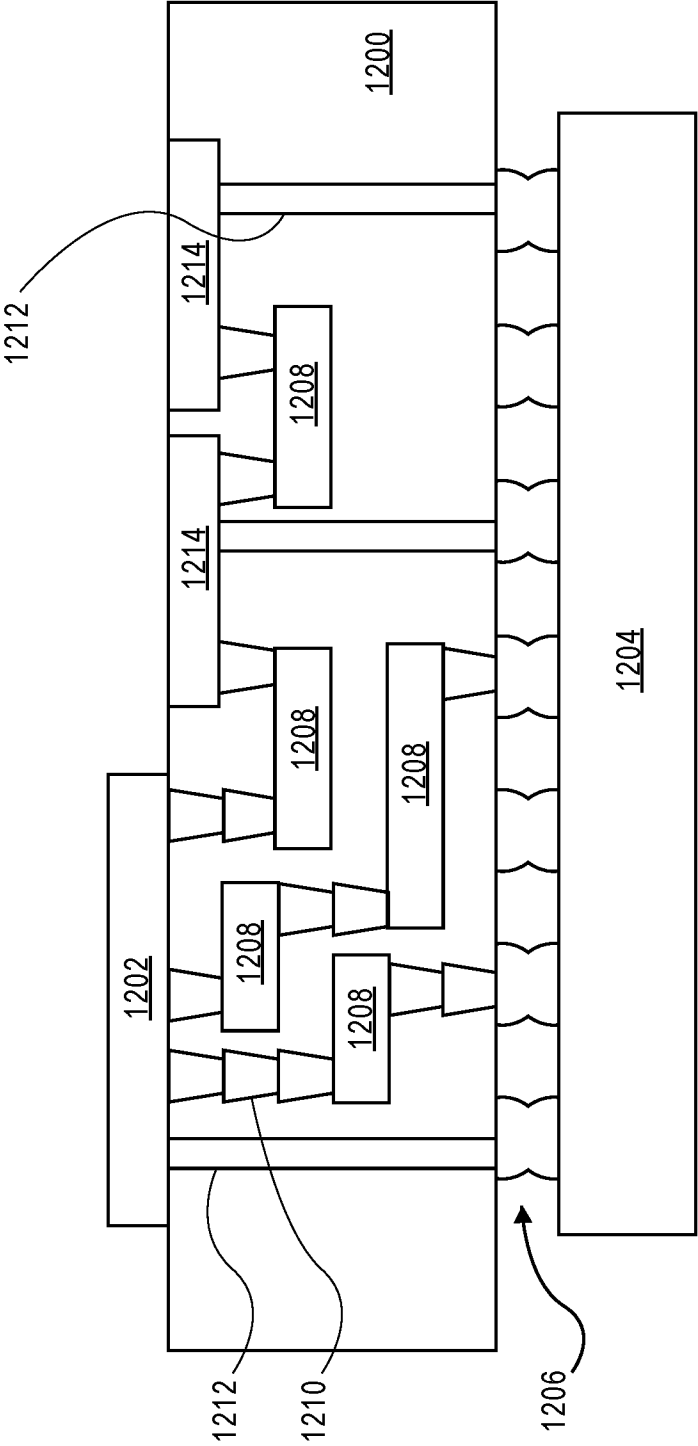


FIG. 12

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

I. Claims 1-7 are directed to a discrete molecule formulation, the discrete molecule comprising a closed central inorganic ring including only E-E bonds.

II. Claims 8-14 are directed to a discrete molecule formulation, the discrete molecule comprising a central inorganic element E and radiating E element bonded to the central element E to provide E-E bonds.

III. Claims 15-22 are directed to a resist composition for EUV or Ebeam lithography.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-7

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

A. CLASSIFICATION OF SUBJECT MATTER

G03F 7/075(2006.01)i, G03F 7/004(2006.01)i, G03F 7/039(2006.01)i, G03F 7/038(2006.01)i, C08G 79/00(2006.01)i, C08G 83/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G03F 7/075; G21K 5/00; G03C 5/00; G03F 7/20; G08G 79/00; G03F 7/004; G03F 7/039; G03F 7/038; C08G 79/00; C08G 83/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & STN (Registry, Caplus) & google & keywords: discrete molecule, resist formulation, closed central inorganic ring, E-E bonds, organic ligands covalently, central inorganic element E, resist composition, polysilane, polygermane, polystannane

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4347304 A (SAKURAI, H. et al.) 31 August 1982 See column 1, lines 4-10; column 1, lines 35-39; column 2, lines 20-23; column 5, line 60-column 6, line 16; column 6, lines 40-59; and claims 1, 5-6.	1-3,5-7
A		4
X	US 5717051 A (HIRAOKA, T. et al.) 10 February 1998 See column 2, lines 25-43; column 14, lines 35-54; column 15, lines 6-10; column 47, lines 10-34; and claim 1.	1-2
A	Beckmann, J. et al., "Optically Active Organotin Compounds Derived from β -Pinene. The Quest for Chiral Polystannanes", Organometallics, 03 August 2008, Vol. 27, pages 1495-1500. See page 1496.	1-7
A	US 2003-0215749 A1 (KATO, H. et al.) 20 November 2003 See claim 1, 2, 4, 9.	1-7
A	ROSS, L. et al., "VIII. Octaphenylcyclotetragerman(Ph ₂ Ge) ₄ , ein Germaniumhomocyclus mit D _{2d} -symmetrie, Journal of Organometallic Chemistry, 1980, Vol. 199, pages 195-204. See abstract; page 196.	1-7



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 April 2017 (28.04.2017)

Date of mailing of the international search report

01 May 2017 (01.05.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/039912

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		TW I223321 B	01/11/2004
		US 7026099 B2	11/04/2006