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(54) Title: THREE-DIMENSIONAL MEMORY DEVICE INCLUDING INCLINED WORD LINE CONTACT STRIPS AND METHODS OF FORMING THE SAME

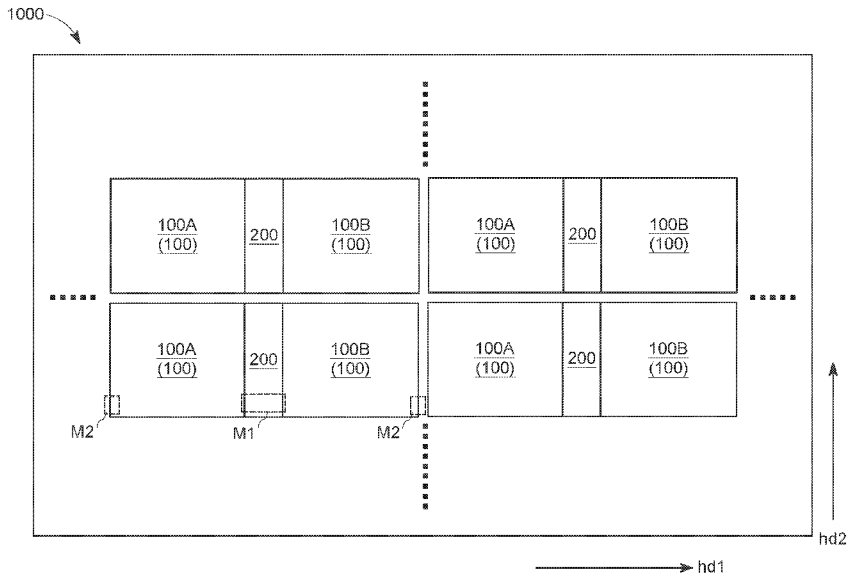

FIG. 1

(57) Abstract: A memory device includes an alternating stack including insulating layers and electrically conductive layers and a tapered sidewall that laterally extends along a first horizontal direction and an inclined along a second horizontal direction, memory opening fill structures extending through each layer within the alternating stack and including memory elements and a vertical semiconductor channel, a cavity in the alternating stack bounded laterally by the tapered sidewall, and having a bottom surface including stepped surfaces of at least some of the electrically conductive layers, an insulating liner located over the tapered sidewall in the cavity, and electrically conductive strips which are adjoined to a respective one of the stepped surfaces at the bottom surface of the cavity, which extend over the insulating liner and the tapered sidewall in the cavity, and which include a respective topmost portion that is located above the topmost surface of the alternating stack.

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THREE-DIMENSIONAL MEMORY DEVICE INCLUDING INCLINED WORD LINE CONTACT STRIPS AND METHODS OF FORMING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of and hereby incorporates by reference, for all purposes, the entirety of the contents of U.S. Nonprovisional Application No 18/450,115, entitled "THREE-DIMENSIONAL MEMORY DEVICE INCLUDING INCLINED WORD LINE CONTACT STRIPS AND METHODS OF FORMING THE SAME" and filed in the United States Patent & Trademark Office on August 15, 2023, which is claims priority of U.S. Provisional application number 63/506,902 filed June 8, 2023.

FIELD

[0002] The present disclosure relates generally to the field of semiconductor devices, and particularly to a three-dimensional memory device including inclined word line contact strips and methods of forming the same.

BACKGROUND

[0003] A three-dimensional memory device including three-dimensional vertical NAND strings having one bit per cell are disclosed in an article by T. Endoh *et al*, titled "Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell", IEDM Proc. (2001) 33-36.

SUMMARY

[0004] According to an embodiment of the present disclosure, a memory device comprises an alternating stack including insulating layers and electrically conductive layers that are interlaced along a vertical direction, wherein the alternating stack comprises a tapered sidewall that laterally extends along a first horizontal direction and which is inclined along a second horizontal direction perpendicular to the first horizontal direction; memory openings vertically extending through each layer within the alternating stack; memory opening fill structures located in the memory openings and including a respective vertical stack of memory elements and a respective vertical semiconductor channel; a cavity in the alternating stack bounded laterally along a first side by the tapered sidewall, and having a bottom surface comprising stepped surfaces of at least some of the electrically conductive layers; an insulating liner located over the tapered sidewall in the cavity; and electrically conductive strips which are adjoined to a respective one of the stepped surfaces at the bottom surface of the cavity, which extend over the insulating liner and the tapered sidewall in the cavity, and which include a respective topmost portion that is located above the topmost surface of the alternating stack.

[0005] According to another aspect of the present disclosure, a method of forming a memory

device comprises forming an alternating stack of insulating layers and sacrificial material layers that are interlaced along a vertical direction; forming a cavity in the alternating stack such that stepped surfaces of the sacrificial material layers of the alternating stack are exposed at a bottom surface of the cavity; forming an insulating liner over the stepped surfaces, over a tapered sidewall of the alternating stack, and over a topmost layer of the alternating stack; forming an elongated opening through the insulating liner, wherein a strip segment of the stepped surfaces is exposed through the elongated opening through the insulating liner; forming a sacrificial liner on the strip segment of the stepped surfaces and over the elongated openings such that the sacrificial liner comprises a top portion that overlies the alternating stack; forming a dielectric fill structure over the sacrificial liner; forming memory openings vertically extending at least through the alternating stack; forming memory opening fill structures in the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements and a respective vertical semiconductor channel; forming lateral isolation trenches and an array of isolation cavities through the alternating stack, wherein the lateral isolation trenches and the array of isolation cavities divide the sacrificial liner into sacrificial liner strips that are laterally spaced apart from each other; and replacing remaining portions of the sacrificial material layers and the sacrificial liner strips with electrically conductive material portions, wherein electrically conductive layers are formed in volumes from which the remaining portions of the sacrificial material layers are removed, and electrically conductive strips are formed in volumes from which the sacrificial liner strips are removed, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a plan view of an exemplary semiconductor die including multiple three-dimensional memory array regions according to an embodiment of the present disclosure.

[0007] FIGS. 2A – 2D are various views of an exemplary structure after formation of optional semiconductor devices, optional lower level dielectric layers, optional lower metal interconnect structures, a semiconductor material layer, a first alternating layer stack of first insulating layers and first sacrificial material layers, and a first cavity according to an embodiment of the present disclosure. FIGS. 2B is a top-down view. FIG. 2A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 2B. FIG. 2C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 2B. FIG. 2D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 2B. The illustrated region of FIGS. 2A – 2D correspond to area M1 in FIG. 1.

[0008] FIGS. 3A – 3E are various views of the exemplary structure after deposition and patterning of a first insulating liner according to an embodiment of the present disclosure. FIGS.

3B is a top-down view. FIG. 3A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 3B. FIG. 3C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 3B. FIG. 3D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 3B. FIG. 3E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 3B.

[0009] FIGS. 4A – 4E are various views of the exemplary structure after deposition and patterning of a first sacrificial liner according to an embodiment of the present disclosure. FIGS. 4B is a top-down view. FIG. 4A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 4B. FIG. 4C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 4B. FIG. 4D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 4B. FIG. 4E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 4B.

[0010] FIGS. 5A – 5E are various views of the exemplary structure after formation of a first insulating cap layer and a first dielectric fill structure according to an embodiment of the present disclosure. FIGS. 5B is a top-down view. FIG. 5A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 5B. FIG. 5C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 5B. FIG. 5D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 5B. FIG. 5E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 5B.

[0011] FIGS. 6A – 6E are various views of the exemplary structure after formation of first-tier memory openings and first-tier support openings according to an embodiment of the present disclosure. FIGS. 6B is a top-down view. FIG. 6A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 6B. FIG. 6C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 6B. FIG. 6D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 6B. FIG. 6E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 6B.

[0012] FIGS. 7A – 7E are various views of the exemplary structure after formation of first-tier sacrificial opening fill structures according to an embodiment of the present disclosure. FIGS. 7B is a top-down view. FIG. 7A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 7B. FIG. 7C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 7B. FIG. 7D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 7B. FIG. 7E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 7B.

[0013] FIGS. 8A – 8E are various views of the exemplary structure after formation of a second alternating layer stack of second insulating layers and second sacrificial material layers, and a second cavity according to an embodiment of the present disclosure. FIGS. 8B is a top-down view. FIG. 8A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 8B. FIG. 8C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 8B. FIG.

8D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 8B. FIG. 8E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 8B.

[0014] FIGS. 9A – 9E are various views of the exemplary structure after deposition and patterning of a second insulating liner according to an embodiment of the present disclosure. FIGS. 9B is a top-down view. FIG. 9A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 9B. FIG. 9C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 9B. FIG. 9D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 9B. FIG. 9E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 9B.

[0015] FIGS. 10A – 10E are various views of the exemplary structure after deposition and patterning of a second sacrificial liner according to an embodiment of the present disclosure. FIGS. 10B is a top-down view. FIG. 10A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 10B. FIG. 10C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 10B. FIG. 10D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 10B. FIG. 10E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 10B.

[0016] FIGS. 11A – 11E are various views of the exemplary structure after formation of a second insulating cap layer and a second dielectric fill structure according to an embodiment of the present disclosure. FIGS. 11B is a top-down view. FIG. 11A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 11B. FIG. 11C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 11B. FIG. 11D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 11B. FIG. 11E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 11B.

[0017] FIGS. 12A – 12E are various views of the exemplary structure after formation of inter-tier memory openings and inter-tier support openings according to an embodiment of the present disclosure. FIGS. 12B is a top-down view. FIG. 12A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 12B. FIG. 12C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 12B. FIG. 12D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 12B. FIG. 12E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 12B.

[0018] FIGS. 13A – 13E are various views of the exemplary structure after formation of sacrificial opening fill structures according to an embodiment of the present disclosure. FIGS. 13B is a top-down view. FIG. 13A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 13B. FIG. 13C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 13B. FIG. 13D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 13B. FIG. 13E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 13B.

[0019] FIGS. 14A – 14E are various views of the exemplary structure after replacement of sacrificial support opening fill structures with support pillar structures according to an embodiment of the present disclosure. FIGS. 14B is a top-down view. FIG. 14A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 14B. FIG. 14C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 14B. FIG. 14D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 14B. FIG. 14E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 14B.

[0020] FIGS. 15A – 15E are various views of the exemplary structure after removal of the sacrificial memory opening fill structures according to an embodiment of the present disclosure. FIGS. 15B is a top-down view. FIG. 15A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 15B. FIG. 15C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 15B. FIG. 15D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 15B. FIG. 15E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 15B.

[0021] FIGS. 16A – 16F are sequential vertical cross-sectional views of an inter-tier memory opening during formation of a memory opening fill structure according to an embodiment of the present disclosure.

[0022] FIGS. 17A – 17G are various views of the exemplary structure after formation of memory opening fill structures according to an embodiment of the present disclosure. FIGS. 17B is a top-down view. FIG. 17A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 17B. FIG. 17C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 17B. FIG. 17D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 17B. FIG. 17E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 17B. FIG. 17F is a vertical cross-sectional view along the vertical plane F – F' of FIG. 17B. FIG. 17G is a vertical cross-sectional view along the vertical plane G – G' of FIG. 17B.

[0023] FIGS. 18A – 18I are various views of the exemplary structure after formation of lateral isolation trenches and isolation cavities according to an embodiment of the present disclosure. FIGS. 18B is a top-down view. FIG. 18A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 18B. FIG. 18C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 18B. FIG. 18D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 18B. FIG. 18E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 18B. FIG. 18F is a vertical cross-sectional view along the vertical plane F – F' of FIG. 18B. FIG. 18G is a vertical cross-sectional view along the vertical plane G – G' of FIG. 18B. FIG. 18H is a vertical cross-sectional view along the vertical plane H – H' of FIG. 18B. FIG. 18I is a vertical cross-sectional view along the vertical plane I – I' of FIG. 18B.

[0024] FIGS. 19A – 19I are various views of the exemplary structure after formation of laterally-extending cavities according to an embodiment of the present disclosure. FIGS. 19B is a top-down view. FIG. 19A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 19B. FIG. 19C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 19B. FIG. 19D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 19B. FIG. 19E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 19B. FIG. 19F is a vertical cross-sectional view along the vertical plane F – F' of FIG. 19B. FIG. 19G is a vertical cross-sectional view along the vertical plane G – G' of FIG. 19B. FIG. 19H is a vertical cross-sectional view along the vertical plane H – H' of FIG. 19B. FIG. 19I is a vertical cross-sectional view along the vertical plane I – I' of FIG. 19B.

[0025] FIGS. 20A – 20I are various views of the exemplary structure after formation of electrically conductive layers and electrically conductive strips and isolation cavities according to an embodiment of the present disclosure. FIGS. 20B is a top-down view. FIG. 20A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 20B. FIG. 20C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 20B. FIG. 20D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 20B. FIG. 20E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 20B. FIG. 20F is a vertical cross-sectional view along the vertical plane F – F' of FIG. 20B. FIG. 20G is a vertical cross-sectional view along the vertical plane G – G' of FIG. 20B. FIG. 20H is a vertical cross-sectional view along the vertical plane H – H' of FIG. 20B. FIG. 20I is a vertical cross-sectional view along the vertical plane I – I' of FIG. 20B.

[0026] FIGS. 21A – 21I are various views of the exemplary structure after formation of lateral isolation trench fill structures and lateral isolation structures according to an embodiment of the present disclosure. FIGS. 21B is a top-down view. FIG. 21A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 21B. FIG. 21C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 21B. FIG. 21D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 21B. FIG. 21E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 21B. FIG. 21F is a vertical cross-sectional view along the vertical plane F – F' of FIG. 21B. FIG. 21G is a vertical cross-sectional view along the vertical plane G – G' of FIG. 21B. FIG. 21H is a vertical cross-sectional view along the vertical plane H – H' of FIG. 21B. FIG. 21I is a vertical cross-sectional view along the vertical plane I – I' of FIG. 21B.

[0027] FIG. 22A is a vertical cross-sectional view of a first alternative configuration of the exemplary structure after formation of lateral isolation trench fill structures and lateral isolation structures according to an embodiment of the present disclosure. FIG. 22B is a top-down view of the first alternative configuration of the exemplary structure of FIG. 22A. The vertical plane A –

A' is the cut plane of FIG. 22A.

[0028] FIG. 23A is a vertical cross-sectional view of a second alternative configuration of the exemplary structure after formation of lateral isolation trench fill structures and lateral isolation structures according to an embodiment of the present disclosure. FIG. 23B is a top-down view of the second alternative configuration of the exemplary structure of FIG. 23A. The vertical plane A – A' is the cut plane of FIG. 23A.

[0029] FIG. 24A is a vertical cross-sectional view of a third alternative configuration of the exemplary structure after formation of lateral isolation trench fill structures and lateral isolation structures according to an embodiment of the present disclosure. FIG. 24B is a top-down view of the third alternative configuration of the exemplary structure of FIG. 24A. The vertical plane A – A' is the cut plane of FIG. 24A.

[0030] FIG. 25A is a vertical cross-sectional view of a fourth alternative configuration of the exemplary structure after formation of lateral isolation trench fill structures and lateral isolation structures according to an embodiment of the present disclosure. FIG. 25B is a top-down view of the fourth alternative configuration of the exemplary structure of FIG. 25A. The vertical plane A – A' is the cut plane of FIG. 25A.

[0031] FIG. 26A is a vertical cross-sectional view of a fifth alternative configuration of the exemplary structure after formation of lateral isolation trench fill structures and lateral isolation structures according to an embodiment of the present disclosure. FIG. 26B is a top-down view of the fifth alternative configuration of the exemplary structure of FIG. 26A. The vertical plane A – A' is the cut plane of FIG. 26A.

[0032] FIGS. 27A – 27E are various views of the exemplary structure after formation of drain-select-level isolation structures according to an embodiment of the present disclosure. FIGS. 27B is a top-down view. FIG. 27A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 27B. FIG. 27C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 27B. FIG. 27D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 27B. FIG. 27E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 27B .

[0033] FIGS. 28A – 28G are various views of the exemplary structure after formation of a contact-level dielectric layer and various metallic via structures according to an embodiment of the present disclosure. FIGS. 28B is a top-down view. FIG. 28A is a vertical cross-sectional view along the vertical plane A – A' of FIG. 28B. FIG. 28C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 28B. FIG. 28D is a vertical cross-sectional view along the vertical plane D – D' of FIG. 28B. FIG. 28E is a vertical cross-sectional view along the vertical plane E – E' of FIG. 28B. FIG. 28F is a cut-away perspective view of a portion of the exemplary

structure. FIG. 28G is a vertical cross-sectional view of FIG. 28B in area M2 of FIG. 1.

DETAILED DESCRIPTION

[0034] As discussed above, the embodiments of the present disclosure are directed to a three-dimensional memory device including inclined word line contact strips which overlie tapered sidewalls of wells exposing word line steps and methods of forming the same, the various aspects of which are now described in detail.

[0035] The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as "first," "second," and "third" are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. The term "at least one" element refers to all possibilities including the possibility of a single element and the possibility of multiple elements.

[0036] The same reference numerals refer to the same element or similar element. Unless otherwise indicated, elements having the same reference numerals are presumed to have the same composition and the same function. Unless otherwise indicated, a "contact" between elements refers to a direct contact between elements that provides an edge or a surface shared by the elements. If two or more elements are not in direct contact with each other or among one another, the two elements are "disjoined from" each other or "disjoined among" one another. As used herein, a first element located "on" a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located "directly on" a second element if there exist a physical contact between a surface of the first element and a surface of the second element. As used herein, a first element is "electrically connected to" a second element if there exists a conductive path consisting of at least one conductive material between the first element and the second element. As used herein, a "prototype" structure or an "in-process" structure refers to a transient structure that is subsequently modified in the shape or composition of at least one component therein.

[0037] As used herein, a "layer" refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the first continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the first continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, or may have one or more

layer thereupon, thereabove, and/or therebelow.

[0038] As used herein, a first surface and a second surface are "vertically coincident" with each other if the second surface overlies or underlies the first surface and there exists a vertical plane or a substantially vertical plane that includes the first surface and the second surface. A substantially vertical plane is a plane that extends straight along a direction that deviates from a vertical direction by an angle less than 5 degrees. A vertical plane or a substantially vertical plane is straight along a vertical direction or a substantially vertical direction, and may, or may not, include a curvature along a direction that is perpendicular to the vertical direction or the substantially vertical direction.

[0039] As used herein, a "memory level" or a "memory array level" refers to the level corresponding to a general region between a first horizontal plane (i.e., a plane parallel to the top surface of the substrate) including topmost surfaces of an array of memory elements and a second horizontal plane including bottommost surfaces of the array of memory elements. As used herein, a "through-stack" element refers to an element that vertically extends through a memory level.

[0040] As used herein, a "semiconducting material" refers to a material having electrical conductivity in the range from 1.0×10^{-5} S/m to 1.0×10^{5} S/m. As used herein, a "semiconductor material" refers to a material having electrical conductivity in the range from 1.0×10^{-5} S/m to 1.0 S/m in the absence of electrical dopants therein, and is capable of producing a doped material having electrical conductivity in a range from 1.0 S/m to 1.0×10^{7} S/m upon suitable doping with an electrical dopant. As used herein, an "electrical dopant" refers to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure . As used herein, a "conductive material" refers to a material having electrical conductivity greater than 1.0×10^{5} S/m. As used herein, an "insulator material" or a "dielectric material" refers to a material having electrical conductivity less than 1.0×10^{-5} S/m. As used herein, a "heavily doped semiconductor material" refers to a semiconductor material that is doped with electrical dopant at a sufficiently high atomic concentration to become a conductive material either as formed as a crystalline material or if converted into a crystalline material through an anneal process (for example, from an initial amorphous state), i.e., to provide electrical conductivity greater than 1.0×10^{5} S/m. A "doped semiconductor material" may be a heavily doped semiconductor material, or may be a semiconductor material that includes electrical dopants (i.e., p-type dopants and/or n-type dopants) at a concentration that provides electrical conductivity in the range from 1.0×10^{-5} S/m to 1.0×10^{7} S/m. An "intrinsic semiconductor material" refers to a semiconductor material that is not doped with electrical dopants. Thus, a semiconductor material may be semiconducting or

conductive, and may be an intrinsic semiconductor material or a doped semiconductor material. A doped semiconductor material may be semiconducting or conductive depending on the atomic concentration of electrical dopants therein. As used herein, a "metallic material" refers to a conductive material including at least one metallic element therein . All measurements for electrical conductivities are made at the standard condition.

[0041] Generally, a semiconductor package (or a "package") refers to a unit semiconductor device that may be attached to a circuit board through a set of pins or solder balls. A semiconductor package may include a semiconductor chip (or a "chip") or a plurality of semiconductor chips that are bonded throughout, for example, by flip-chip bonding or another chip-to-chip bonding. A package or a chip may include a single semiconductor die (or a "die") or a plurality of semiconductor dies. A die is the smallest unit that may independently execute external commands or report status. Typically, a package or a chip with multiple dies is capable of simultaneously executing as many number of external commands as the total number of dies therein. Each die includes one or more planes. Identical concurrent operations may be executed in each plane within a same die, although there may be some restrictions. In case a die is a memory die, i.e., a die including memory elements, concurrent read operations, concurrent write operations, or concurrent erase operations may be performed in each plane within a same memory die. In a memory die, each plane contains a number of memory blocks (or "blocks"), which are the smallest unit that may be erased by in a single erase operation . Each memory block contains a number of pages, which are the smallest units that may be selected for programming. A page is also the smallest unit that may be selected to a read operation.

[0042] Referring to FIG. 1, an exemplary semiconductor die 1000 according to an embodiment of the present disclosure is illustrated. The exemplary semiconductor die 1000 includes multiple three-dimensional memory array regions and multiple contact regions. The first exemplary semiconductor die 1000 can include multiple planes, each of which includes two memory array regions 100, such as a first memory array region 100A and a second memory array region 100B that are laterally spaced apart by a respective contact region 200. Generally, a semiconductor die 1000 may include a single plane or multiple planes. The total number of planes in the semiconductor die 1000 may be selected based on performance requirements on the semiconductor die 1000. A pair of memory array regions 100 in a plane may be laterally spaced apart along a first horizontal direction hd1 (which may be the word line direction). For example, each pair of memory array regions 100 in a plane may include first memory array region 100A and a second memory array region 100B that are laterally spaced apart along the first horizontal direction hd1 by an contact region 200. A second horizontal direction hd2 (which may be the bit line direction) can be perpendicular to the first horizontal direction hd1. The exemplary

semiconductor die 1000 of FIG. 1 can be manufactured employing various embodiments of the present disclosure to be described below.

[0043] Referring to FIGS. 2A – 2D, an exemplary structure according to an embodiment of the present disclosure is illustrated. The exemplary structure comprises a substrate 8 including a substrate semiconductor layer 9. The substrate 8 may be a single crystalline silicon wafer, a silicon on insulator (SOI) substrate, or an insulating (e.g., glass or quartz) substrate. The substrate semiconductor layer 9 may be a single crystalline semiconductor material layer such as a single crystalline silicon layer that is epitaxially grown on a silicon wafer or SOI substrate, or a doped well in an upper portion of a silicon wafer or SOI substrate. Semiconductor devices 720 can be formed on the top surface of the substrate semiconductor layer 9. For example, the semiconductor devices 720 may include field effect transistors, resistors, capacitors, diodes, and/or various other semiconductor devices known in the art. In one embodiment, the semiconductor devices 720 may include a peripheral (i.e., driver) circuit for controlling the operation of three-dimensional memory arrays to be subsequently formed thereabove. Metal interconnect structures embedded in dielectric material layers can be formed above the semiconductor devices. The metal interconnect structures are herein referred to as lower-level metal interconnect structures 780, and the dielectric material layers are herein referred to as lower-level dielectric material layers 760 . The lower-level metal interconnect structures 780 are electrically connected to various nodes of the semiconductor devices 720, and can include metal line structures and metal via structures located at various levels of the lower-level dielectric material layers 760 .

[0044] A semiconductor material layer 110 can be formed on the top surface of the lower-level dielectric material layers 760. The semiconductor material layer 110 may be single crystalline or polycrystalline, and may be formed by a layer transfer from a source substrate (such as a single crystalline silicon layer including a buried hydrogen implantation layer), or may be formed by deposition of a semiconductor material (which may be a polycrystalline semiconductor material, such as polysilicon).

[0045] A first alternating stack of first insulating layers 132 and first sacrificial material layers 142 can be formed over the semiconductor material layer 110 . As used herein, an alternating stack refers to a sequence of multiple instances of a first element and multiple instances of a second element that is arranged such that an instance of the second element is located between each vertically neighboring pair of instances of the first element, and an instance of the first element is located between each vertically neighboring pair of instances of the second element . As such, instances of the first material layer and the instances of the second material layer are interlaced within an alternating stack.

[0046] The first insulating layers 132 may comprise, and/or may consist essentially of, the first material. The first sacrificial material layers 142 may comprise, and/or may consist essentially of, the second material, which is different from the first material . Each of the first insulating layers 132 continuously extends over the entire area of the substrate 8, and may have a uniform thickness throughout. Each of the first sacrificial material layers 142 continuously extends over the entire area of the substrate 8, and may have a uniform thickness throughout. Insulating materials that may be used for the first insulating layers 132 include, but are not limited to silicon oxide (including doped or undoped silicate glass), silicon nitride, silicon oxynitride, organosilicate glass (OSG), spin-on dielectric materials, dielectric metal oxides that are commonly known as high dielectric constant (high-k) dielectric oxides (e.g., aluminum oxide, hafnium oxide, etc.) and silicates thereof, dielectric metal oxynitrides and silicates thereof, and organic insulating materials. In one embodiment, the first material of the first insulating layers 132 may be silicon oxide.

[0047] The second material of the first sacrificial material layers 142 is a first-tier sacrificial material that may be removed selective to the first material of the first insulating layers 132. As used herein, a removal of a first material is "selective to" a second material if the removal process removes the first material at a rate that is at least twice the rate of removal of the second material. The ratio of the rate of removal of the first material to the rate of removal of the second material is herein referred to as a "selectivity" of the removal process for the first material with respect to the second material. The second material of the first sacrificial material layers 142 may be subsequently replaced with electrically conductive electrodes which may function, for example, as control gate electrodes of a vertical NAND device . In one embodiment, the first sacrificial material layers 142 may be material layers that comprise silicon nitride .

[0048] Each first insulating layer 132 may have a first thickness, which may be in a range from 15 nm to 60 nm, although lesser and greater thicknesses may also be employed. Each first sacrificial material layer 142 may have a second thickness, which may be in a range from 15 nm to 60 nm, although lesser and greater thicknesses may also be employed. The total number of repetitions of a pair of an first insulating layer 132 and a first sacrificial material layer 142 in the first alternating stack (132, 142) may be in a range from 16 to 1,024, such as from 64 to 512, although lesser and greater numbers may also be employed.

[0049] In an alternative embodiment, the semiconductor devices 720, the lower-level metal interconnect structures 780, and the lower-level dielectric material layers 760 may be located next to the first alternating stack (132, 142) over the substrate 8 rather than underneath the first alternating stack (132, 142). In yet another alternative embodiment, the semiconductor devices 720, the lower-level metal interconnect structures 780, and the lower-level dielectric material

layers 760 may be omitted and not formed over the substrate 8. Instead, the semiconductor devices 720 of the peripheral (i.e., driver) circuit may be formed over a separate substrate and then bonded over the three-dimensional memory device. Optionally, the semiconductor material layer 110 may also be omitted in case the substrate 8 is later removed and a top source contact layer is formed on an exposed surface of the memory device, or it may be modified to function as part of a lateral source contact (e.g., direct strap contact) which is subsequently formed under the alternating stack.

[0050] In case multiple tier structures are formed over the substrate 8, the first insulating layers 132 may be a first subset of insulating layers 32 that are formed over the substrate 8, and the first sacrificial material layers 142 may be a first subset of sacrificial material layers 42 that are formed over the substrate 8.

[0051] Multiple stepped surfaces S can be formed within the contact regions 200 simultaneously by patterning the first alternating stack (132, 142). In one embodiment, the pattern of the stepped surfaces S may be repeated along the second horizontal direction hd2 with a periodicity. In this case, a unit pattern can be formed within a unit area, and the unit pattern may be repeated along the second horizontal direction hd2 such that the lateral dimension of the unit pattern along the second horizontal direction hd2 is the same as periodicity of repetition of the unit pattern along the second horizontal direction hd2. The area of each unit pattern is herein referred to as a repetition unit RU.

[0052] In one embodiment, a hard mask layer (not shown) such as a metallic or dielectric mask material layer can be formed over the first alternating stack (132, 142), and can be patterned to form multiple rectangular openings. The areas of openings within the hard mask layer correspond to areas in which cavities 169 including stepped bottom surfaces are to be subsequently formed. Each opening through the hard mask layer may be rectangular, and may have a pair of sides that are parallel to the first horizontal direction (e.g., word line direction) hd1 and a pair of sides that are parallel to the second horizontal direction (e.g., bit line direction) hd2. The rectangular openings through the hard mask layer may be arranged along the second horizontal direction hd2, and may, or may not, be alternately staggered along the first horizontal direction hd1 .

[0053] A trimmable mask layer (not shown) can be applied over the alternating stack. The trimmable mask layer can include a trimmable photoresist layer that can be controllably trimmed by a timed ashing process. The trimmable mask layer can be patterned with an initial pattern such that a segment of each rectangular opening in the hard mask layer that is most proximal to the memory array regions 100 is not masked by the trimmable mask layer, while the rest of each rectangular opening is covered by the trimmable mask layer. For example, the trimmable mask

layer can have a rectangular shape having straight edges that are parallel to the second horizontal direction hd2, such that the straight edges are located over a vertical step of respective stepped surfaces S that is most proximal to one of the memory array regions 100.

[0054] The stepped surfaces S can be formed within the areas of the rectangular openings in the hard mask layer by iteratively performing a set of layer patterning processing steps. The set of layer patterning processing steps comprises an anisotropic etch process that etches unmasked portions of a pair of a first insulating layer 132 and a first sacrificial material layer 142, and a mask trimming process in which the trimmable mask layer is isotropically trimmed to provide shifted sidewalls that are shifted away from the most proximal memory array region 100. A final anisotropic etch process can be performed after the last mask trimming process, and the trimmable mask layer can be removed, for example, by ashing. The hard mask layer can be removed selective to the materials of the first alternating stack (132, 142), for example, by an isotropic etch process (such as a wet etch process). Alternatively, any other suitable process may be used to form the stepped surfaces.

[0055] A first cavity 169 having a respective stepped bottom surface can be formed within each area of the rectangular opening in the hard mask layer. Each first cavity 169 can include a cliff region in which a first end wall EW1 of the first alternating stack (32, 42) extends from the bottommost first sacrificial material layer 142 of the first alternating stack (132, 142) to the topmost layer of the first alternating stack (132, 142). The first end wall EW1 may be tapered (i.e., inclined) at an angle of 1 to 30 degrees along the first horizontal direction hd1 with respect to a vertical direction which is normal to the top surface of the substrate. Each first cavity 169 has stepped bottom surfaces. The stepped bottom surface of each cavity 169 laterally extend along the first horizontal direction hd1, and underlies the volume of the void of the first cavity 169. Generally, the stepped surfaces S can be formed by patterning the first alternating stack (132, 142) in each contact region 200, which is located between a respective first memory array region 100A and a second memory array region 100B.

[0056] Generally, each first cavity 169 may have stepped surfaces S including vertically-extending surface segments that are interlaced with horizontally-extending surface segments which form the bottom surface of the first cavity 169. Further, each first cavity 169 may comprise a pair of first tapered (e.g., inclined) sidewalls TS1 that are parallel to the first horizontal direction hd1, laterally spaced from each other along the second horizontal direction hd2, and having a respected stepped bottom end adjoined to a respective stepped periphery of the stepped bottom surface. The first tapered sidewalls TS1 may be tapered (i.e., inclined) at an angle of 5 to 45 degrees with respect to the vertical direction. The lateral distance between the pair of first tapered sidewalls TS1 along the second horizontal direction hd2 is the width of a

respective first cavity 169, which increases with a vertical distance from the substrate 8.

[0057] Referring to FIGS. 3A – 3E, a first insulating liner 160 can be conformally deposited over the underlying structure. The first insulating liner 160 comprises an insulating material, such as silicon oxide. The material of the first insulating liner 160 is different from the material of the first sacrificial material layers 142. The first insulating liner 160 is deposited over the stepped surfaces S of the first alternating stack (132, 142), over each first tapered sidewall TS1 of the first alternating stack (132, 142), and over the topmost layer of the first alternating stack (132, 142). The thickness of the first insulating liner 160 may be in a range from 50 nm to 200 nm, such as from 100 nm to 150 nm, although lesser and greater thicknesses may also be employed.

[0058] A photoresist layer (not illustrated) can be formed over the first insulating liner 160, and can be lithographically patterned to form an elongated opening, such as a rectangular opening, the straddles a middle portion of a stepped bottom surface of a respective first cavity 169. In one embodiment, the width of rectangular opening along the second horizontal direction hd2 is less than the width of the bottommost horizontal surface of the stepped bottom surface. In one embodiment, each horizontal surface segment of the stepped bottom surface may have two horizontal surface segments that are not covered by the patterned photoresist layer and are laterally spaced apart along the second horizontal direction hd2. An etch process can be performed to etch unmasked portions of the first insulating liner 160. The etch process may process may comprise an isotropic etch process or an anisotropic etch process. An elongated opening is formed through the first insulating liner 160 within the area of each first cavity 169. A strip segment of the stepped surfaces S is exposed through the elongated opening through the first insulating liner 160 underneath a first cavity 169 that is present within the volume of a respective first cavity 169 .

[0059] In one embodiment, the elongated opening through the first insulating liner 160 laterally extends along a first horizontal direction hd1, and may have a uniform width along the second horizontal direction hd2. In one embodiment, each first insulating liner 160 includes a first horizontally-extending portion overlying the first alternating stack (132, 142), and a plurality of tapered vertically-extending portions that overlie a respective first tapered sidewall TS1. In one embodiment, each first insulating liner 160 includes a plurality of second horizontally-extending portions overlying a bottom surface of a respective first cavity 169 within an array of first cavities 169. A pair of second horizontally-extending portions of a first insulating liner 160 may contact segments of a respective top surface of a first sacrificial material layer 142, and may be laterally spaced apart from each other by a rectangular region of an opening through the first insulating liner 160.

[0060] Referring to FIGS. 4A – 4E, a first sacrificial liner material can be conformally deposited over the first insulating liner 160, and can be subsequently patterned to form a first sacrificial liner 182. The first sacrificial liner material comprises a material that can be subsequently removed selective to materials of the first insulating layers 132 and the first insulating liner 160. In one embodiment, the first sacrificial liner material may be the same as the first-tier sacrificial material of the first sacrificial material layers 142. In one embodiment, the first sacrificial liner 182 may comprise or may consist essentially of silicon nitride. The thickness of each first sacrificial liner 182 may be in a range from 10 nm to 50 nm, such as from 15 nm to 30 nm, although lesser and greater thicknesses may also be employed.

[0061] Within an area of each repetition unit RU, a first sacrificial liner 182 may be formed such that the entirety of the physically exposed sidewalls of the first sacrificial liner 182 is formed above the horizontal plane including the topmost surface of the first alternating stack (132, 142). In other words, the end portions of the first sacrificial liner 182 extend over the tapered sidewalls TS1 and over the top of the first alternating stack (132, 142) along the second horizontal direction hd2. Thus, the first sacrificial liner 182 may have a longer length along the second horizontal direction hd2 than the length of the underlying first cavity 169 along the second horizontal direction hd2. The first sacrificial liner 182 may have the same, shorter or longer length along the first horizontal direction hd1 compared to the length of the underlying first cavity 169 along the first horizontal direction hd1. The first cavity 169 is present within the volume that is laterally enclosed by the first sacrificial liner 182. The first sacrificial liner 182 can be formed directly on the physically exposed portion of the stepped surfaces S of the first alternating stack (132, 142) such that each first sacrificial layer 142 comprises a respective horizontal top surface segment HS1 that contacts a respective bottom surface segment BP1 of the first sacrificial liner 182. As shown in FIG. 4C, the first sacrificial liner 182 comprises a horizontally-extending top portion TP1 that overlies the first alternating stack (132, 142) and overlies a horizontally-extending top portion of the first insulating liner 160 . In one embodiment, the first insulating liner 160 contacts the entirety of a pair of first tapered sidewalls TS1 and a first end wall EW1, and the first sacrificial liner 182 is spaced from the pair of first tapered sidewalls TS1 and the first end wall EW1 by the first insulating liner 160.

[0062] Referring to FIGS. 5A – 5E, a first dielectric fill material, such as undoped silicate glass (i.e., silicon oxide) or a doped silicate glass, can be deposited over the first sacrificial liner 182 and the first alternating stack (132, 142) to fill the first cavity 169. A planarization process, such as a chemical mechanical polishing process, can be performed to remove potions of the first dielectric fill material from above the horizontal plane including the topmost surface of the first sacrificial liner 182. The first sacrificial liner 182 may be employed as an endpoint detection

structure and/or as a planarization stopping structure. Each remaining portion of the first dielectric fill material that fills a respective first cavity 169 constitutes a first dielectric fill structure 165. A continuous remaining portion the first dielectric fill material that overlies the top surface of the horizontally-extending portion of the first insulating liner 160 above the first alternating stack (132, 142) constitutes a first insulating cap layer 170. A first-tier structure is thus formed over the semiconductor material layer 110. The first-tier structure comprises all material portions that are located above the semiconductor material layer 110 at this processing step.

[0063] Referring to FIGS. 6A – 6E, a first etch mask layer (not shown) can be formed over the first insulating cap layer 170 and the first dielectric fill structures 165, and can be lithographically patterned to form various discrete openings therein. A first anisotropic etch process can be performed to transfer the pattern of the discrete openings in the first etch mask layer through the first insulating cap layer 170, the first alternating stack (132, 142), and the first dielectric fill structures 165. Various openings can be formed through the first insulating cap layer 170, the first alternating stack (132, 142), and the first dielectric fill structures 165. The various openings may comprise first-tier memory openings 149 that are formed in the memory array regions 100 and first-tier support openings 119 that are formed in the contact region 200. Each of the first-tier memory openings 149 and the first-tier support openings 119 can vertically extend through the first alternating stack (132, 142) and into the semiconductor material layer 110.

[0064] In one embodiment, the memory array regions 100 may be laterally spaced apart from the contact region 300 along a first horizontal direction hd1. The first-tier memory openings 149 may comprise rows of first-tier memory openings 149 that are arranged along the first horizontal direction hd1 and laterally spaced apart along a second horizontal direction hd2 that is perpendicular to the first horizontal direction hd2. Each area of a memory array region 100 located within a repetition unit RU includes a respective two-dimensional array of first-tier memory openings 149 that are arranged as a cluster. Neighboring clusters of first-tier memory openings 149 may be laterally spaced apart along the second horizontal direction hd2 .

[0065] In one embodiment, the first-tier support openings 119 in the contact region 200 may be arranged as two-dimensional periodic arrays of first-tier support openings 119 located within a respective one of the repetition units RU. In one embodiment, each two-dimensional periodic array of first-tier support openings 119 may be a respective rectangular periodic array of first-tier support openings 119.

[0066] In one embodiment, the first-tier support openings 119 in the contact region 200 may be elongated along the second horizontal direction hd2. In another embodiment, the first-tier

support openings 119 in the contact region 200 may have a circular horizontal cross-section. In one embodiment, columns of first-tier support openings 119 arranged along the second horizontal direction hd2 may cut through a respective vertically-extending straight surface segment of a stepped bottom surface of the first alternating stack (132, 142) . The vertically-extending straight surface segment can be perpendicular to the first horizontal direction hd1.

[0067] Referring to FIGS. 7A – 7E, an optional etch stop liner (not shown) and a first sacrificial fill material can be deposited in the first-tier memory openings 149 and the first-tier support openings 129. The optional etch stop liner (if present) comprises a thin silicon oxide layer having a thickness in a range from 1 nm to 6 nm. The first sacrificial fill material may comprise a carbon-based material, such as amorphous carbon or diamond-like carbon, or a semiconductor material, such as amorphous silicon. Excess portions of the first sacrificial fill material that overlies the horizontal plane including the top surface of the first insulating cap layer 170 may be removed by a planarization process, which may employ a recess etch process or a chemical mechanical polishing process. Each remaining portion of the first sacrificial fill material that fills a first-tier memory openings 149 constitute a first-tier sacrificial memory opening fill material portion 148. Each remaining portion of the first sacrificial fill material that fills a first-tier support opening 119 constitutes a first-tier sacrificial support opening fill material portion 118.

[0068] Referring to FIGS. 8A – 8E, a second alternating stack of second insulating layers 232 and second sacrificial material layers 242 can be formed over the first-tier structure . The second insulating layers 232 may comprise and/or may consist essentially of the same material as the first insulating layers 132. The second sacrificial material layers 242 may comprise and/or may consist essentially of the same material as the first sacrificial material layers 142 . Each of the second insulating layers 232 continuously extends over the entire area of the substrate 8, and may have a uniform thickness throughout. Each of the second sacrificial material layers 242 continuously extends over the entire area of the substrate 8, and may have a uniform thickness throughout .

[0069] The thickness range for the second insulating layers 232 may be the same as the thickness range for the first insulating layers 132. The thickness range for the second sacrificial material layers 242 may be the same as the thickness range for the first sacrificial material layers 142. The total number of repetitions of a pair of an second insulating layer 232 and a second sacrificial material layer 242 in the second alternating stack (232, 242) may be in a range from 26 to 1,024, such as from 64 to 512, although lesser and greater numbers may also be employed . The second insulating layers 232 are a second subset of the insulating layers 32 that are formed over the substrate 8, and the second sacrificial material layers 242 are a second subset of the

sacrificial material layers 42 that are formed over the substrate 8.

[0070] Multiple stepped surfaces S can be formed within the contact regions 200 simultaneously by patterning the second alternating stack (232, 242). In one embodiment, a hard mask layer (not shown) such as a metallic or dielectric mask material layer can be formed over the second alternating stack (232, 242), and can be patterned to form multiple rectangular openings. The areas of openings within the hard mask layer correspond to areas in which cavities 269 including stepped bottom surfaces are to be subsequently formed. Each opening through the hard mask layer may be rectangular, and may have a pair of sides that are parallel to the second horizontal direction hd2 and a pair of sides that are parallel to the second horizontal direction hd2. The rectangular openings through the hard mask layer may be arranged along the second horizontal direction hd2, and may, or may not, be alternately staggered along the second horizontal direction hd2 .

[0071] A trimmable mask layer (not shown) can be applied over the second alternating stack. The trimmable mask layer can include a trimmable photoresist layer that can be controllably trimmed by a timed ashing process. The trimmable mask layer can be patterned with an initial pattern such that a segment of each rectangular opening in the hard mask layer that is most proximal to a memory array regions 100 is not masked by the trimmable mask layer, while the rest of each rectangular opening is covered by the trimmable mask layer. For example, the trimmable mask layer can have a rectangular shape having straight edges that are parallel to the second horizontal direction hd2, such that the straight edges are located over a vertical step of respective stepped surfaces that is most proximal to one of the memory array regions 200 .

[0072] The stepped surfaces S can be formed within the areas of the rectangular openings in the hard mask layer by iteratively performing a set of layer patterning processing steps. The set of layer patterning processing steps comprises an anisotropic etch process that etches unmasked portions of a pair of a second insulating layer 232 and a second sacrificial material layer 242, and a mask trimming process in which the trimmable mask layer is isotropically trimmed to provide shifted sidewalls that are shifted away from the most proximal memory array region 200. A final anisotropic etch process can be performed after the last mask trimming process, and the trimmable mask layer can be removed, for example, by ashing. The hard mask layer can be removed selective to the materials of the second alternating stack (32, 42), for example, by an isotropic etch process (such as a wet etch process). Alternatively, any other suitable process may be used to form the stepped surfaces.

[0073] A second cavity 269 having a respective stepped bottom surface can be formed within each area of the rectangular opening in the hard mask layer. Each second cavity 269 can include a cliff region in which a second end wall EW2 of the second alternating stack (32, 42) extends

from the bottommost layer of the second alternating stack (232, 242) to the topmost layer of the second alternating stack (232, 242). The second end wall EW1 may be tapered (i.e., inclined) at an angle of 1 to 30 degrees with respect to the vertical direction. Each second cavity 269 has stepped bottom surfaces. The stepped bottom surface of each cavity 269 laterally extend along the second horizontal direction hd2, and underlies the volume of the void of the second cavity 269. Generally, the stepped surfaces S can be formed by patterning the second alternating stack (232, 242) in each contact region 200, which is located between a respective first memory array region 100A and a second memory array region 100B. All layers of the second alternating stack (232, 242) may be removed within the area that overlies the underlying first dielectric fill structure 165 . In one embodiment, the entirety of the top surface of a first dielectric fill structure may be physically exposed upon formation of the second cavities 269.

[0074] Generally, each second cavity 269 may have stepped surfaces S including vertically-extending surface segments that are interlaced with horizontally-extending surface segments which form the bottom surface of the second cavity 269. Further, each second cavity 269 may comprise a pair of second tapered (e.g., inclined) sidewalls TS2 that are parallel to the first horizontal direction hd1, laterally spaced from each other along the second horizontal direction hd2, and having a respected stepped bottom end adjoined to a respective stepped periphery of the stepped bottom surface. The second tapered sidewalls TS2 may be tapered (i.e., inclined) at an angle of 5 to 45 degrees with respect to the vertical direction. The lateral distance between the pair of second tapered sidewalls TS2 along the second horizontal direction hd2 is the width of a respective second cavity 269, which increases with a vertical distance from the substrate 8.

[0075] In summary, at least one alternating stack of insulating layers 32 and first-tier sacrificial material layers 42 can be formed, and at least one cavity (169, 269) can be formed through the at least one alternating stack (32, 42). The combination of the first alternating stack (132, 142) and the second alternating stack (232, 242) constitutes another alternating stack of a greater height, which may be referred to as an alternating stack (32, 42) of insulating layers 32 and first-tier sacrificial material layers 42. The horizontal plane including the topmost surface of the alternating stack (32, 42) is herein referred to as a first horizontal plane HP1, and the horizontal plane including the bottommost surface of the alternating stack (32, 42) is herein referred to as a second horizontal plane HP2.

[0076] A cavity (169, 269) can be formed in the alternating stack (32, 42) such that stepped surfaces S of the alternating stack (32, 42) are exposed underneath the cavity (169, 269). The alternating stack (32, 42) comprises tapered sidewalls (TS1, TS2) that laterally extend along a first horizontal direction hd1 in the contact region 200.

[0077] Referring to FIGS. 9A – 9E, a second insulating liner 260 can be conformally

deposited over the underlying structure. The second insulating liner 260 comprises an insulating material such as silicon oxide. The material of the second insulating liner 260 is different from the material of the second sacrificial material layers 242. The second insulating liner 260 is deposited over the stepped surfaces of the second alternating stack (232, 242), over each second tapered sidewall TS2 of the second alternating stack (232, 242), and over the topmost layer of the second alternating stack (232, 242). The thickness of the second insulating liner 260 may be in a range from 50 nm to 200 nm, such as from 100 nm to 150 nm, although lesser and greater thicknesses may also be employed.

[0078] A photoresist layer (not illustrated) can be formed over the second insulating liner 260, and can be lithographically patterned to form an opening that laterally extends through the entire lateral extent of the stepped surfaces of the second alternating stack (232, 242) and an underlying first dielectric fill structure 165. An etch process can be performed to etch unmasked portions of the second insulating liner 260. The etch process may process may comprise an isotropic etch process or an anisotropic etch process. An opening is formed through the second insulating liner 260 within the area of each second cavity 269. The opening may comprise a first rectangular area overlying the stepped surfaces of the second alternating stack (232, 242) and a second rectangular area under which a horizontally-extending portion of the first sacrificial liner 182 that overlies the first alternating stack (132, 142) and an entirety of the top surface of an underlying first dielectric fill structure 165 is exposed. A strip segment of the stepped surfaces of the second alternating stack (232, 242) is exposed through the elongated opening through the second insulating liner 260 underneath a second cavity 269 that is present within the volume of a respective second cavity 269. The physically exposed surface of the first sacrificial liner 182 may have a general shape of a rectangular frame, i.e., the shape of a first rectangle from which an area of a smaller second rectangle is subtracted such that an outer rectangular periphery of the shape is spaced from an inner rectangular periphery of the shape.

[0079] In one embodiment, the portion of the opening through the second insulating liner 260 that overlies the stepped surfaces of the second alternating stack (232, 242) laterally extends along the second horizontal direction hd2, and may have a uniform width along the second horizontal direction hd2. In one embodiment, each second insulating liner 260 includes a first horizontally-extending portion overlying the second alternating stack (232, 242), and a plurality of tapered vertically-extending portions that overlie a respective second tapered sidewall TS2. In one embodiment, each second insulating liner 260 includes a plurality of second horizontally-extending portions overlying a bottom surface of a respective second cavity 269 within an array of second cavities 269. A pair of second horizontally-extending portions of a second insulating liner 260 may contact segments of a respective top surface of a second sacrificial material layer

242, and may be laterally spaced apart from each other by a rectangular region of an opening through the second insulating liner 260.

[0080] Referring to FIGS. 10A – 10E, a second sacrificial liner material can be conformally deposited over the second insulating liner 160, and can be subsequently patterned to form a second sacrificial liner 282. The second sacrificial liner material comprises a material that can be subsequently removed selective to materials of the second insulating layers 232 and the second insulating liner 260. In one embodiment, the second sacrificial liner material may be the same as the first-tier sacrificial material of the second sacrificial material layers 242. In one embodiment, the second sacrificial liner 282 may comprise or may consist essentially of silicon nitride. The thickness of each second sacrificial liner 282 may be in a range from 10 nm to 50 nm, such as from 15 nm to 30 nm, although lesser and greater thicknesses may also be employed.

[0081] Within an area of each repetition unit RU, a second sacrificial liner 282 may be formed such that the entirety of the physically exposed sidewalls of the second sacrificial liner 282 is formed above the horizontal plane including the topmost surface of the second alternating stack (232, 242). In other words, the end portions of the second sacrificial liner 282 extend over the tapered sidewalls TS2 and over the top of the second alternating stack (232, 242) along the second horizontal direction hd2. Thus, the second sacrificial liner 282 may have a longer length along the second horizontal direction hd2 than the length of the underlying second cavity 269 along the second horizontal direction hd2. The second sacrificial liner 282 may have the same, shorter or longer length along the first horizontal direction hd1 compared to the length of the underlying second cavity 269 along the first horizontal direction hd1. The second cavity 269 is present within the volume that is laterally enclosed by the second sacrificial liner 282. The second sacrificial liner 282 can be formed directly on the physically exposed portion of the stepped surfaces S of the second alternating stack (232, 242) such that each second sacrificial layer 242 comprises a respective horizontal top surface segment HS2 that contacts a respective bottom surface segment BP1 of the second sacrificial liner 282, as shown in FIG. 10D. The second sacrificial liner 282 comprises a horizontally-extending top portion TP2 that overlies the second alternating stack (232, 242) and overlies a horizontally-extending top portion of the second insulating liner 260 . In one embodiment, the second insulating liner 260 contacts the entirety of a pair of second tapered sidewalls TS2 and a second end wall EW2, and the second sacrificial liner 282 is spaced from the pair of second tapered sidewalls TS2 and the second end wall EW2 by the second insulating liner 260.

[0082] Referring to FIGS. 11A – 11E, a second dielectric fill material, such as undoped silicate glass or a doped silicate glass, can be deposited over the second sacrificial liner 282 and the second alternating stack (232, 242) to fill the second cavity 269. A planarization process such

as a chemical mechanical polishing process can be performed to remove potions of the second dielectric fill material from above the horizontal plane including the topmost surface of the second sacrificial liner 282. The second sacrificial liner 282 may be employed as an endpoint detection structure and/or as a planarization stopping structure. Each remaining portion of the second dielectric fill material that fills a respective second cavity 269 constitutes a second dielectric fill structure 265. A continuous remaining portion the second dielectric fill material that overlies the top surface of the horizontally-extending portion of the second insulating liner 260 above the second alternating stack (232, 242) constitutes a second insulating cap layer 270. A second-tier structure is thus formed over the first-tier structure. The second-tier structure comprises all material portions that are located above the first-tier structure at this processing step.

[0083] Referring to FIGS. 12A – 12E, a second etch mask layer (not shown) can be formed over the second insulating cap layer 270 and the second dielectric fill structures 265, and can be lithographically patterned to form various discrete openings therein. The pattern of the openings in the second etch mask layer can be the same as the pattern of the first-tier memory openings 149 and the first-tier support openings 119. A second anisotropic etch process can be performed to transfer the pattern of the discrete openings in the second etch mask layer through the second insulating cap layer 270, the second alternating stack (232, 242), and the second dielectric fill structures 265. Various openings can be formed through the second insulating cap layer 270, the second alternating stack (232, 242), and the second dielectric fill structures 265. The various openings may comprise second-tier memory openings 249 that are formed in the memory array regions 100, and second-tier support openings 219 that are formed in the contact region 200. Each of the second-tier memory openings 249 can be formed directly on a top surface of a respective one of the first-tier sacrificial memory opening fill portions 148. Each of the second-tier support openings 219 can be formed directly on a top surface of a respective one of the first-tier sacrificial support opening fill portions 118 .

[0084] The second-tier memory openings 249 may comprise rows of second-tier memory openings 249 that are arranged along the first horizontal direction hd1 and laterally spaced apart along the second horizontal direction hd2. Each area of a memory array region 100 located within a repetition unit RU includes a respective two-dimensional array of second-tier memory openings 249 that are arranged as a cluster. Neighboring clusters of second-tier memory openings 249 may be laterally spaced apart along the second horizontal direction hd2 .

[0085] In one embodiment, the second-tier support openings 219 in the contact region 200 may be arranged as two-dimensional periodic arrays of second-tier support openings 219 located within a respective one of the repetition units RU. In one embodiment, each two-dimensional

periodic array of second-tier support openings 219 may be a respective rectangular periodic array of second-tier support openings 219.

[0086] In one embodiment, the second-tier support openings 219 in the contact region 200 may be elongated along the second horizontal direction hd2. In another embodiment, the second-tier support openings 219 in the contact region 200 may have a circular horizontal cross-section. In one embodiment, columns of second-tier support openings 219 arranged along the second horizontal direction hd2 may cut through a respective vertically-extending straight surface segment of a stepped bottom surface of the second alternating stack (232, 242) . The vertically-extending straight surface segment can be perpendicular to the first horizontal direction hd1.

[0087] The first-tier sacrificial memory opening fill structures 148 and the first-tier sacrificial support opening fill structures 118 can be subsequently removed by ashing or selective etching selective to the materials of the first alternating stack (132, 142), the second alternating stack (232, 242), the dielectric fill structures (165, 265), the insulating liners (160, 260), the sacrificial liners (182, 282), and the semiconductor material layer 110. A muti-tier memory opening 49, which is also referred to as a memory opening 49, are formed in each contiguous volume that includes a volume of a second-tier memory opening 249 and a volume of a first-tier memory opening 149. A multi-tier support opening 19, which is also referred to as a support opening 19, is formed in each continuous volume that includes a volume of a second-tier support opening 219 and a volume of a first-tier support opening 119.

[0088] Referring to FIGS. 13A – 13E, a sacrificial fill material, such as amorphous carbon or amorphous silicon can be deposited in the memory openings 49 and in the support openings 19. Excess portions of the sacrificial fill material can be removed from above the horizontal plane including the top surface of the second insulating cap layer 270. Each remaining portion of the sacrificial fill material that fills a respective memory opening 49 constitutes a sacrificial memory opening fill structure 48. Each remaining portion of the sacrificial fill material that fills a respective support opening 19 constitutes a sacrificial support opening fill structure 18. The sacrificial support opening fill structures 18 may be arranged as columns of sacrificial support opening fill structures 18 that extend through a respective vertically-extending sidewall of the stepped surfaces of the alternating stack (32, 42) that is perpendicular to the first horizontal direction hd1 . Alternatively, instead of removing the first-tier sacrificial memory opening fill structures 148 and the first-tier sacrificial support opening fill structures 118 at the step shown in FIGS. 12A – 12E, additional sacrificial fill material may be deposited into the second-tier memory openings 249 and the second-tier support openings 219 over the respective first-tier sacrificial memory opening fill structures 148 and the first-tier sacrificial support opening fill structures 118 to form the above described sacrificial memory opening fill structures 48 and

sacrificial support opening fill structures 18.

[0089] Referring to FIGS. 14A – 14E, a sacrificial etch mask layer (not shown) can be applied over the exemplary structure, and can be lithographically patterned to cover the memory array regions 100 without covering the contact region 200. The sacrificial etch mask layer may comprise a silicon oxide layer or a silicon nitride layer having a thickness in a range from 10 m to 50 nm, although lesser and greater thicknesses may also be employed. The sacrificial opening fill structures 18 can be removed from inside the volumes of the support openings 19, for example, by ashing or selective etching .

[0090] A dielectric fill material, such as silicon oxide, can be deposited in the voids within the support openings 19. Excess portions of the dielectric fill material can be removed from above the horizontal plane including the top surface of the second insulating cap layer 270 by performing a planarization process such as a chemical mechanical polishing process or a recess etch process. The sacrificial etch mask layer can be collaterally removed during removal of the dielectric fill material from above the horizontal plane including the top surface of the second insulating cap layer 270. Each remaining portion of the dielectric fill material that fills the support openings 19 constitutes a support pillar structure 20. In one embodiment, a two-dimensional array of support pillar structures 20 may be formed in the contact region 200. The two-dimensional array of support pillar structures 20 may comprise columns of support pillar structures 20 each arranged along the second horizontal direction hd2 and vertically extending through a respective vertically-extending planar surface of the stepped surfaces of the first alternating stack (132, 142) or the second alternating stack (232, 242) that is perpendicular to the first horizontal direction hd1. At this processing step, the first sacrificial liner 182 is a unitary structure (i.e., a single continuous structure in which each point can be continuously connected to any other point through a respective path contained entirely within the volume of the single continuous structure) through which columns of support pillar structures 20 vertically extend. Likewise, the second sacrificial liner 282 is a unitary structure through which columns of support pillar structures 20 vertically extend.

[0091] Referring to FIGS. 15A – 15E, the sacrificial memory opening fill structures 48 can be removed from inside the memory openings 49, for example, by performing an ashing process or a selective etching process. Cavities are formed in the volumes of the memory openings 49.

[0092] FIGS. 16A – 16F are sequential vertical cross-sectional views of an inter-tier memory opening 49 during formation of a memory opening fill structure 58 according to an embodiment of the present disclosure.

[0093] Referring to FIG. 16A, a memory opening 49 is illustrated after removal of a sacrificial memory opening fill structure 48. The memory opening 49 extends through the

alternating stack {(132, 142), (232, 242)} and optionally into an upper portion of the semiconductor material layer 110 . The recess depth of the bottom surface of each memory opening 49 with respect to the top surface of the semiconductor material layer 110 can be in a range from 0 nm to 30 nm, although greater recess depths can also be employed. Optionally, the sacrificial material layers 42 can be laterally recessed partially to form laterally-extending cavities (not shown), for example, by an isotropic etch .

[0094] An optional pedestal channel portion 11 (which may be a silicon pedestal) can be formed at the bottom portion of each memory opening 49, for example, by a selective semiconductor deposition process. In one embodiment, the pedestal channel portion 11 can be doped with electrical dopants of the same conductivity type as the semiconductor material layer 110, which is a first conductivity type. In one embodiment, the top surface of each pedestal channel portion 11 can be formed below a horizontal plane including the top surface of the bottommost insulating layer 32. The pedestal channel portion 11 can be a portion of a transistor channel that extends between a source region to be subsequently formed in the semiconductor material layer 110 and a drain region to be subsequently formed in an upper portion of the memory opening 49. A memory cavity 49' is present in the unfilled portion of the memory opening 49 above the pedestal channel portion 11 .

[0095] Referring to FIG. 16B, a stack of layers including a blocking dielectric layer 52, a memory material layer 54, and an optional dielectric liner 56 can be deposited in each memory opening 49. The stack of layers is herein referred to as a memory film 50.

[0096] The blocking dielectric layer 52 can include a single dielectric material layer or a stack of a plurality of dielectric material layers. In one embodiment, the blocking dielectric layer 52 can include a dielectric metal oxide layer consisting essentially of a dielectric metal oxide. In one embodiment, the blocking dielectric layer 52 can include a dielectric metal oxide having a dielectric constant greater than 7.9, i.e., having a dielectric constant greater than the dielectric constant of silicon nitride. Alternatively or additionally, the blocking dielectric layer 52 can include a dielectric semiconductor compound such as silicon oxide, silicon oxynitride, silicon nitride, or a combination thereof. In one embodiment, the blocking dielectric layer 52 can include silicon oxide. In this case, the dielectric semiconductor compound of the blocking dielectric layer 52 can be formed by a conformal deposition method such as low pressure chemical vapor deposition, atomic layer deposition, or a combination thereof. The thickness of the dielectric semiconductor compound can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0097] The memory material layer 54 may comprise any memory material such as a charge storage material, a ferroelectric material, a phase change material, or any material that can store

data bits in the form of presence or absence of electrical charges, a direction of ferroelectric polarization, electrical resistivity, or another measurable physical parameter. In one embodiment, the memory material layer 54 can be a continuous layer or patterned discrete portions of a charge trapping material including a dielectric charge trapping material, which can be, for example, silicon nitride. Alternatively, the memory material layer 54 can include a continuous layer or patterned discrete portions of a conductive material such as doped polysilicon or a metallic material that is patterned into multiple electrically isolated portions (e.g., floating gates), for example, by being formed within laterally-extending cavities into sacrificial material layers 42. In one embodiment, the memory material layer 54 includes a silicon nitride layer. In one embodiment, the sacrificial material layers 42 and the insulating layers 32 can have vertically coincident sidewalls, and the memory material layer 54 can be formed as a single continuous layer. Generally, the memory material layer 54 may comprise vertical stack of memory elements that are located at levels of the sacrificial material layers 42. For example, the vertical stack of memory elements may be embodied as annular portions of the memory material layer 54 located at levels of the sacrificial material layers 42.

[0098] The optional dielectric liner 56, if present, comprises a dielectric liner material. In one embodiment, the dielectric liner 56 may comprise a tunneling dielectric layer through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-dimensional NAND string memory device to be formed. The dielectric liner 56 can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the dielectric liner 56 can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO stack. In one embodiment, the dielectric liner 56 can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the dielectric liner 56 can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0099] Optionally, a sacrificial cover material layer 601 may be formed over the memory film 50. Referring to FIG. 16C, the optional sacrificial cover material layer 601, the dielectric liner 56, the memory material layer 54, the blocking dielectric layer 52 are sequentially anisotropically etched employing at least one anisotropic etch process. The portions of the sacrificial cover material layer 601, the dielectric liner 56, the memory material layer 54, and the

blocking dielectric layer 52 located above the top surface of the second insulating cap layer 270 can be removed by the at least one anisotropic etch process.

[0100] Further, the horizontal portions of the sacrificial cover material layer 601, the dielectric liner 56, the memory material layer 54, and the blocking dielectric layer 52 at a bottom of each memory cavity 49' can be removed to form openings in remaining portions thereof. Each of the sacrificial cover material layer, the dielectric liner 56, the memory material layer 54, and the blocking dielectric layer 52 can be etched by a respective anisotropic etch process employing a respective etch chemistry, which may or may not be the same for the various material layers.

[0101] Each remaining portion of the sacrificial cover material layer 601, if employed, can have a tubular configuration . A surface of the pedestal channel portion 11 (or a surface of the semiconductor material layer 110 in case a pedestal channel portions 11 is not employed) can be physically exposed underneath the opening through the sacrificial cover material layer, the dielectric liner 56, the memory material layer 54, and the dielectric metal oxide blocking dielectric layer 52. Optionally, the physically exposed semiconductor surface at the bottom of each memory cavity 49' can be vertically recessed so that the recessed semiconductor surface underneath the memory cavity 49' is vertically offset from the topmost surface of the pedestal channel portion 11 (or of the semiconductor material layer 110 in case pedestal channel portions 11 are not employed) by a recess distance. In one embodiment, the sacrificial cover material layer 601, the dielectric liner 56, the memory material layer 54, and the blocking dielectric layer 52 can have vertically coincident sidewalls . The sacrificial cover material layer 601 can be subsequently removed selective to the material of the dielectric liner 56. In case the sacrificial cover material layer 601 includes amorphous silicon, a wet etch process employing hot trimethyl-2 hydroxyethyl ammonium hydroxide ("hot TMY") or tetramethyl ammonium hydroxide (TMAH) can be performed to remove the sacrificial cover material layer. Alternatively, the sacrificial cover material layer 601 may be retained in the final device if it comprises a silicon material.

[0102] Referring to FIG. 16D, a semiconductor channel layer 60L can be deposited directly on the semiconductor surface of the pedestal channel portion 11 or the semiconductor material layer 110 if the pedestal channel portion 11 is omitted, and directly on the memory film 50. The semiconductor channel layer 60L includes a semiconductor material such as at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. In one embodiment, the semiconductor channel layer 60L includes amorphous silicon or polysilicon. The semiconductor channel layer 60L can have a doping of a first conductivity type, which is the same as the conductivity type of the

semiconductor material layer 110 and the pedestal channel portions 11. The semiconductor channel layer 60L can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the semiconductor channel layer 60L can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. The semiconductor channel layer 60L may partially fill the memory cavity 49' in each memory opening, or may fully fill the cavity in each memory opening .

[0103] Referring to FIG. 16E, a dielectric core layer can be deposited to fill any remaining portion of the memory cavity 49' within each memory opening 49. The dielectric core layer includes a dielectric material such as silicon oxide or organosilicate glass. The dielectric core layer can be deposited by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD), or by a self-planarizing deposition process such as spin coating.

[0104] The horizontal portion of the dielectric core layer can be removed, for example, by a recess etch process such that each remaining portions of the dielectric core layer is located within a respective memory opening 49 and has a respective top surface below the horizontal plane including the top surface of the second insulating cap layer 270. Each remaining portion of the dielectric core layer constitutes a dielectric core 62.

[0105] Referring to FIG. 16F, a doped semiconductor material having a doping of a second conductivity type can be deposited within each recessed region above the dielectric cores 62. The deposited semiconductor material can have a doping of a second conductivity type that is the opposite of the first conductivity type. For example, if the first conductivity type is p-type, the second conductivity type is n-type, and vice versa. The dopant concentration in the deposited semiconductor material can be in a range from 5.0 x 1018/cm3 to 2.0 x 1021/cm3, although lesser and greater dopant concentrations can also be employed. The doped semiconductor material can be, for example, doped polysilicon.

[0106] Excess portions of the deposited semiconductor material having a doping of the second conductivity type and a horizontal portion of the semiconductor channel layer 60L can be removed from above the horizontal plane including the top surface of the second insulating cap layer 270, for example, by chemical mechanical planarization (CMP) or a recess etch process. Each remaining portion of the doped semiconductor material having a doping of the second conductivity type constitutes a drain region 63. Each remaining portion of the semiconductor channel layer 60L (which has a doping of the first conductivity type) constitutes a vertical semiconductor channel 60.

[0107] Each combination of a memory film 50 and a vertical semiconductor channel 60 within a memory opening 49 constitutes a memory stack structure 55. The memory stack structure 55 is a combination of a vertical semiconductor channel 60, an optional dielectric liner

56, a plurality of memory elements comprising portions of the memory material layer 54, and an optional blocking dielectric layer 52. Each combination of a pedestal channel portion 11 (if present), a memory stack structure 55, a dielectric core 62, and a drain region 63 within a memory opening 49 is herein referred to as a memory opening fill structure 58 .

[0108] In the alternative embodiment in which the support openings are formed at the same time as the memory openings 49, the support pillar structures 20 may be formed in the support openings at the same time as the memory opening fill structures 58. In this alternative embodiment, the support pillar structures 20 have the same composition as the memory opening fill structures 58, but are not electrically connected to the subsequently formed bit lines.

[0109] Referring to FIGS. 17A – 17G, the exemplary structure is illustrated after formation of memory opening fill structures 58 and support pillar structure 20 within the memory openings 49 and the support openings 19, respectively. An instance of a memory opening fill structure 58 can be formed within each memory opening 49. An instance of the support pillar structure 20 can be formed within each support opening. Other memory stack structures including different layer stacks or structures for the memory film 50 and/or for the vertical semiconductor channel 60 may also be used.

[0110] Generally, each of the memory opening fill structures 58 comprises a respective vertical stack of memory elements and a respective vertical semiconductor channel 60. In one embodiment, the vertical stack of memory elements may comprise portions of the memory film 50 (such as portions of the memory material layer 54) located at levels of the sacrificial material layers (142, 242), which are subsequently replaced with electrically conductive layers.

[0111] Referring to FIGS. 18A – 18I, a capping dielectric layer 280 can be formed over the second insulating cap layer 270, the memory opening fill structures 58, and the support pillar structures 20. The capping dielectric layer 280 comprises a dielectric material, such as undoped silicate glass or a doped silicate glass, and may have a thickness in a range from 30 nm to 300 nm, although lesser and greater thicknesses may also be employed. In one embodiment, top surfaces of the memory opening fill structures 58 are located within the first horizontal plane HP1, which includes the bottom surface of the capping dielectric layer 280.

[0112] A photoresist layer (not shown) may be applied over the capping dielectric layer 280, and can be lithographically patterned to form openings therein. The openings in the patterned photoresist layer may comprise elongated openings that laterally extend along the first horizontal direction hd1 through the memory array regions 100 and the contact region 200 between respective pairs of clusters of memory opening fill structures 58. Further, the openings in the patterned photoresist layer may comprise arrays of discrete openings arranged such that the combination of the areas of the support pillar structures 20 and the areas of the discrete openings

cover all vertically-extending surfaces of the stepped surfaces of the alternating stack (32, 42) that are not covered by the elongated openings.

[0113] An anisotropic etch process can be performed to transfer the pattern of the openings through the capping dielectric layer 280, the second-tier structure, and the first-tier structure, and down to at least a top surface of the semiconductor material layer 110. Lateral isolation trenches 79 can be formed underneath the elongated openings in the photoresist layer. The lateral isolation trenches 79 laterally extend along the first horizontal direction hd1, and may have a uniform width along the second horizontal direction hd2 that is greater than the maximum thickness of the sacrificial material layers 42. In one embodiment, the uniform width of the lateral isolation trenches 79 may be in a range from twice the average thickness of the sacrificial material layers 42 to ten times the average thickness of the sacrificial material layers 42.

[0114] Arrays of isolation cavities 77 are formed underneath the arrays of discrete openings in the photoresist layer. The isolation cavities 77 may have a maximum lateral dimension (i.e., a length) in a range from about one half the average thickness of the sacrificial material layers 42 to about five times the average thickness of the sacrificial material layers 42, and may have a width (i.e., a maximum dimension along a horizontal direction that is perpendicular to the length) in a range from 1/4 of the average thickness of the sacrificial material layers 42 to about twice the average thickness of the sacrificial material layers 42. In one embodiment, the isolation cavities 77 may be elongated along the second horizontal direction hd2 such that the length each isolation cavity 77 along the second horizontal direction hd2 is greater than its width along the first horizontal direction hd1. Alternatively, the isolation cavities 77 may have a circular horizontal cross-sectional shape .

[0115] The lateral isolation trenches 79 laterally extend along the first horizontal direction hd1, and are laterally spaced apart from each other along a second horizontal direction hd2. The lateral isolation trenches 79 may comprise first lateral isolation trenches 79 located at edges of a respective repetition unit RU and not contacting any of the dielectric fill structures (165, 265), and second lateral isolation trenches 79 that divide a respective first dielectric fill structure 165 and a respective second dielectric fill structure 265 into a respective pair of first dielectric fill structures 165 and a respective pair of second dielectric fill structures 265. Thus, each first lateral isolation trench 79 is laterally offset from the cavities (169, 269) within the alternating stack (32, 42) along the second horizontal direction hd2. Each second lateral isolation trench 79 cuts through a respective stack of a first cavity 169 and a second cavity 269 (which is filled with a stack of a first dielectric fill structure 165 and a second dielectric fill structure 265 prior to formation of the lateral isolation trenches 79).

[0116] Generally, lateral isolation trenches 79 and arrays of isolation cavities 77 can be formed through the alternating stack (32, 42). The lateral isolation trenches 79 and the arrays of isolation cavities 77, in conjunction with the support pillar structures 20, divide each of the sacrificial liners (182, 282) into a respective array of sacrificial liner strips (182', 282') that are laterally spaced apart from each other along the first horizontal direction hd1. Specifically, each first sacrificial liner 182 is divided into an array of first sacrificial liner strips 182', and each second sacrificial liner 282 is divided into an array of second sacrificial liner strips 282'. The sacrificial liner strips (182', 282') are exposed to a respective second lateral isolation trench 79 upon formation of the lateral isolation trenches 79. Each of the sacrificial liner strips (182', 282') contacts one stepped surface S of a respective sacrificial material layer 42 in the respective cavity (169, 269).

[0117] Each tapered sidewall (TS1, TS2) of the cavities (169, 269) can be divided into a plurality of tapered sidewalls (TS1, TS2) (each having a lesser area than a respective original tapered sidewall prior to division) upon formation of the support pillar structures 20 or upon formation of the arrays of isolation cavities 77. Generally, the support pillar structures 20 and/or the arrays of isolation cavities 77 divide each of the tapered sidewalls (TS1, TS2) of the cavities (169, 269) in the alternating stack (32, 42) into a respective plurality of tapered sidewalls (TS1, TS2) that are laterally spaced apart along the first horizontal direction hd1.

[0118] In one embodiment, each of the sacrificial liner strips (182', 282') comprises a first horizontally-extending portion which is a topmost portion; a tapered vertically-extending portion that overlies the respective tapered sidewall (TS1, TS2) of the plurality of tapered sidewalls (TS1, TS2), and a second horizontally-extending portion which is a bottommost portion and which is adjoined to the respective one of the sacrificial material layers 42.

[0119] The tapered vertically-extending portion extends between the topmost and bottommost portions generally at a non-zero angle relative to the vertical direction in a straight or stepped inclined (e.g., diagonal) plane. The second horizontally-extending portion may contact a top of the stepped surface of the respective one of the sacrificial material layers 42 in the respective cavity (169, 269).

[0120] In one embodiment, each of the sacrificial liner strips (182', 282') may comprise a stepped contoured portion that is proximal to an opening in a respective insulating liner (160, 260). In this case, each of the sacrificial liner strips (182', 282') further comprises a vertically-extending portion that is adjoined to the second horizontally-extending portion; and a third horizontally-extending portion that is adjoined to the vertically-extending portion and to a bottom end of the tapered vertically-extending portion. In case where the first alternating stack (132, 142) and the second alternating stack (232, 242) are both present within the alternating

stack (32, 42), a top end of a first sacrificial liner strip 182' may contact a bottom surface of a respective second sacrificial liner strip 282' . Each second sacrificial material layer 242 may have a respective top surface segment that contacts a bottom surface of a respective second sacrificial liner strip 282'. Each first sacrificial material layer 142 may have a respective top surface segment that contacts a bottom surface of a respective first sacrificial liner strip 182', which has a respective top surface that contacts a bottom surface of a respective second sacrificial liner strip 282'.

[0121] Optionally, an ion implantation process may be performed to implant dopants of the second conductivity type into surface portions of the semiconductor material layer 110 that underlie the lateral isolation trenches 79 or the arrays of isolation cavities 77. Source regions 61 having a doping of the first conductivity type may be formed in the implanted portions of the semiconductor material layer 110.

[0122] Referring to FIGS. 19A – 19I, an isotropic etch process can be performed to isotropically etch the materials of the sacrificial material layers 42 and the sacrificial liner strips (182', 282') selective to the materials of the insulating layers 32, the insulating liners (160, 260), the insulating cap layers (170, 270), the dielectric capping layer 280, and the semiconductor material layer 110. An isotropic etchant can be introduced into the lateral isolation trenches 79 and into the isolation cavities 77 during the isotropic etch process. For example, if the sacrificial material layers 42 and the sacrificial liner strips (182', 282') comprise silicon nitride, the isotropic etch process may comprise a wet etch process employing hot phosphoric acid.

[0123] Laterally-extending cavities 43 are formed in volumes from which portions of the sacrificial material layers 42 are removed by the isotropic etch process. The laterally-extending cavities 43 may comprise first laterally-extending cavities 143 that are formed in volumes from which first sacrificial material layers 142 are removed, and second laterally-extending cavities 243 that are formed in volumes from which the second sacrificial material layers 242 are removed. Strip-shaped cavities (183, 283) are formed in volumes from which the sacrificial liner strips (182', 282') are removed. The strip-shaped cavities (183, 283) comprise first strip-shaped cavities 183 that are formed in volumes from which first sacrificial liner strips 182' are removed, and second strip-shaped cavities 283 that are formed in volumes from which second sacrificial liner strips 282' are removed. The insulating layers 32, the dielectric fill structures (165, 265), the insulating cap layers (170, 270), and the dielectric capping layer 280 can be structurally supported by the memory opening fill structures 58 and the support pillar structures 20 during and after formation of the laterally-extending cavities 43 and the strip-shaped cavities (183, 283).

[0124] Referring to FIGS. 20A – 20I, at least one conductive material can be deposited in unfilled volumes of the laterally-extending cavities 43 and the strip-shaped cavities (183, 283) by

providing at least one reactant gas into the laterally-extending cavities 43 and into the strip-shaped cavities (183, 283) through the lateral isolation trenches 79 and through the isolation cavities 77 . For example, the at least one conductive material may comprise a metallic barrier layer and a metallic fill material. The metallic barrier layer includes an electrically conductive metallic material that can function as a diffusion barrier layer and/or adhesion promotion layer for a metallic fill material to be subsequently deposited. The metallic barrier layer can include a conductive metallic nitride material such as TiN, TaN, WN, MoN or a stack thereof, or can include a conductive metallic carbide material such as TiC, TaC, WC, or a stack thereof. In one embodiment, the metallic barrier layer can be deposited by a conformal deposition process such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). The thickness of the metallic barrier layer can be in a range from 2 nm to 8 nm, such as from 3 nm to 6 nm, although lesser and greater thicknesses can also be employed. In one embodiment, the metallic barrier layer can consist essentially of a conductive metal nitride such as TiN.

[0125] The metal fill material can be deposited over the metallic barrier layer to form a metallic fill material layer. The metallic fill material can be deposited by a conformal deposition method, which can be, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless plating, electroplating, or a combination thereof. In one embodiment, the metallic fill material layer can consist essentially of at least one elemental metal. The at least one elemental metal of the metallic fill material layer can be selected, for example, from tungsten, cobalt, ruthenium, titanium, or tantalum. In one embodiment, the metallic fill material layer can consist essentially of a single elemental metal. In one embodiment, the metallic fill material layer can be deposited employing a fluorine-containing precursor gas, such as WF6. In one embodiment, the metallic fill material layer can be a tungsten layer including a residual level of fluorine atoms as impurities. The metallic fill material layer is spaced from the insulating layers 32, the insulating liners (160, 260), the memory opening fill structures 58, and the support pillar structures 20 by the metallic barrier layer that blocks diffusion of fluorine atoms therethrough.

[0126] A plurality of electrically conductive layers 46 can be formed in the plurality of laterally-extending cavities 43. Electrically conductive strips 84 can be formed in a first subset of the strip-shaped cavities (183, 283) that adjoins a respective underlying electrically conductive layer 46. An additional electrically conductive strip 84’ that is not electrically connected to any underlying electrically conductive layer 46 may be formed over a respective set of at least one end wall (EW1, EW2) of a respective set of at least one cavity (169, 269). A continuous metallic material layer (not shown) can be formed over the dielectric capping layer 280 and on the sidewalls and bottom surfaces of the lateral isolation trenches 79 and the isolation cavities 77. Each electrically conductive layer 46 includes a portion of the metallic barrier layer and a portion

of the metallic fill material layer that are located between a vertically neighboring pair of dielectric material layers such as a pair of insulating layers 32. The continuous metallic material layer includes a continuous portion of the metallic barrier layer and a continuous portion of the metallic fill material layer that are located in the lateral isolation trenches 79 or above the dielectric capping layer 280.

[0127] The deposited metallic material of the continuous electrically conductive material layer is etched back from above the dielectric capping layer 280 and from the sidewalls and the bottom surfaces of the lateral isolation trenches 79 and the isolation cavities 77 by performing an etch process that etches the at least one conductive material of the continuous electrically conductive material layer. The etch process may comprise an anisotropic etch process and/or an isotropic etch process. Each remaining portion of the deposited metallic material in the laterally-extending cavities 43 constitutes an electrically conductive layer 46. Each electrically conductive layer 46 can be a conductive line structure. Thus, the sacrificial material layers 42 are replaced with the electrically conductive layers 46. The electrically conductive layer 46 comprise first electrically conductive layers 146 that replace first sacrificial material layers 142, and second electrically conductive layers 246 that replace second sacrificial material layers 242. The electrically conductive layers 46 may comprise source side select gate electrodes, word lines overlying the source side select gate electrodes, and drain side select gate electrodes overlying the word lines.

[0128] Electrically conductive strips 84 are formed in the volumes of the strip-shaped cavities (183, 283). Generally, remaining portions of the sacrificial material layers (142, 242) and the sacrificial liner strips (182', 282') are replaced with electrically conductive material portions that include the electrically conductive layers 46 and the electrically conductive strips 84, respectively. The electrically conductive layers 46 are formed in volumes from which the remaining portions of the sacrificial material layers 42 are removed, and electrically conductive strips 84 fill volumes from which the sacrificial liner strips (182', 282') are removed, respectively.

[0129] An alternating stack (32, 46) of insulating layers 32 and electrically conductive layers 46 is formed between each neighboring pair of lateral isolation trenches 79. The alternating stack (32, 46) may include a first alternating stack of first insulating layers 132 and first electrically conductive layers 146 and a second alternating stack of second insulating layers 232 and second electrically conductive layers 246.

[0130] In one embodiment, each of the electrically conductive strips 84 is adjoined to a respective one of the electrically conductive layers 46 at a bottom portion of a respective one of the cavities (169, 269), and overlies, but does not contact, a respective tapered sidewall (TS1,

TS2) of a plurality of tapered sidewalls (TS1, TS2) that are arranged along the first horizontal direction hd1. Each of the electrically conductive strips 84 includes a respective topmost portion 84T that is located above a first horizontal plane HP1 including the topmost surface of the alternating stack (32, 46). In one embodiment, each of the electrically conductive strips is spaced from the respective tapered sidewall (TS1, TS2) by a respective tapered vertically-extending portion of a respective insulating liner (160, 260).

[0131] In one embodiment, each of the electrically conductive strips 84 comprises: a first horizontally-extending portion which is a topmost portion 84T; a tapered vertically-extending portion 84V that overlies the respective tapered sidewall (TS1, TS2) of the tapered sidewalls (TS1, TS2); and a second horizontally-extending portion which is a bottommost portion 84V and is adjoined to the respective one of the electrically conductive layers 46. The tapered vertically-extending portion 84V extends between the topmost and bottommost portions (84T, 84B) at a generally non-zero angle relative to the vertical direction in a straight or stepped inclined (e.g., diagonal) plane.

[0132] In one embodiment, each of the electrically conductive strips 84 further comprises: a vertically-extending portion 84X that is adjoined to the second horizontally-extending portion; and a third horizontally-extending portion 84Y that is adjoined to the vertically-extending portion and to a bottom end of the tapered vertically-extending portion.

[0133] In one embodiment, each of the electrically conductive strips 84 and the respective one of the electrically conductive layers 46 are formed as a unitary structure (i.e., a single continuous structure) including a conductive material portion (such as a metallic barrier layer or a metallic fill material portion) that extends continuously between a volume of a respective electrically conductive strip 84 and the respective one of the electrically conductive layers 46. Thus, the second horizontally-extending portion of a strip 84 forms a step on the top surface of the respective electrically conductive layer 46 within the unitary structure, as shown in FIGS. 20A, 20C and 20D. Therefore, the strips 84 function as word line contact via structures.

[0134] In one embodiment, the drain side select gate electrodes (i.e., the uppermost second electrically conductive layers 246) may have separate contact via structures located in a separate staircase region located on opposite end of each memory array region 100 from the end which faces the contact region 200. In this embodiment, the strips 84 function as word line contact via structures and source side select gate electrode contact via structures, but not as drain side select gate electrode contact via structures.

[0135] In one embodiment, each insulating liner (160, 260) includes a first horizontally-extending portion overlying a plurality of electrically conductive layers 46, and a plurality of additional tapered vertically-extending portions that overlie a respective tapered sidewall (TS1,

TS2) of the tapered sidewalls (TS1, TS2). In one embodiment, each insulating liner (160, 260) includes a plurality of second horizontally-extending portions overlying a bottom surface of a respective cavity (169, 269) and underlying the second horizontally-extending portion of a respective one of the electrically conductive strips 84.

[0136] Referring to FIGS. 21A – 21I, an insulating material layer can be conformally deposited in the lateral isolation trenches 79, in the isolation cavities 77, and over the dielectric capping layer 280. In one embodiment, the insulating material layer may have a thickness that is greater than one half of the maximum width of the isolation cavities 77. In this case, the insulating material layer may fill the isolation cavities 77 in a manner that plugs a least a top portion of each isolation cavity 77.

[0137] An anisotropic etch process can be performed to remove horizontally-extending portions of the insulating material layer. Each remaining vertically-extending portion of the insulating material layer that is formed in a respective lateral isolation trench 79 constitutes an insulating isolation trench spacer 74. Each remaining portion of the insulating material layer that fills the isolation cavities 77 constitutes an isolation pillar structure 73 .

[0138] At least one conducive material can be deposited in remaining unfilled volumes of the lateral isolation trenches 79 to form source contact via structures 76, which can be conductive wall structures laterally extending along the first horizontal direction hd1. Each contiguous combination of an insulating isolation trench spacer 74 and a source contact via structure 76 constitutes a lateral isolation trench fill structure (74, 76) that fills a respective lateral isolation trench 79 . The lateral isolation trench fill structures (74, 76) comprise first lateral isolation trench fill structures (74, 76) that contact a respective pair of at least one dielectric fill structure (165, 265), and second lateral isolation trench fill structures (74, 76) that do not contact any dielectric fill structure (165, 265).

[0139] The isolation pillar structures 73 and the support pillar structures 20 are lateral isolation structures that provide electrical isolation between neighboring pairs of electrically conductive strips 84 that are laterally spaced apart along the first horizontal direction hd1 between a respective lateral isolation trench fill structure (74, 76) and a respective set of tapered sidewalls (TS1, TS2) of the alternating stack of insulating layers 32 and electrically conductive layers 46. Each lateral isolation structures (73, 20) can include a respective contiguous set of at least one support pillar structure 20 and at least one isolation pillar structure 73 that continuously extends along the second horizontal direction hd2 between a respective lateral isolation trench fill structure (74, 76) and a respective set of tapered sidewalls (TS1, TS2) of an alternating stack of insulating layers 32 and electrically conductive layers 46.

[0140] The lateral isolation structures separate (73, 20) adjacent strips 84 along first horizontal direction (i.e., the word line direction) hd1, such that each strip 84 contacts only one respective electrically conductive layer 46 in the stepped cavities (169, 269), since the electrically conductive layers 46 form the stepped bottom surfaces of the stepped cavities. This prevents the strips 84 from short circuiting vertically separated electrically conductive layers 46.

[0141] Generally, an array of lateral isolation structures (20, 73) vertically extends from a first horizontal plane HP1 including the topmost surface of the alternating stack (32, 46) to a second horizontal plane HP2 including a bottommost surface of the alternating stack (32, 46) and located between a respective neighboring pair of tapered sidewalls (TS1, TS2) among the tapered sidewalls (TS1, TS2) of the alternating stack (32, 46).

[0142] In one embodiment, a first lateral isolation trench fill structure (74, 76) may have a first lengthwise sidewall that contacts each layer of the alternating stack (32, 46) and laterally extends along the first horizontal direction hd1. A second lateral isolation trench fill structure (74, 76) may have a second lengthwise sidewall, which contacts each layer of the alternating stack (32, 46) and laterally extends along the first horizontal direction hd1 and is laterally spaced from the first lateral isolation trench fill structure (74, 76) along the second horizontal direction hd2 . An array of lateral isolation structures (20, 73) contacts the first lateral isolation trench fill structure (74, 76) and does not contact the second lateral isolation trench fill structure (74, 76).

[0143] In one embodiment, a lateral isolation structure (20, 73) within the array of lateral isolation structures (20, 73) comprises: at least one support pillar structures 20 vertically extending from the horizontal plane including the bottom surface of the capping dielectric layer 280 and at least to a second horizontal plane HP2 including a bottommost surface of the alternating stack (32, 46); and at least one isolation pillar structure 73 vertically extending from a horizontal plane including a top surface of the capping dielectric layer 280 and at least to the second horizontal plane HP2 and in contact with the at least two support pillar structures 20 .

[0144] Each volume that is laterally surrounded by a first lateral isolation trench fill structure (74, 76), a tapered sidewall (TS1, TS2) of an alternating stack of insulating layers 32 and electrically conductive layers 46, and a neighboring pair of lateral isolation structures (20, 73) constitutes a well. The well can be filled with a respective patterned set of a second dielectric fill structure 265, optionally within a respective portion of a first dielectric fill structure 165, at least one insulating liner (160, 260), and an electrically conductive strip 84.

[0145] Each layer of the alternating stack (32, 46) is present within the first and second memory array regions (100A, 100B). At least a portion of the first electrically conductive layers 146 and at least a portion of the second electrically conductive layers 246 continuously extend from the first memory array region 100A to the second memory array region 100B through an

array interconnection region (e.g., "bridge" region) 220 located between the respective lateral isolation trench fill structure (74, 76) and the respective contact any dielectric fill structure (165, 265) in the respective cavity (169, 269) in the contact region 200. The first horizontally-extending portion of each of the electrically conductive strips 84 overlies the alternating stack (32, 46) in the interconnection region 220. The vertically-extending portion of each of the electrically conductive strips 84 overlies the respective tapered sidewall (TS1, TS2) of the interconnection region 220.

[0146] In one embodiment, the alternating stack (32, 46) laterally extends from the first lateral isolation trench fill structure (74, 76) to the second lateral isolation trench fill structure (74, 76) in the first memory array region 100A and in the second memory array region 100B, and has a lesser extent along the second horizontal direction hd2 within the interconnection region 220 of the contact region 200 than a lateral spacing between the first lateral isolation trench structure (74, 76) and the second lateral isolation trench structure (74, 76). The interconnection region 220 is located between the first lateral isolation trench fill structure (74, 76) and the tapered sidewalls (TS1, TS2) of the alternating stack (32, 46).

[0147] Referring to FIGS. 22A and 22B, a first alternative configuration of the exemplary structure is illustrated, which can be derived from the exemplary structure illustrated in FIGS. 18A – 18I by forming elongated isolation cavities that are elongated along the second horizontal direction hd2 in lieu of the isolation cavities described with reference to FIGS. 18A – 18I, and by forming isolation wall structures 173 in lieu of isolation pillar structures 72 at the processing steps described with reference to FIGS. 21A – 21I . Each isolation wall structure 173 may laterally extend along the second horizontal direction hd2.

[0148] In this embodiment, a lateral isolation structure (20, 173) within the array of lateral isolation structures (20, 173) comprises: at least one support pillar structures 20 vertically extending from the horizontal plane including the bottom surface of the capping dielectric layer 280 and at least to a second horizontal plane HP2 including a bottommost surface of the alternating stack (32, 46); and an elongated isolation wall structure 173 vertically extending from a horizontal plane including a top surface of the capping dielectric layer 280 and at least to the second horizontal plane HP2 and in contact with the at least two support pillar structures 20 .

[0149] Referring to FIGS. 23A and 23B, a second alternative configuration of the exemplary structure is illustrated, which can be derived from the first alternative configuration of the exemplary structure by further elongating the isolation trenches along the second horizontal direction hd2 so that the elongated isolation trenches are adjoined to a respective one of the lateral isolation trenches 79 and intersects a respective tapered sidewall (TS1, TS2). In this case,

isolation wall structures 173 may be adjoined to a respective insulating isolation trench spacer 74.

[0150] In this embodiment, a lateral isolation structure 173 within the array of lateral isolation structures 173 comprises an elongated isolation wall structure 173 vertically extending from a horizontal plane including a top surface of the capping dielectric layer 280 and at least to the second horizontal plane HP2 and in contact with the at least two support pillar structures 20. The first lateral isolation trench fill structure (74, 76) comprises first insulating wall segments that are laterally spaced apart along the first horizontal direction hd1 and in contact with a respective subset of layers within the alternating stack (32, 46) and located within a same vertical plane, and the lateral isolation structure comprising the isolation wall structure 173 comprises a second insulating wall segment (such as a contoured vertical sidewall of the isolation wall structure 173) that is adjoined to a neighboring pair of first insulating wall segments within the first lateral isolation trench fill structure (74, 76).

[0151] Referring to FIGS. 24A and 24B, a third alternative configuration of the exemplary structure is illustrated, which can be derived from any of the exemplary structures illustrated in FIGS. 21A – 21I, 22A and 22B, or 23A and 23B by reducing thickness of the insulating material layer such that a void is present within the volumes of the isolation cavities 77 or within volumes of elongated isolation cavities after an anisotropic etch process that forms the insulating isolation trench spacers 74. In this case, each remaining portion of the insulating material layer that remains within the volumes of the isolation cavities 77 or within the volumes of the elongated isolation cavities constitutes an isolation liner 73' having the same lateral thickness as the insulating isolation trench spacers 74. In one embodiment, the isolation liners 73' may be formed in a tubular configuration. A conductive fill structure 75 may be formed within each remaining volume of the isolation cavities 77 or elongated isolation cavities 77. Each conductive fill structure 75 may be laterally surrounded by a respective isolation liner 73'. Each contiguous combination of an isolation liner 73' and a conductive fill structure 75 constitutes a component of a lateral isolation structure (20, 73', 75) .

[0152] In this embodiment, a lateral isolation structure (20, 73', 75) within the array of lateral isolation structures (20, 73', 75) comprises: at least one support pillar structures 20 vertically extending from the horizontal plane including the bottom surface of the capping dielectric layer 280 and at least to a second horizontal plane HP2 including a bottommost surface of the alternating stack (32, 46); an isolation liner 73' which may optionally have a respective tubular configuration, and a conductive fill structure 75 which may be partially or completely surrounded by the isolation liner 73'. Thus, the lateral isolation structure (20, 73', 75) within the array of lateral isolation structures (20, 73', 75) comprises an isolation liner 73' and a conductive

fill structure 75 that is laterally spaced from the alternating stack (32, 46) by the isolation liner 73'.

[0153] Referring to FIGS. 25A and 25B, a fourth alternative configuration of the exemplary structure can be derived from the third configuration of the exemplary structure by employing elongated isolation cavities in lieu of the isolation trenches employed in the third alternative configuration of the exemplary structure. For example, elongated isolation cavities illustrated in the structure of FIGS. 22A and 22B may be employed. In one embodiment, the isolation liners 73' may be formed in a tubular configuration. A conductive fill structure 75 may be formed within each remaining volume of the isolation cavities 77 or elongated isolation cavities 77. Each conductive fill structure 75 may be laterally surrounded by a respective isolation liner 73'. Each contiguous combination of an isolation liner 73' and a conductive fill structure 75 constitutes a component of a lateral isolation structure (20, 73', 75) .

[0154] In one embodiment, a lateral isolation structure (20, 73', 75) within the array of lateral isolation structures (20, 73', 75) comprises: at least one support pillar structures 20 vertically extending from the horizontal plane including the bottom surface of the capping dielectric layer 280 and at least to a second horizontal plane HP2 including a bottommost surface of the alternating stack (32, 46); an isolation liner 73' which may have a respective tubular configuration, and a conductive fill structure 75 which may be completely surrounded by, or may be partially surrounded by, the isolation liner 73'. In one embodiment, a lateral isolation structure (20, 73', 75) within the array of lateral isolation structures (20, 73', 75) comprises an isolation liner 73' and a conductive fill structure 75 that is laterally spaced from the alternating stack (32, 46) by the isolation liner 73'.

[0155] FIG. 26A is a vertical cross-sectional view of a fifth alternative configuration of the exemplary structure after formation of lateral isolation trench fill structures (74, 76) and lateral isolation structures (73', 75). For example, elongated isolation cavities may merge with lateral isolation trenches 79, as illustrated in FIGS. 23A and 23B. In this embodiment, the isolation liners 73' may be adjoined to a respective insulating isolation trench spacer 74. Further, the conductive fill structures 75 may be adjoined to a respective source contact via structure 76. Each contiguous combination of an isolation liner 73' and a conductive fill structure 75 constitutes a component of a lateral isolation structure (73', 75) .

[0156] In this embodiment, a lateral isolation structure (73', 75) within the array of lateral isolation structures (73', 75) comprises: an isolation liner 73' which is adjoined to an insulating isolation trench spacer 74, and a conductive fill structure 75 which is partially surrounded by the isolation liner 73' and adjoined to a source contact via structure 76. In one embodiment, a lateral isolation structure (73', 75) within the array of lateral isolation structures (73', 75) comprises an

isolation liner 73' and a conductive fill structure 75 that is laterally spaced from the alternating stack (32, 46) by the isolation liner 73'.

[0157] Referring to FIGS. 27A – 27I, drain-select-level isolation structures 72 can be formed through a subset of electrically conductive layers 46 including the topmost electrically conductive layer 46. For example, a photoresist layer (not shown) can be applied over the dielectric capping layer 280, and can be lithographically patterned to form elongated openings that laterally extend along the first horizontal direction hd1 within each of the memory array regions 100. An anisotropic etch process can be performed to transfer the pattern of the elongated openings through a subset of layers in the alternating stack (32, 46) that includes the topmost electrically conductive layer 46. Drain-select-level isolation trenches can be formed between neighboring rows of memory opening fill structures 58 that are arranged along the first horizontal direction hd1. The photoresist layer can be removed, and a dielectric fill material such as silicon oxide can be deposited in the drain-select-level isolation trenches. Excess portions of the dielectric fill material can be removed from above the horizontal plane including the top surface of the dielectric capping layer 280. Each remaining portion of the dielectric fill material that fills a respective drain-select-level isolation trench constitutes a drain-select-level isolation structure 72 .

[0158] Referring to FIGS. 28A – 28G, a contact-level dielectric layer 290 can be formed over the dielectric capping layer 280. The contact-level dielectric layer 290 comprises a dielectric material, such as undoped silicate glass or a doped silicate glass. The thickness of the contact-level dielectric layer 290 may be in a range from 50 nm to 500 nm, such as from 100 nm to 300 nm, although lesser and greater thicknesses may also be employed.

[0159] In one embodiment shown in FIG. 28G, additional staircase regions 300 are formed on the ends of each memory plane along the first (e.g., word line) horizontal direction, including in areas M2 shown in FIG. 1. FIG. 28G shows a part of area M2 at the end of the alternating stack (32, 46) of the second memory array region 100B. Specifically, stepped surfaces are only formed in the uppermost electrically conductive layers that function as drain side select gate electrodes 246D (e.g., 46D). In one embodiment, the electrically conductive layers 46 which function as word lines or source side select electrodes lack stepped surfaces in the additional staircase regions 300. The stepped surfaces of the additional staircase regions 300 are formed at the ends of the memory array regions 100 which are opposite to the ends of the memory array region 100 which abut the contact region 200.

[0160] A photoresist layer (not shown) can be applied over the contact-level dielectric layer 290, and can be lithographically patterned to form discrete openings overlying a respective one of the drain regions 63 in the memory opening fill structures 58, overlying a topmost planar

portion of a respective electrically conductive strip 84 in the interconnection region 220 or overlying a stepped surface of the drain side select gate electrodes 46D in the additional staircase regions 300. An anisotropic etch process can be performed to form drain contact via cavities overlying the drain regions 63 and to from connection via cavities overlying the topmost planar portions of the electrically conductive strips 84 and the drain side select gate electrodes 46D. The photoresist layer can be subsequently removed .

[0161] At least one conductive material can be deposited in the drain contact via cavities and in the connection via cavities. Excess portions of the at least one conductive material can be removed from above the horizontal plane including the top surface of the contact-level dielectric layer 290 by a planarization process such as a chemical mechanical planarization (CMP) process or a recess etch process. Each remaining portion of the at least one conductive material filling a respective drain contact via cavity and contacting a top surface of a respective drain region 63 constitutes a drain contact via structure 88. Each remaining portion of the at least one conductive material filling a respective connection via cavity and contacting a top surface of a respective electrically conductive strip 84 constitutes a connection via structure 86. Each remaining portion of the at least one conductive material filling a respective connection via cavity and contacting a top surface of a respective drain side select electrode constitutes a select gate via structure 186. In this embodiment, the electrically conductive strips 84 do not electrically contact the drain side select gate electrodes 46D.

[0162] In an alternative embodiment, the additional staircase regions 300 and separate select gate via structures 186 are omitted. In this embodiment, a subset of the electrically conductive strips 84 contact the drain side select gate electrodes 46D in the interconnection region 220 instead of the select gate via structures 186.

[0163] Additional metal interconnect structures (not shown), additional dielectric material layers (not shown), metal bonding pads (not shown) may be subsequently formed to provide a memory die.

[0164] Referring to all drawings and according to various embodiments of the present disclosure, a memory device comprises an alternating stack (32,46) including insulating layers 32 and electrically conductive layers 46 that are interlaced along a vertical direction, wherein the alternating stack comprises a tapered sidewall (TS1, TS2) that laterally extends along a first horizontal direction hd1 and which is inclined along a second horizontal hd2 direction perpendicular to the first horizontal direction; memory openings 49 vertically extending through each layer within the alternating stack; memory opening fill structures 58 located in the memory openings and including a respective vertical stack of memory elements (e.g., portions of the memory film 50) and a respective vertical semiconductor channel 60; a cavity (169, 269) in the

alternating stack bounded laterally along a first side by the tapered sidewall (TS1, TS2) and having a bottom surface comprising stepped surfaces S of at least some of the electrically conductive layers 46; an insulating liner (160, 260) located over the tapered sidewall in the cavity; and electrically conductive strips 84 which are adjoined to a respective one of the stepped surfaces at a bottom surface of the cavity (169, 269), which extend over the insulating liner and the tapered sidewall in the cavity, and which include a respective topmost portion 84T that is located above the topmost surface of the alternating stack (32, 46).

[0165] In one embodiment, each of the electrically conductive strips 84 is spaced from the tapered sidewall (TS1, TS2) by a tapered vertically-extending portion of the insulating liner (160, 260). The insulating liner (160, 260) further comprises a first horizontally-extending portion overlying stepped surfaces S and a second horizontally extending portion located between the topmost surface of the alternating stack (32, 46) (e.g., horizontal plane HP1) and the topmost portions 84T of the electrically conductive strips 84.

[0166] In one embodiment, each of the electrically conductive strips comprises: a first horizontally-extending portion 84T which is a topmost portion; a tapered vertically-extending portion 84V that overlies the tapered sidewall (TS1, TS2); and a second horizontally-extending portion 84B which is a bottommost portion and is adjoined to the respective one of the stepped surfaces S of the electrically conductive layers 46 in the cavity (169, 269). Optionally, each of the electrically conductive strips 84 further comprises a vertically-extending portion 84X that is adjoined to the second horizontally-extending portion; and a third horizontally-extending portion 84Y that is adjoined to the vertically-extending portion 84V and to a bottom end of the tapered vertically-extending portion 84X.

[0167] In one embodiment, a dielectric fill structure (165, 265) is located in the cavity (169, 269) over the electrically conductive strips 84 and over the stepped surfaces S. In one embodiment, each of the electrically conductive strips 84 and the respective one of the electrically conductive layers 46 are formed as a unitary structure including a conductive material portion that extends continuously between a volume of a respective electrically conductive strip and the respective one of the electrically conductive layers.

[0168] In one embodiment, lateral isolation structures (20, 73, 173) are located in the cavity (169, 269), vertically extending from the stepped surfaces S to at least the topmost surface HP1 of the alternating stack (32, 46), and each located between a respective neighboring pair the electrically conductive strips 84 along the first horizontal direction hd1. A first lateral isolation trench fill structure (74, 76) has a first lengthwise sidewall that contacts each layer of the alternating stack and laterally extends along the first horizontal direction; and a second lateral isolation trench fill structure (74, 76) has a second lengthwise sidewall that contacts each layer of

the alternating stack (32, 46) and laterally extends along the first horizontal direction hd1 and laterally spaced from the first lateral isolation trench fill structure along the second horizontal direction hd2. The lateral isolation structures (20, 73, 173) contact the first lateral isolation trench fill structure and do not contact the second lateral isolation trench fill structure.

[0169] In one embodiment, a first set of the memory opening fill structures 58 is located in a first memory array region 100A and a second set of the memory opening fill structures 58 is located in a second memory array region 100B which is laterally spaced from the first memory array region 100A along the first horizontal direction hd1 by a contact region 200. The cavity (169, 269) and the electrically conductive strips 84 are located in the contact region 200. At least a portion of the electrically conductive layers 46 continuously extend from the first memory array region 100A to the second memory array region 100B through an interconnection region 220 located between the second lateral isolation trench fill structure (74, 76) and the cavity (169, 269) in the contact region 200. The alternating stack (32, 46) laterally extends from the first lateral isolation trench fill structure to the second lateral isolation trench fill structure in the first memory array region 100A and in the second memory array region 100B, and has a lesser extent along the second horizontal direction hd2 within the interconnection region 220 than a lateral spacing between the first lateral isolation trench structure and the second lateral isolation trench structure. The topmost portions 84T of the electrically conductive strips 84 are located above the topmost surface HP1 of the alternating stack (32, 46) in the interconnection region 220.

[0170] In one embodiment shown in FIG. 28G, the memory device also includes a staircase region 300 located in the alternating stack (32, 46) adjacent to a first end of the second memory array region 100B opposite to a second end of the second memory array region 100B which abuts the contact region 200. Stepped surfaces are located in the staircase region 300 in only in an uppermost set of the electrically conductive layers 46 that function as drain side select gate electrodes 46D. Connection via structures 86 contact topmost portions 84T of the respective electrically conductive strips 84, and select gate via structures 186 contact top surfaces of the respective drain side select gate electrodes 46D in the staircase region 300.

[0171] In one embodiment, the cavity (169, 269) is further laterally bounded along a second side opposite to the first side by the first lateral isolation trench fill structure (74, 76), along a third side by a first tapered end wall (EW1, EW2) which extends along the second horizontal direction hd2 and which is inclined along the first horizontal direction hd1, and along a fourth side by the stepped surfaces S.

[0172] In one embodiment, the first lateral isolation trench fill structure (74, 76) comprises first insulating wall segments that are laterally spaced apart along the first horizontal direction

hd2 and in contact with a respective subset of layers within the alternating stack (32, 46), and second insulating wall segments that contact the lateral isolation structures.

[0173] In one embodiment, each of the lateral isolation structures comprises at least one support pillar structure 20 and at least one isolation pillar structure 73 in contact with the at one support pillar structure 20. In another embodiment, each of the lateral isolation structures comprises an isolation wall structure 173 which extends in the second horizontal direction hd2.

[0174] The various embodiments of the present disclosure can be employed to provide electrically conductive strips 84 that is formed integrally with and electrically connected to a respective one of the electrically conductive layer 46. Reliable electrical contact to the electrically conductive layers 46 can be made without employing an anisotropic etch process which can punch through the electrically conductive layers 46 by forming electrically conductive strips 84.

[0175] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Compatibility is presumed among all embodiments that are not alternatives of one another. The word "comprise" or "include" contemplates all embodiments in which the word "consist essentially of" or the word "consists of" replaces the word "comprise" or "include," unless explicitly stated otherwise. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. If publications, patent applications, and/or patents are cited herein, each of such documents is incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A memory device, comprising:

an alternating stack including insulating layers and electrically conductive layers that are interlaced along a vertical direction, wherein the alternating stack comprises a tapered sidewall that laterally extends along a first horizontal direction and which is inclined along a second horizontal direction perpendicular to the first horizontal direction;

memory openings vertically extending through each layer within the alternating stack;

memory opening fill structures located in the memory openings and including a respective vertical stack of memory elements and a respective vertical semiconductor channel;

a cavity in the alternating stack bounded laterally along a first side by the tapered sidewall and having a bottom surface comprising stepped surfaces of at least some of the electrically conductive layers;

an insulating liner located over the tapered sidewall in the cavity; and

electrically conductive strips which are adjoined to a respective one of the stepped surfaces at the bottom surface of the cavity, which extend over the insulating liner and the tapered sidewall in the cavity, and which include a respective topmost portion that is located above the topmost surface of the alternating stack.

2. The memory device of Claim 1, wherein each of the electrically conductive strips is spaced from the tapered sidewall by a tapered vertically-extending portion of the insulating liner.

3. The memory device of Claim 2, wherein the insulating liner further comprises a first horizontally-extending portion overlying stepped surfaces and a second horizontally extending portion located between the topmost surface of the alternating stack and the topmost portions of the electrically conductive strips.

4. The memory device of Claim 1, wherein each of the electrically conductive strips comprises:

a first horizontally-extending portion which is a topmost portion;

a tapered vertically-extending portion that overlies the tapered sidewall; and

a second horizontally-extending portion which is a bottommost portion and is adjoined to the respective one of the stepped surfaces of the electrically conductive layers in the cavity.

5. The memory device of Claim 4, wherein each of the electrically conductive strips further comprises:

a vertically-extending portion that is adjoined to the second horizontally-extending portion; and

a third horizontally-extending portion that is adjoined to the vertically-extending portion and to a bottom end of the tapered vertically-extending portion.

6. The memory device of Claim 1, further comprising a dielectric fill structure located in the cavity over the electrically conductive strips and over the stepped surfaces.

7. The memory device of Claim 1, wherein each of the electrically conductive strips and the respective one of the electrically conductive layers are formed as a unitary structure including a conductive material portion that extends continuously between a volume of a respective electrically conductive strip and the respective one of the electrically conductive layers.

8. The memory device of Claim 1, further comprising lateral isolation structures located in the cavity, vertically extending from the stepped surfaces to at least the topmost surface of the alternating stack, and each located between a respective neighboring pair the electrically conductive strips along the first horizontal direction.

9. The memory device of Claim 8, further comprising:

a first lateral isolation trench fill structure having a first lengthwise sidewall that contacts each layer of the alternating stack and laterally extending along the first horizontal direction; and

a second lateral isolation trench fill structure having a second lengthwise sidewall that contacts each layer of the alternating stack and laterally extending along the first horizontal direction and laterally spaced from the first lateral isolation trench fill structure along the second horizontal direction,

wherein the lateral isolation structures contact the first lateral isolation trench fill structure and do not contact the second lateral isolation trench fill structure.

10. The memory device of Claim 9, wherein:

a first set of the memory opening fill structures is located in a first memory array region;

a second set of the memory opening fill structures is located in a second memory array region which is laterally spaced from the first memory array region along the first horizontal direction by a contact region;

the cavity and the electrically conductive strips are located in the contact region;

at least a portion of the electrically conductive layers continuously extend from the first

memory array region to the second memory array region through an interconnection region located between the second lateral isolation trench fill structure and the cavity in the contact region;

the alternating stack laterally extends from the first lateral isolation trench fill structure to the second lateral isolation trench fill structure in the first memory array region and in the second memory array region, and has a lesser extent along the second horizontal direction within the interconnection region than a lateral spacing between the first lateral isolation trench structure and the second lateral isolation trench structure; and

the topmost portions of the electrically conductive strips are located above the topmost surface of the alternating stack in the interconnection region.

11. The memory device of claim 10, further comprising:

a staircase region located in the alternating stack adjacent to a first end of the second memory array region opposite to a second end of the second memory array region which abuts the contact region;

stepped surfaces located in the staircase region in only in an uppermost set of the electrically conductive layers that function as drain side select gate electrodes;

connection via structures contacting topmost portions of the respective electrically conductive strips; and

select gate via structures contacting top surfaces of the respective drain side select gate electrodes in the staircase region.

12. The memory device of claim 9, wherein the cavity is further laterally bounded along a second side opposite to the first side by the first lateral isolation trench fill structure, along a third side by a first tapered end wall which extends along the second horizontal direction and which is inclined along the first horizontal direction, and along a fourth side by the stepped surfaces.

13. The memory device of Claim 9, wherein:

the first lateral isolation trench fill structure comprises first insulating wall segments that are laterally spaced apart along the first horizontal direction and in contact with a respective subset of layers within the alternating stack; and

second insulating wall segments that contact the lateral isolation structures.

14. The memory device of Claim 8, wherein each of the lateral isolation structures comprises at

least one support pillar structure and at least one isolation pillar structure in contact with the at one support pillar structure.

15. The memory device of Claim 8, wherein each of the lateral isolation structures comprises an isolation wall structure which extends in the second horizontal direction.

16. A method of forming a memory device, comprising:

forming an alternating stack of insulating layers and sacrificial material layers that are interlaced along a vertical direction;

forming a cavity in the alternating stack such that stepped surfaces of the sacrificial material layers of the alternating stack are exposed at a bottom surface of the cavity;

forming an insulating liner over the stepped surfaces, over a tapered sidewall of the alternating stack, and over a topmost layer of the alternating stack;

forming an elongated opening through the insulating liner, wherein a strip segment of the stepped surfaces is exposed through the elongated opening through the insulating liner;

forming a sacrificial liner on the strip segment of the stepped surfaces and over the elongated openings such that the sacrificial liner comprises a top portion that overlies the alternating stack;

forming a dielectric fill structure over the sacrificial liner;

forming memory openings vertically extending at least through the alternating stack;

forming memory opening fill structures in the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements and a respective vertical semiconductor channel;

forming lateral isolation trenches and an array of isolation cavities through the alternating stack, wherein the lateral isolation trenches and the array of isolation cavities divide the sacrificial liner into sacrificial liner strips that are laterally spaced apart from each other; and

replacing remaining portions of the sacrificial material layers and the sacrificial liner strips with electrically conductive material portions, wherein electrically conductive layers are formed in volumes from which the remaining portions of the sacrificial material layers are removed, and electrically conductive strips are formed in volumes from which the sacrificial liner strips are removed, respectively.

17. The method of Claim 16, further comprising filling the lateral isolation trenches and the isolation cavities with lateral isolation trench fill structures and lateral isolation structures, respectively.

18. The method of Claim 16, further comprising:

forming support openings through the dielectric fill structure and the alternating stack; and

forming support pillar structures comprising a dielectric fill material in the support openings, wherein the sacrificial liner strips are laterally spaced apart from each other by a combination of the support pillar structures and the array of isolation cavities.

19. The method of Claim 16, further comprising:

forming a contact-level dielectric layer over the electrically conductive strips and over the memory opening fill structures; and

forming connection via structures on top surfaces of the electrically conductive strips.

20. The method of Claim 16, wherein:

the elongated opening through the insulating liner laterally extends along a first horizontal direction;

the lateral isolation trenches laterally extend along the first horizontal direction and are laterally spaced apart from each other along a second horizontal direction;

the lateral isolation trenches comprise a first lateral isolation trench that is laterally offset from the cavity along the second horizontal direction, and a second lateral isolation trench that cuts through the cavity; and

the sacrificial liner strips are exposed in the second lateral isolation trench upon formation of the second lateral isolation trench.

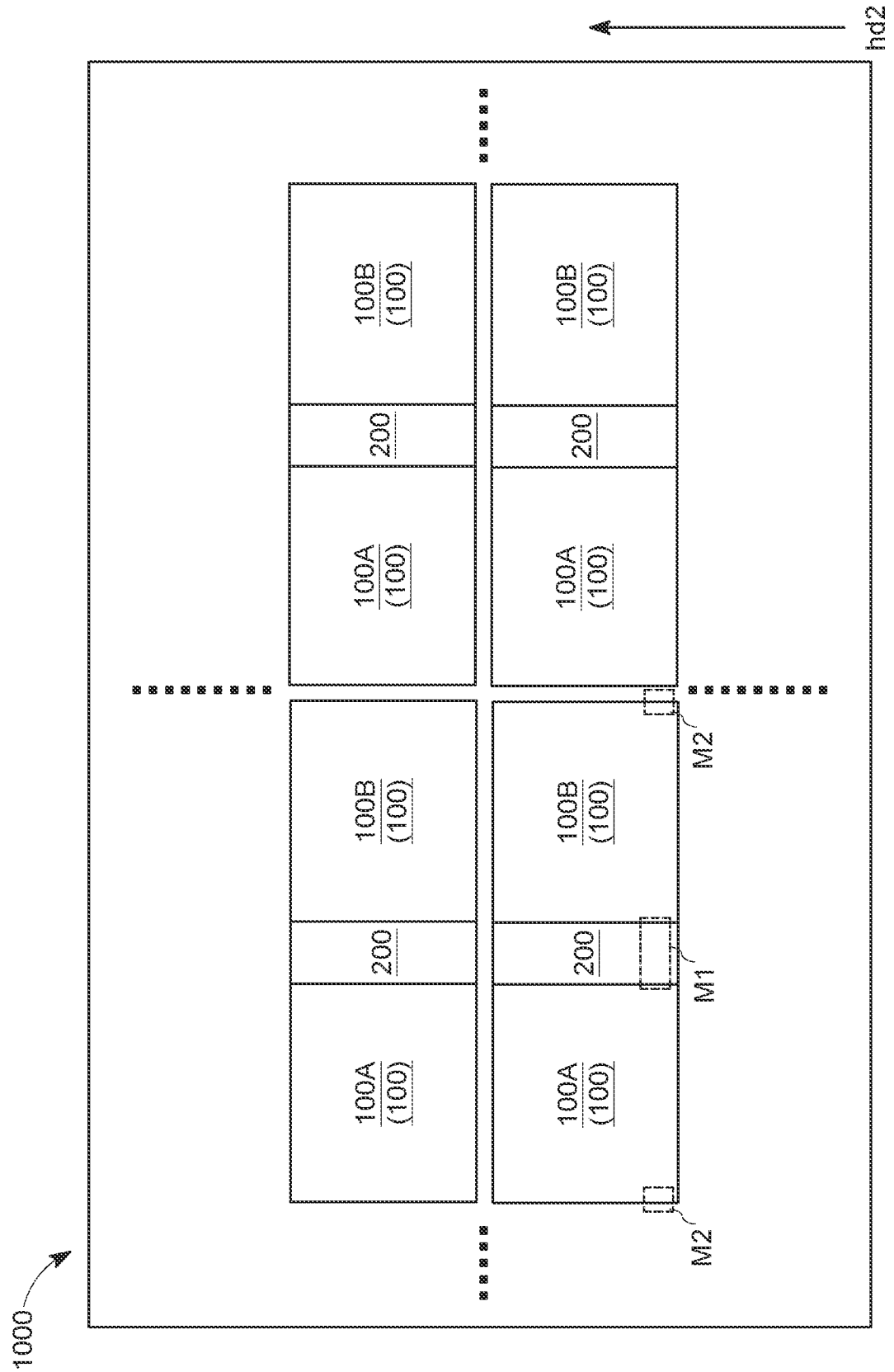

FIG. 1

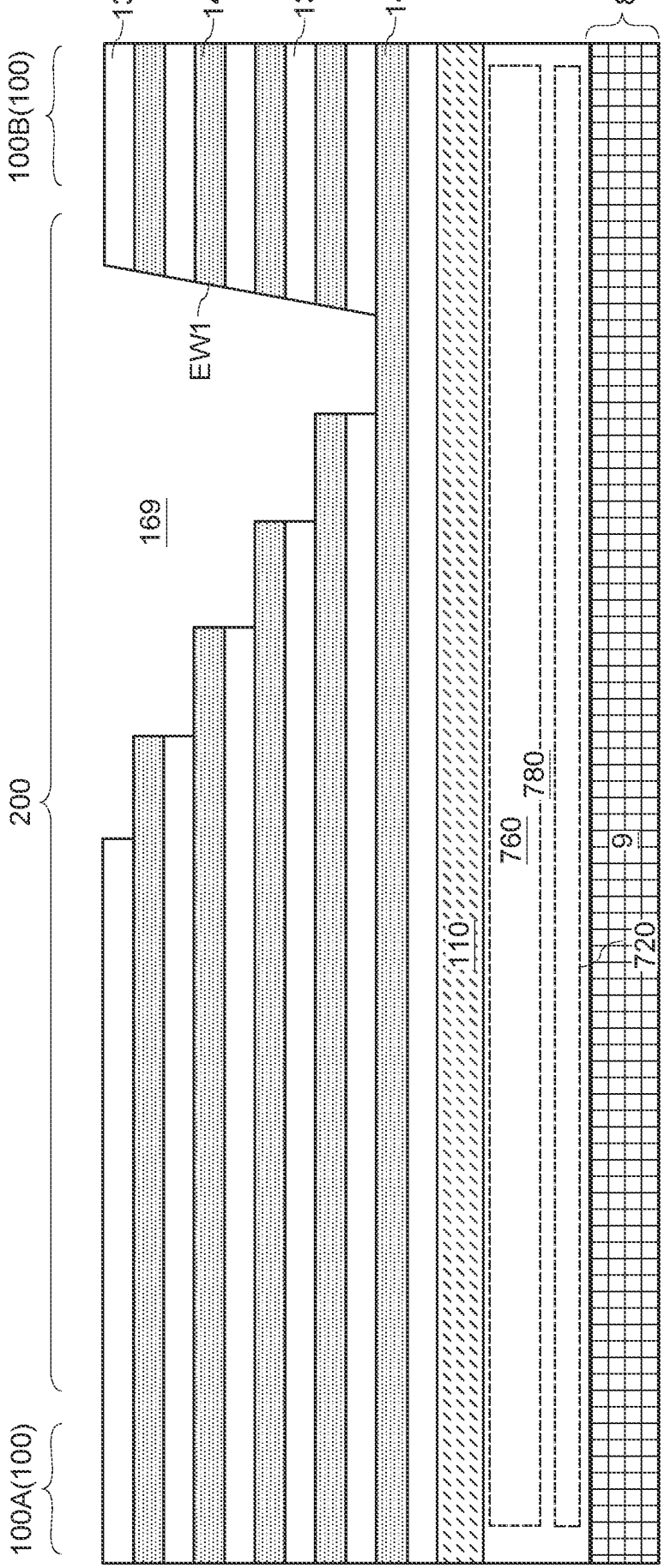
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FIG. 2A

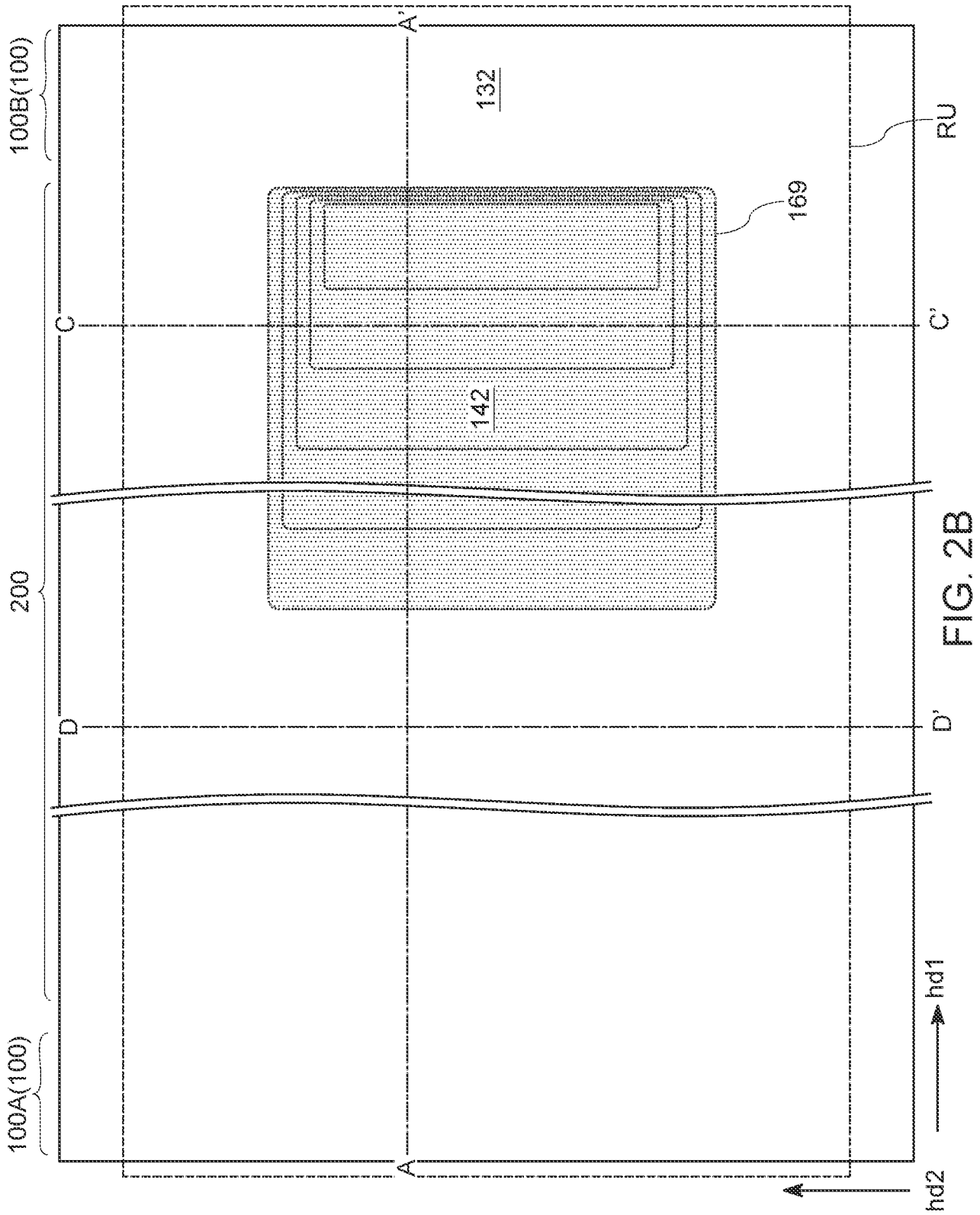

FIG. 2B

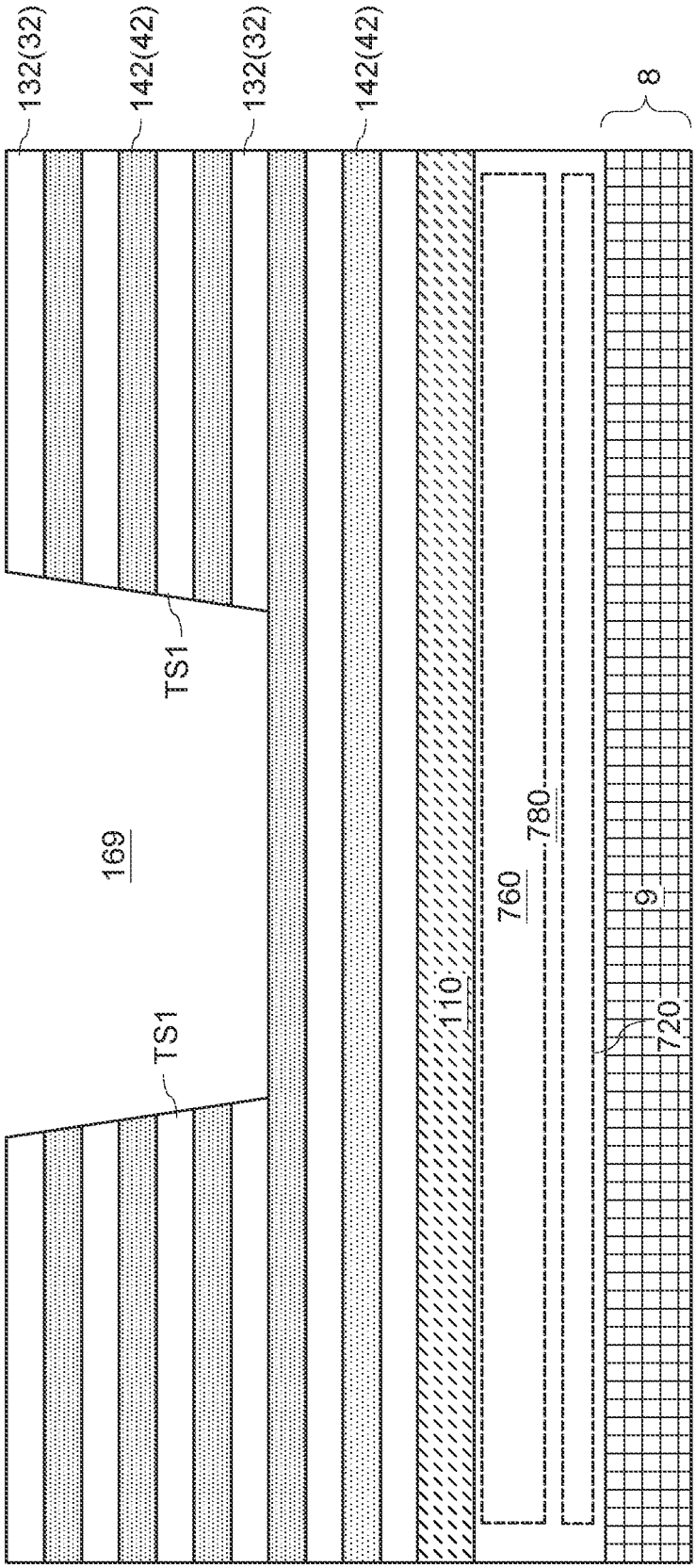

FIG. 2C

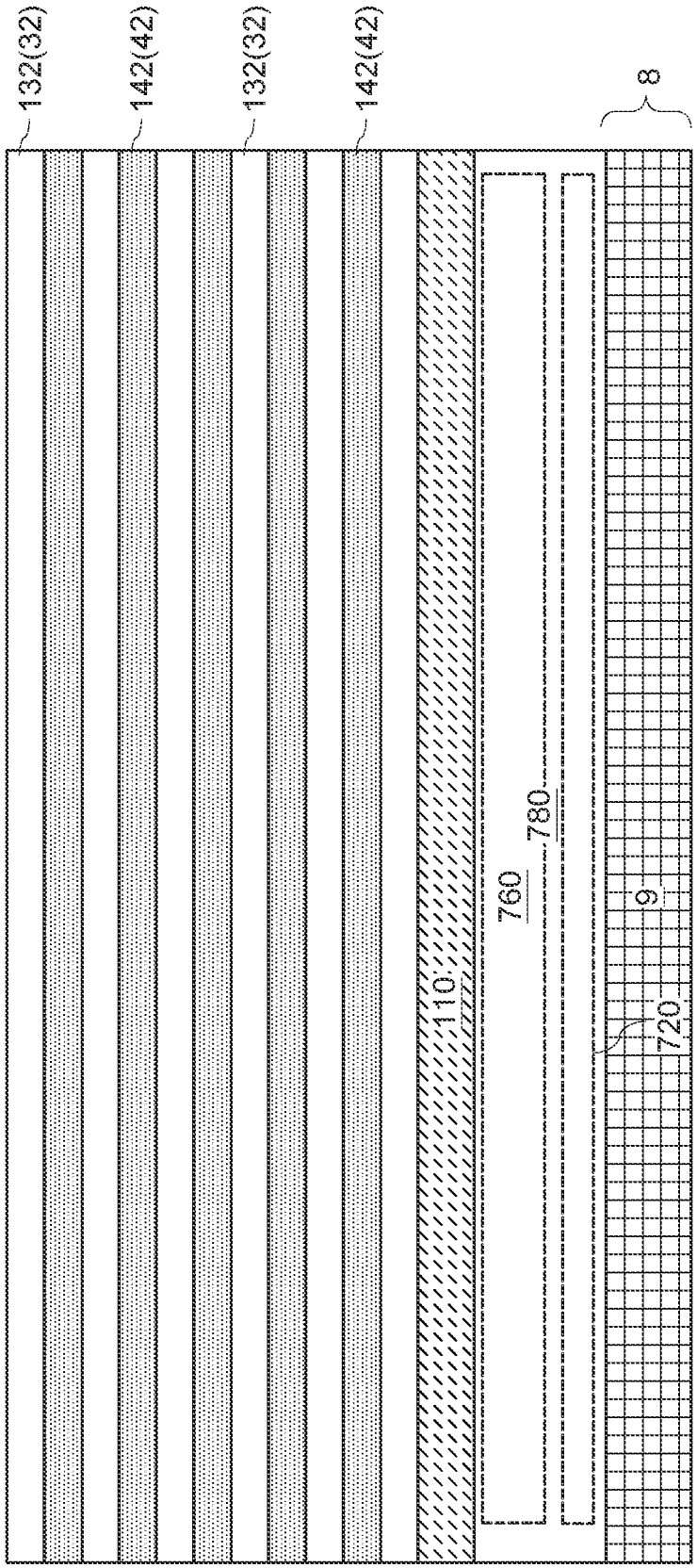

FIG. 2D

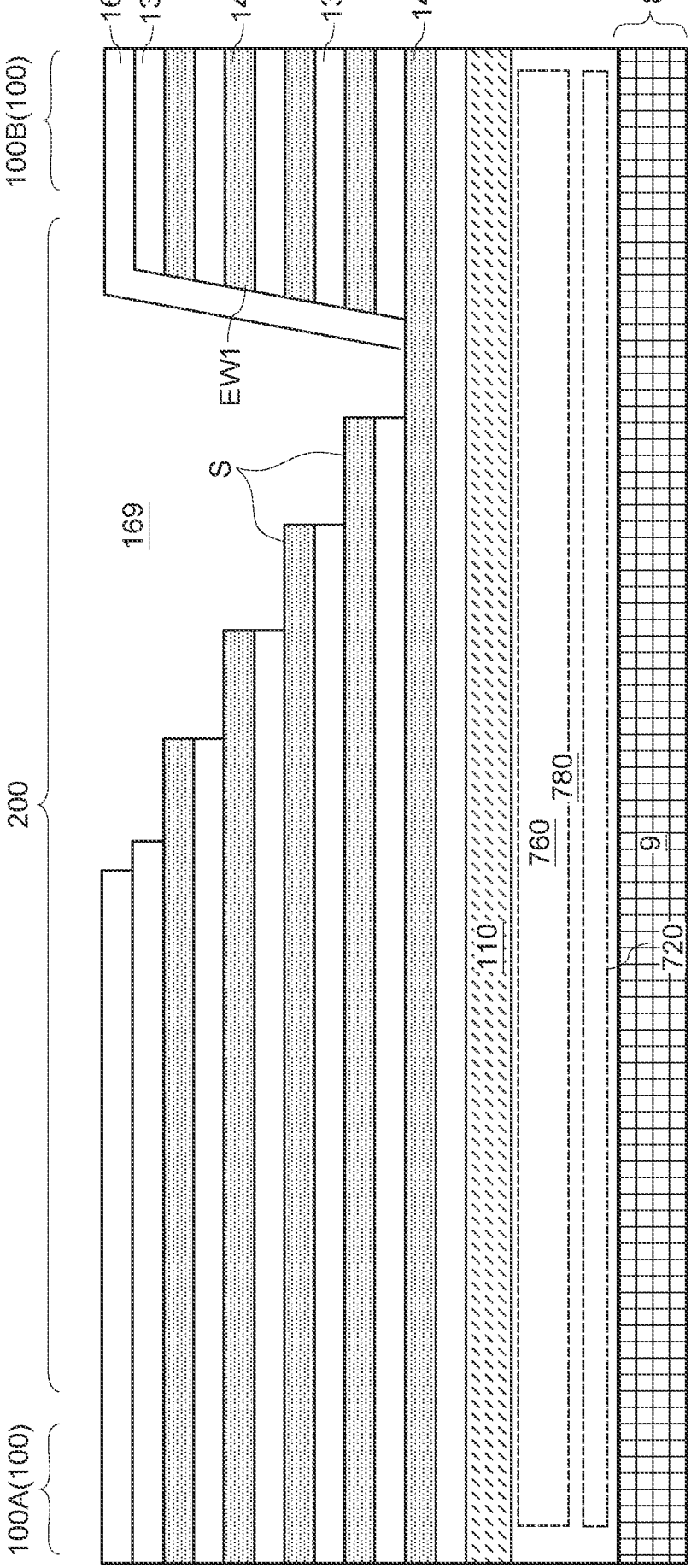
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FIG. 3A

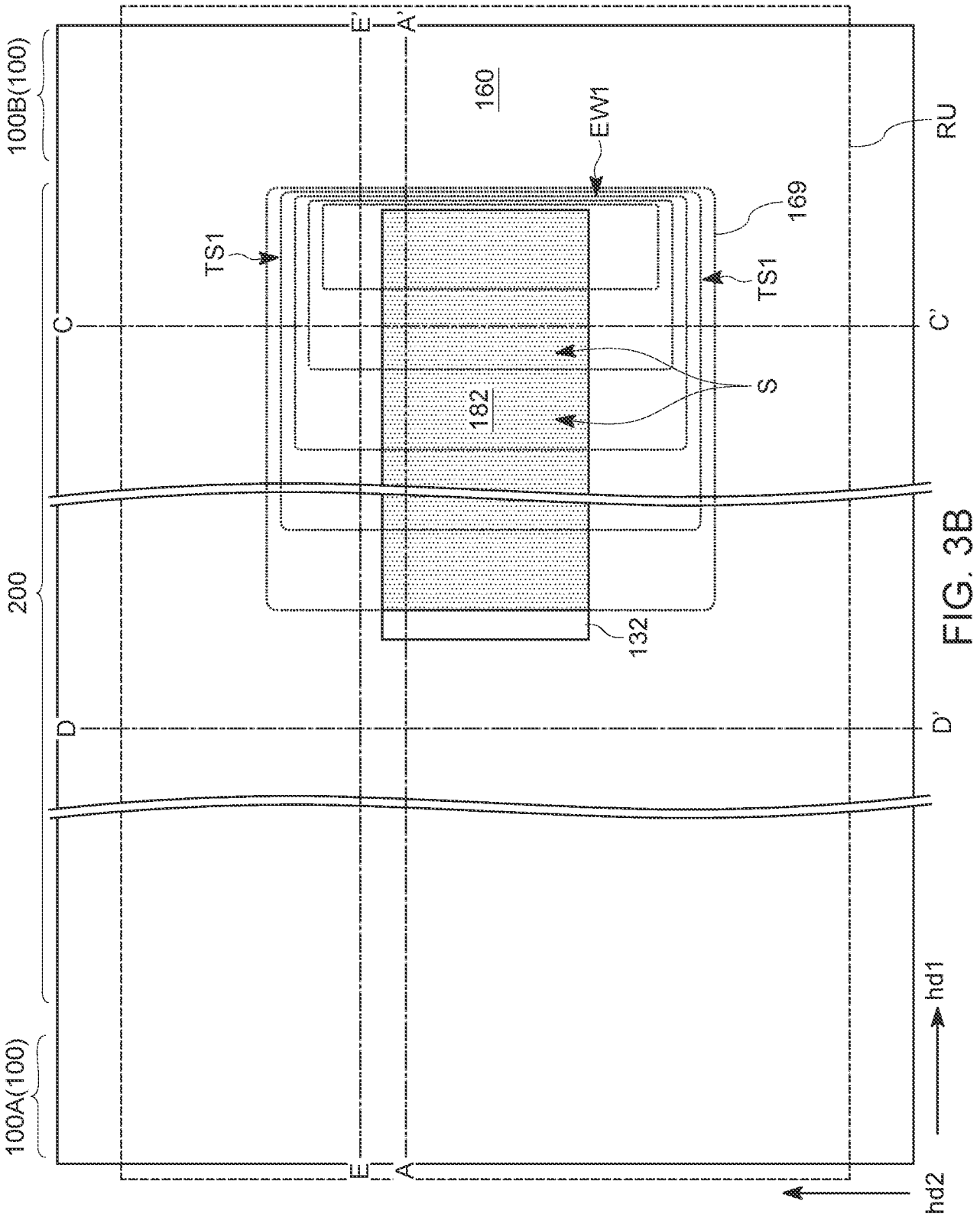
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FIG. 3B

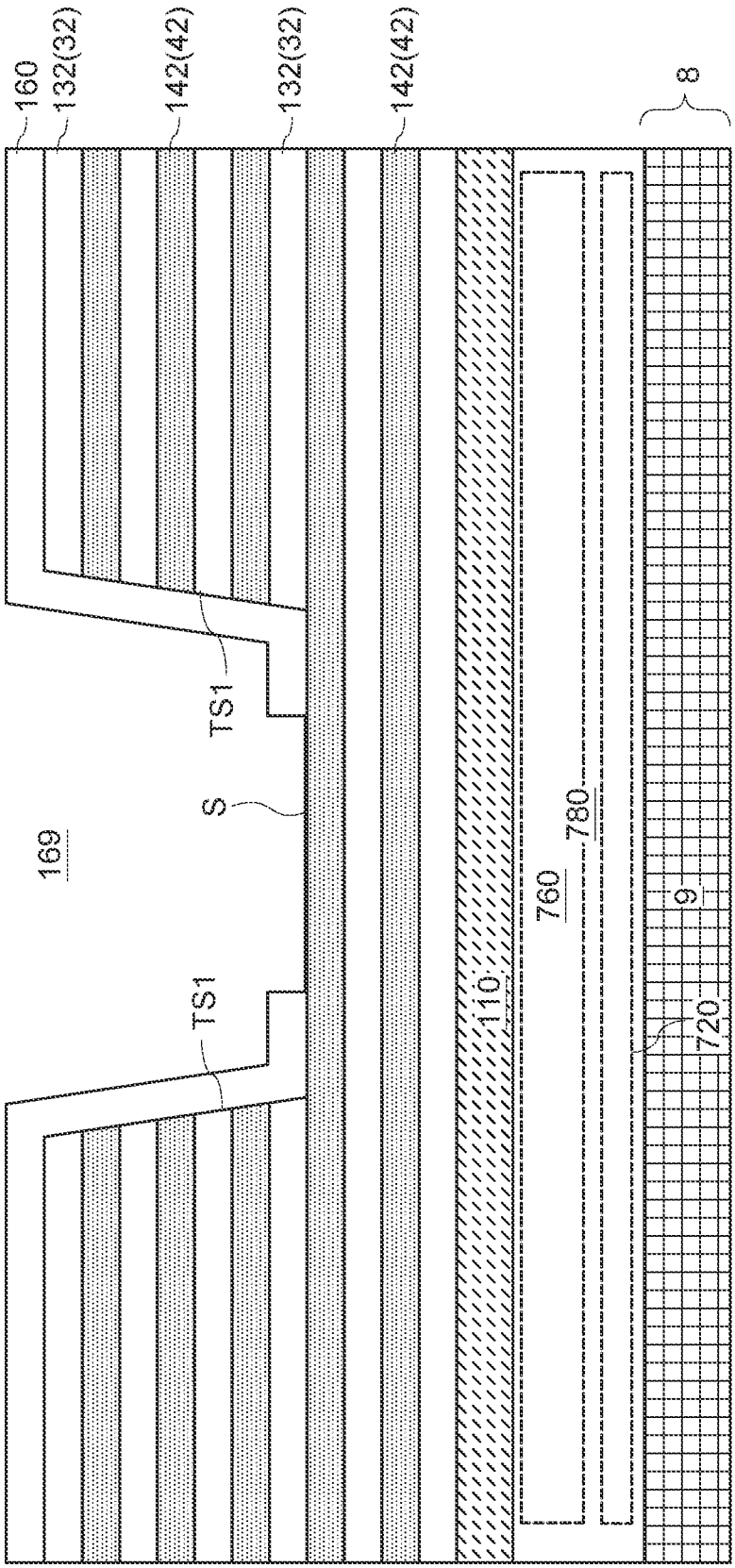

FIG. 3C

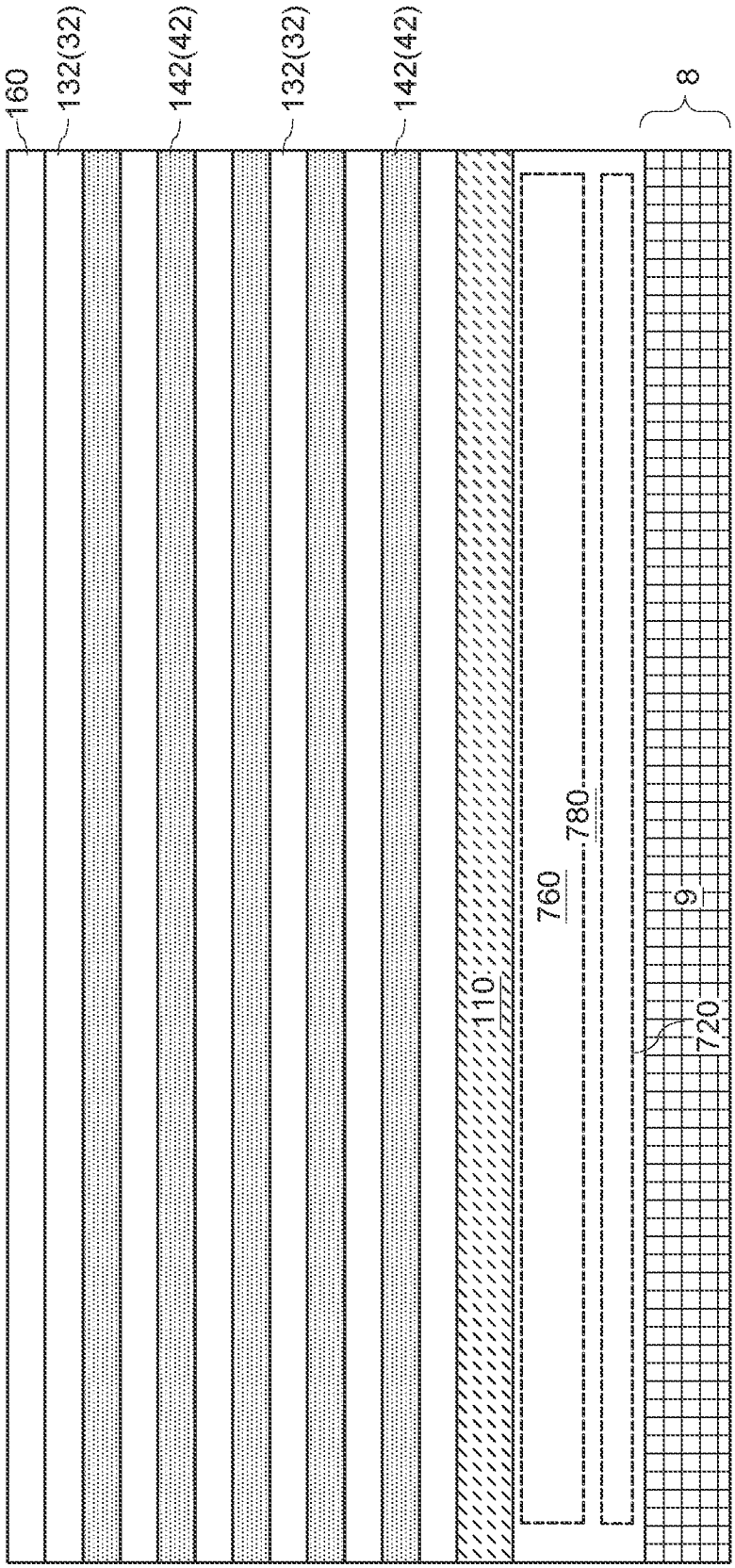

FIG. 3D

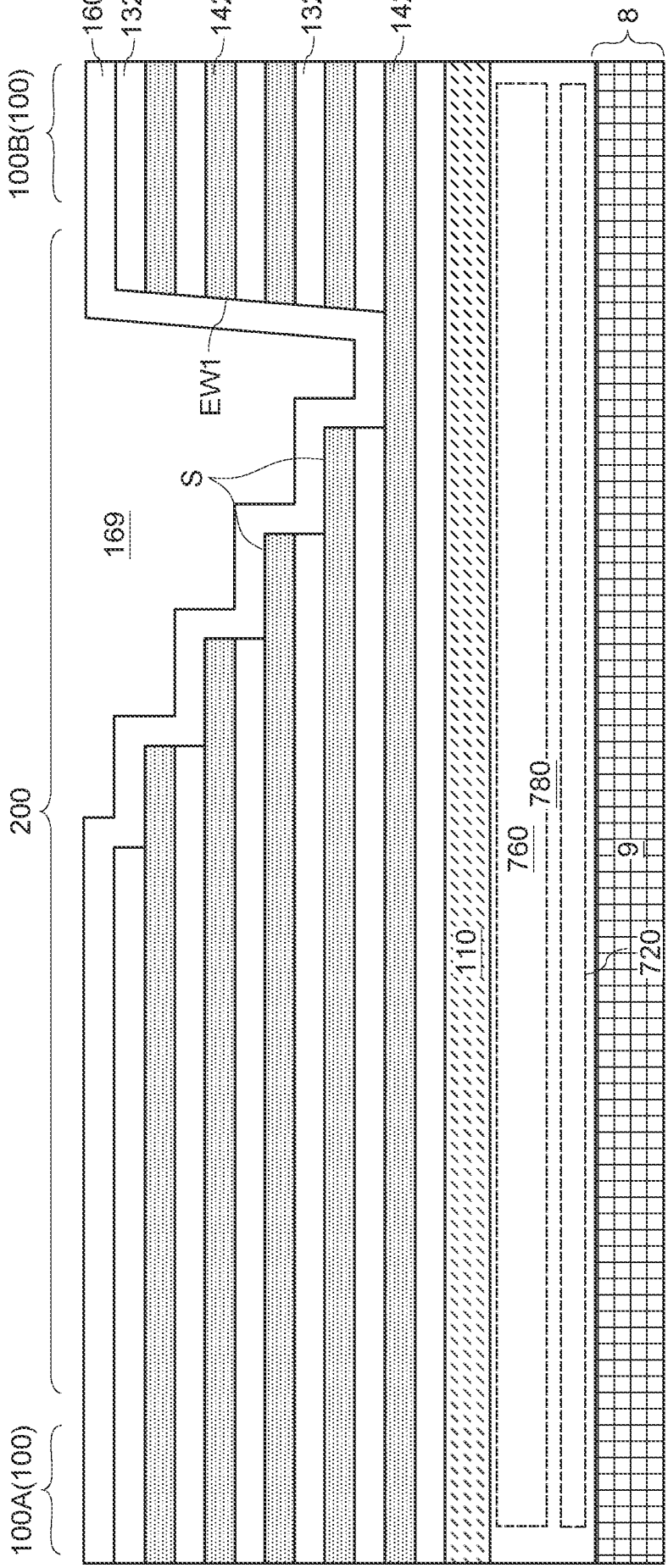
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FIG. 3E

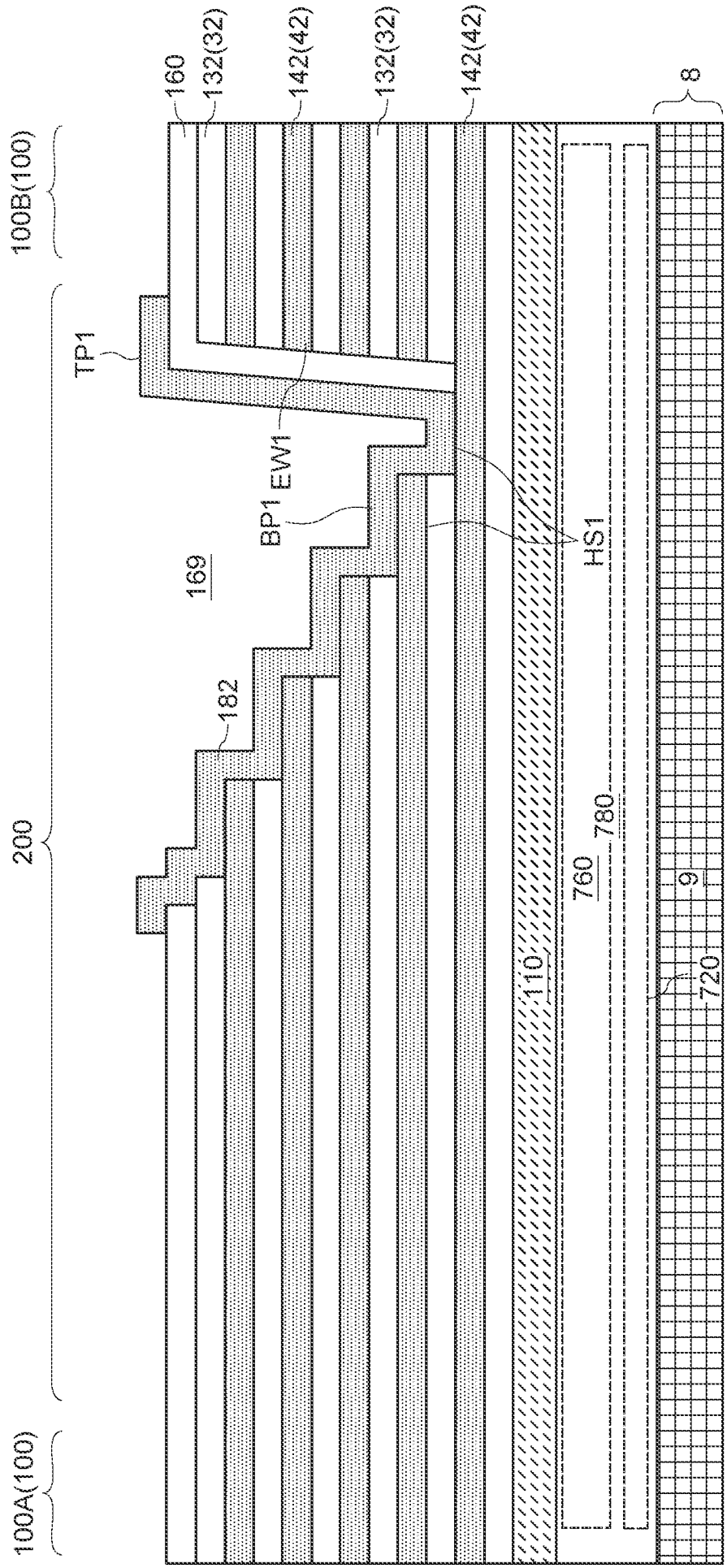
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FIG. 4A

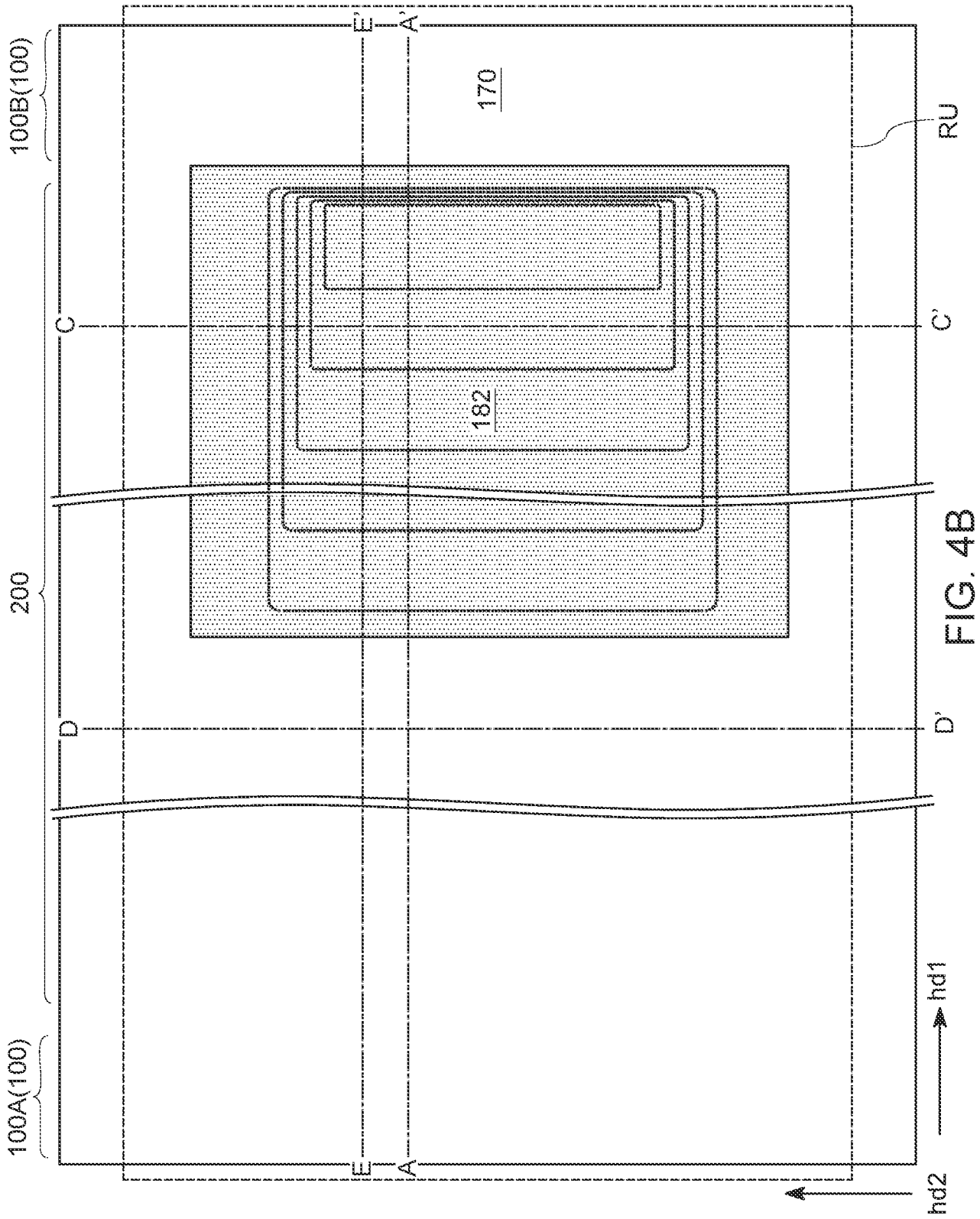

FIG. 4B

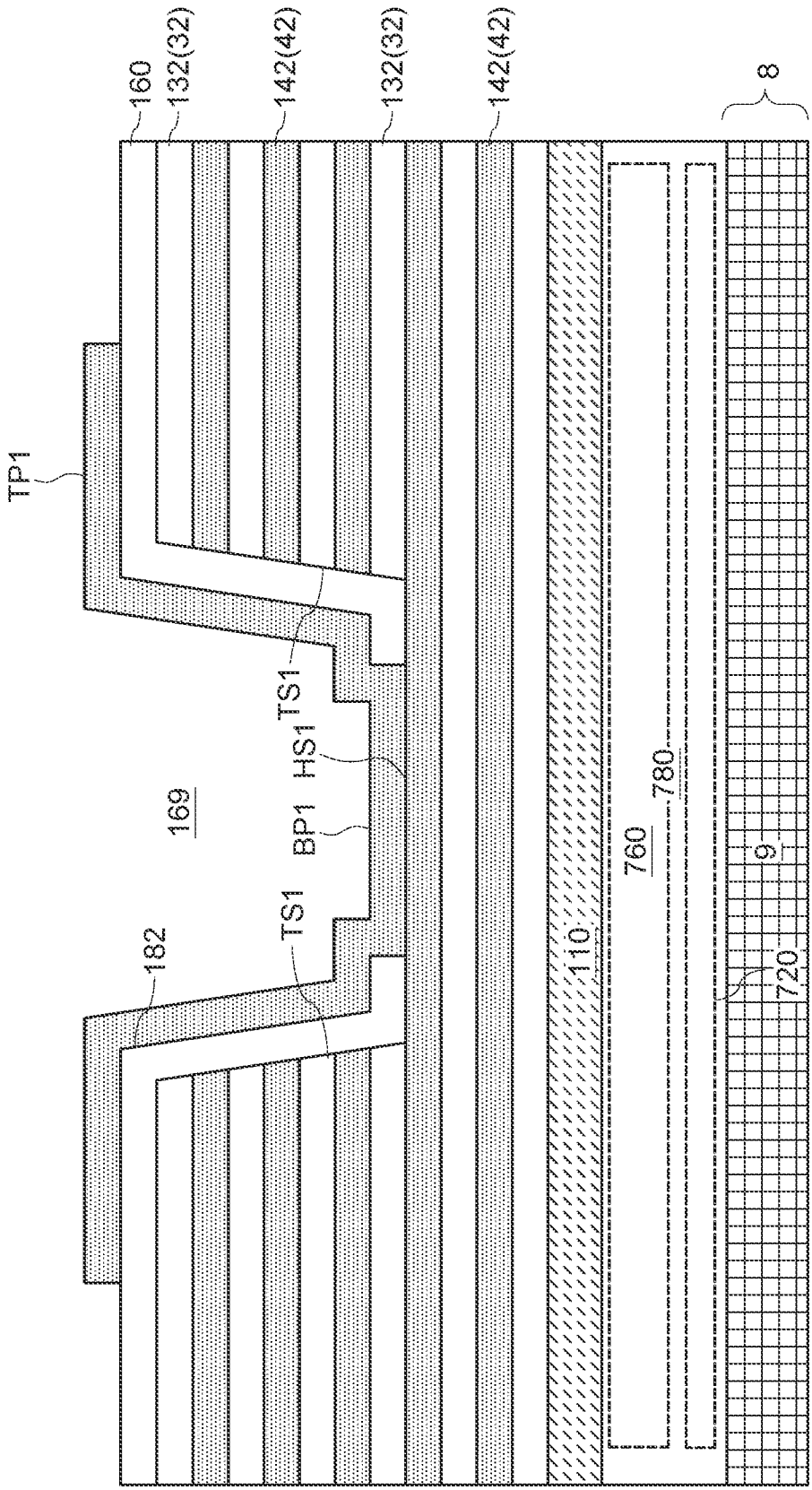
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FIG. 4C

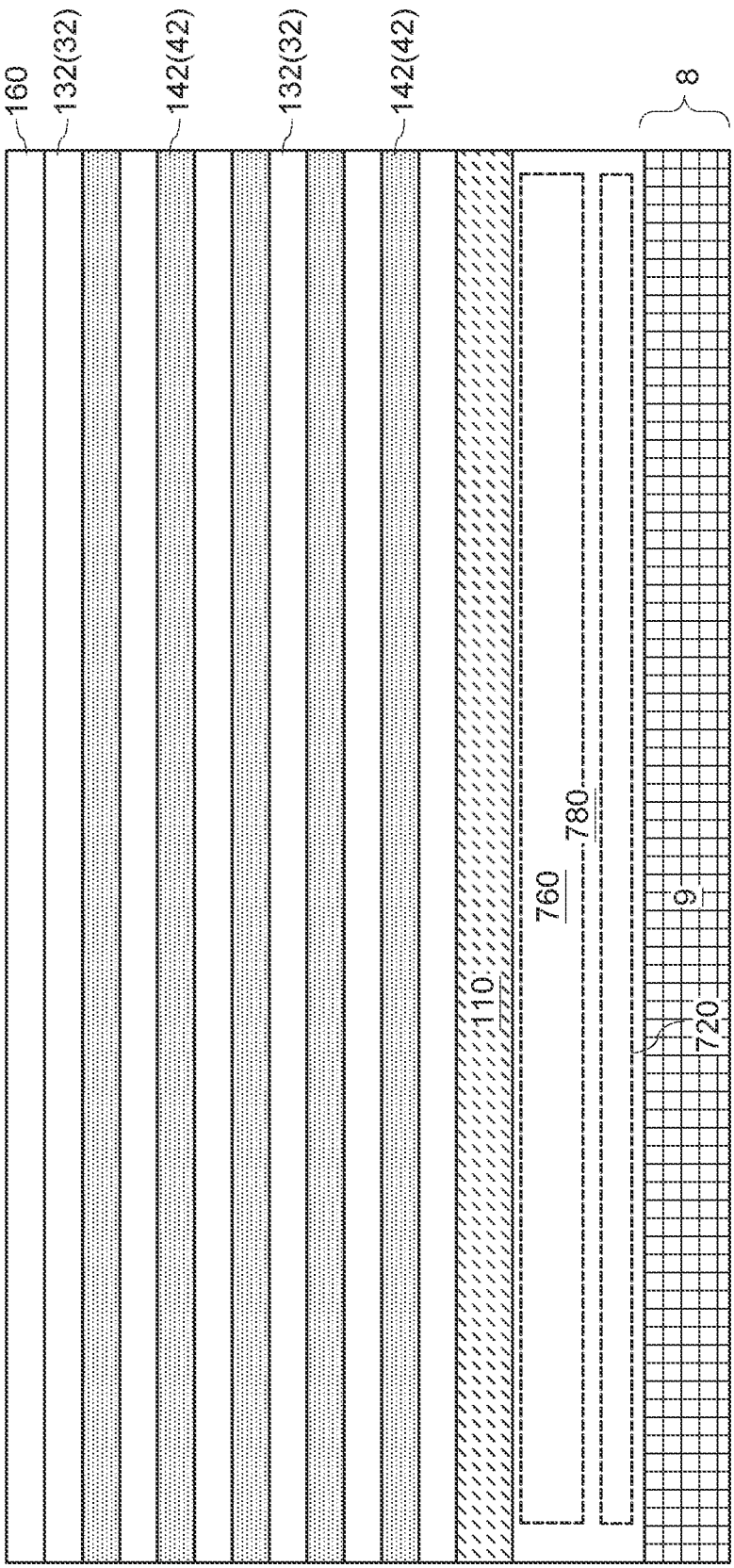

FIG. 4D

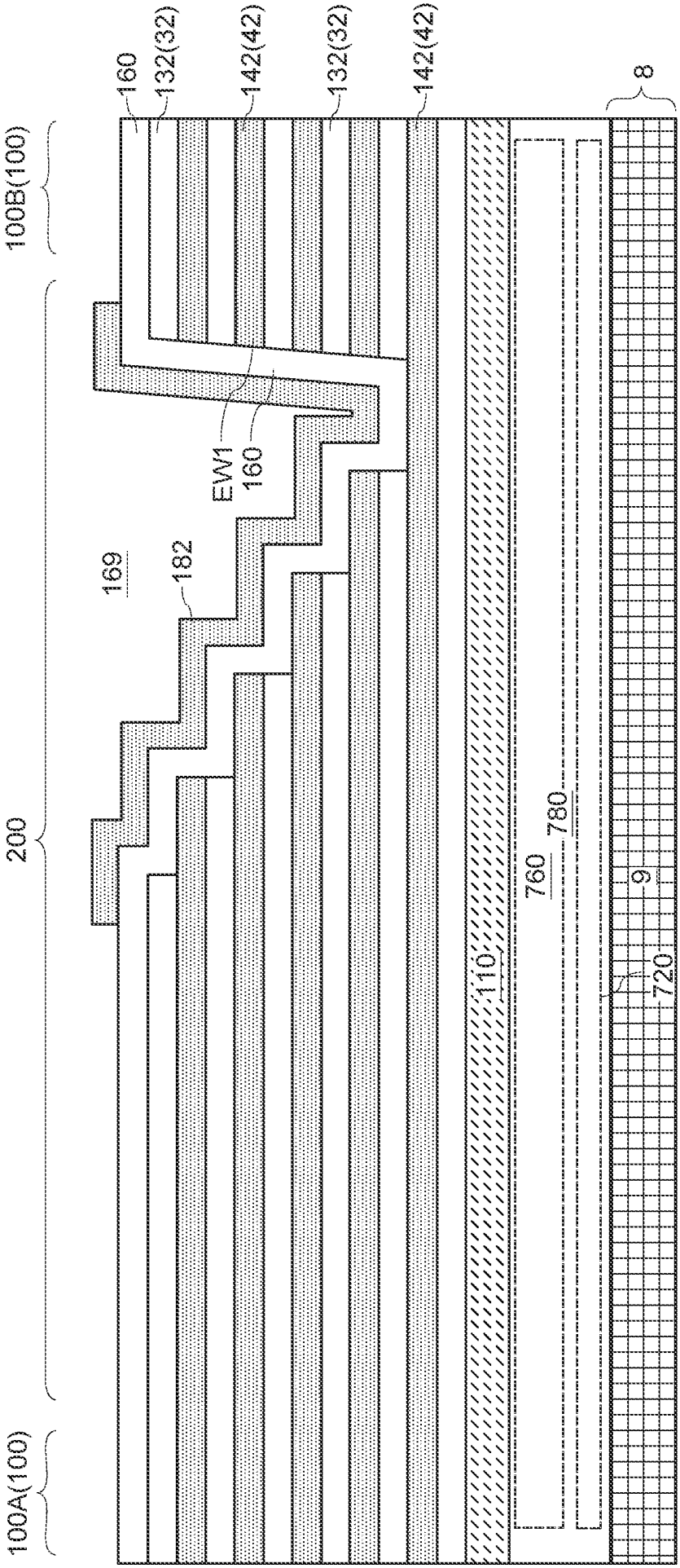
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FIG. 4E

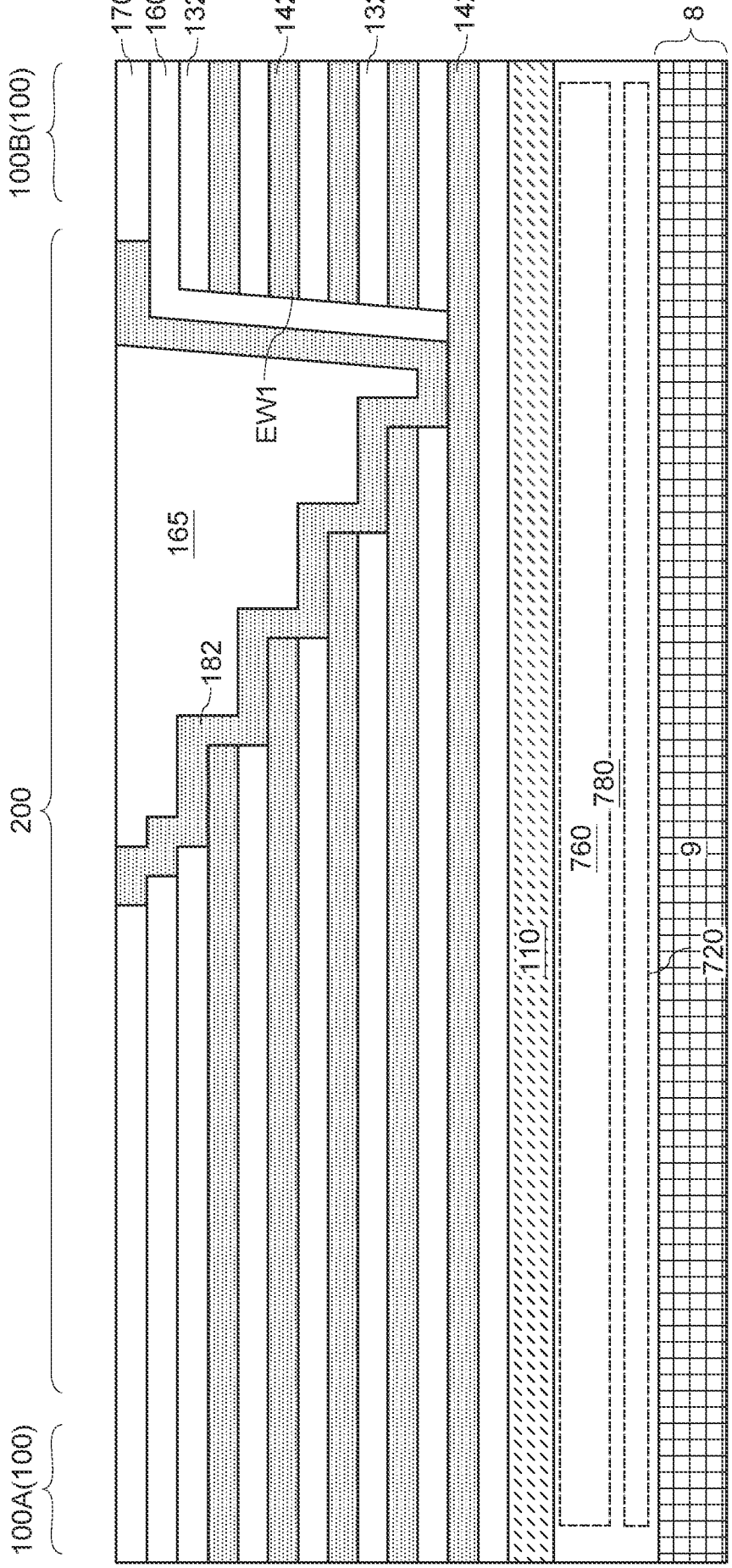
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FIG. 5A

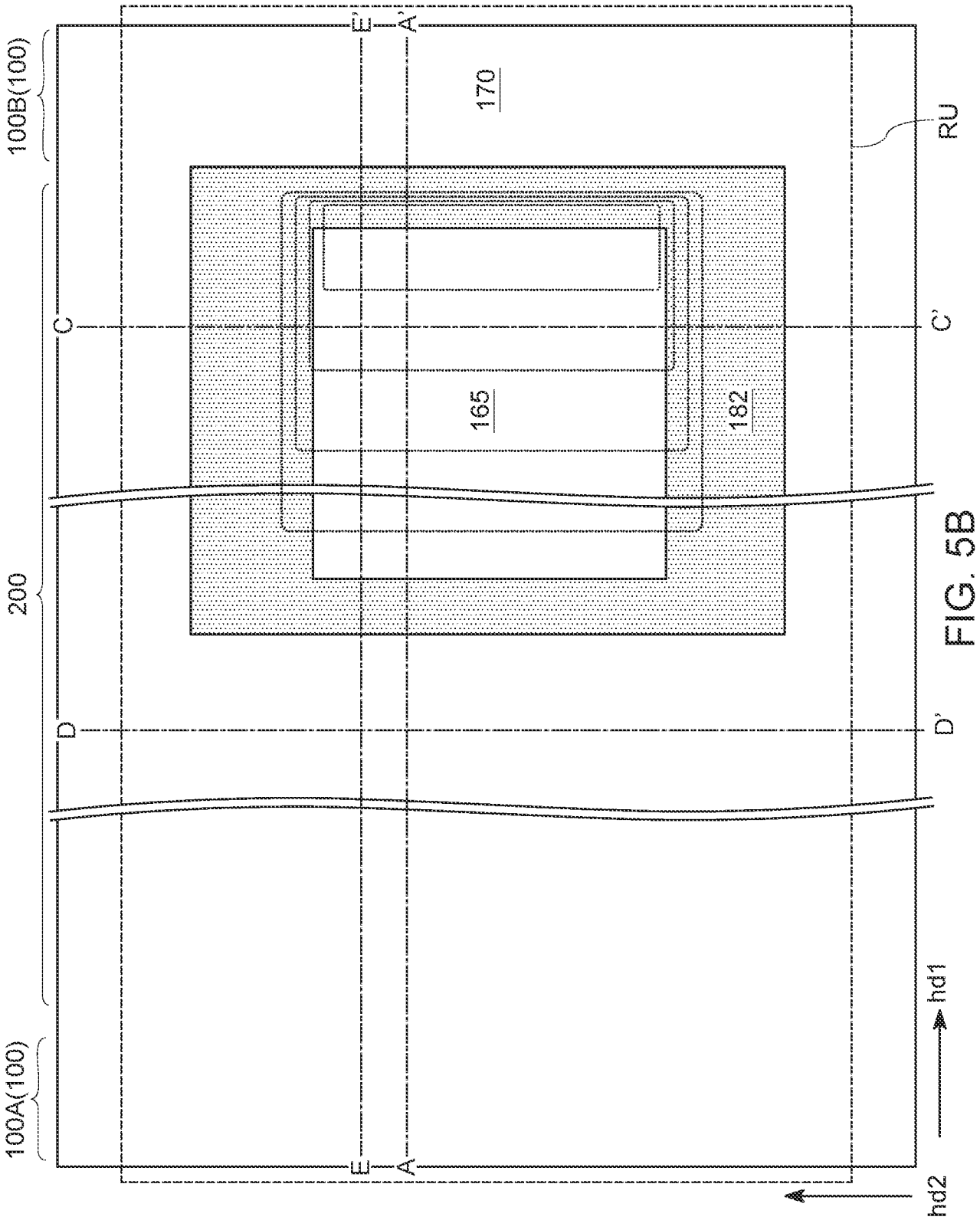

FIG. 5B

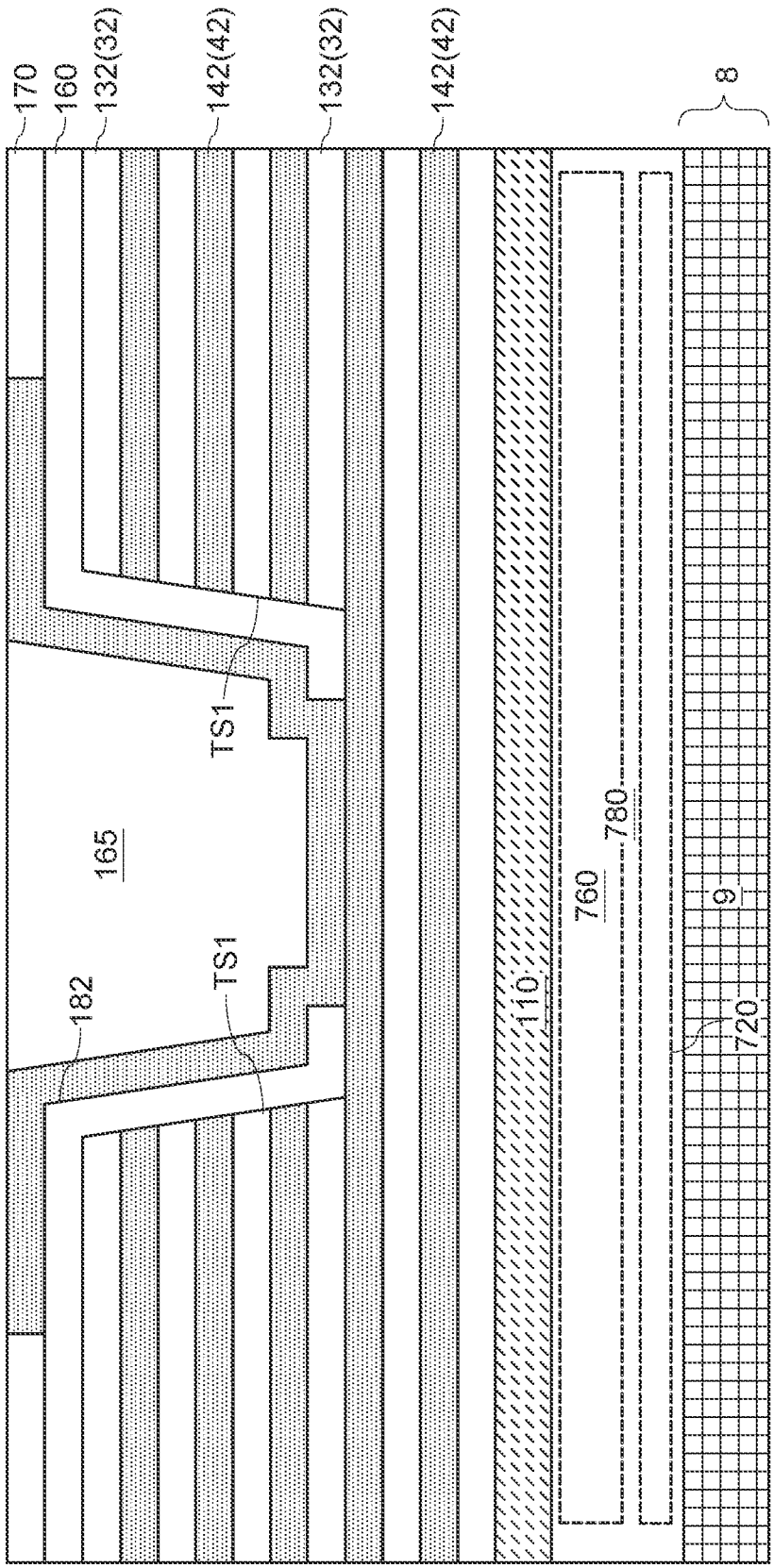
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FIG. 5C

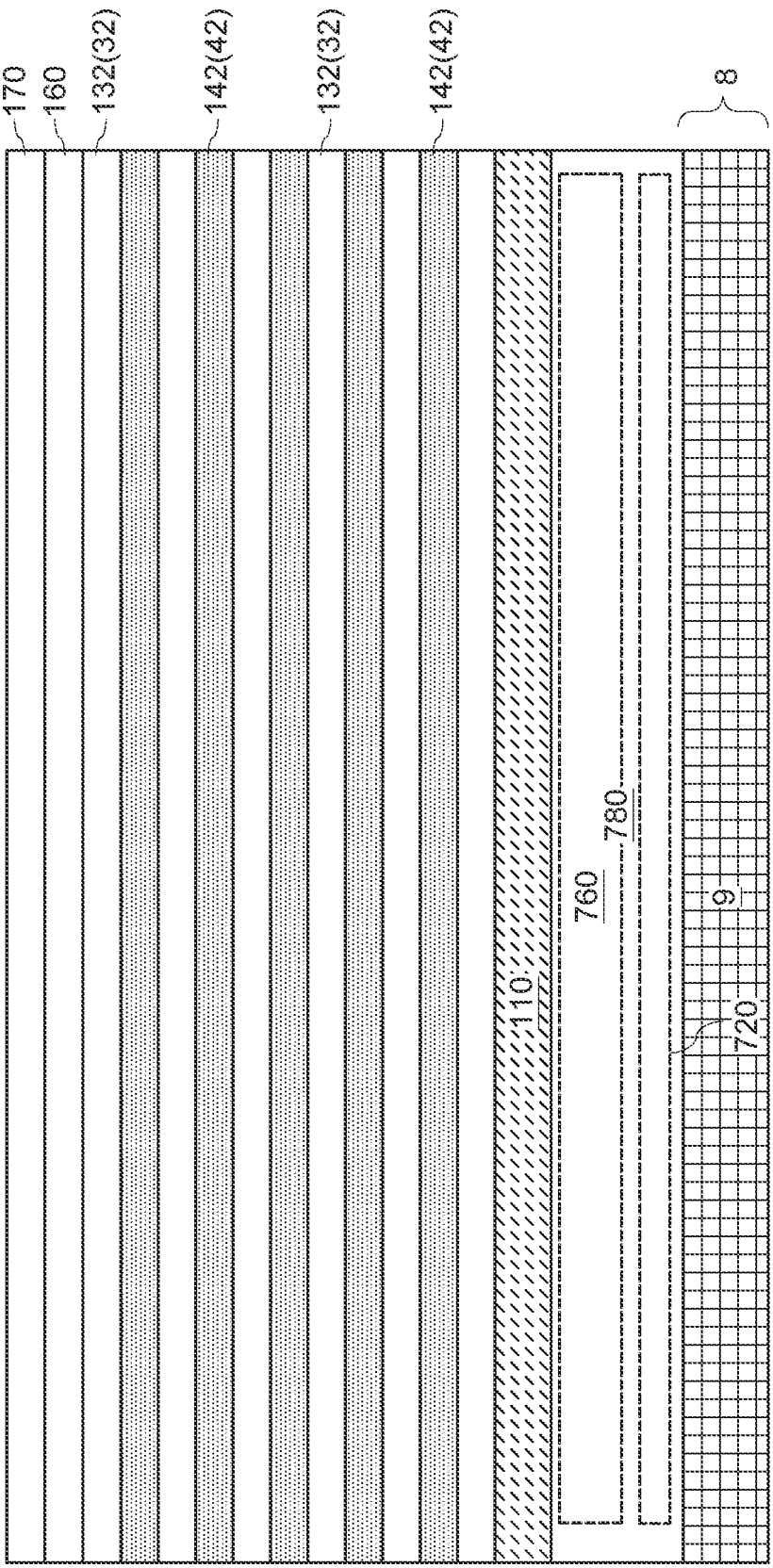

FIG. 5D

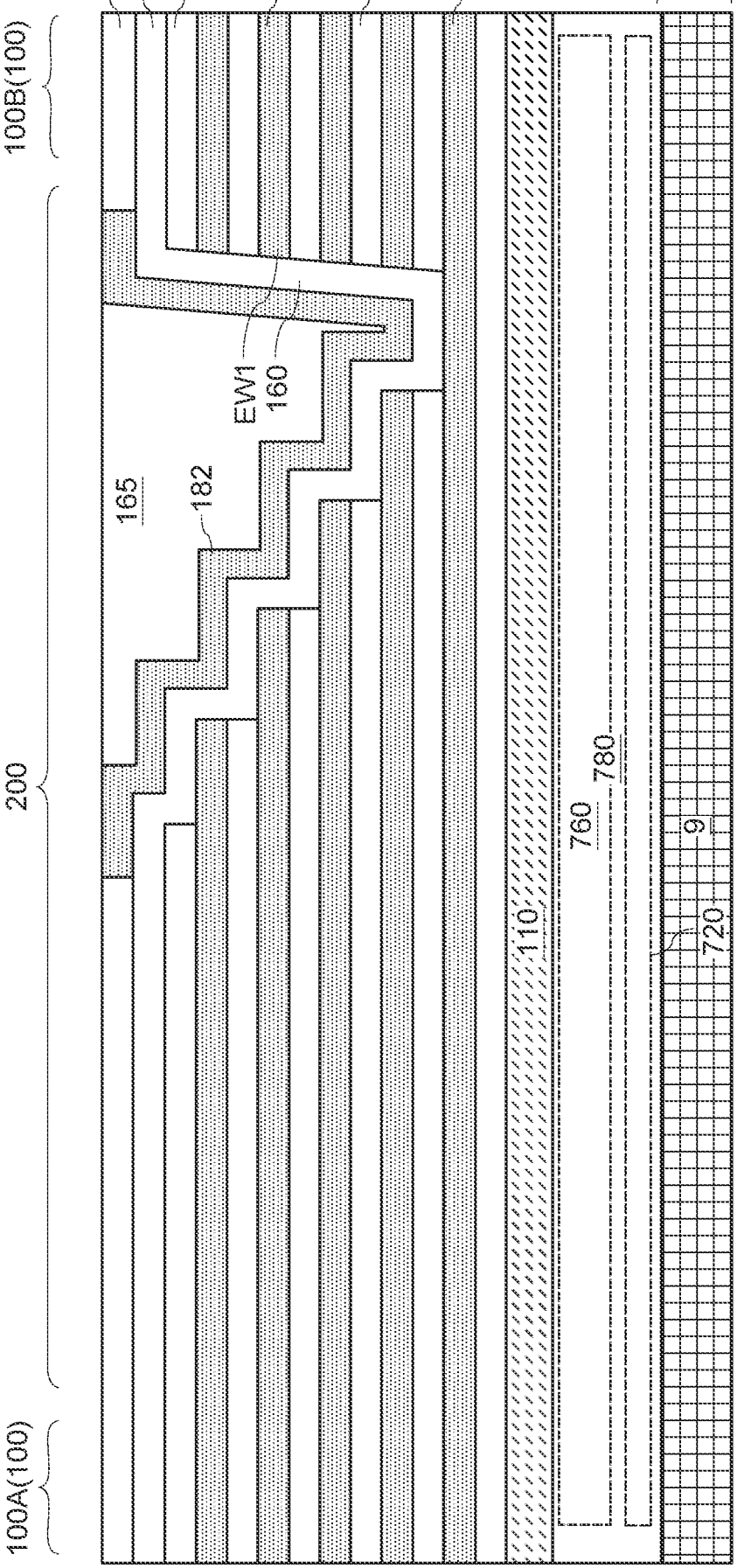
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FIG. 5E

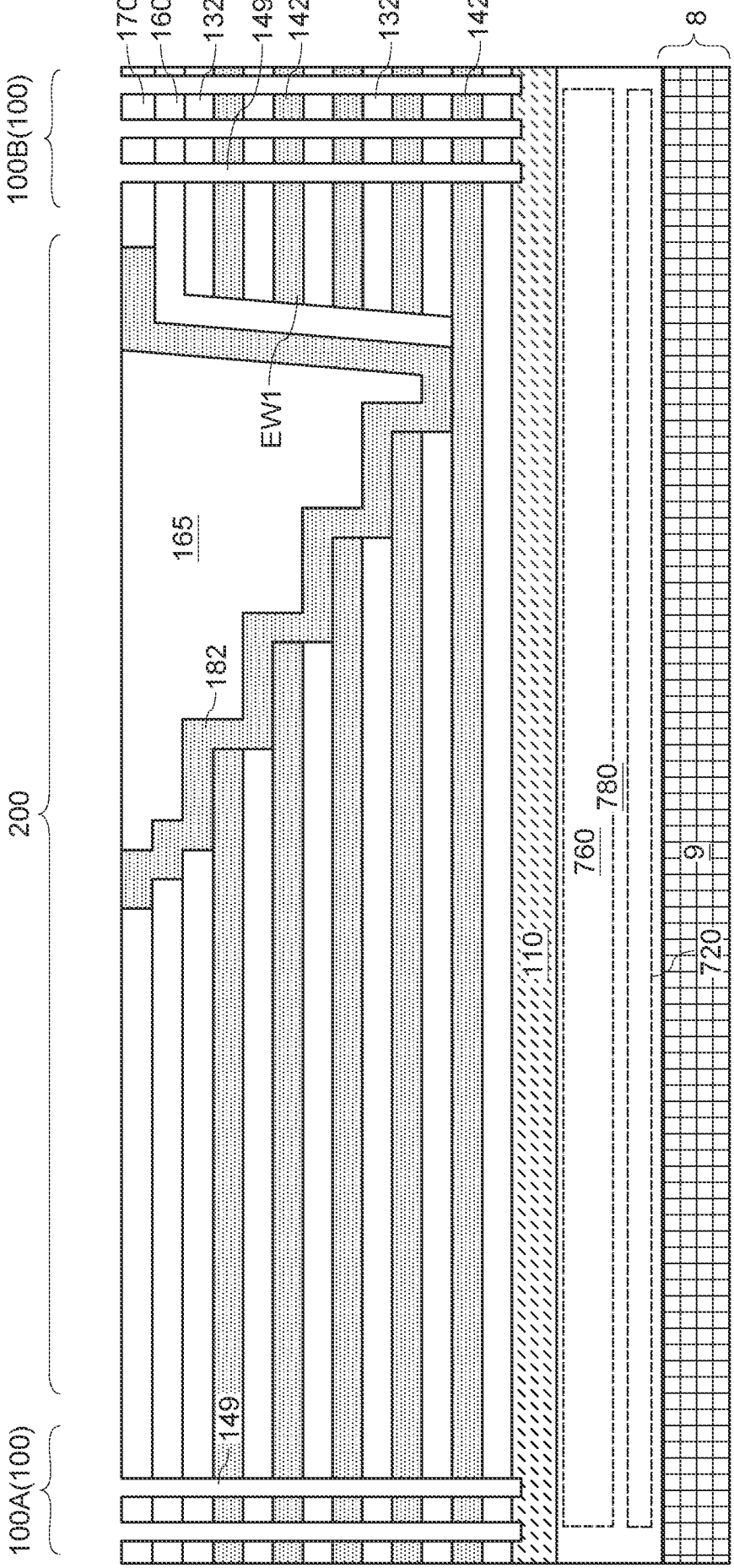
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FIG. 6A

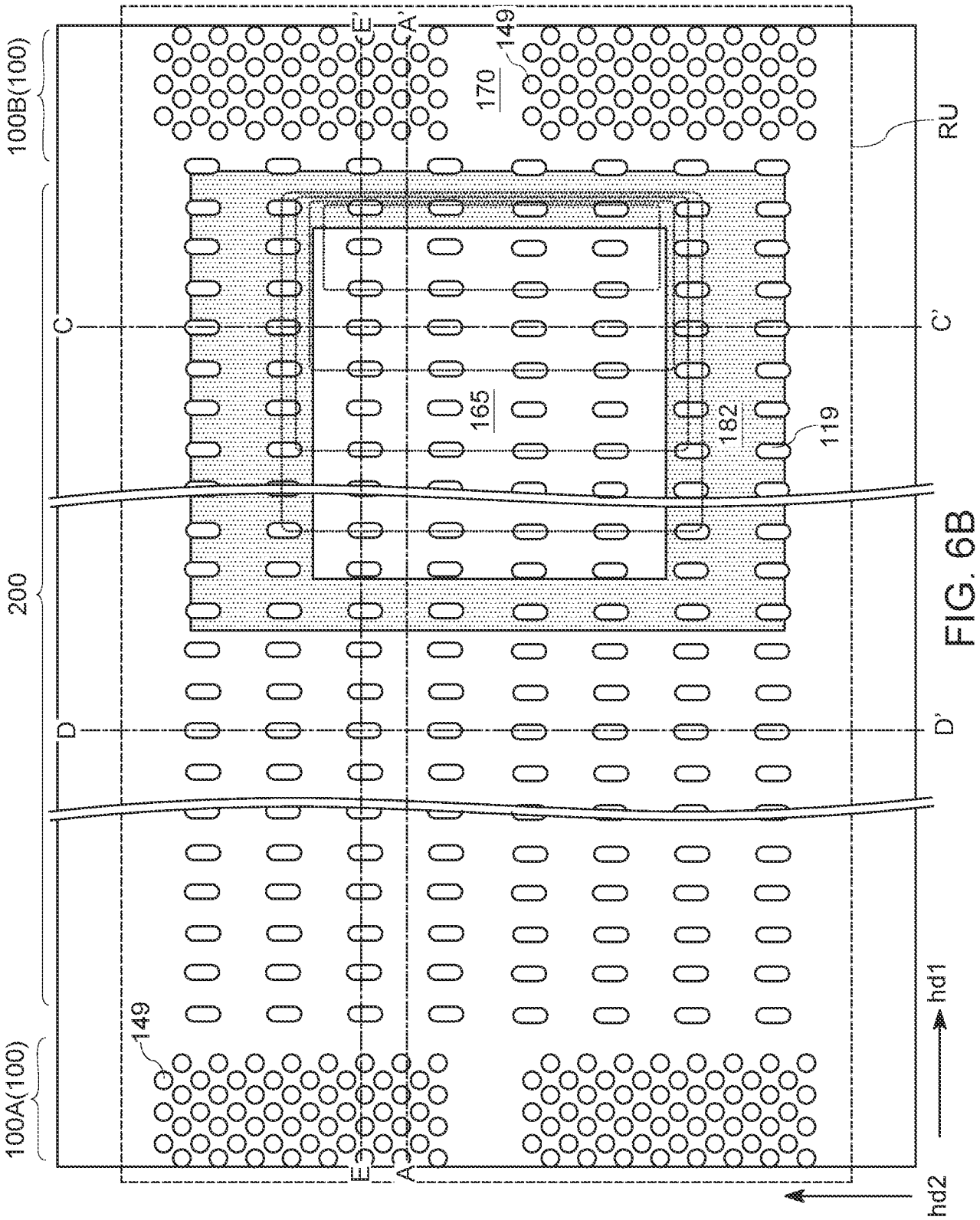

FIG. 6B

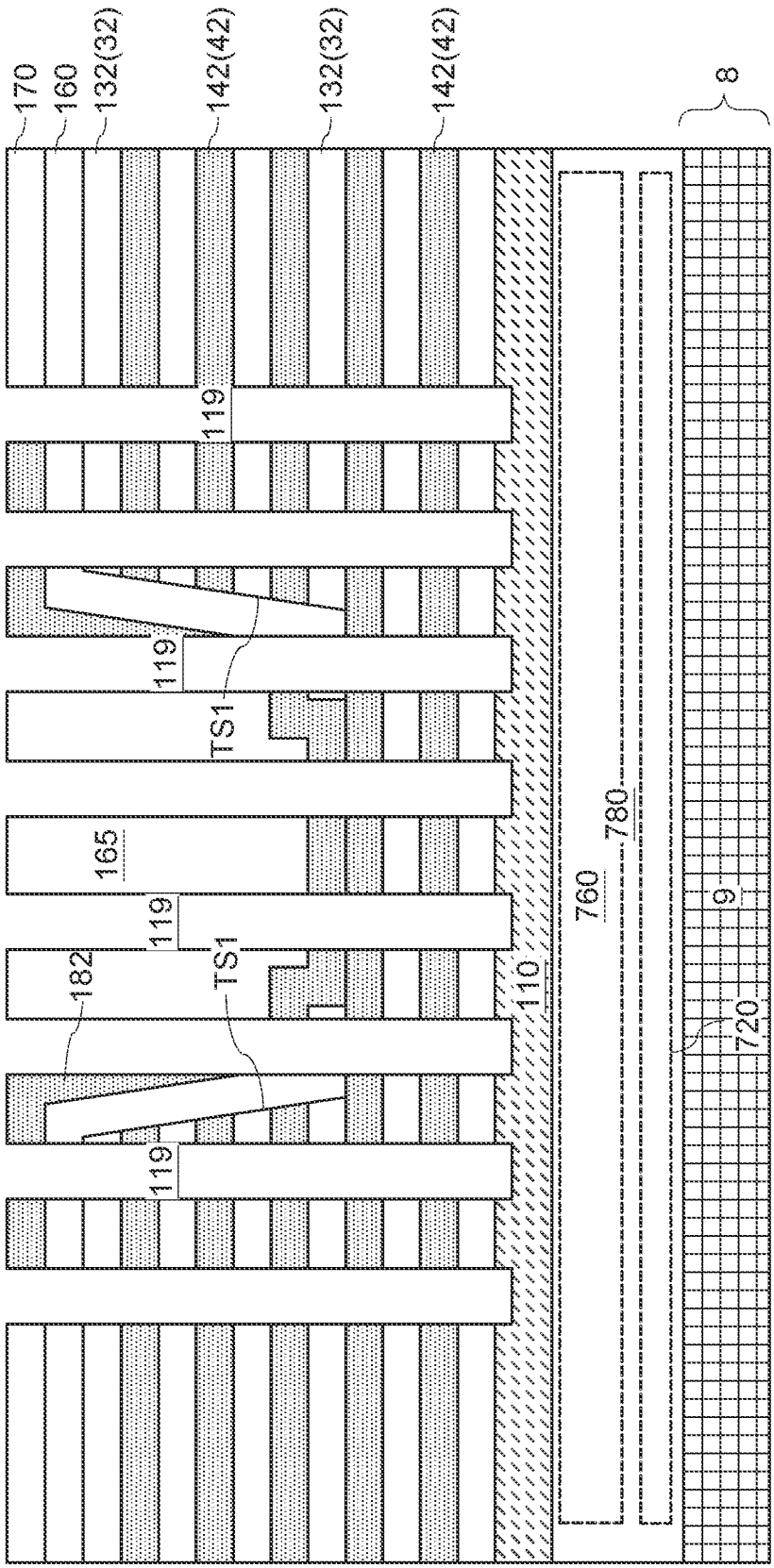
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FIG. 6C

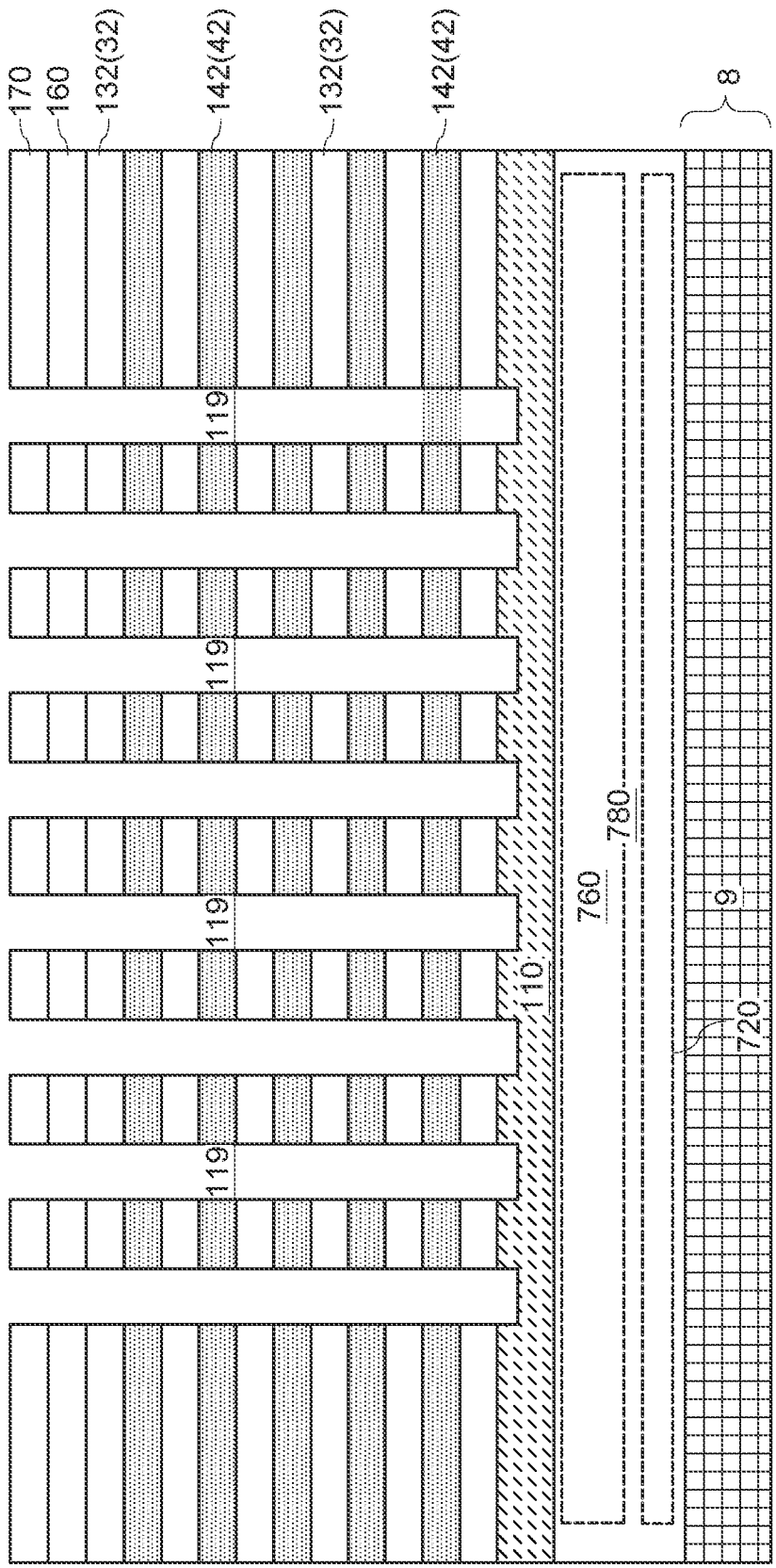
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FIG. 6D

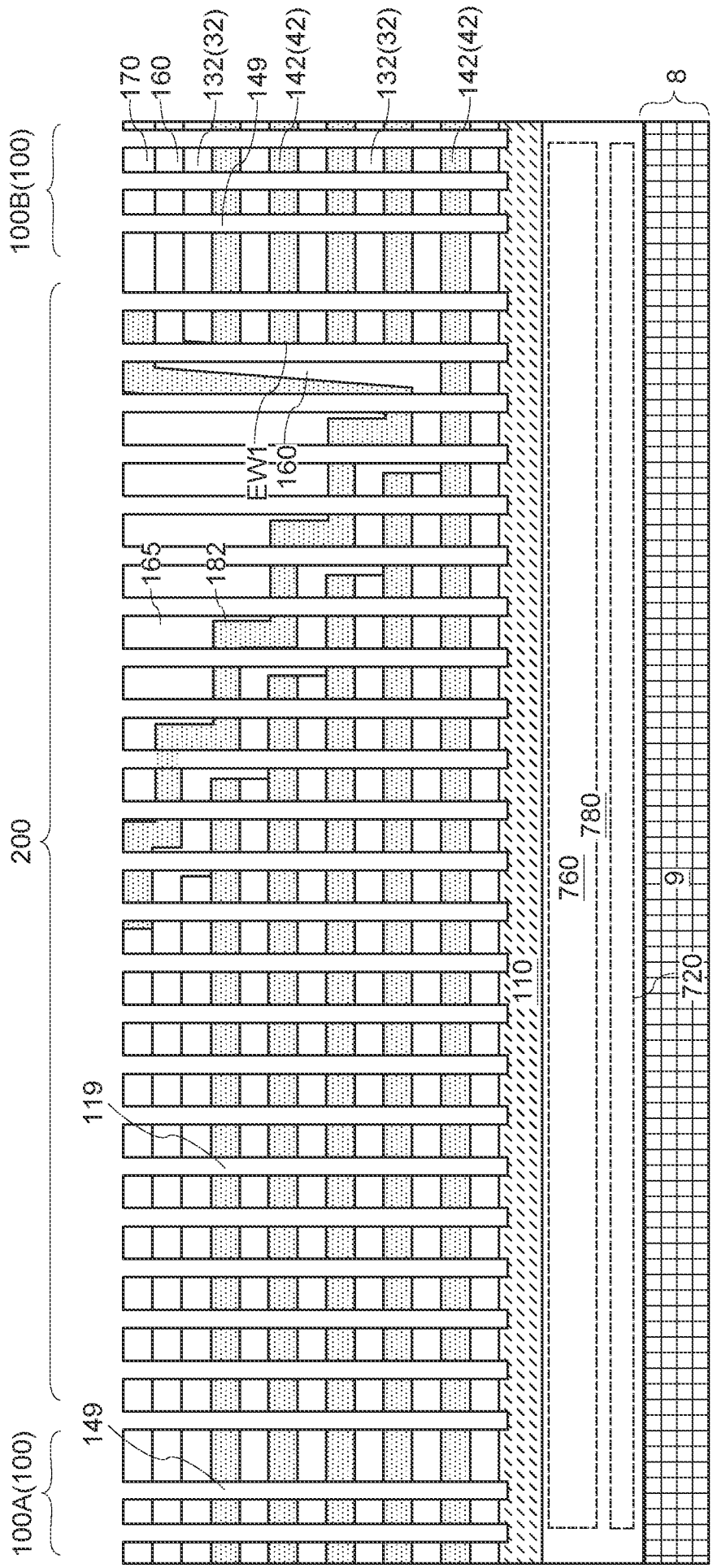
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FIG. 6E

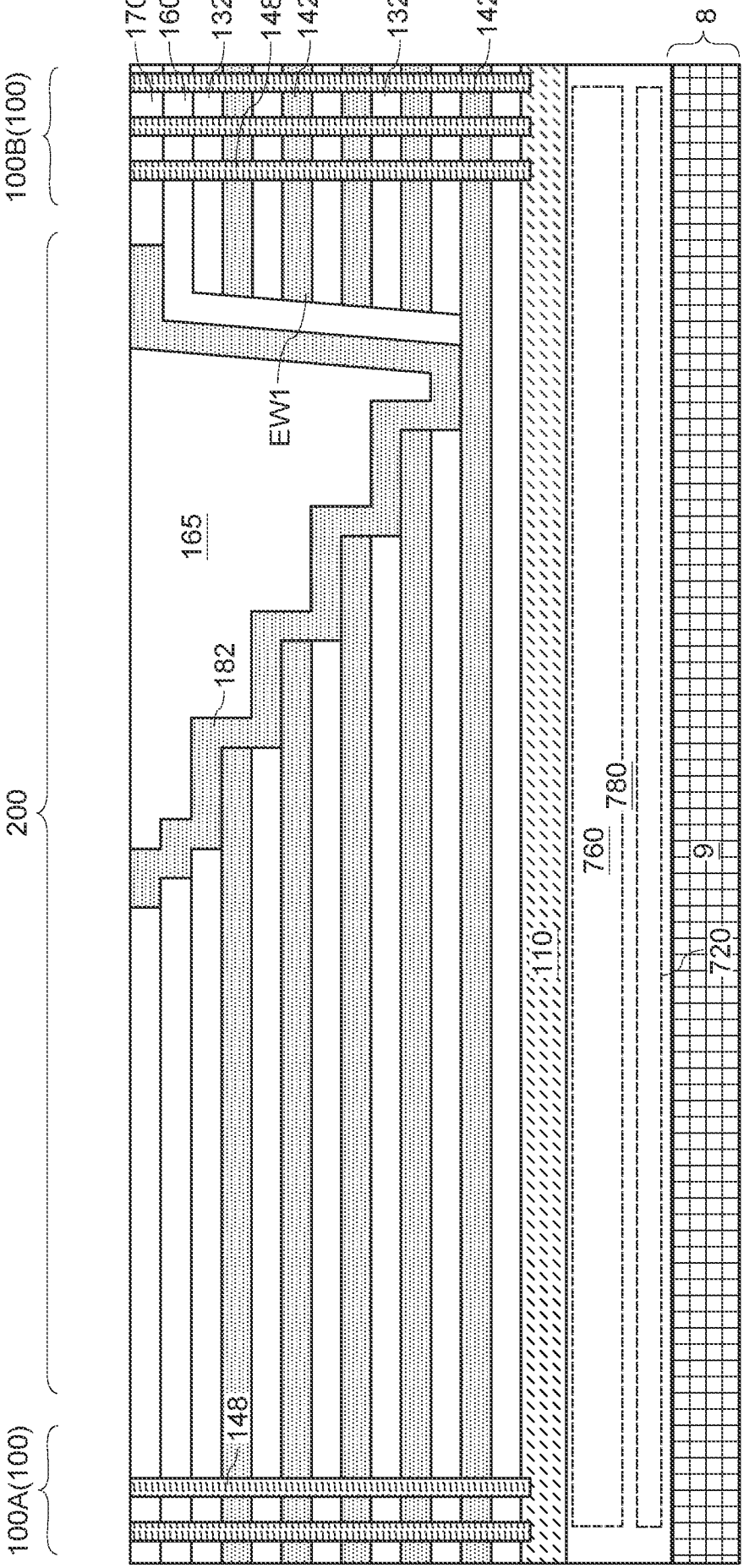
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FIG. 7A

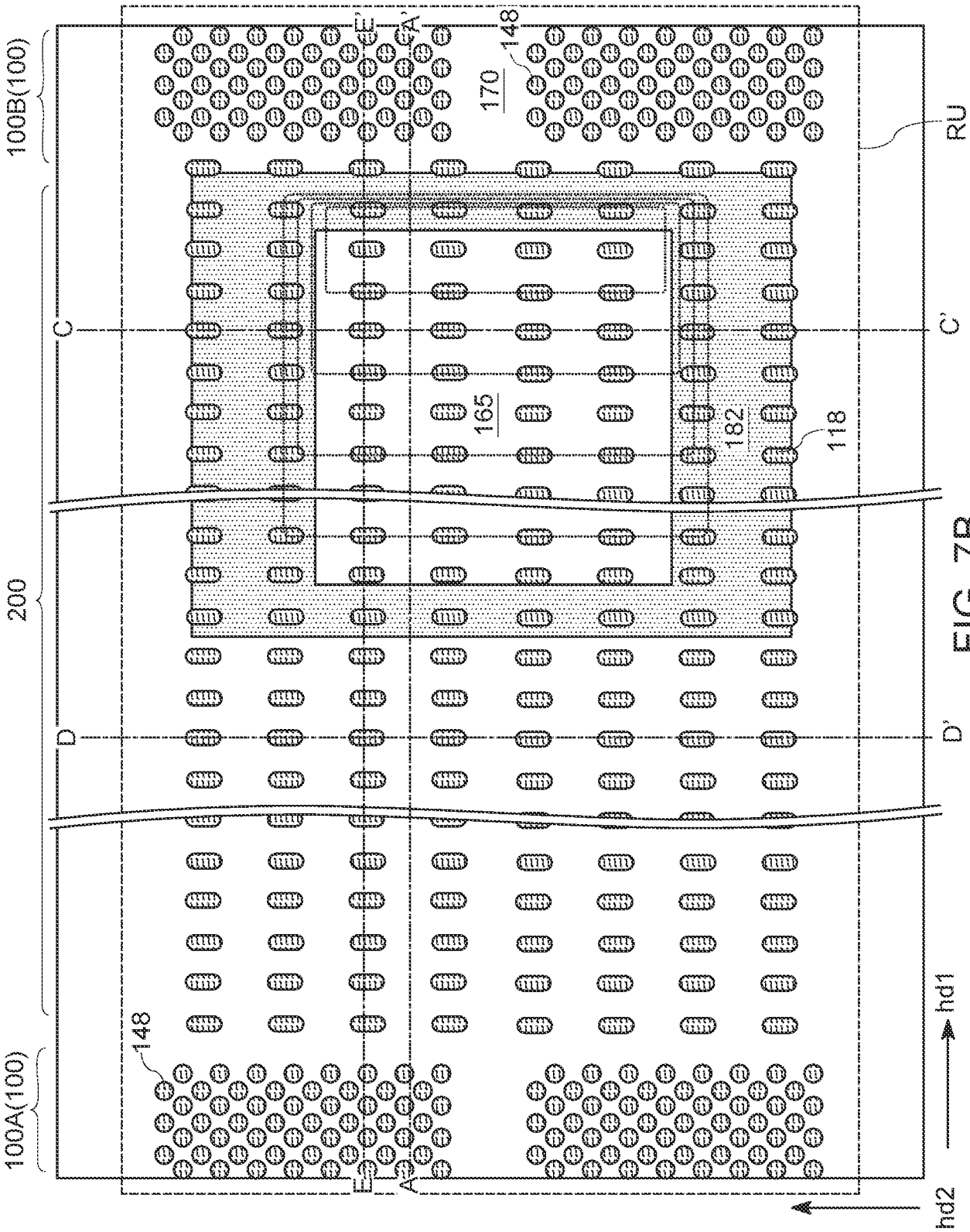
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FIG. 7B

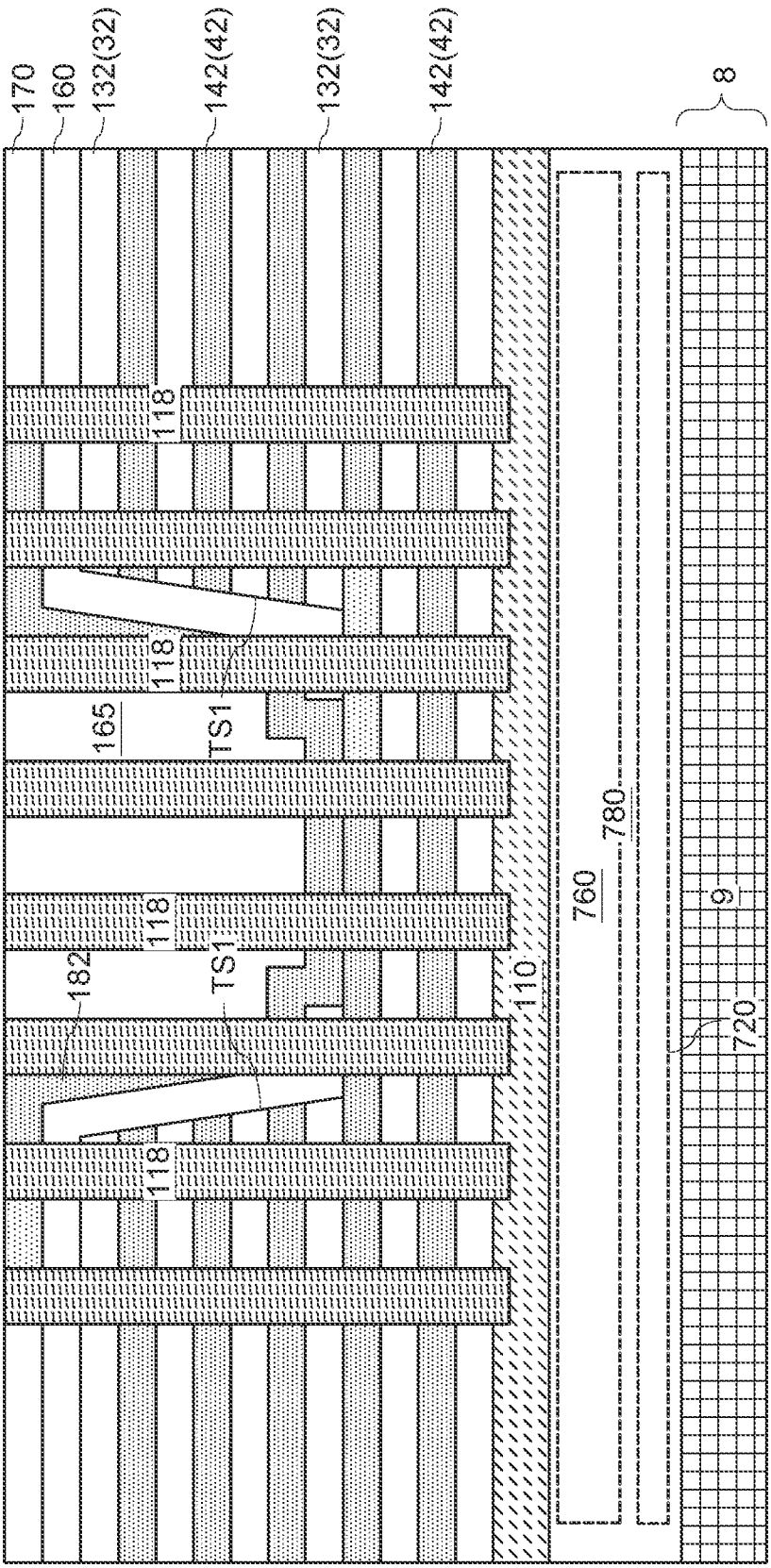
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FIG. 7C

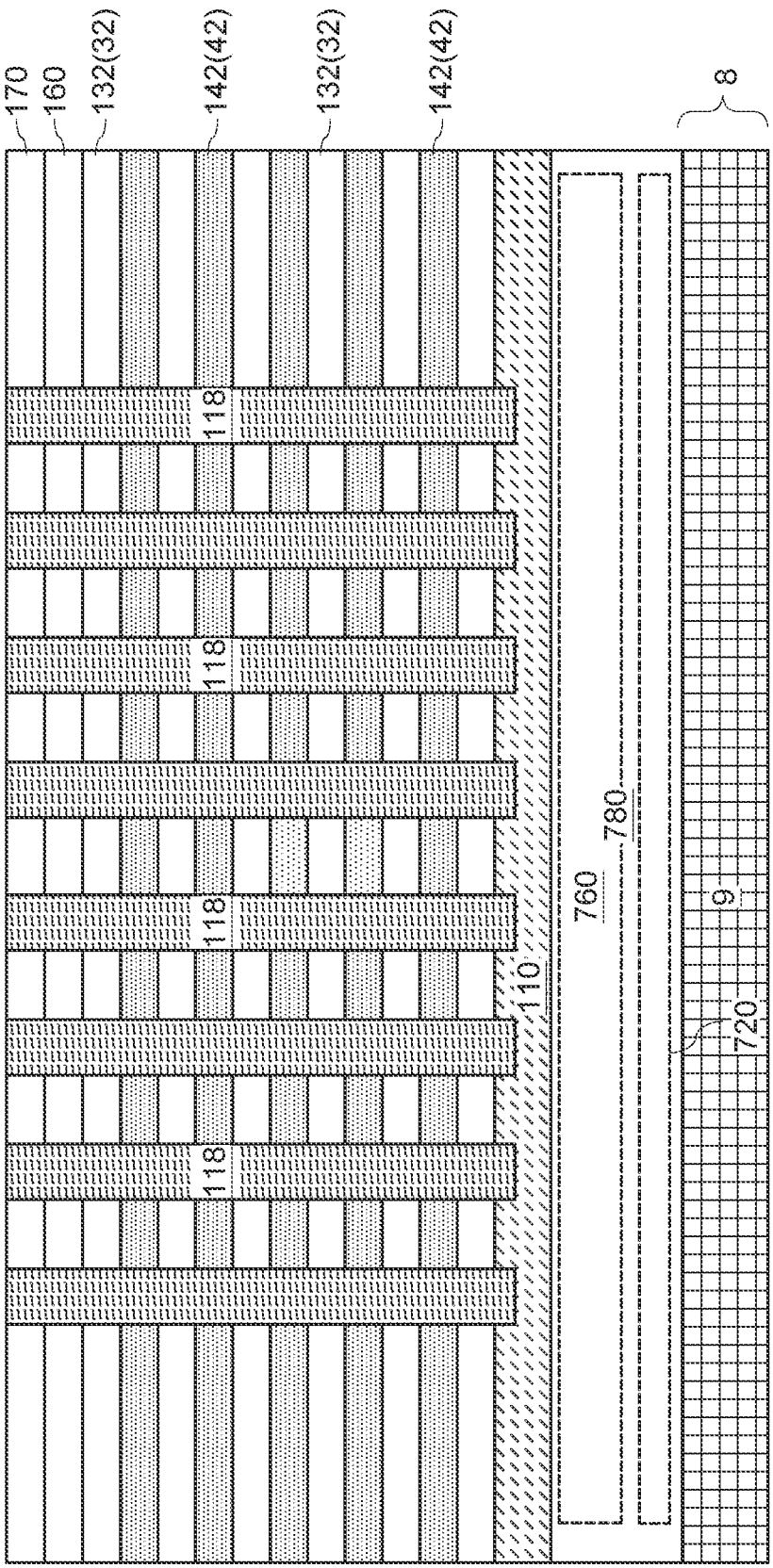
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FIG. 7D

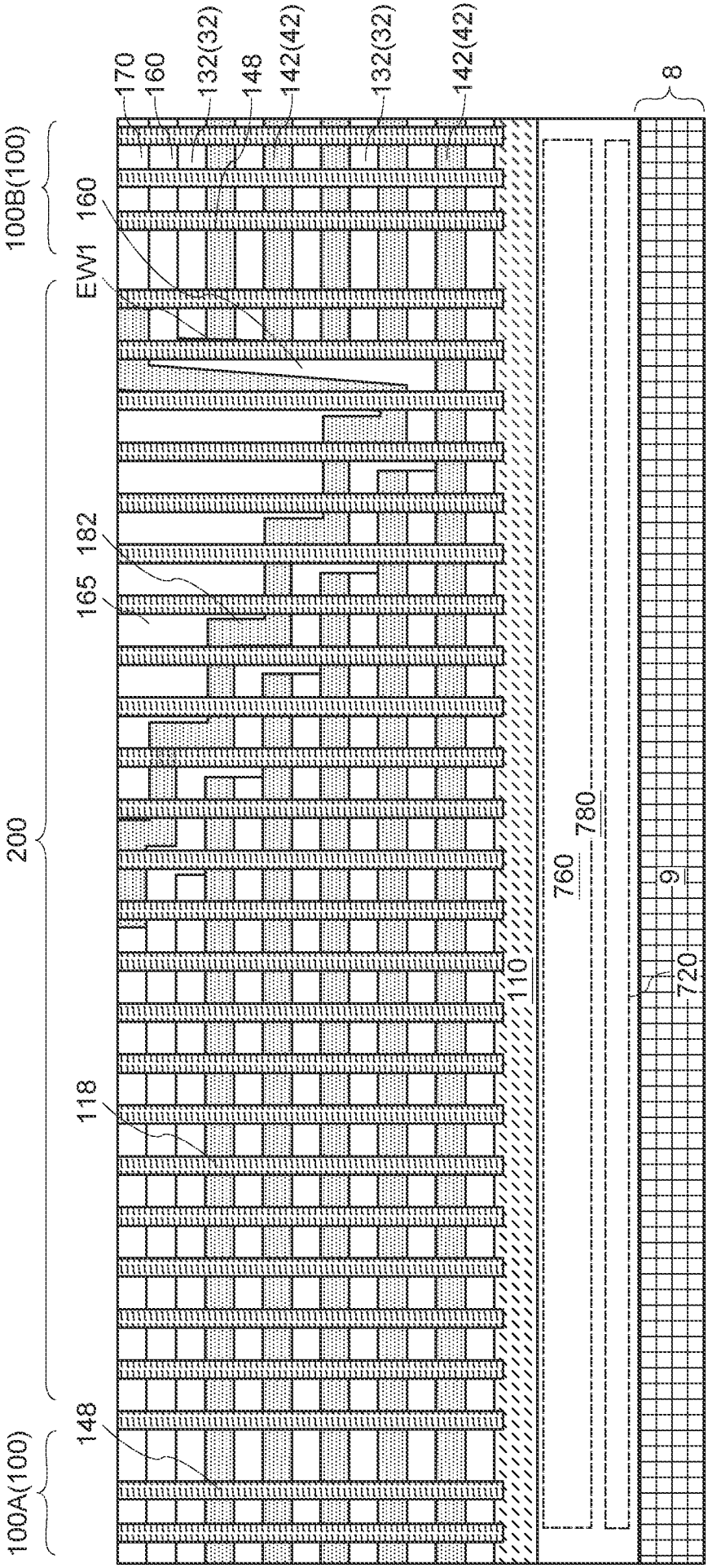
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FIG. 7E

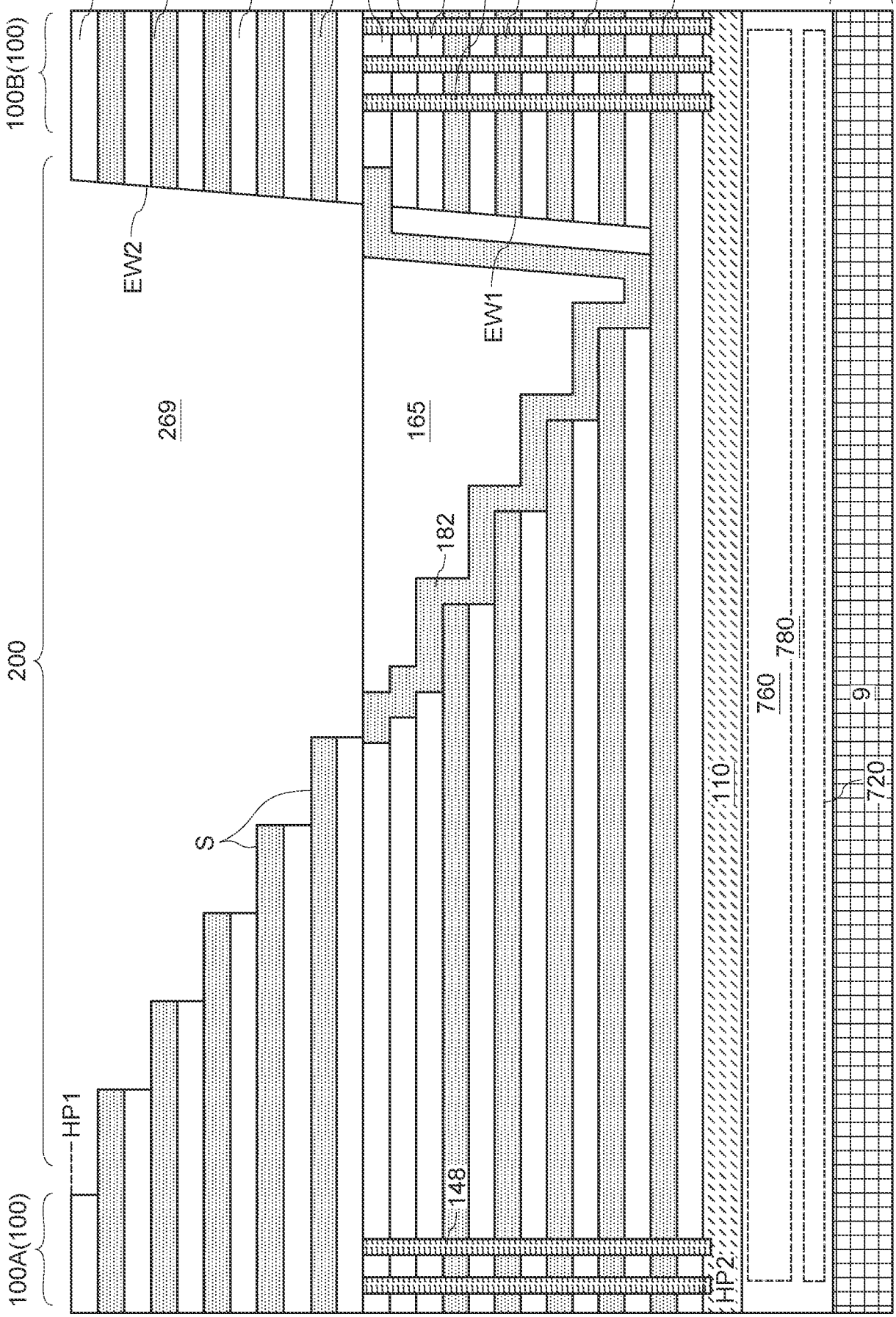
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FIG. 8A

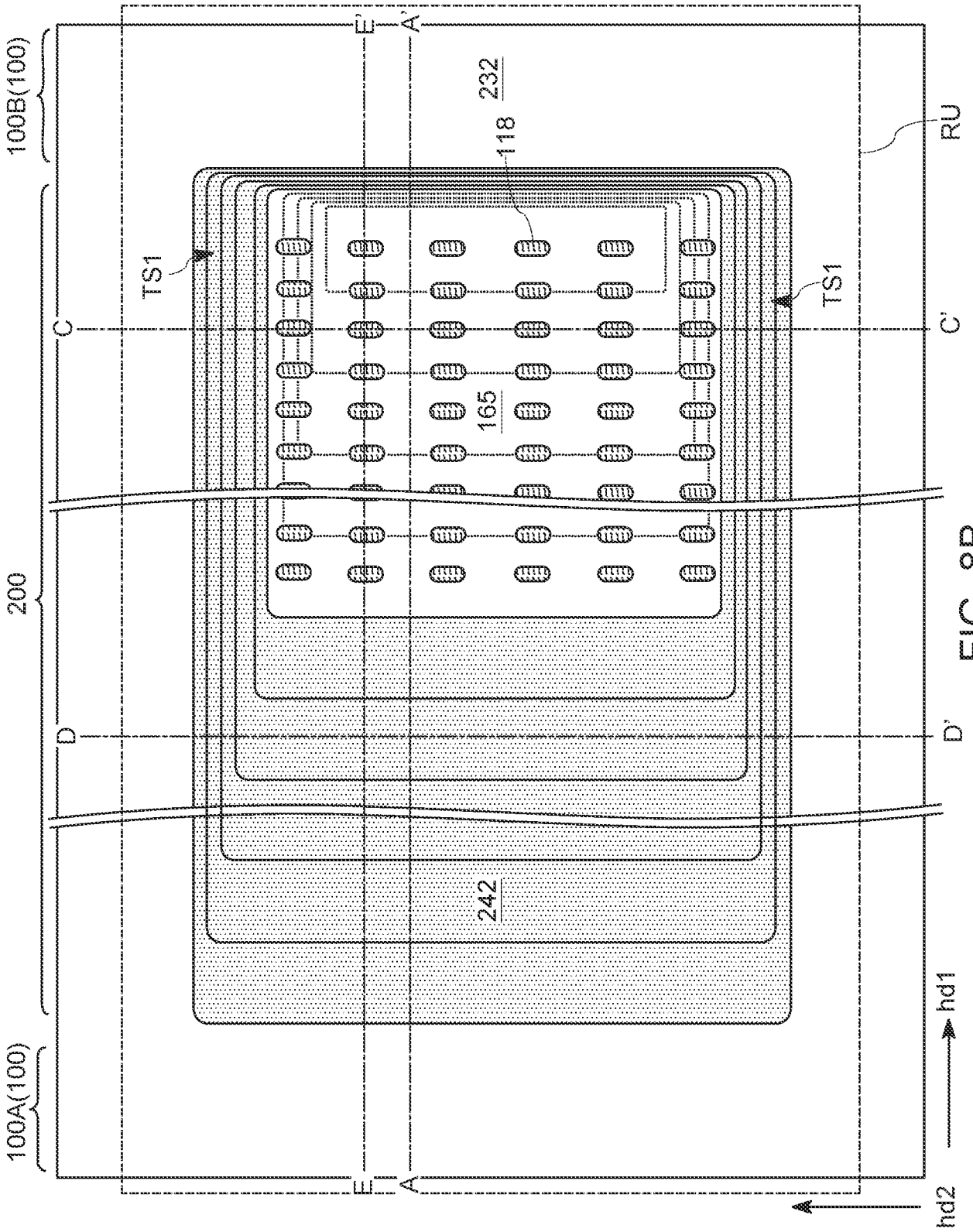
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FIG. 8B

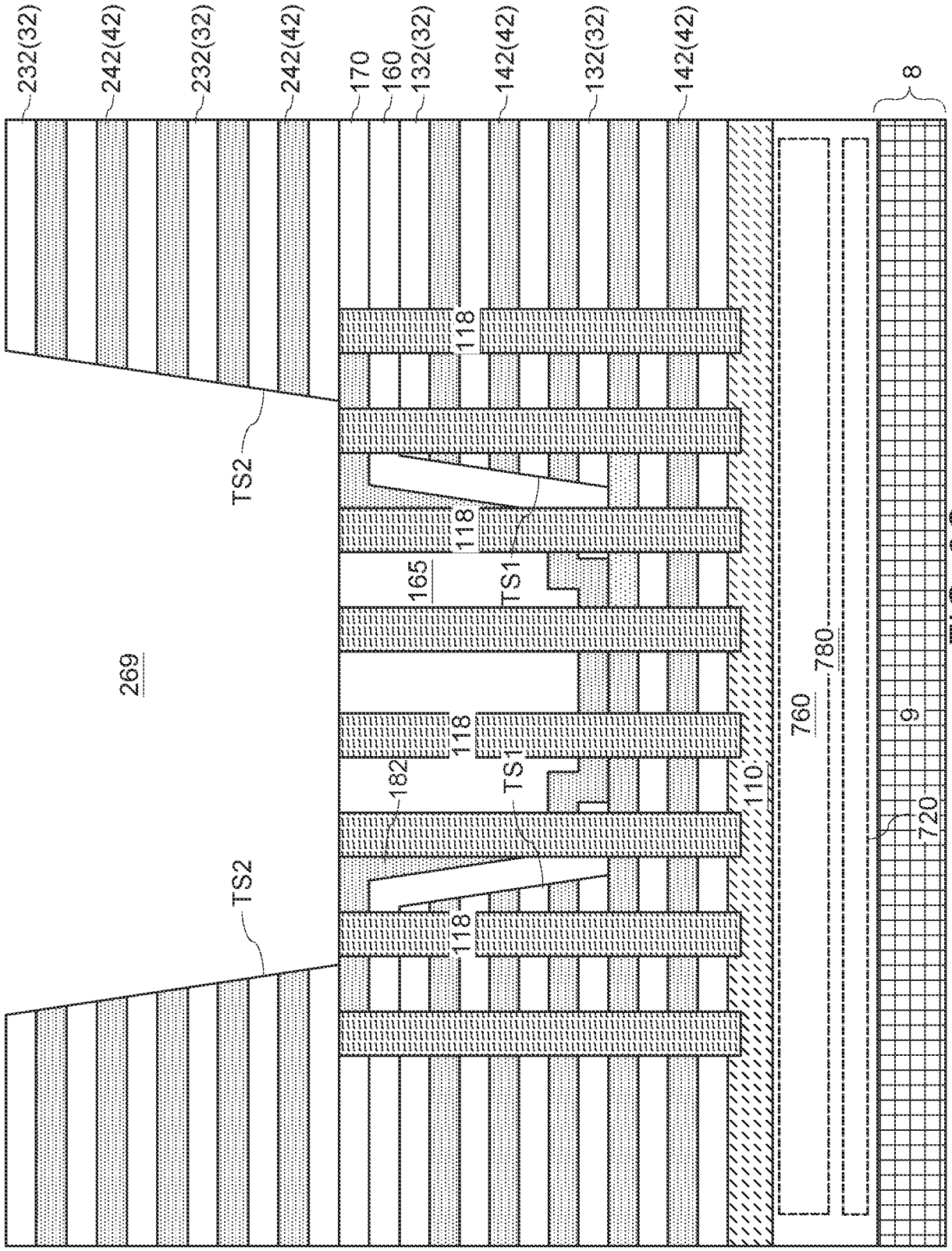
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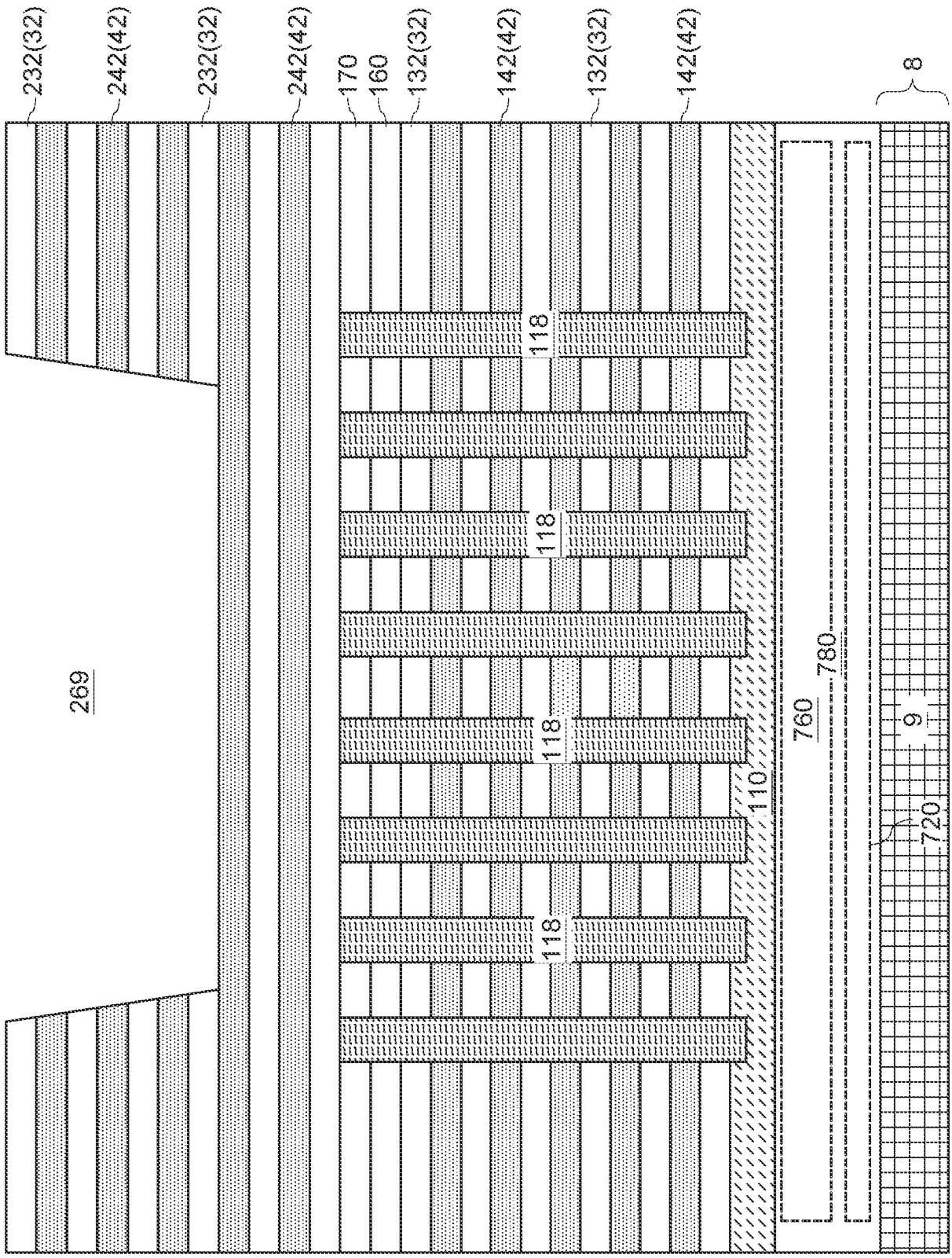
FIG. 8C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142(42)
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118
269
110
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780
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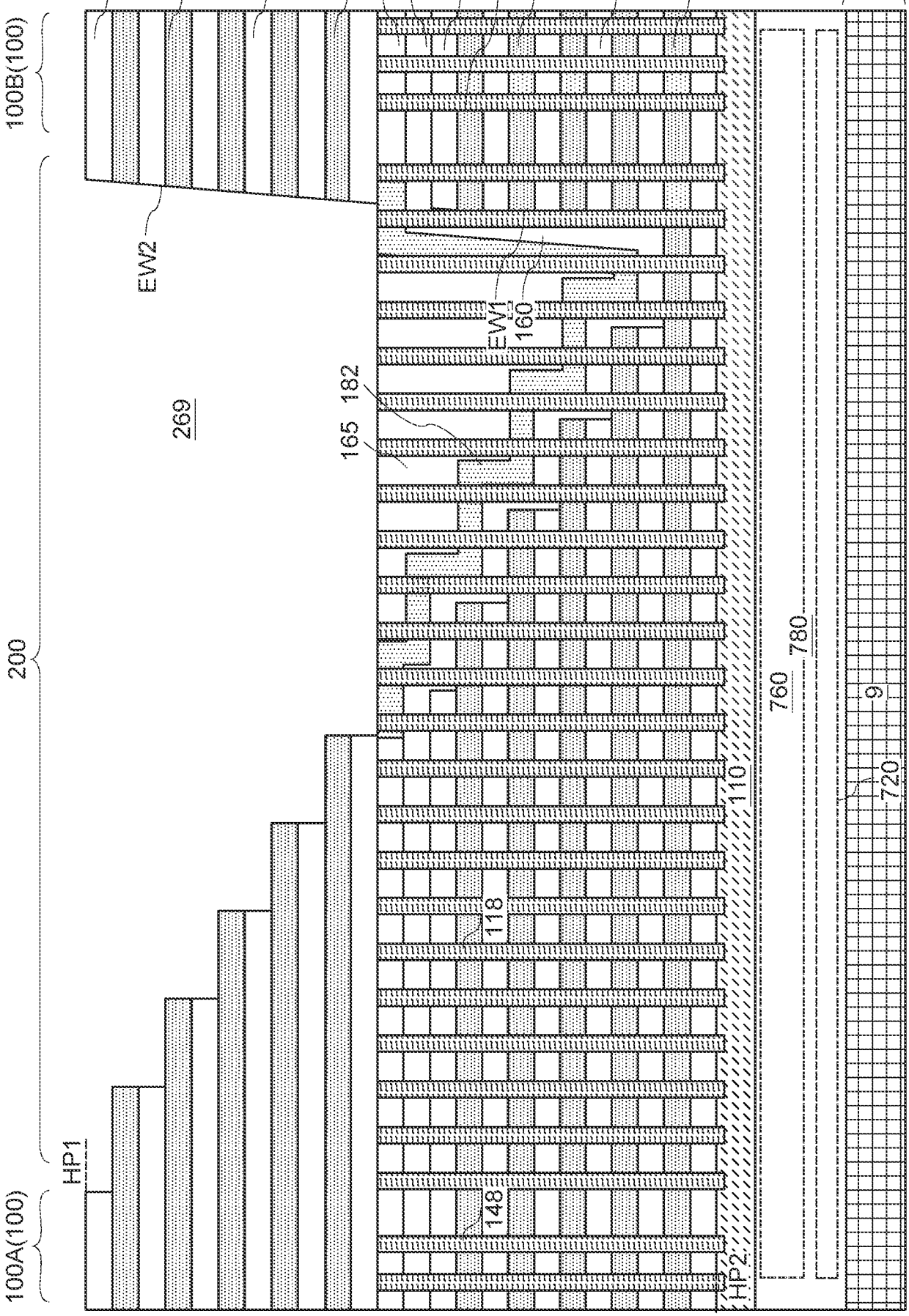
720

FIG. 8D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232(32)
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142(42)
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142(42)
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100B(100)
EW2
EW1
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269
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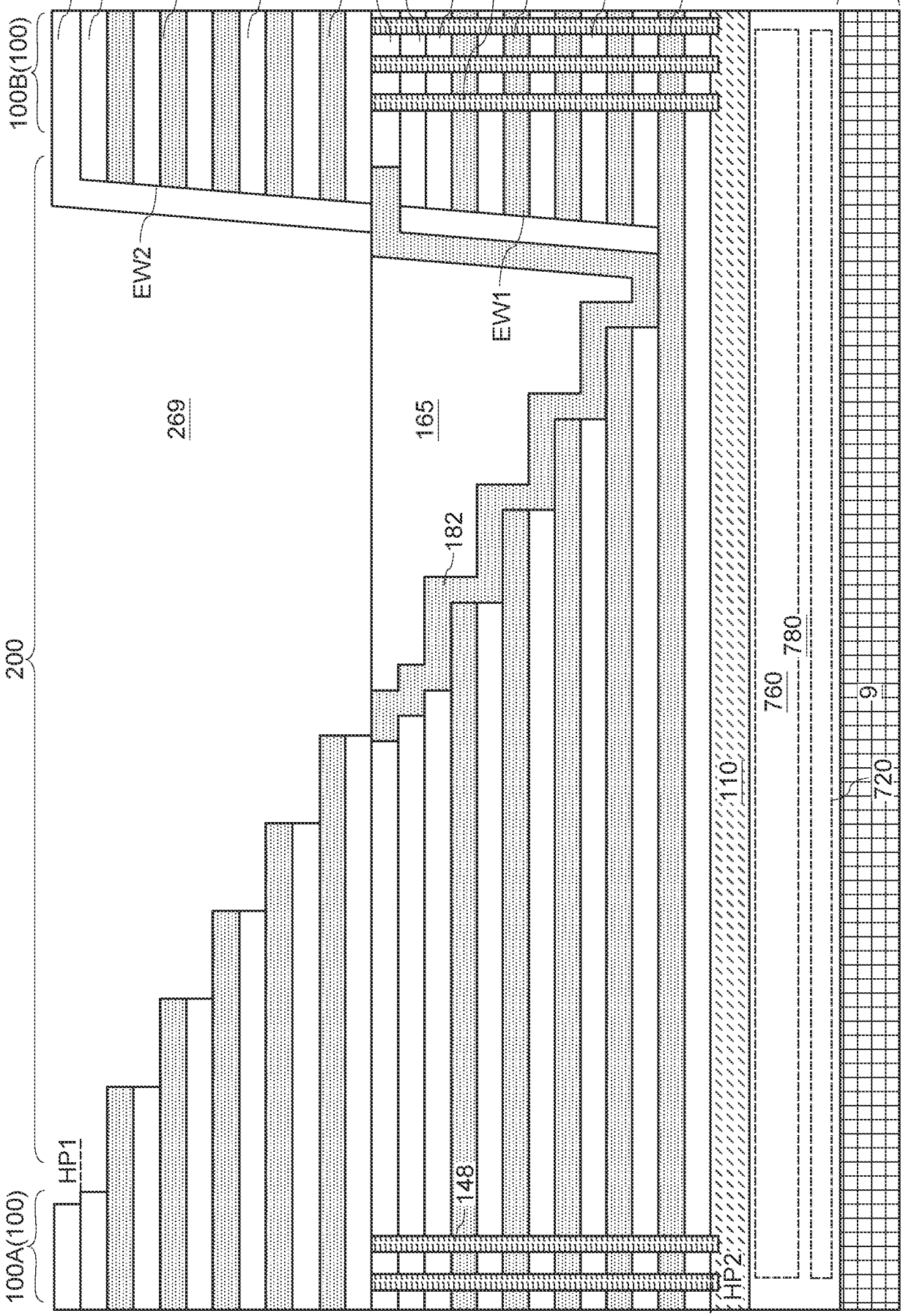
110
118
148
HP1
HP2
100A(100)

FIG. 8E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232(32)
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142(42)
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100B(100)
EW2
EW1
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165
182
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760
780
9
720
110
148
HP1
HP2
100A(100)

FIG. 9A

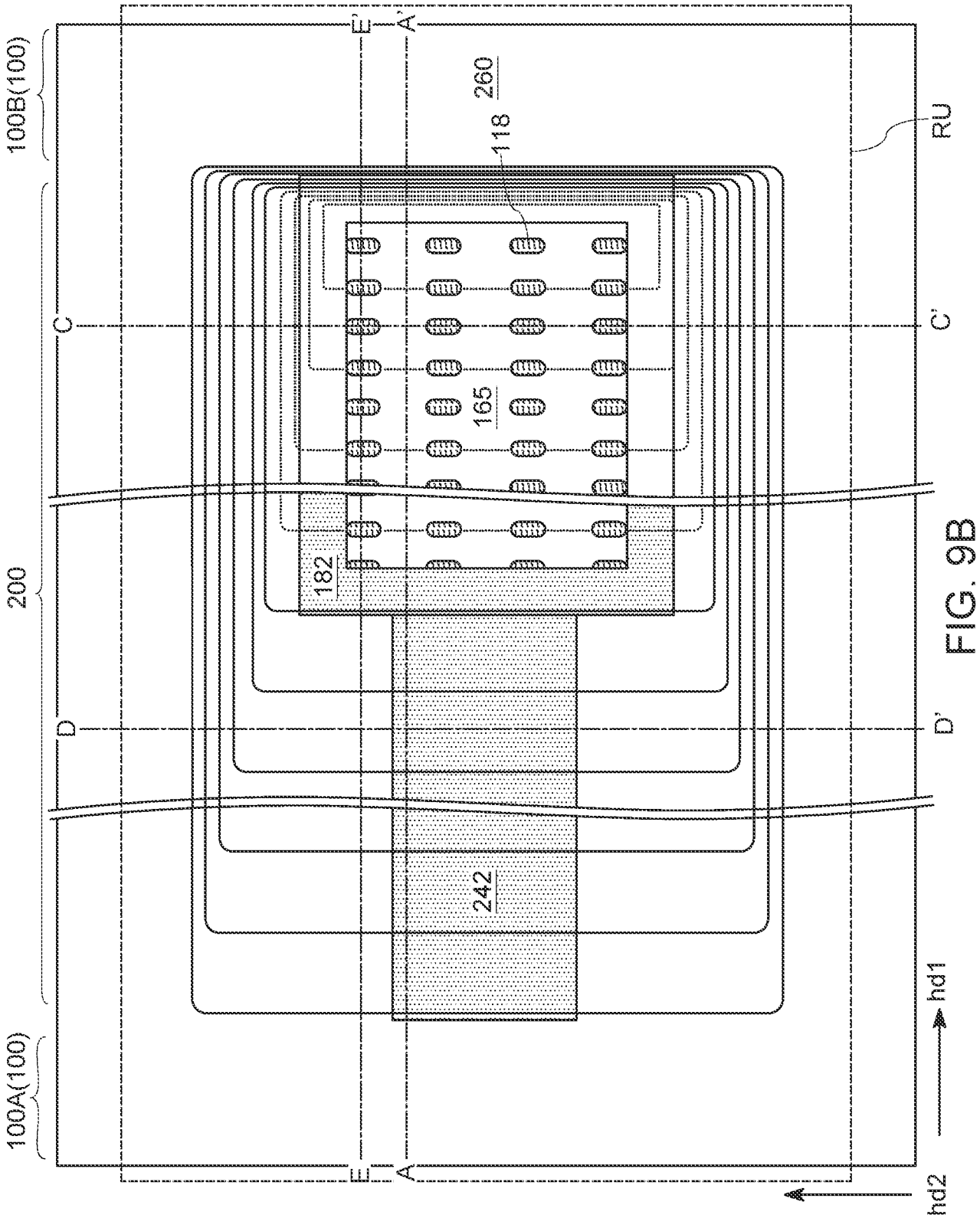
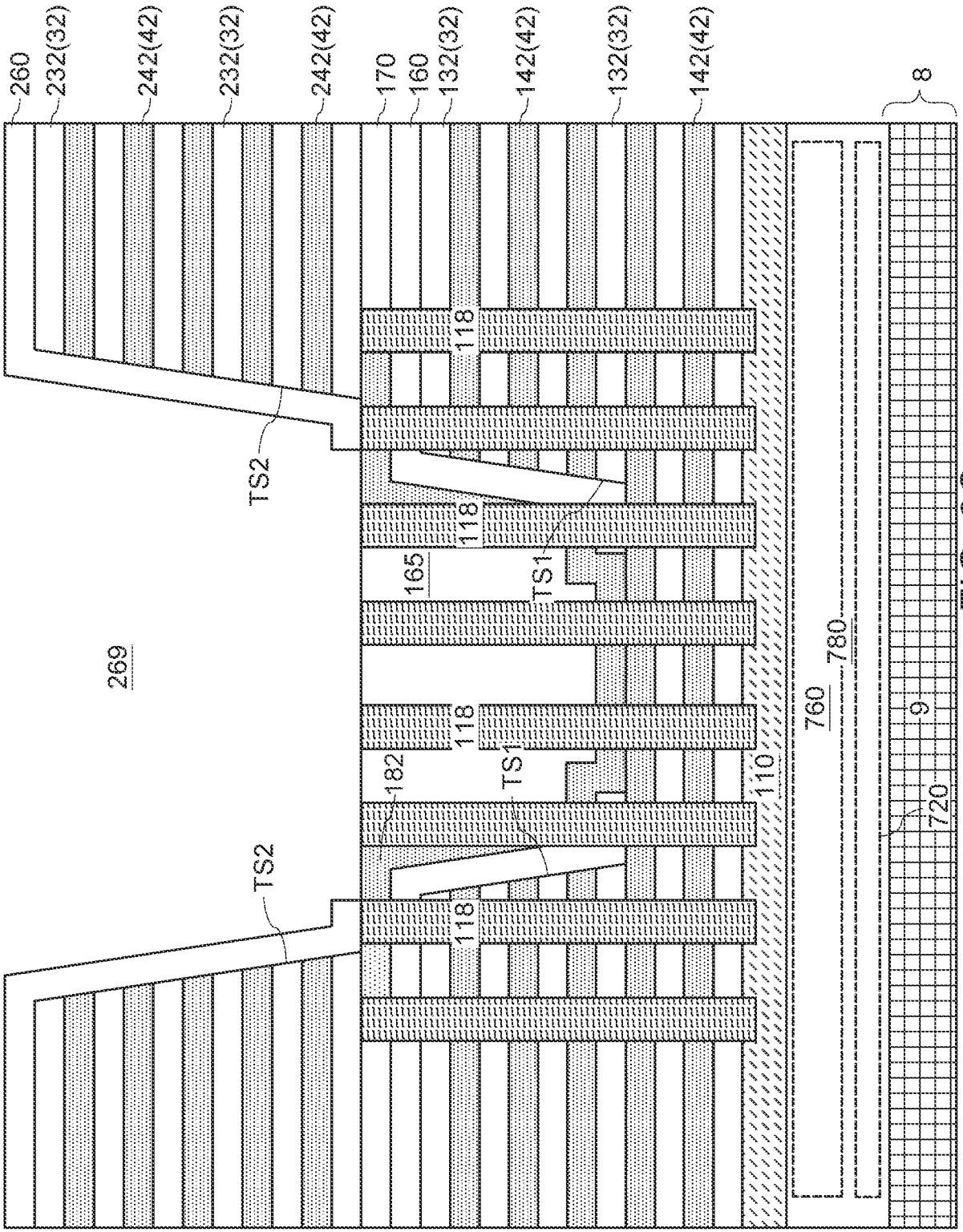


FIG. 9B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142(42)
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TS1
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780
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TS1
182
110
9
720
TS2
118

FIG. 9C

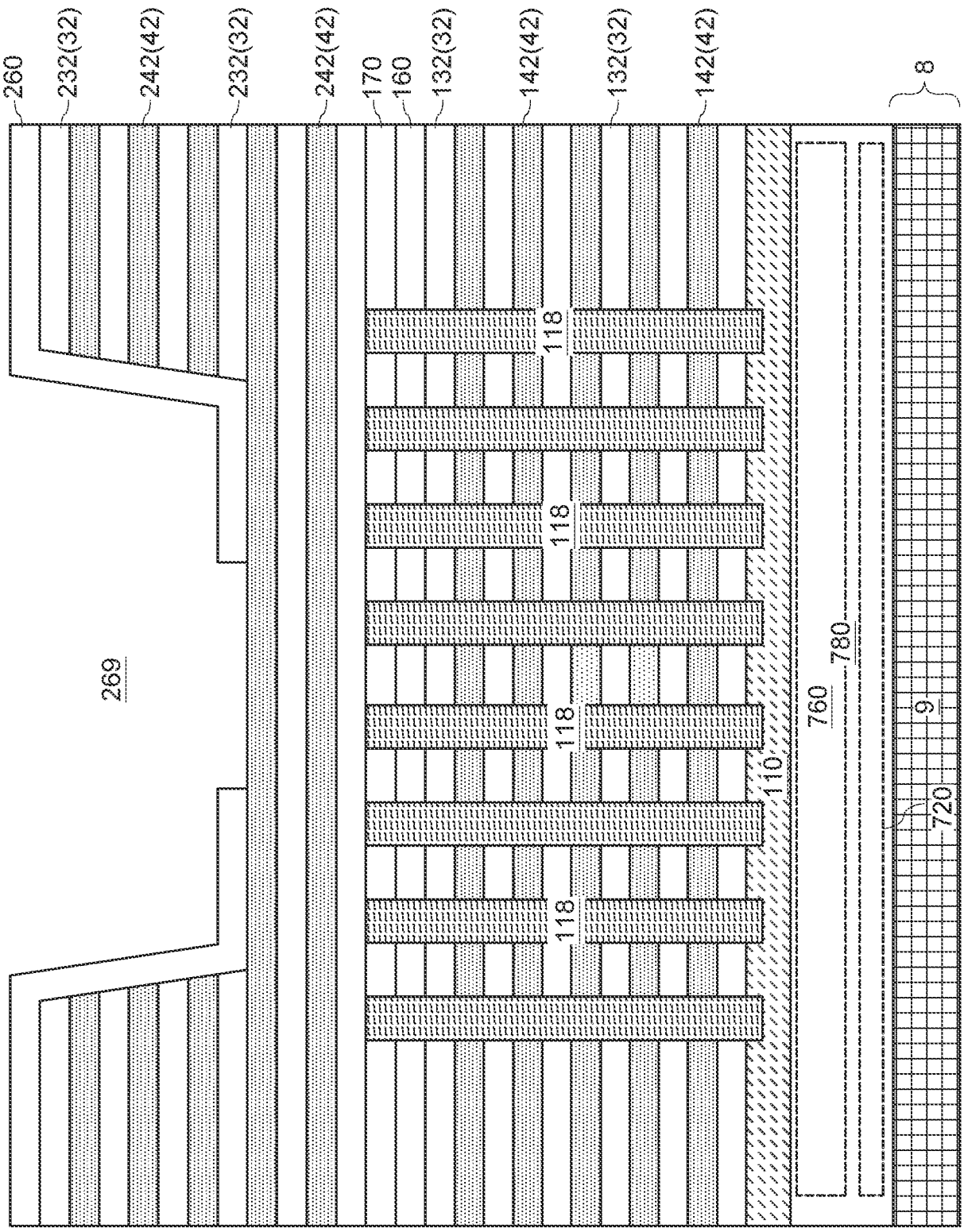
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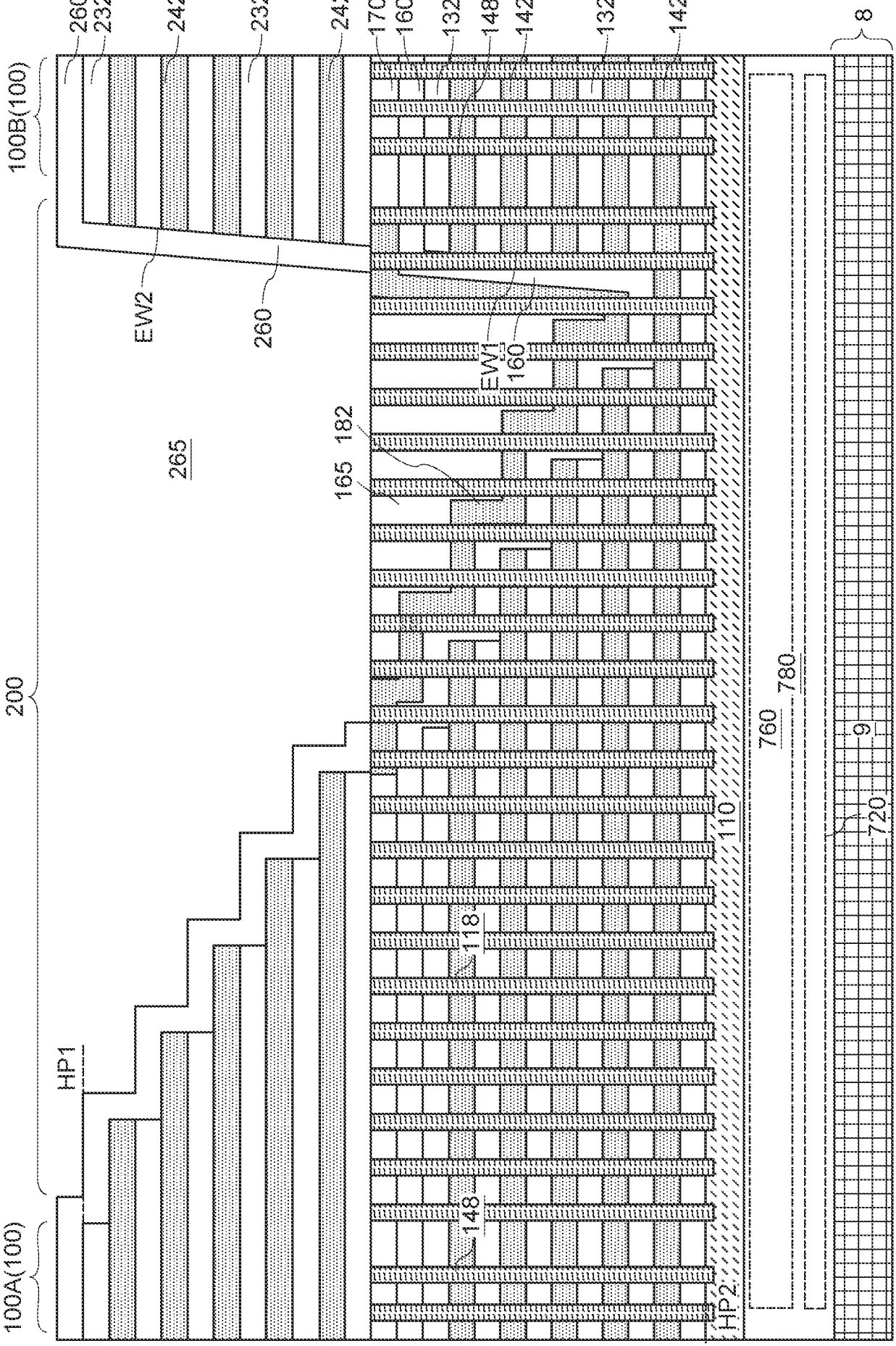
FIG. 9D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EW2
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100A(100)
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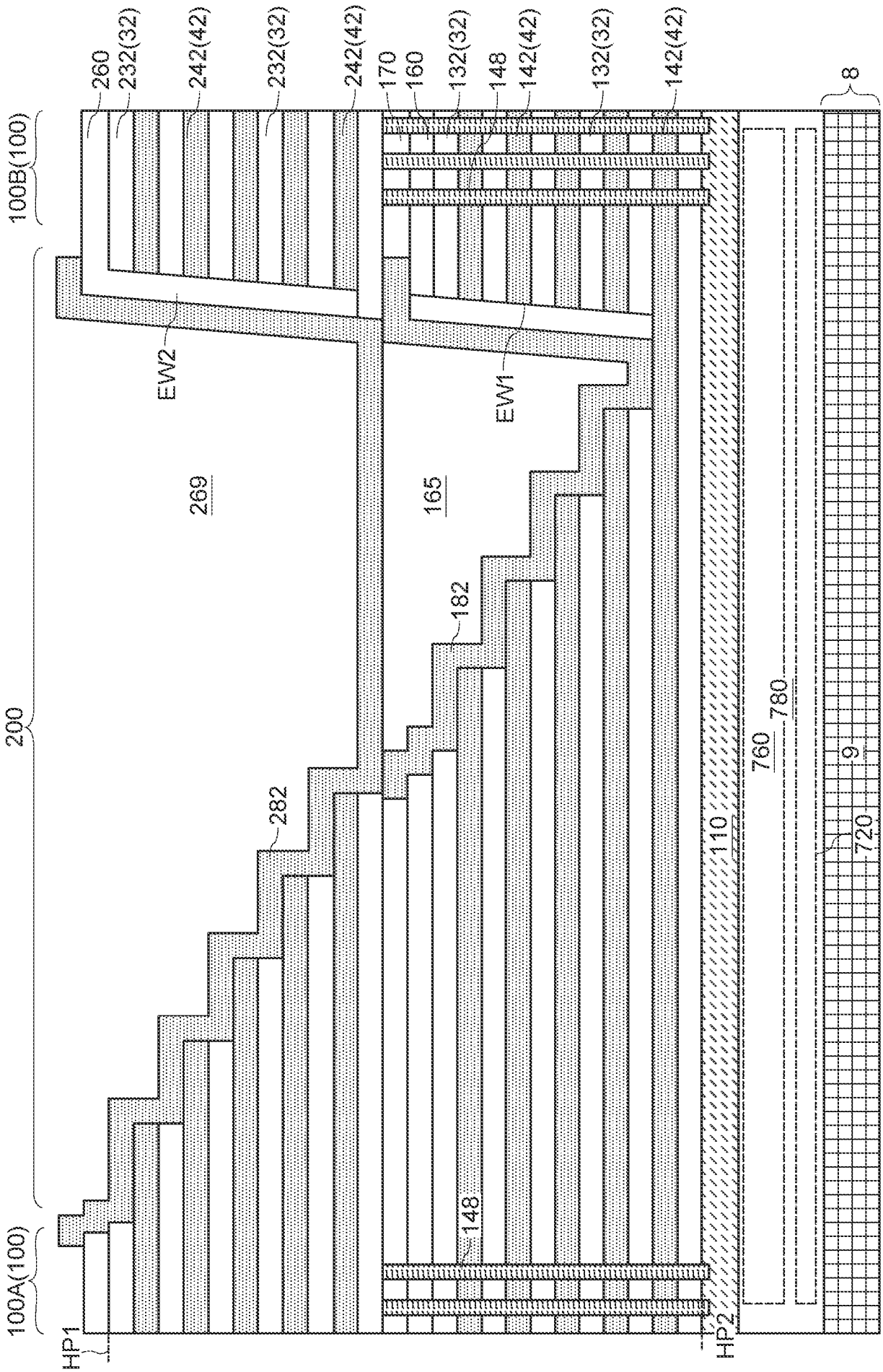
118
110
760
780
9
720
HP2

FIG. 9E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EW2
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282
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148
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780
9
720
100A(100)
HP1
HP2

FIG. 10A

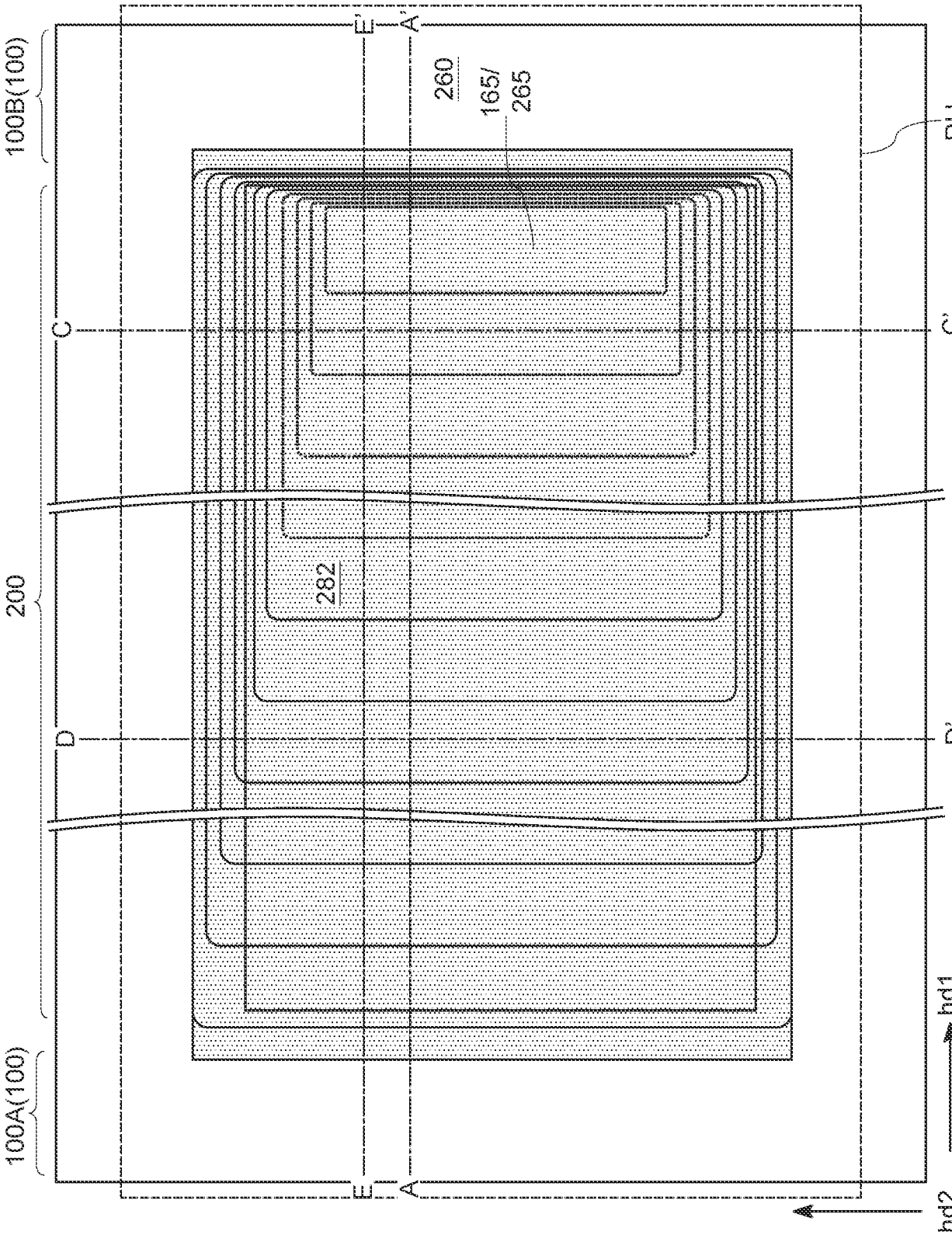
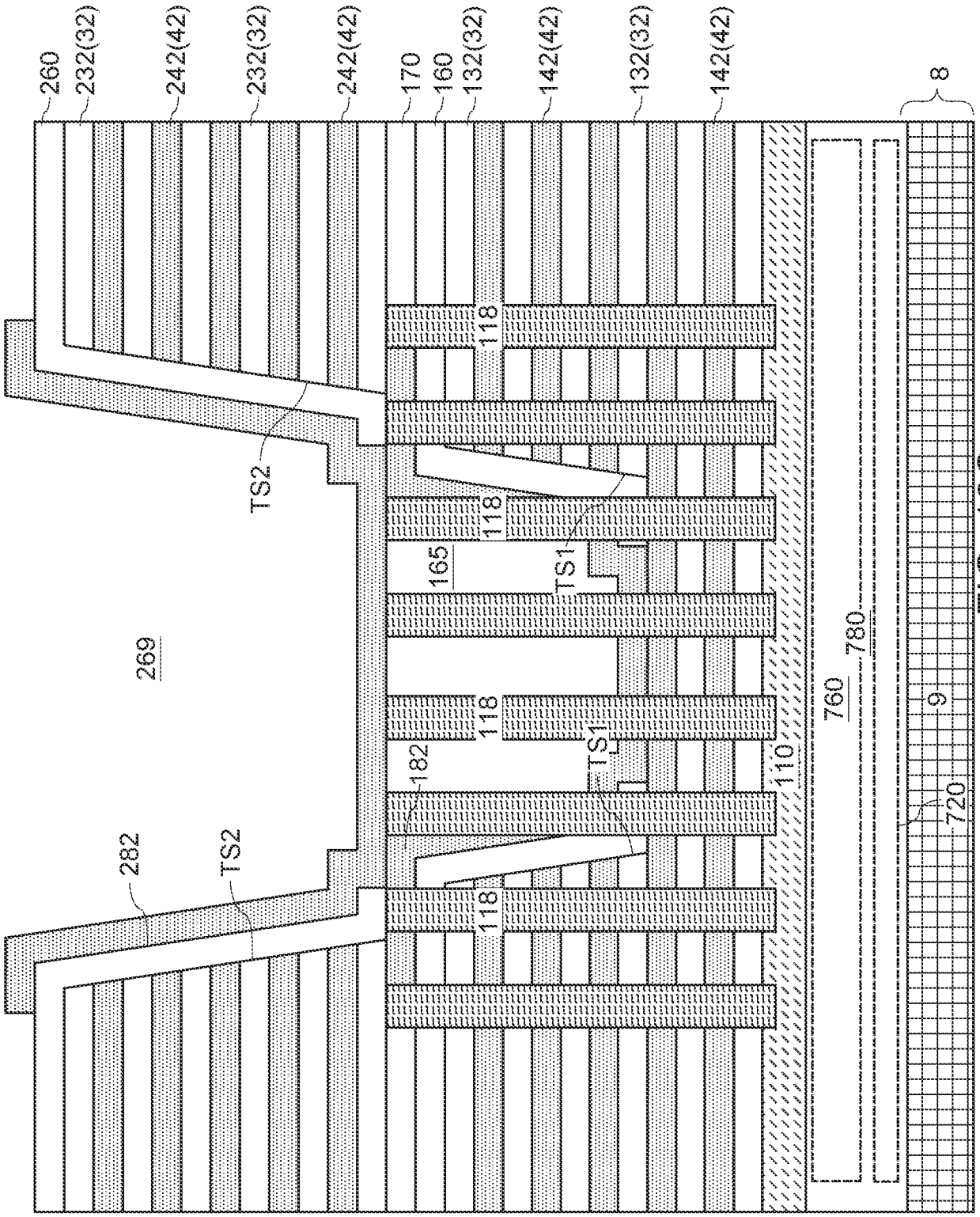


FIG. 10B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132(32)
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132(32)
142(42)
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TS2
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TS1
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TS1
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TS2
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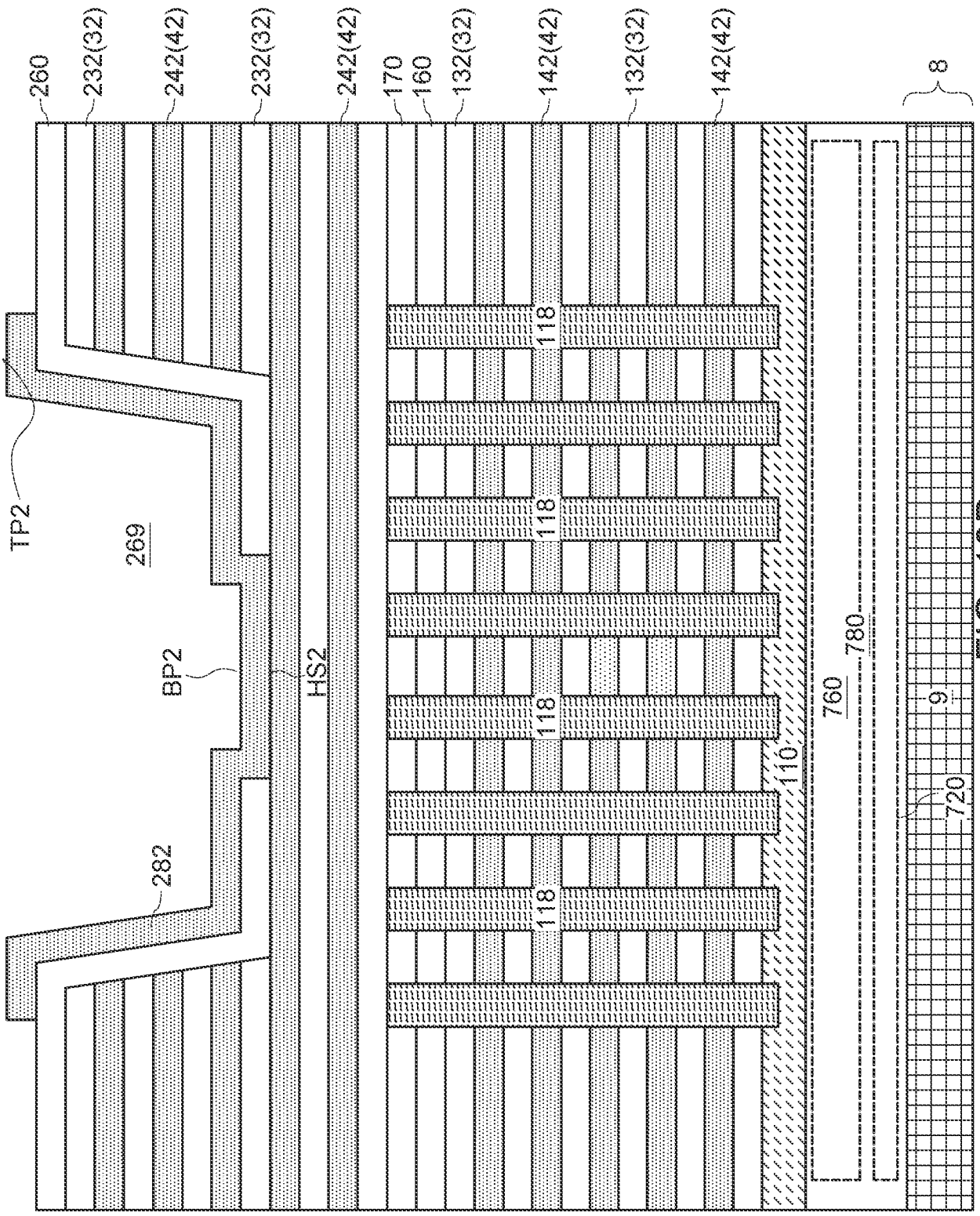
FIG. 10C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BP2
HS2
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118
118
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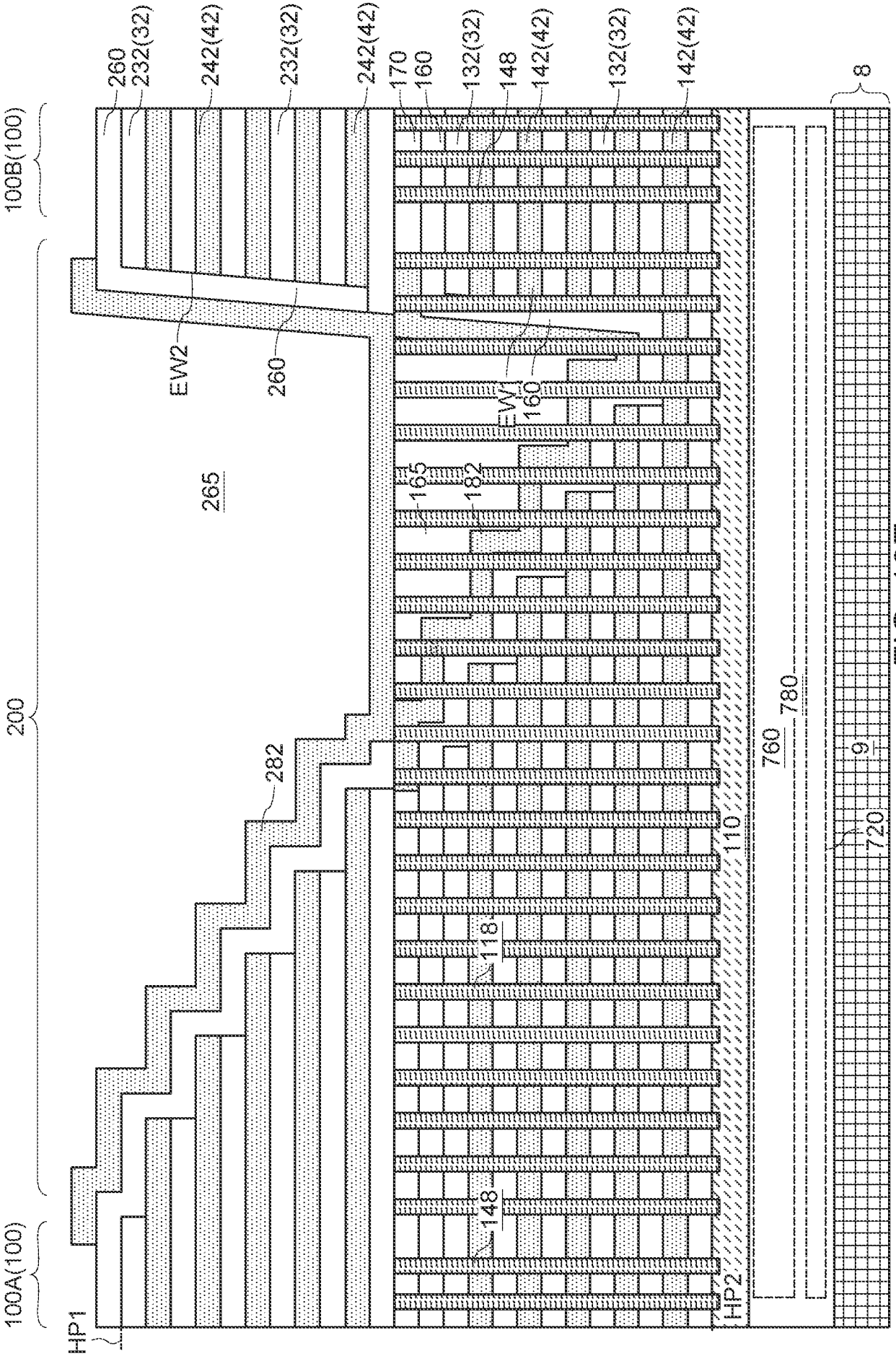
720

FIG. 10D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142(42)
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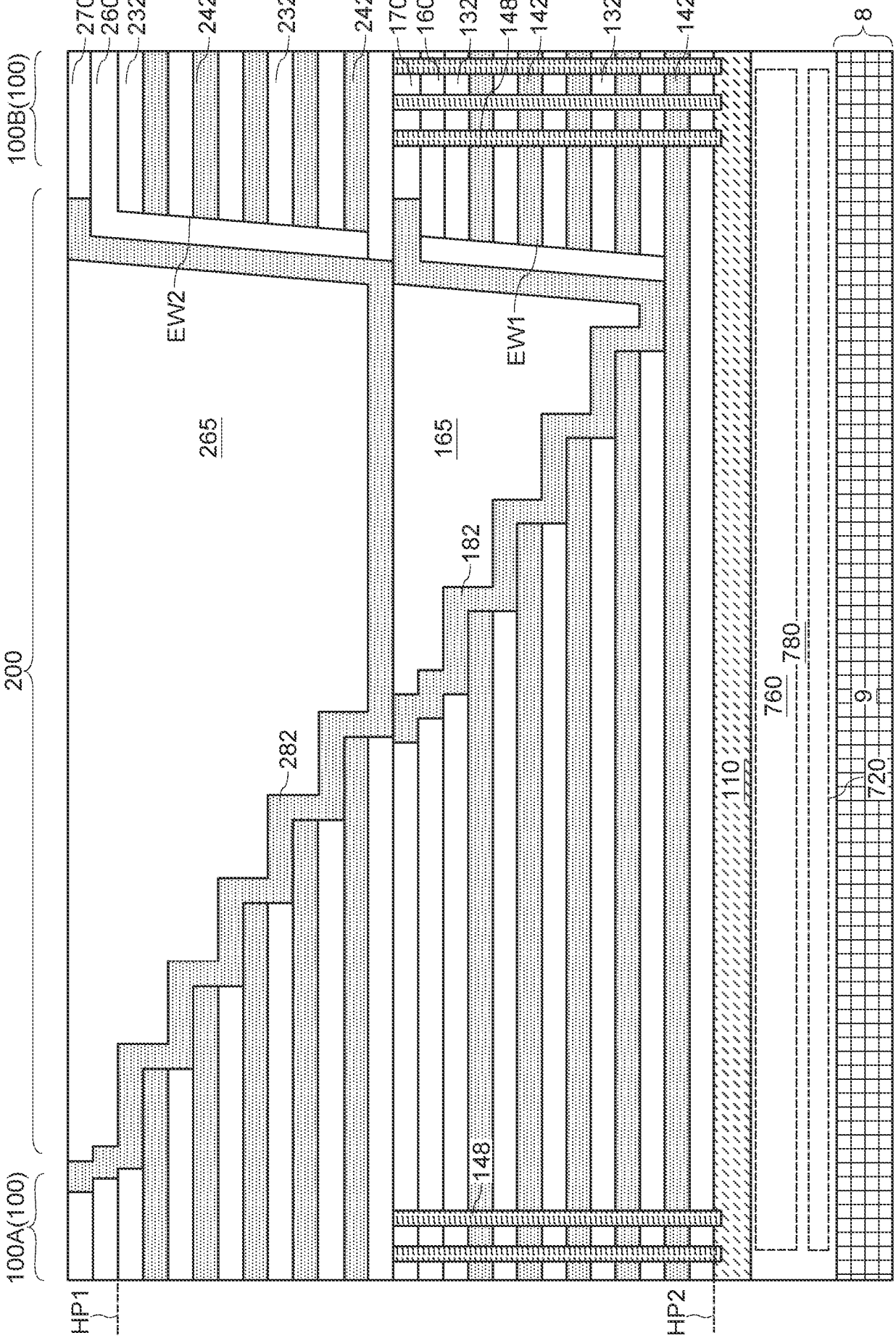
148
100A(100)
HP1
HP2

FIG. 10E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100B(100)
200
100A(100)
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EW1
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HP1
HP2

FIG. 11A

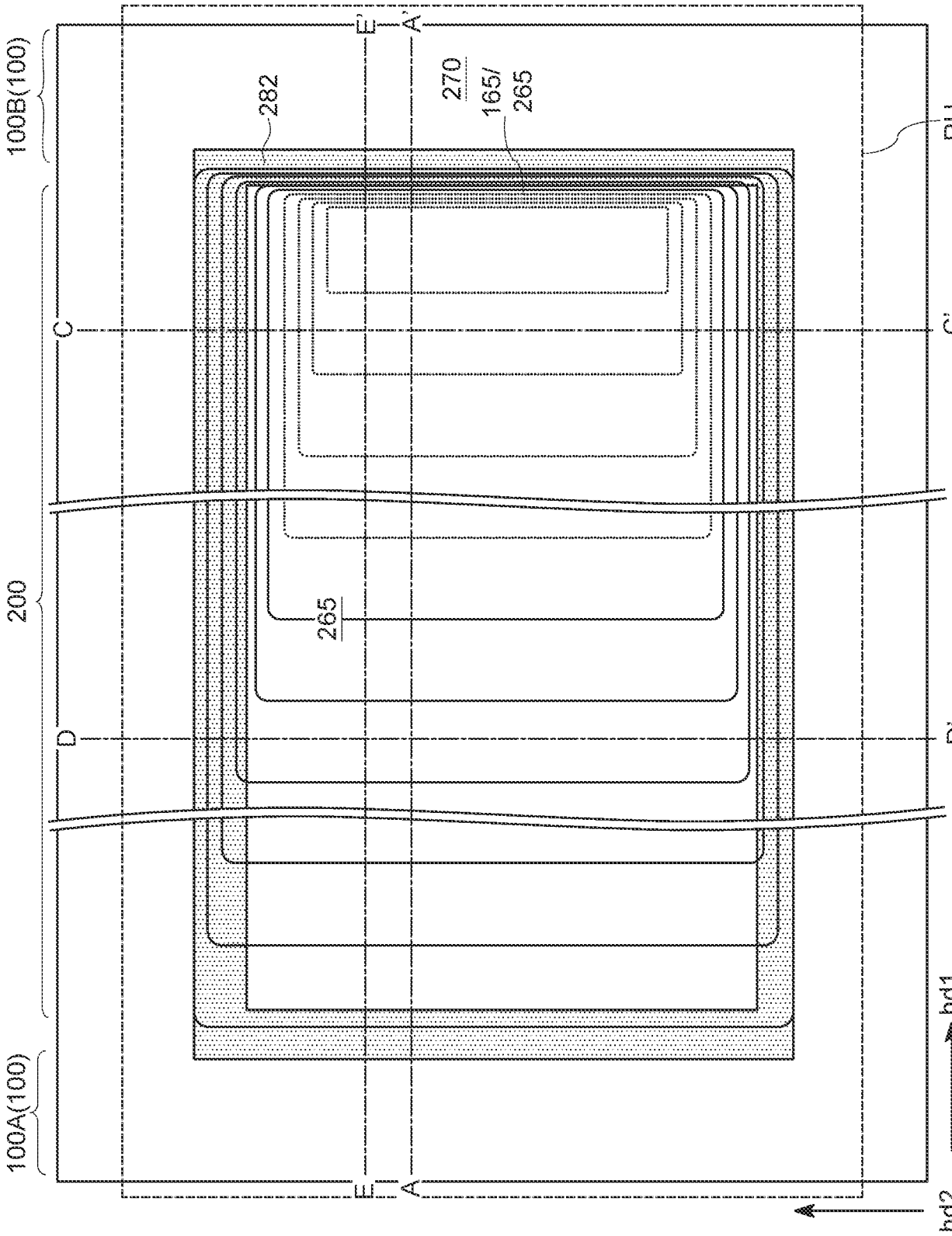
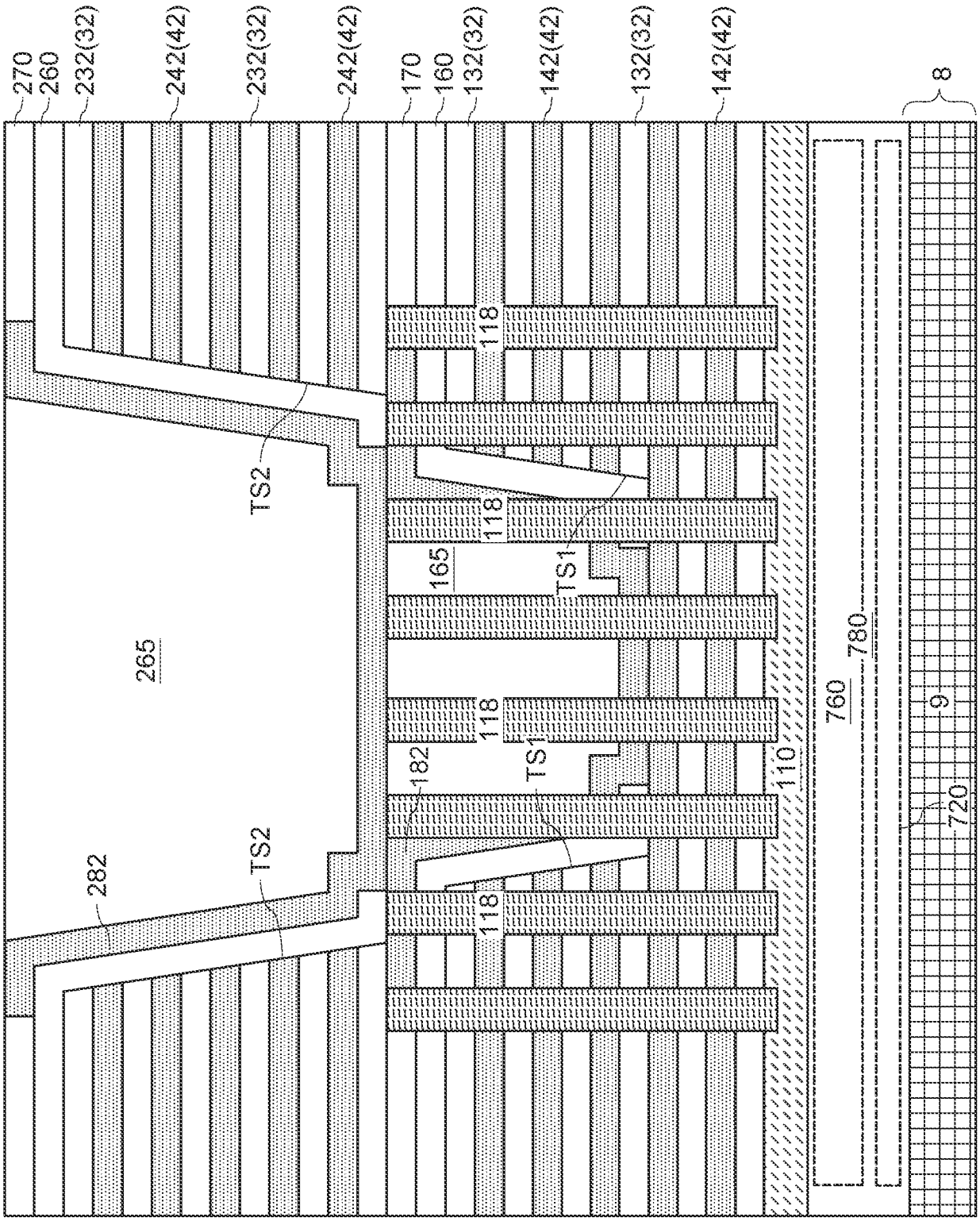


FIG. 11B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132(32)
142(42)
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142(42)
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TS2
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TS1
265
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760
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TS1
182
110
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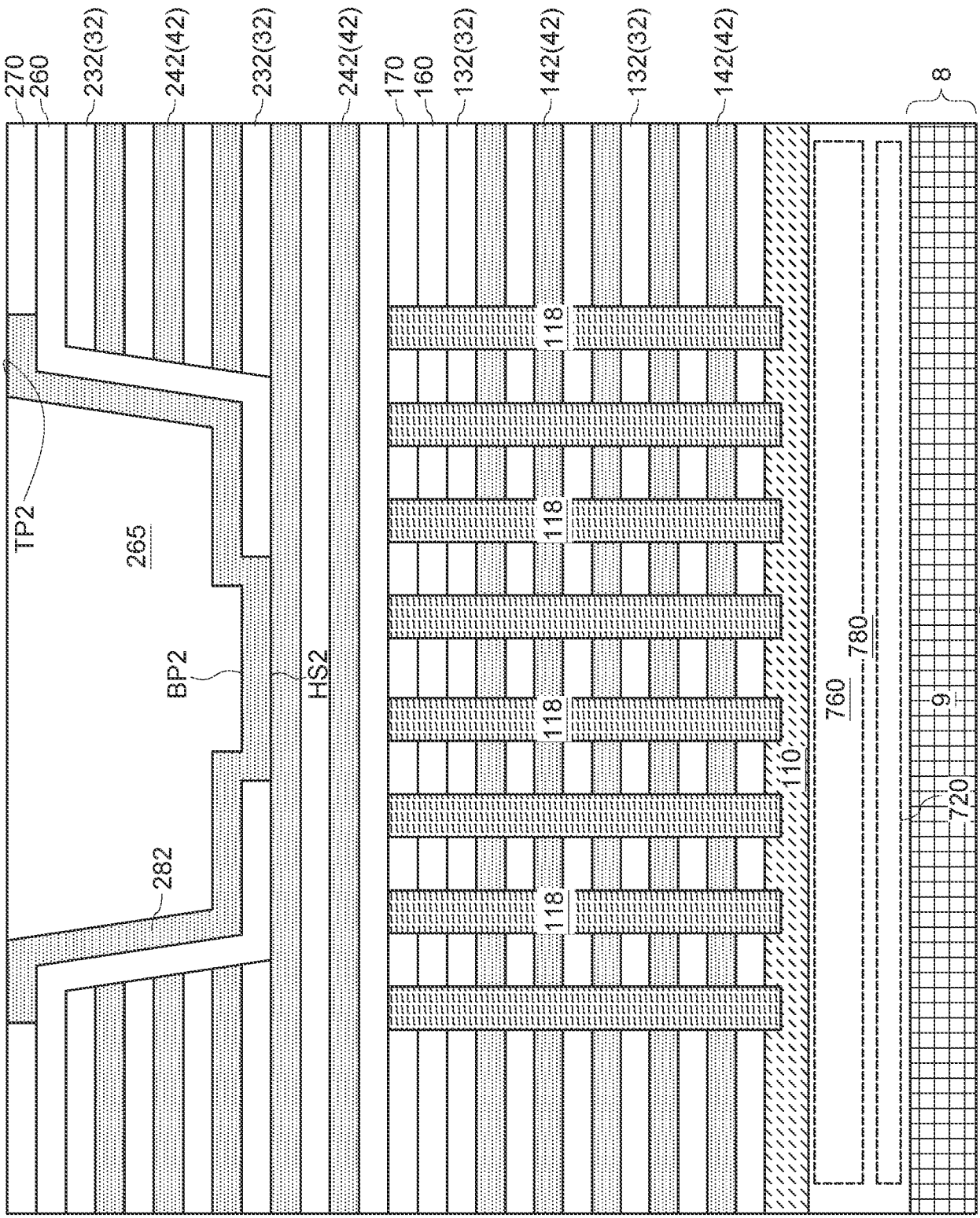
720
282
TS2
118

FIG. 11C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242(42)
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132(32)
142(42)
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142(42)
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TP2
265
BP2
HS2
282
118
118
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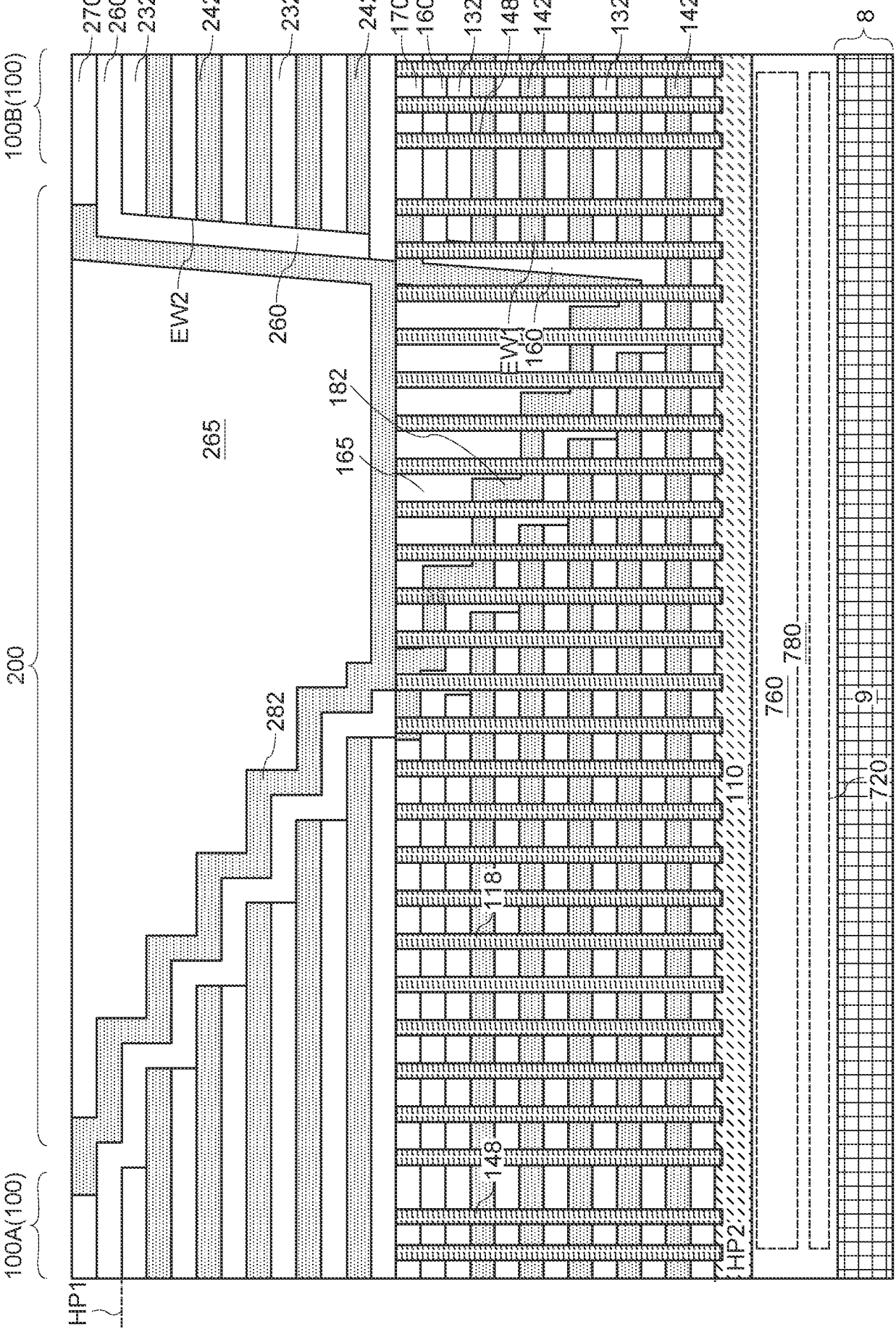
118
110
760
780
9
720

FIG. 11D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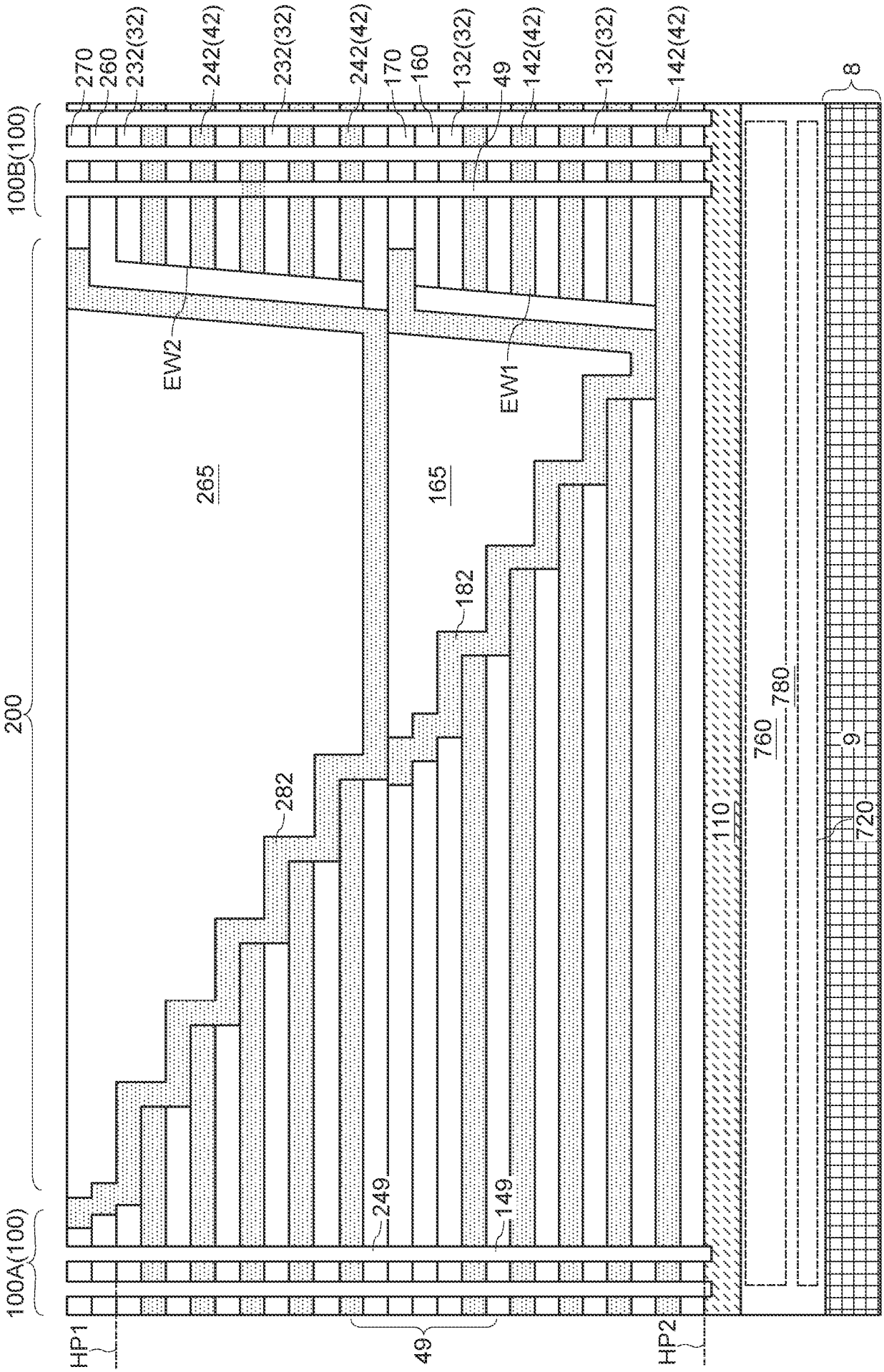
142(42)
132(32)
142(42)
8
100B(100)
200
100A(100)
HP1
HP2
EW2
260
EW1
160
182
165
265
282
118
148
110
760
780
9
720

FIG. 11E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142(42)
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142(42)
8
100B(100)
EW2
EW1
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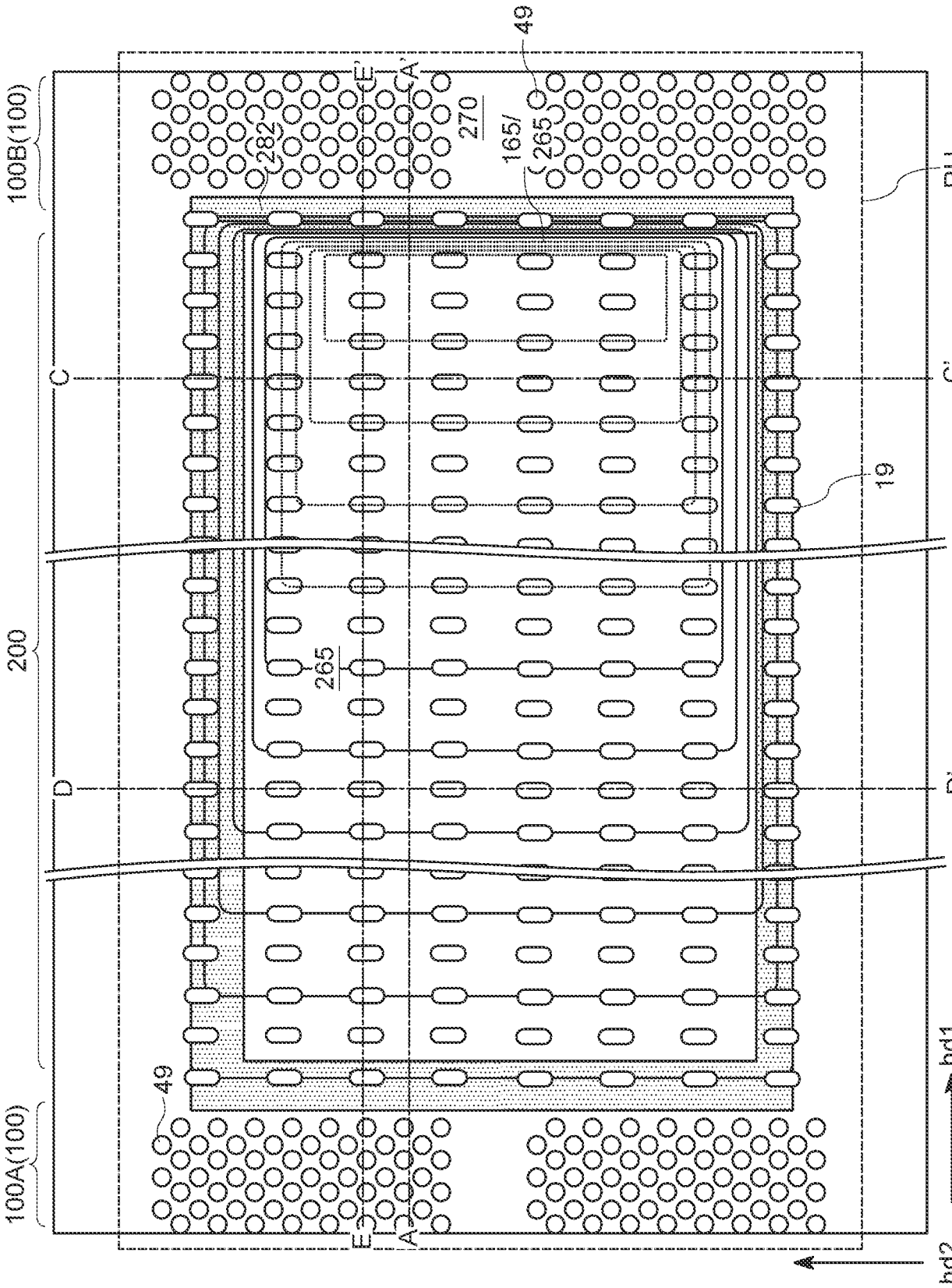
165
182
282
200
249
149
110
760
780
9
720
100A(100)
HP1
49
HP2

FIG. 12A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E'
A'
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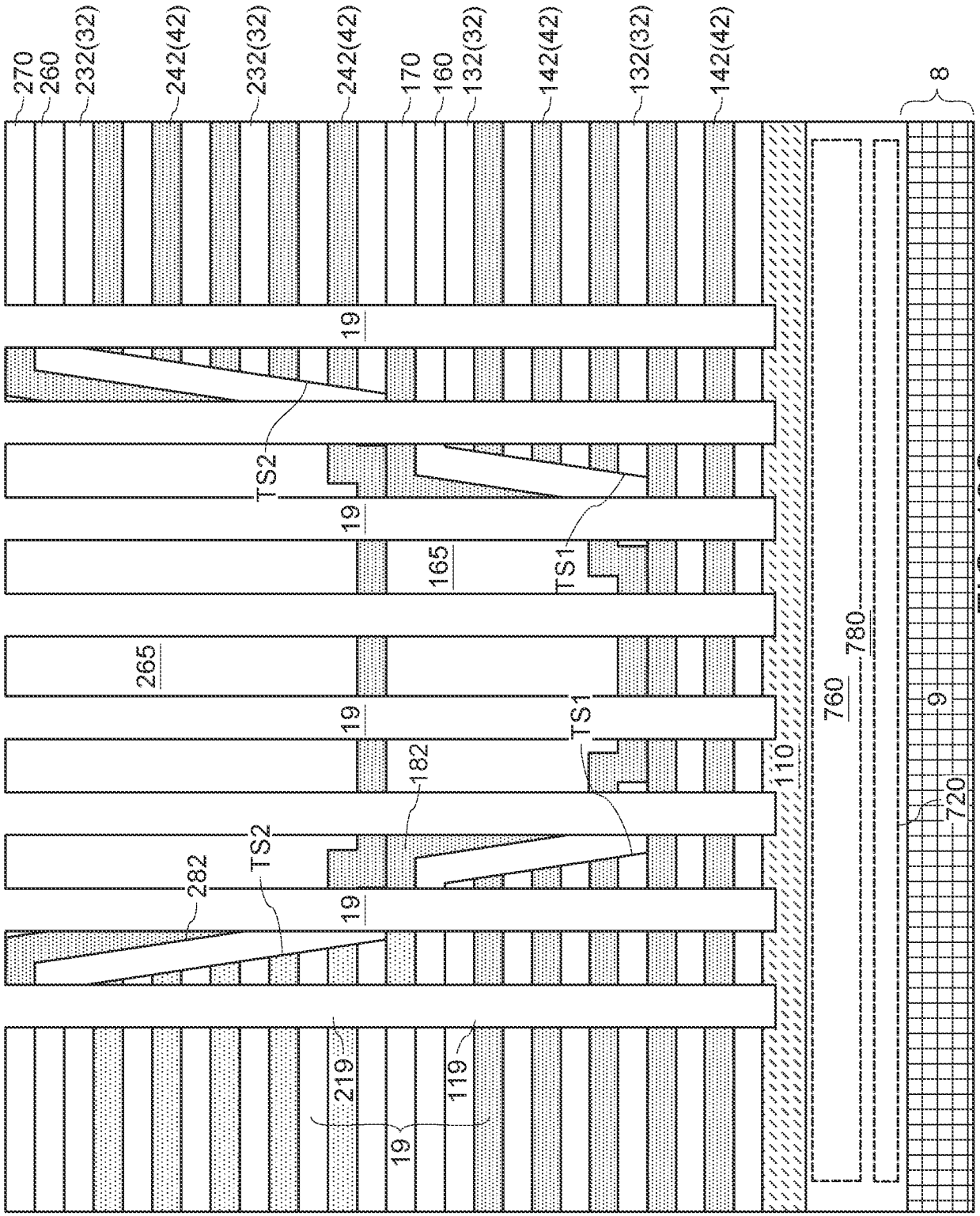
282
165/
265
RU
100B(100)
C
C'
19
200
265
D
D'
49
100A(100)
E
A
hd1
hd2

FIG. 12B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160
132(32)
142(42)
132(32)
142(42)
8
19
TS2
19
165
TS1
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780
760
19
TS1
182
110
720
9
282
TS2
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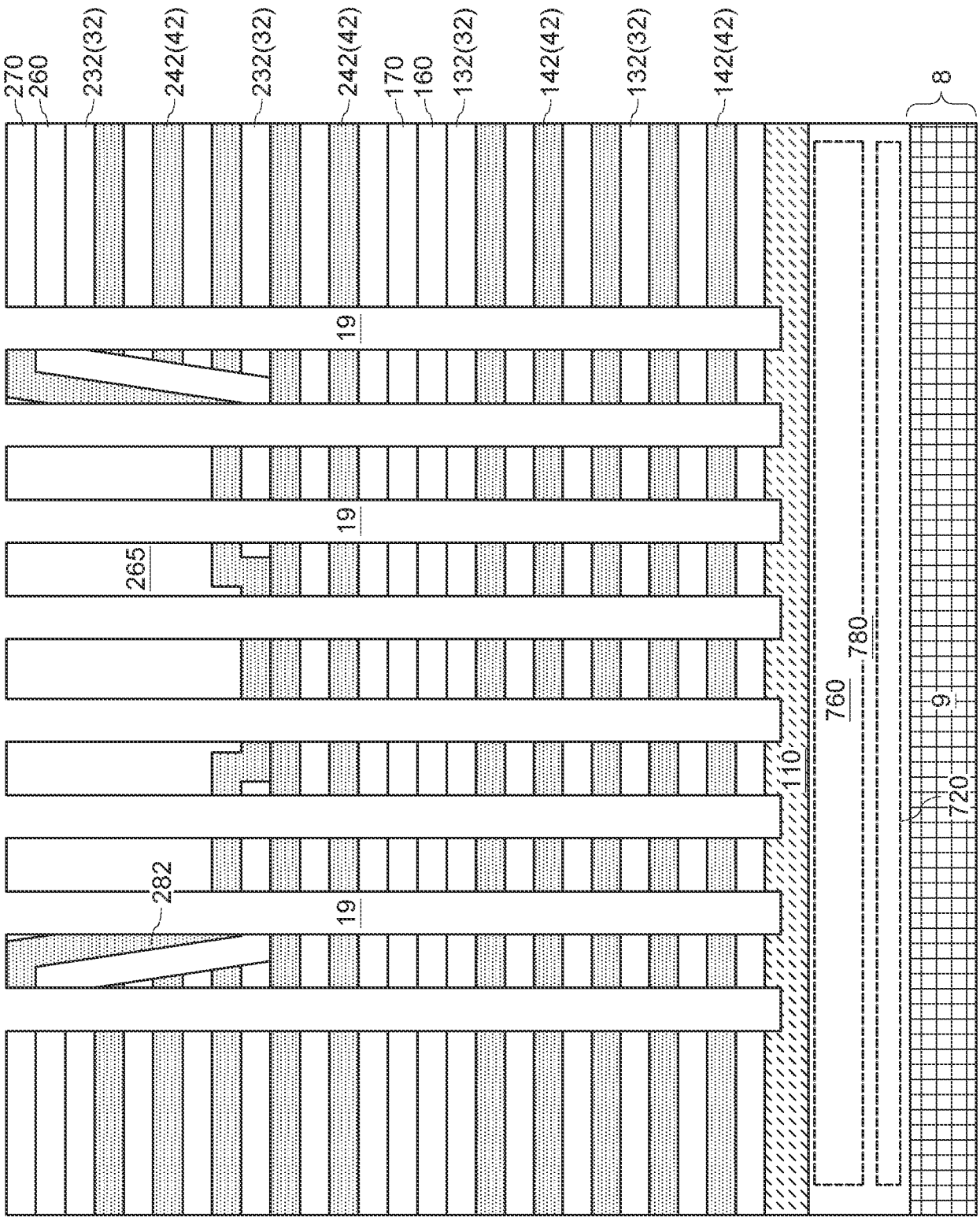
219
119
19

FIG. 12C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170
160
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142(42)
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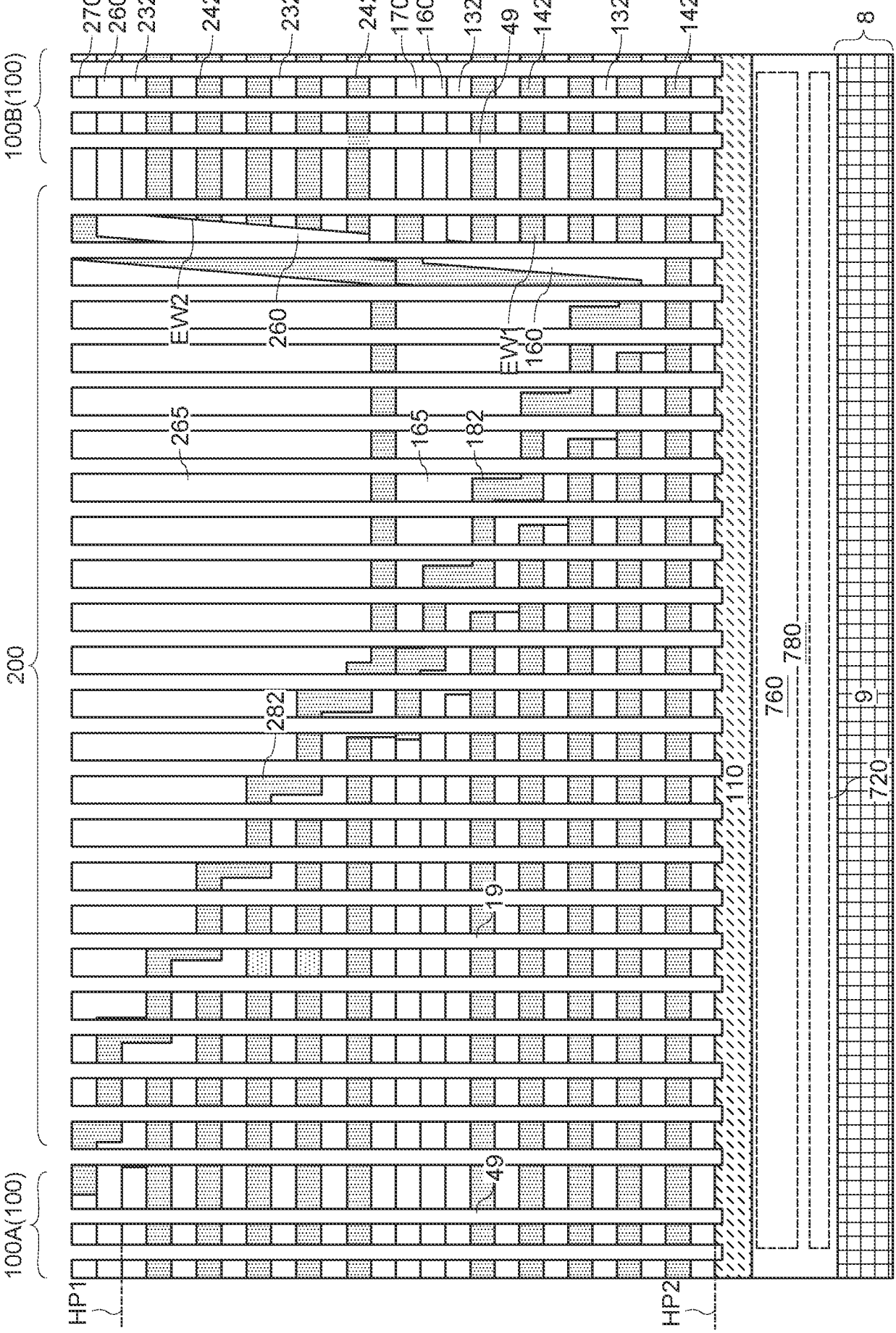
19
265
19
282
780
760
9
110
720

FIG. 12D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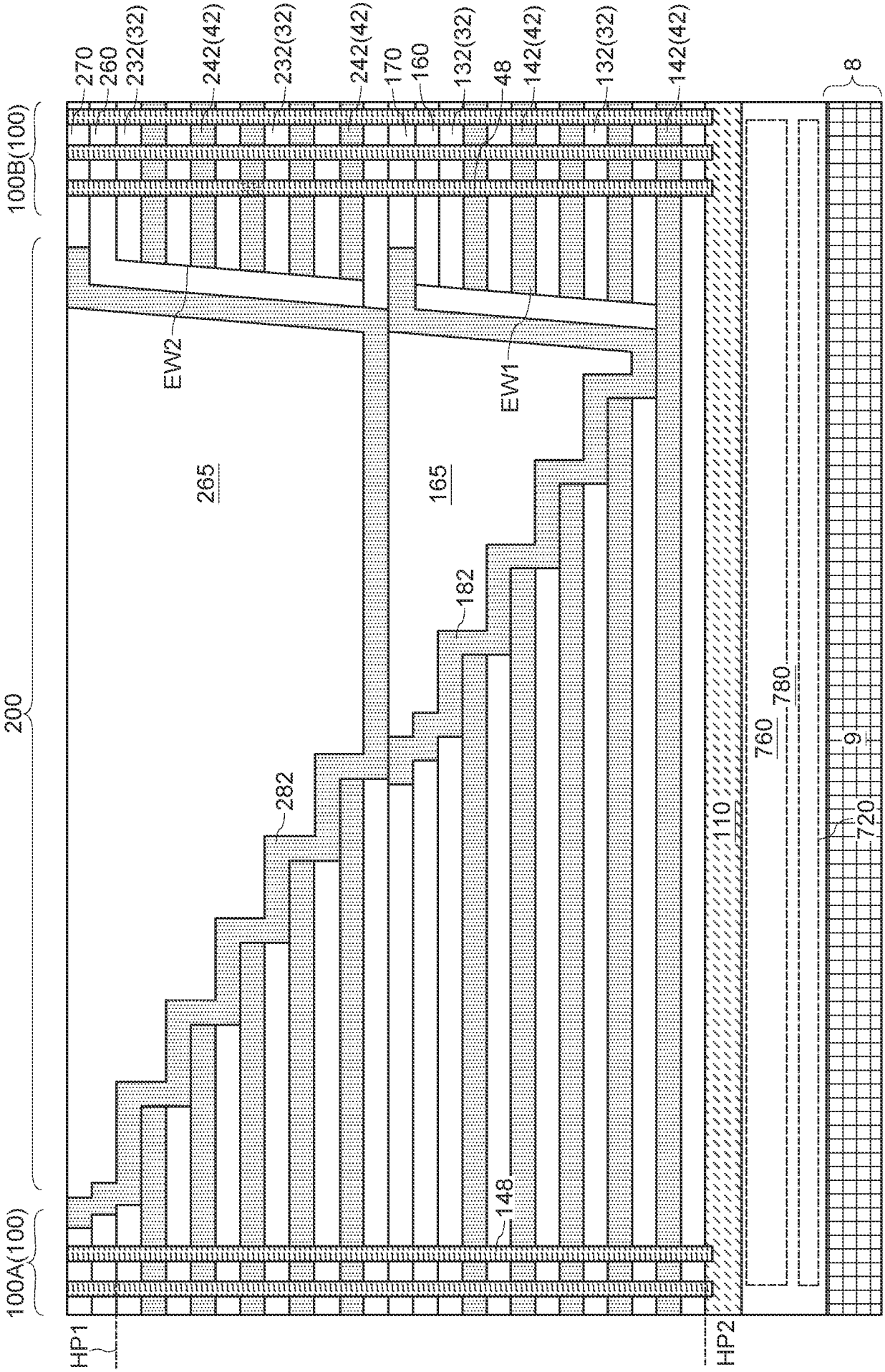
142(42)
132(32)
142(42)
8
100B(100)
200
100A(100)
EW2
260
EW1
160
265
165
182
282
760
780
9
720
110
19
49
HP1
HP2

FIG. 12E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142(42)
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142(42)
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100B(100)
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100A(100)
EW2
EW1
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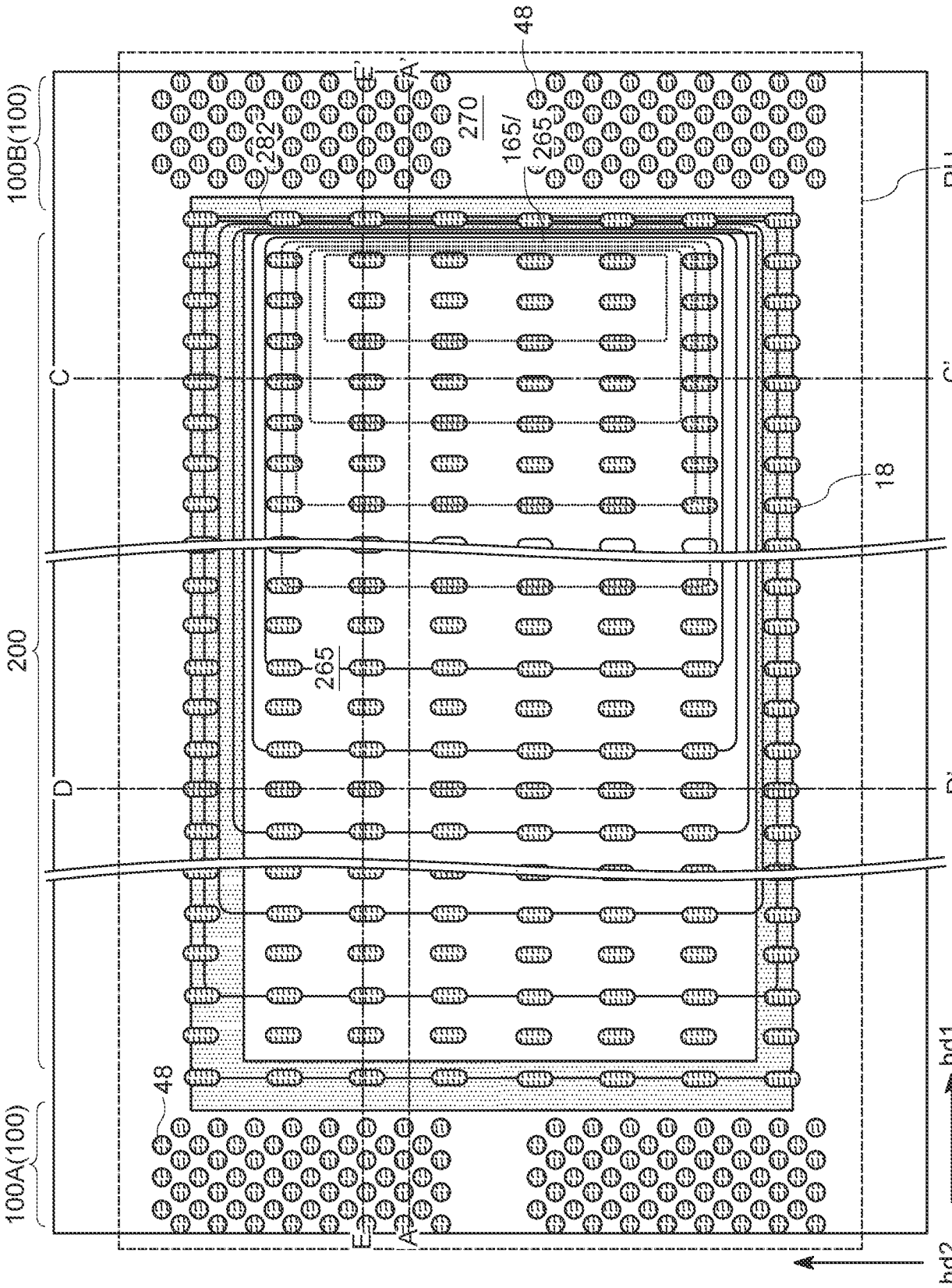
165
182
282
148
110
760
780
9
720
HP1
HP2

FIG. 13A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E
E'
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A'
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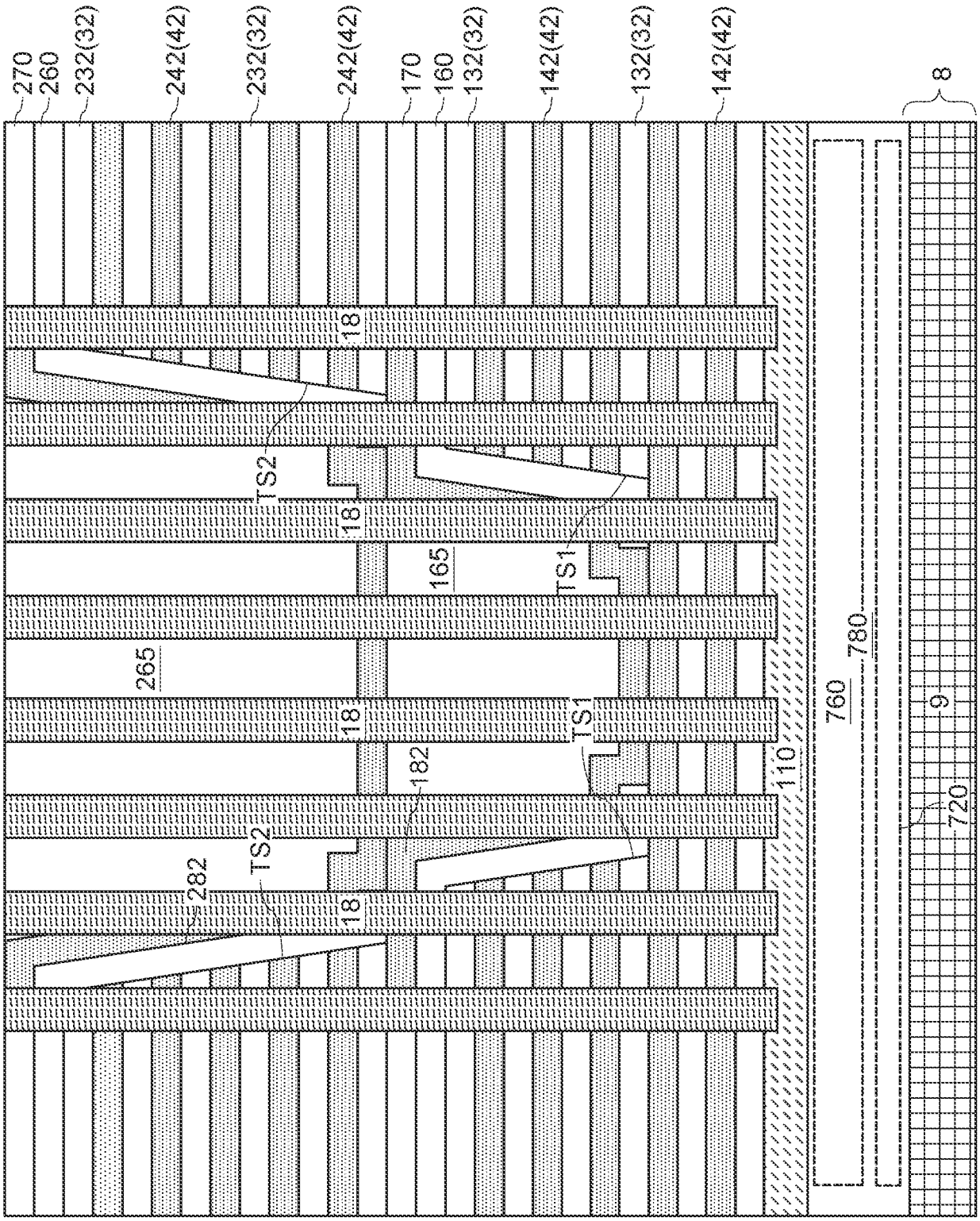
282
165/265
RU
100B(100)
C
C'
18
200
265
D
D'
48
100A(100)
E
A
hd1
hd2

FIG. 13B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132(32)
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142(42)
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TS2
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165
TS1
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760
18
TS1
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110
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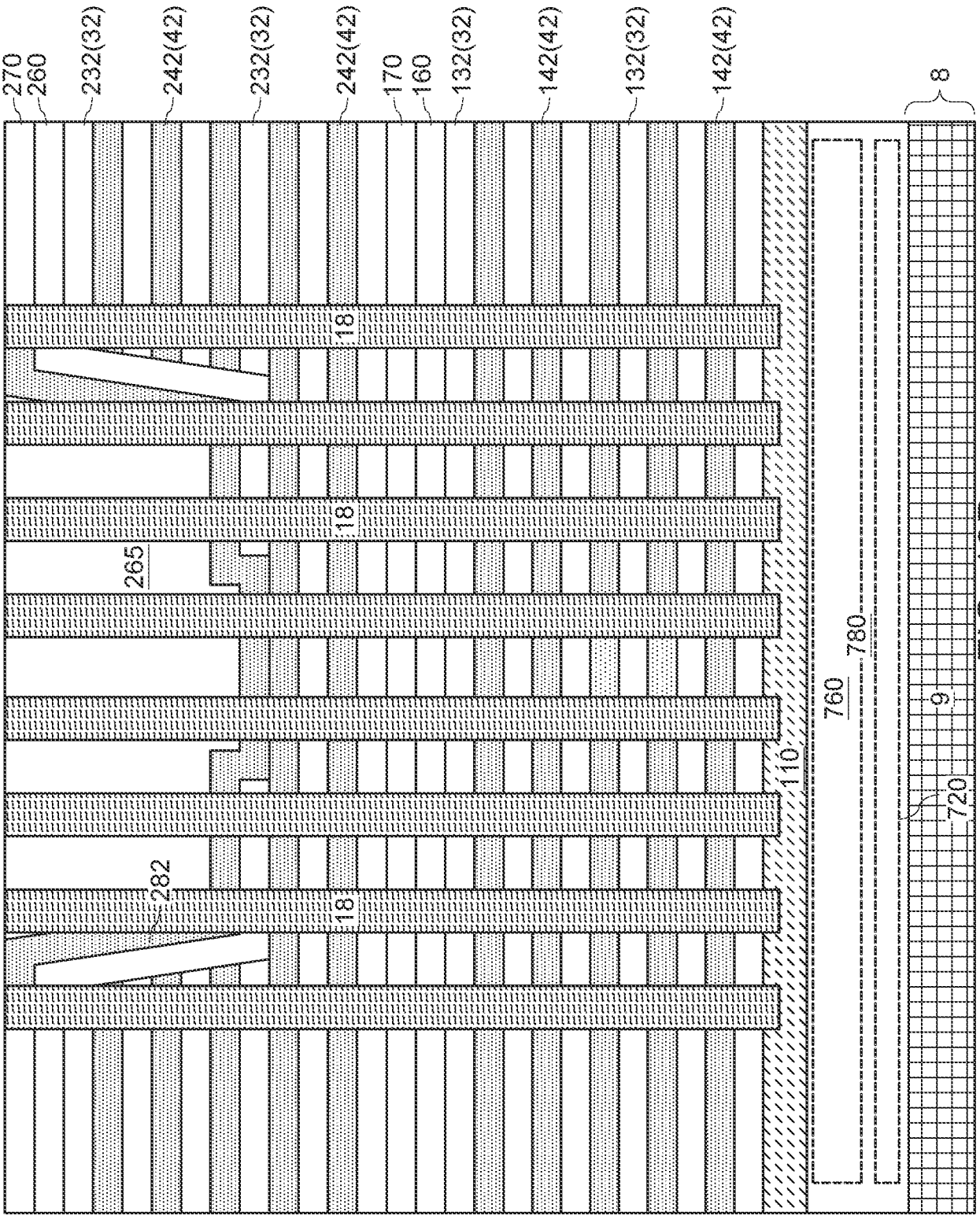
720
TS2
282
18

FIG. 13C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18
282
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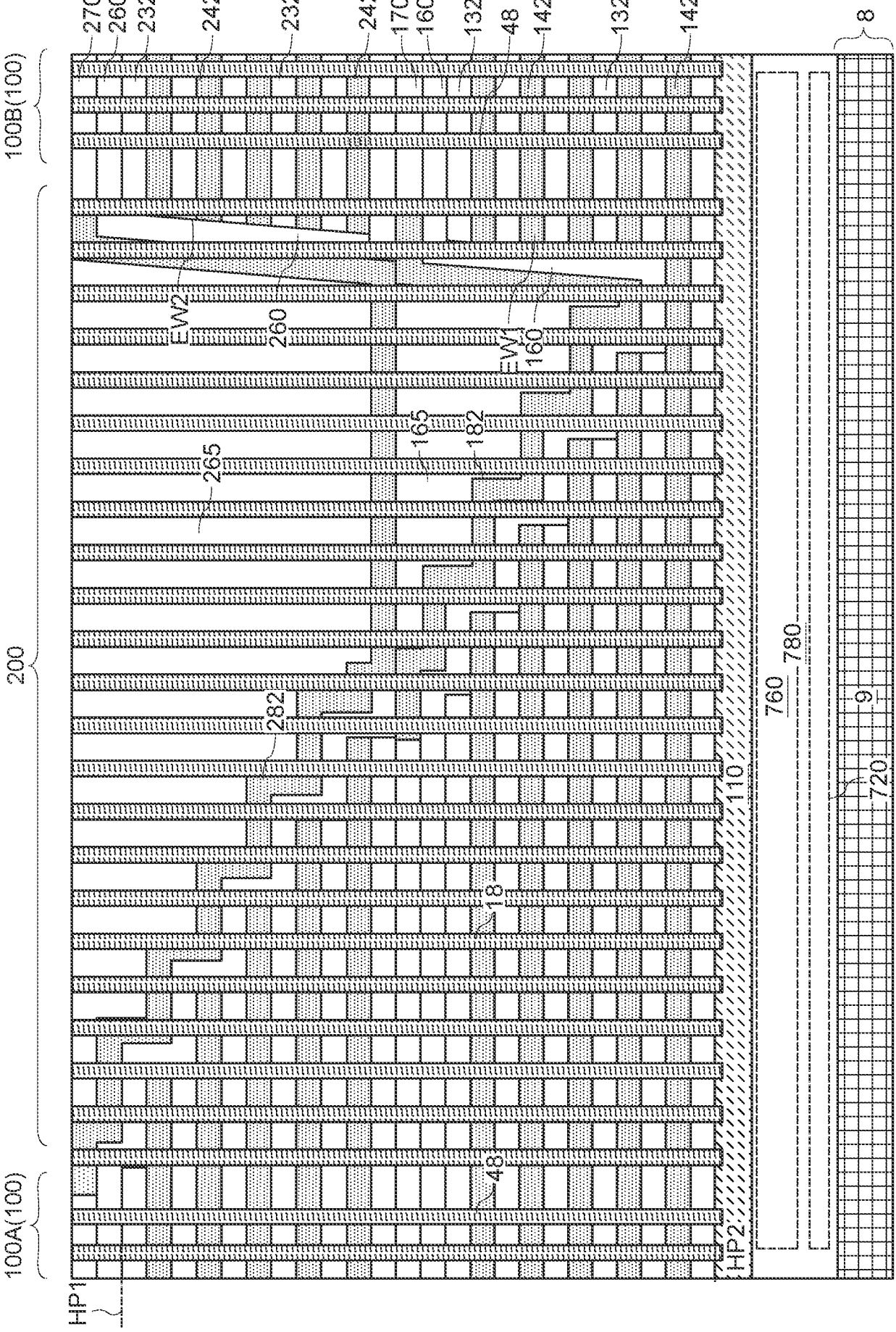
780
9
720

FIG. 13D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100B(100)
200
100A(100)
EW2
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EW1
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182
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282
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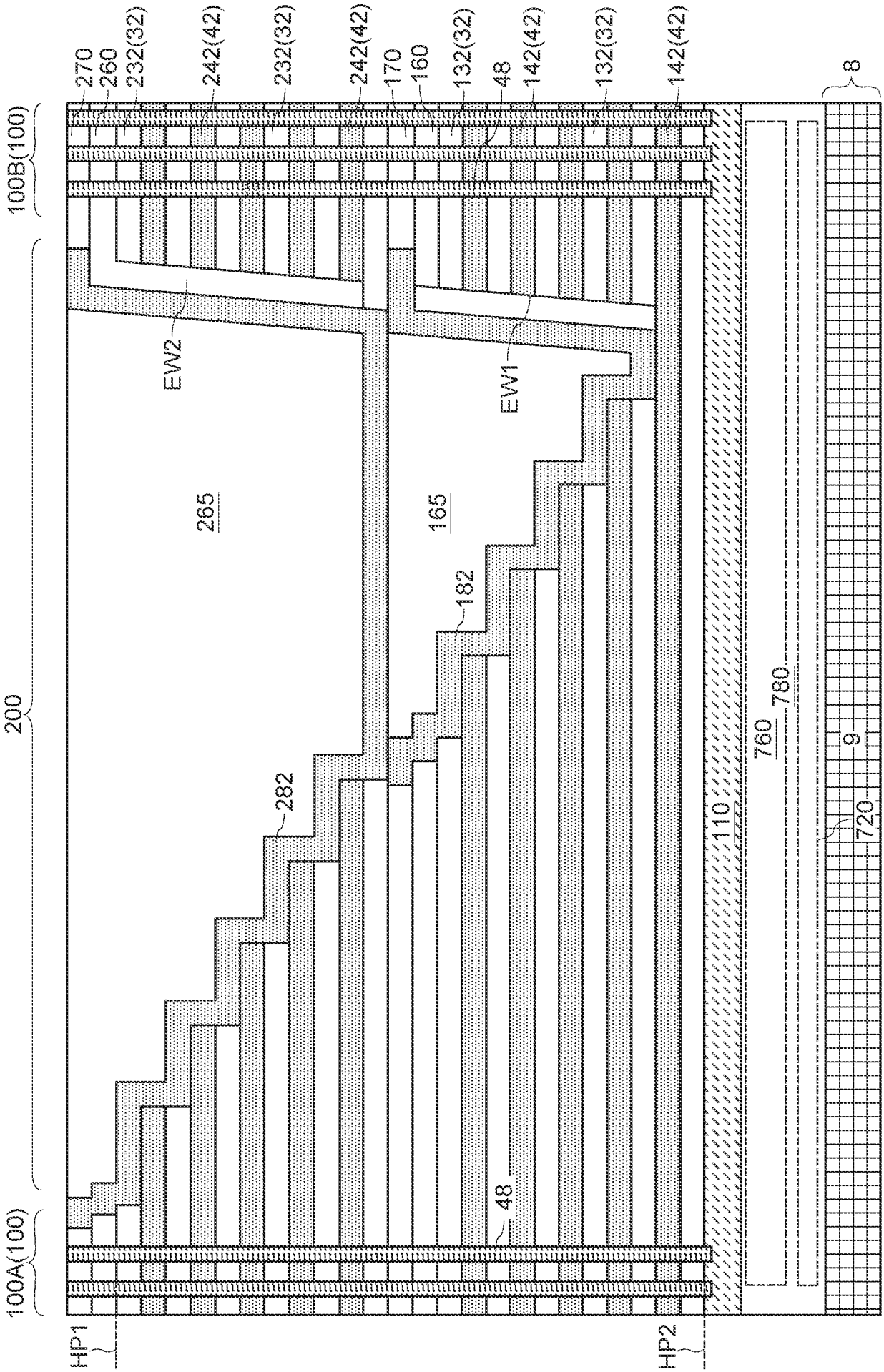
720
HP1
HP2

FIG. 13E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232(32)
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100B(100)
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EW2
EW1
265
165
182
282
48
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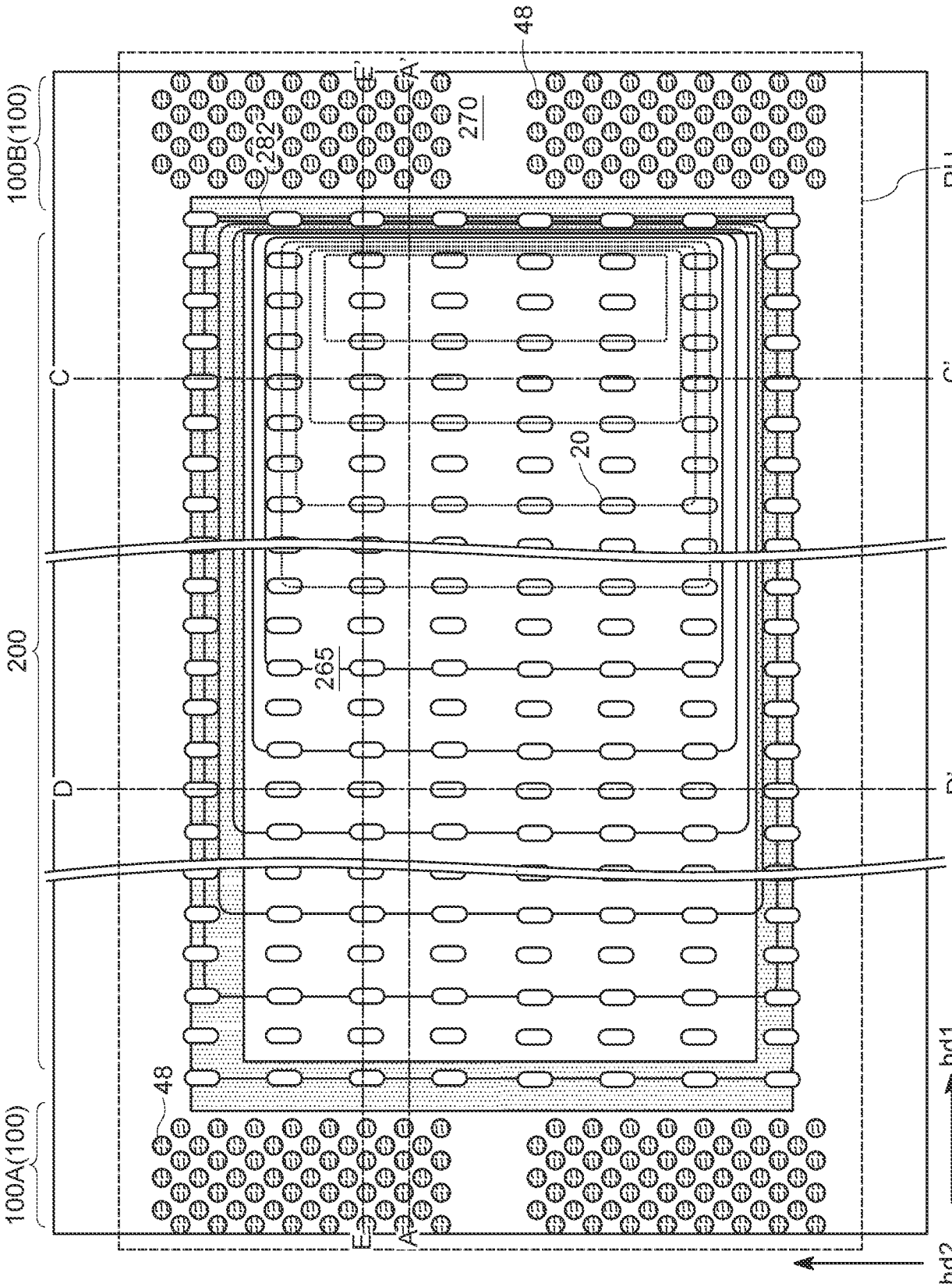
720
100A(100)
HP1
HP2

FIG. 14A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E
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A'
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282
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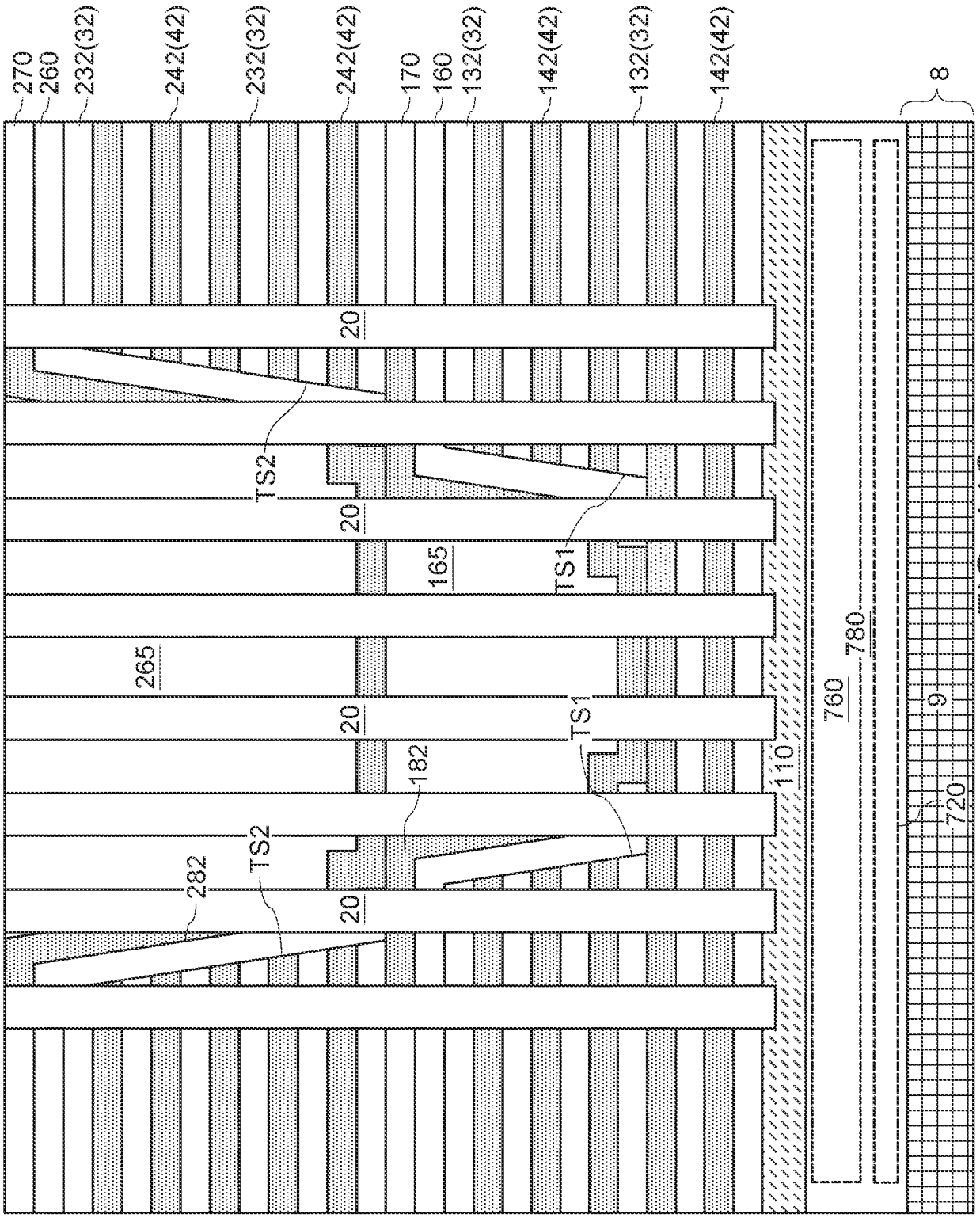
C'
20
200
265
D
D'
48
100A(100)
E
A
hd1
hd2

FIG. 14B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142(42)
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TS2
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165
TS1
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TS1
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182
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FIG. 14C

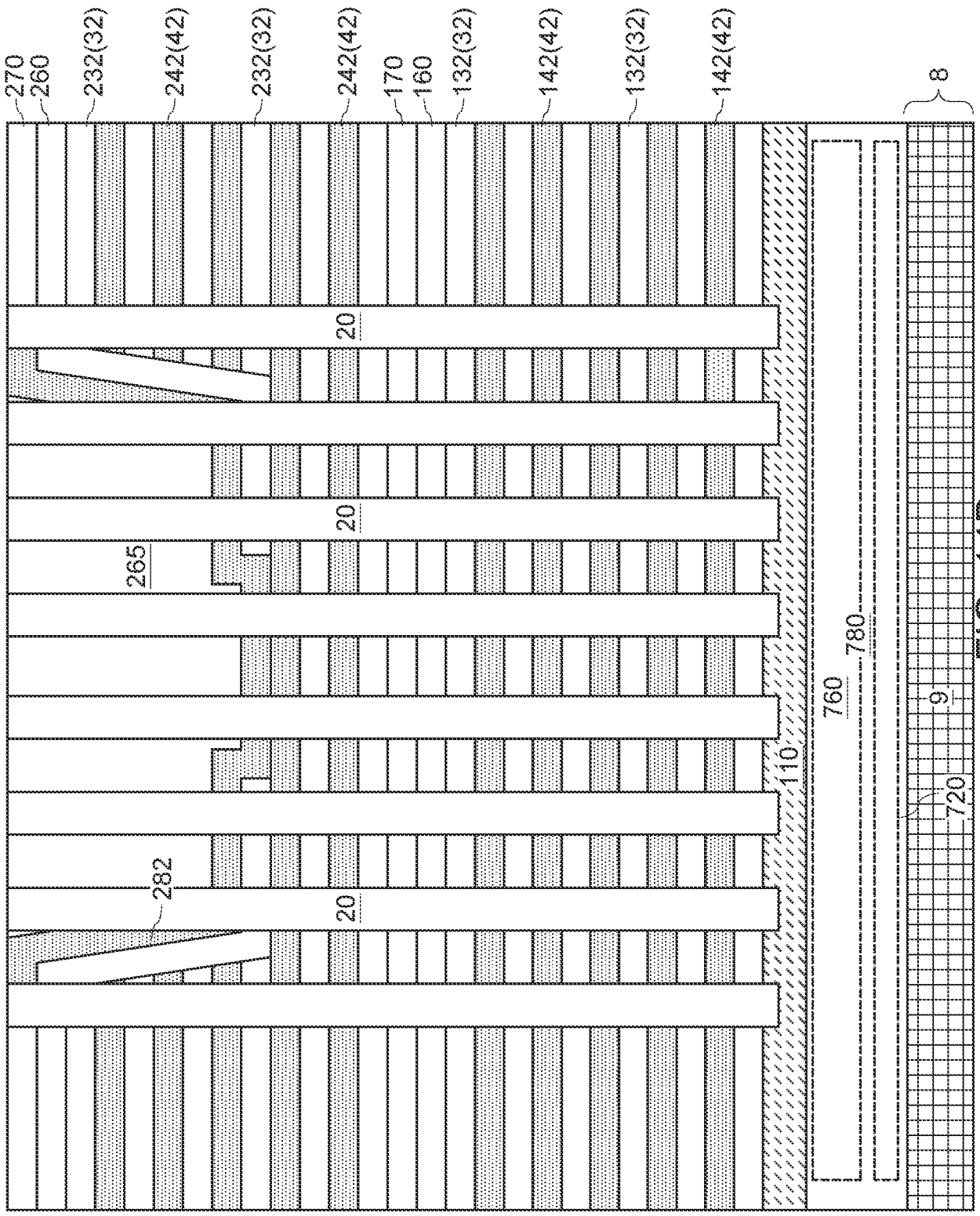
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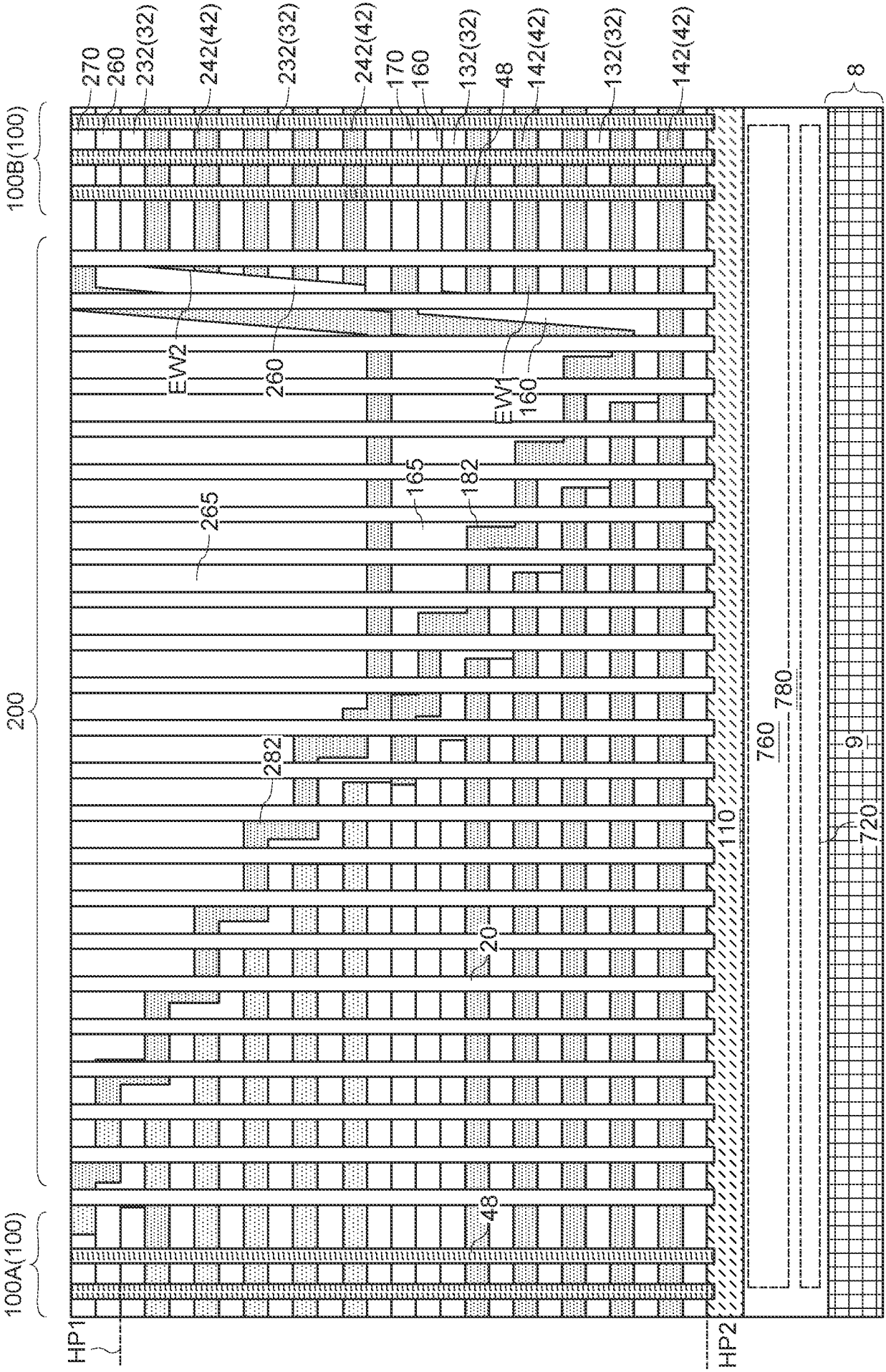
FIG. 14D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100A(100)
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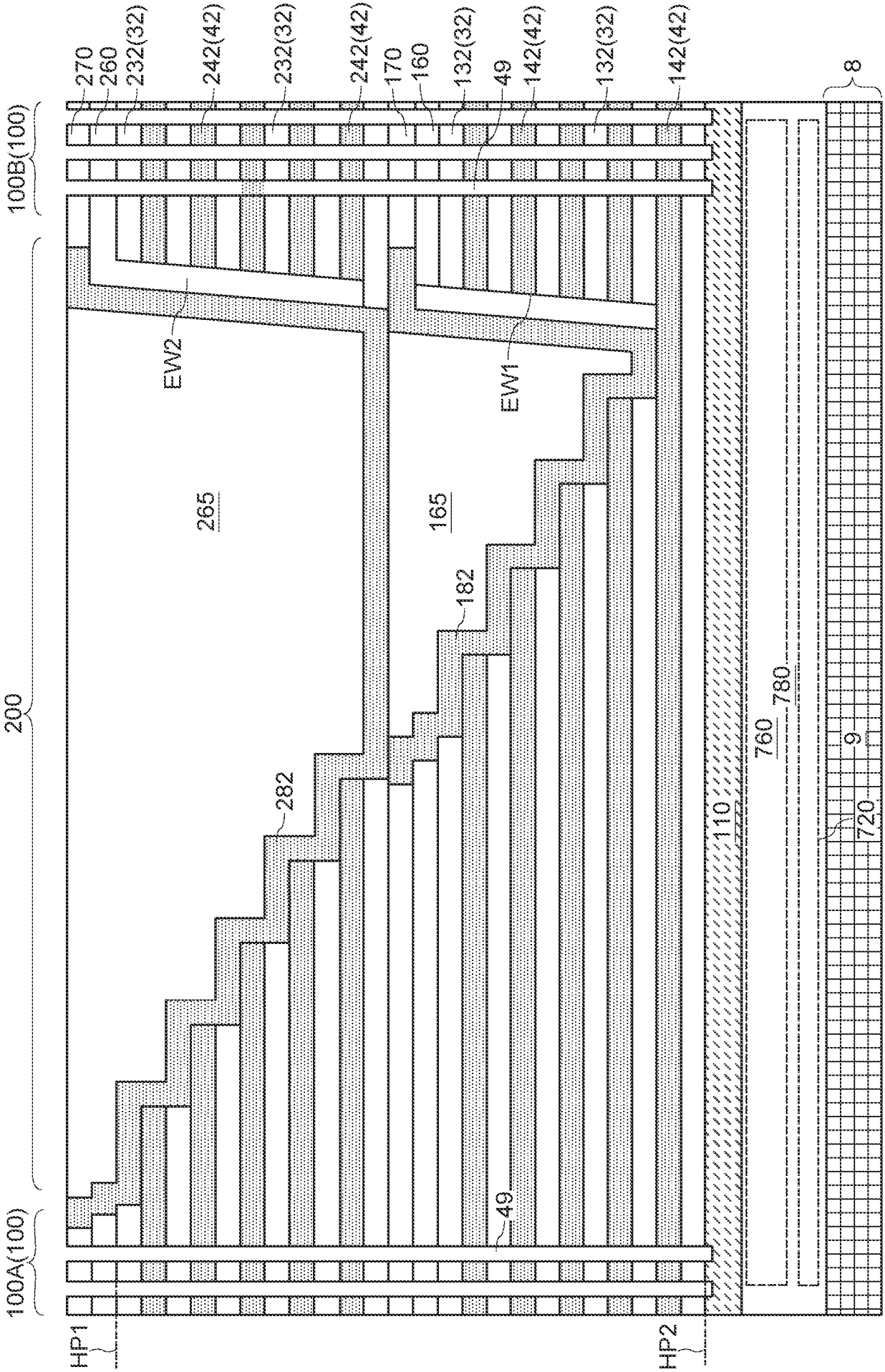
HP1
HP2

FIG. 14E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EW1
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182
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110
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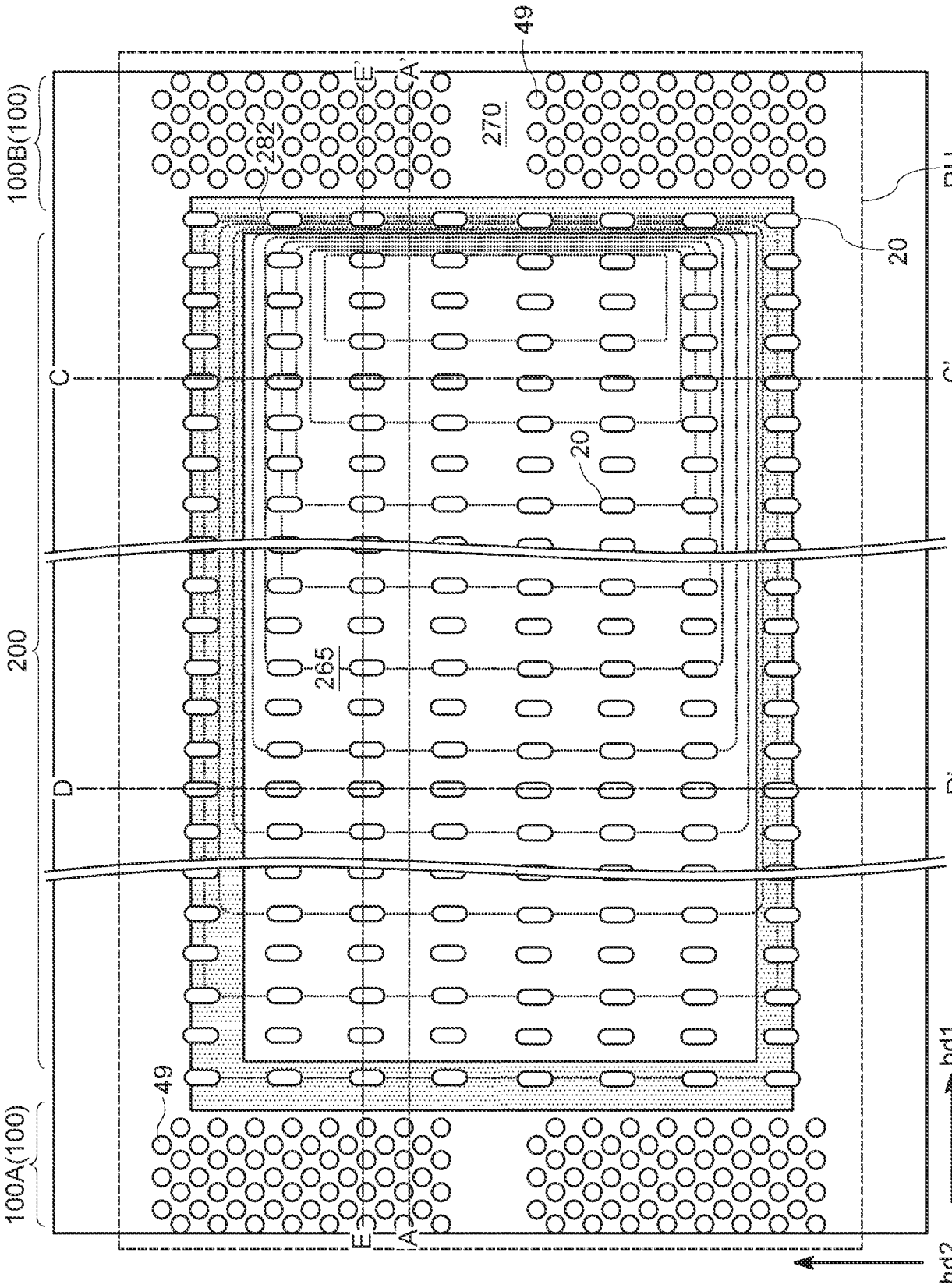
720
100A(100)
HP1
HP2

FIG. 15A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E'
A'
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282
RU
100B(100)
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C'
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200
265
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D'
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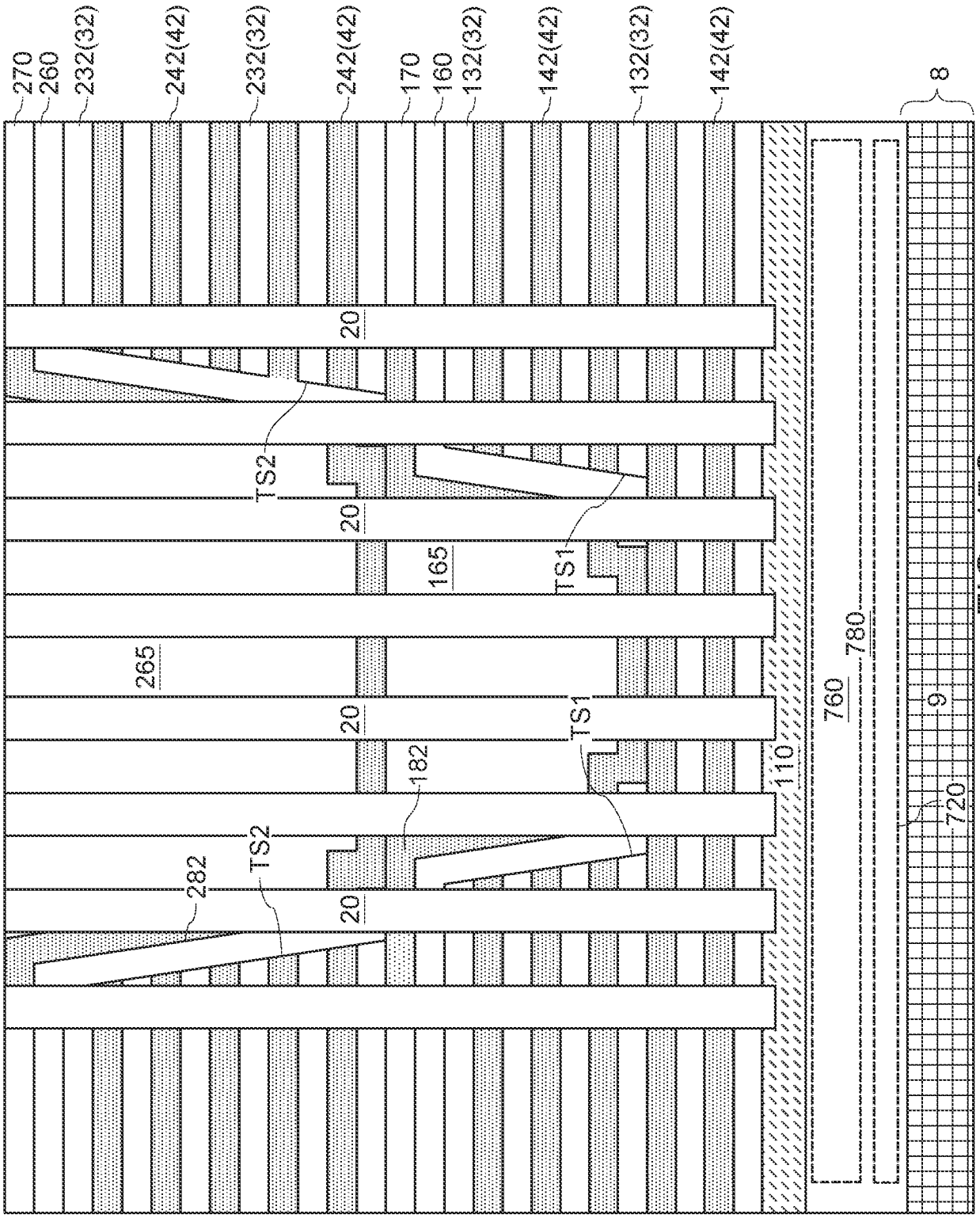
100A(100)
E
A
hd1
hd2

FIG. 15B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8
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TS2
20
165
TS1
265
780
760
20
TS1
9
182
110
720
TS2
282
20

FIG. 15C

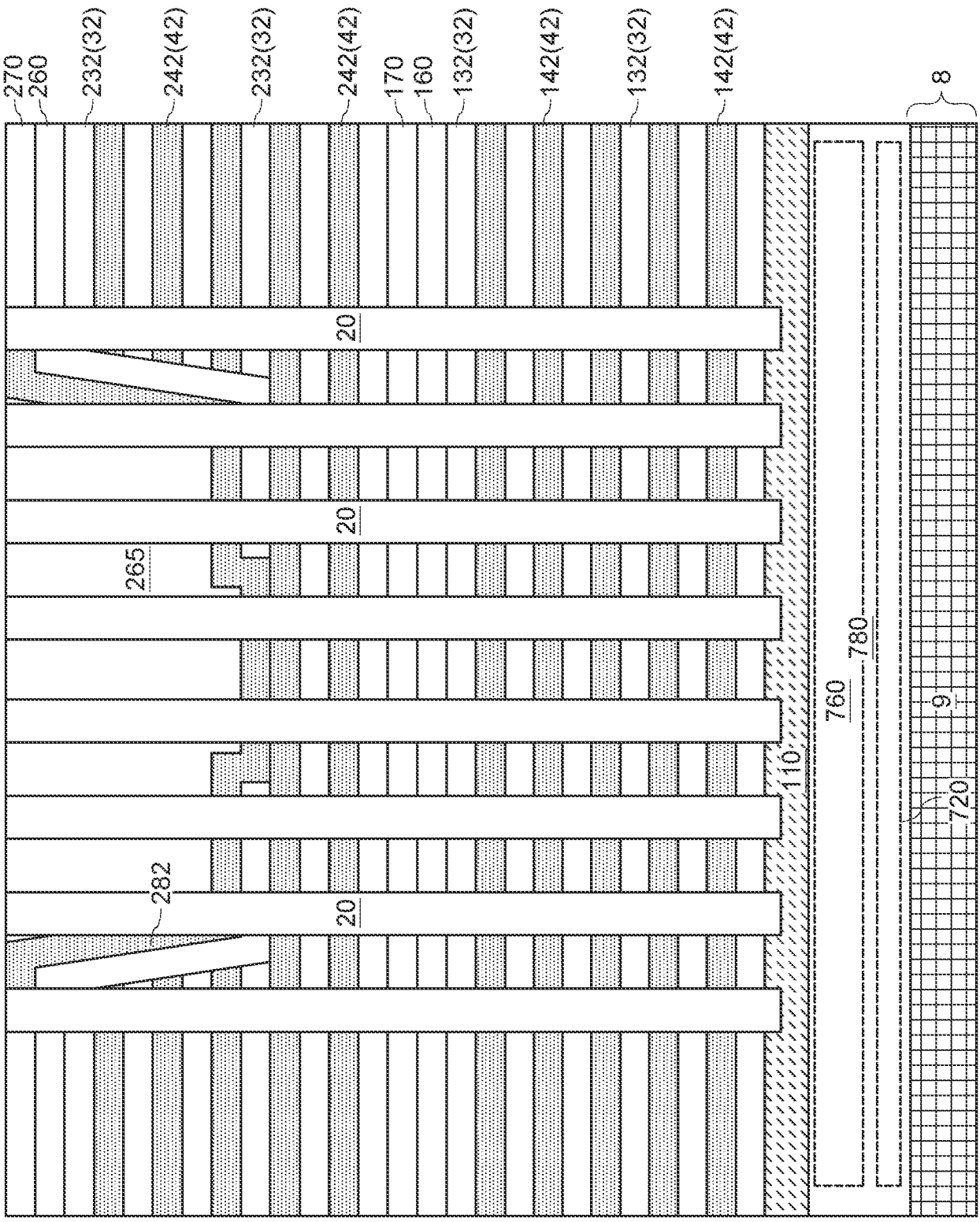

270
260
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
8
20
20
265
20
282
110
760
780
9
720

FIG. 15D

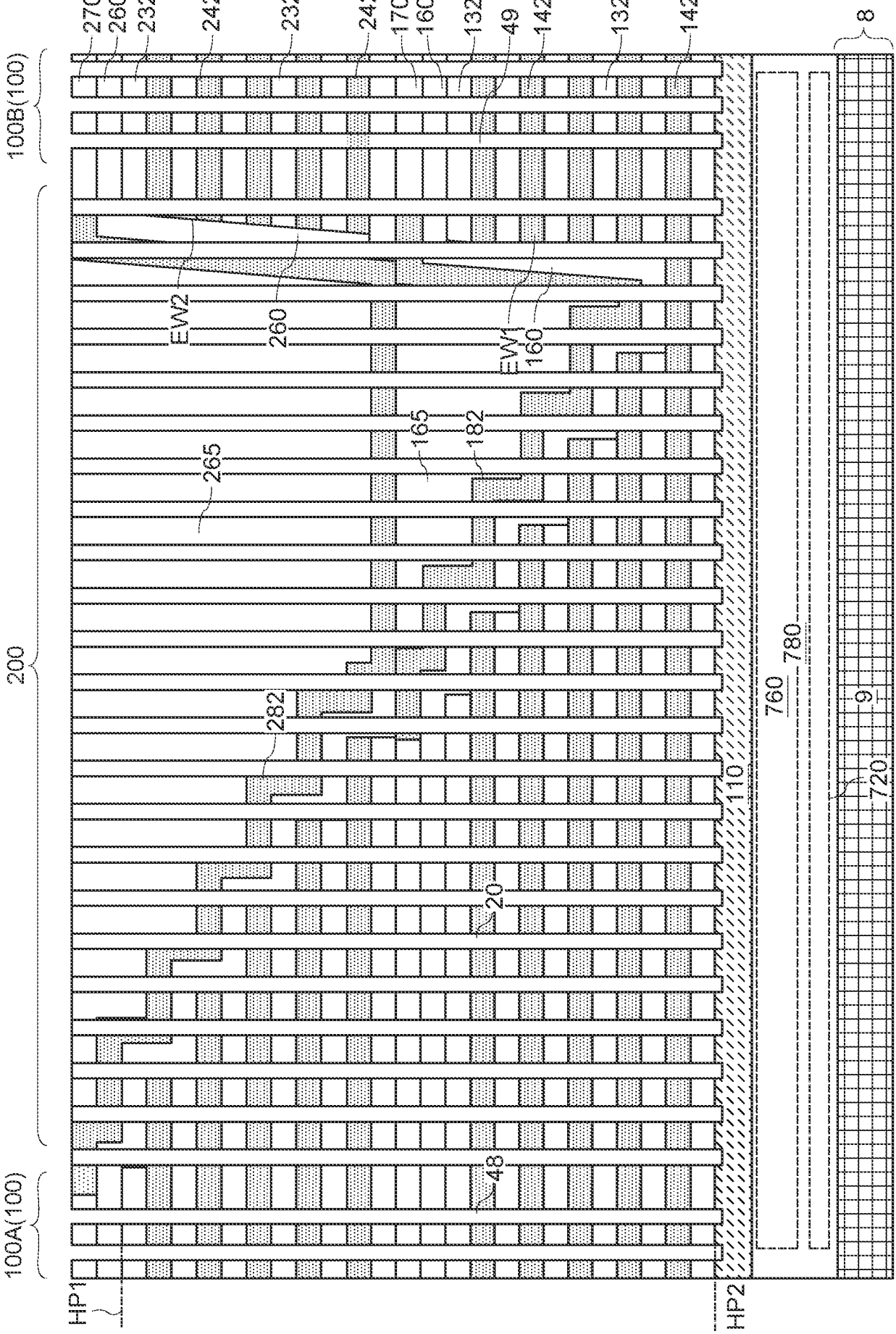

270
260
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
49
142(42)
132(32)
142(42)
8
100B(100)
200
100A(100)
EW2
260
EW1
160
165
182
265
282
110
20
48
760
780
9
720
HP1
HP2

FIG. 15E

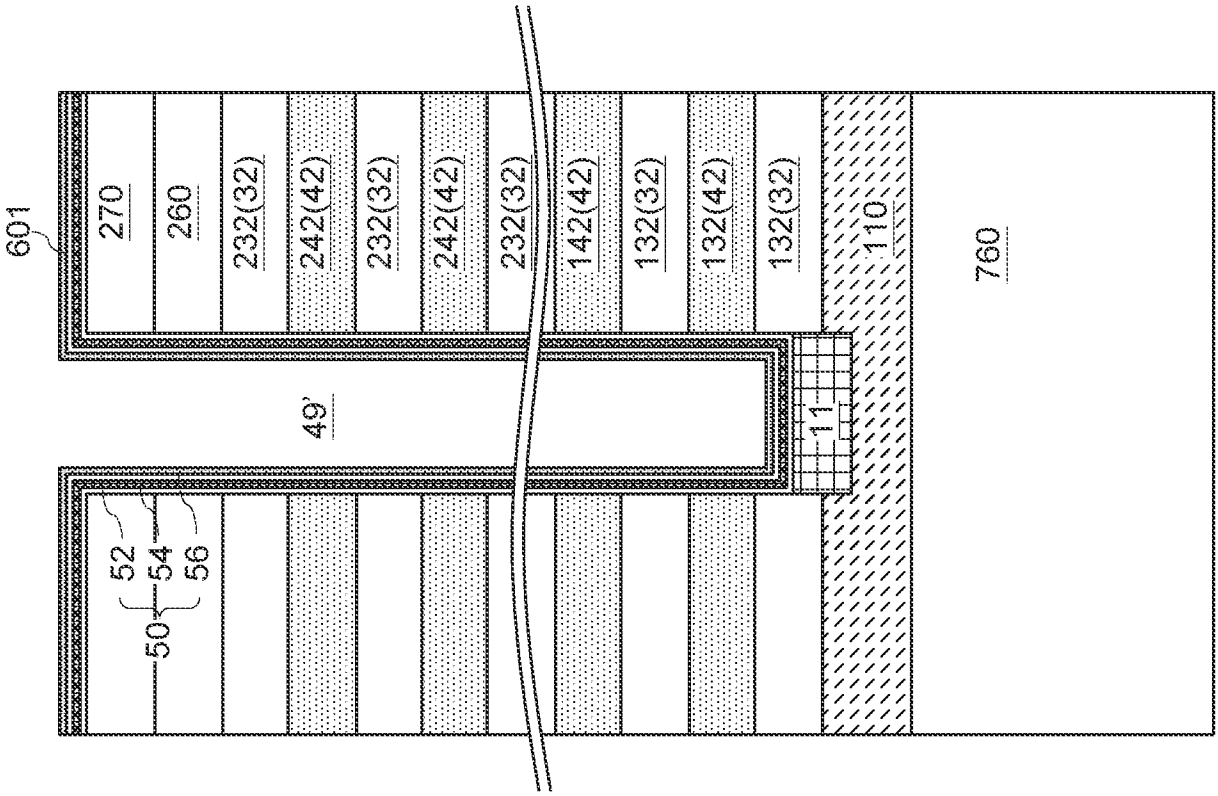


FIG. 16B

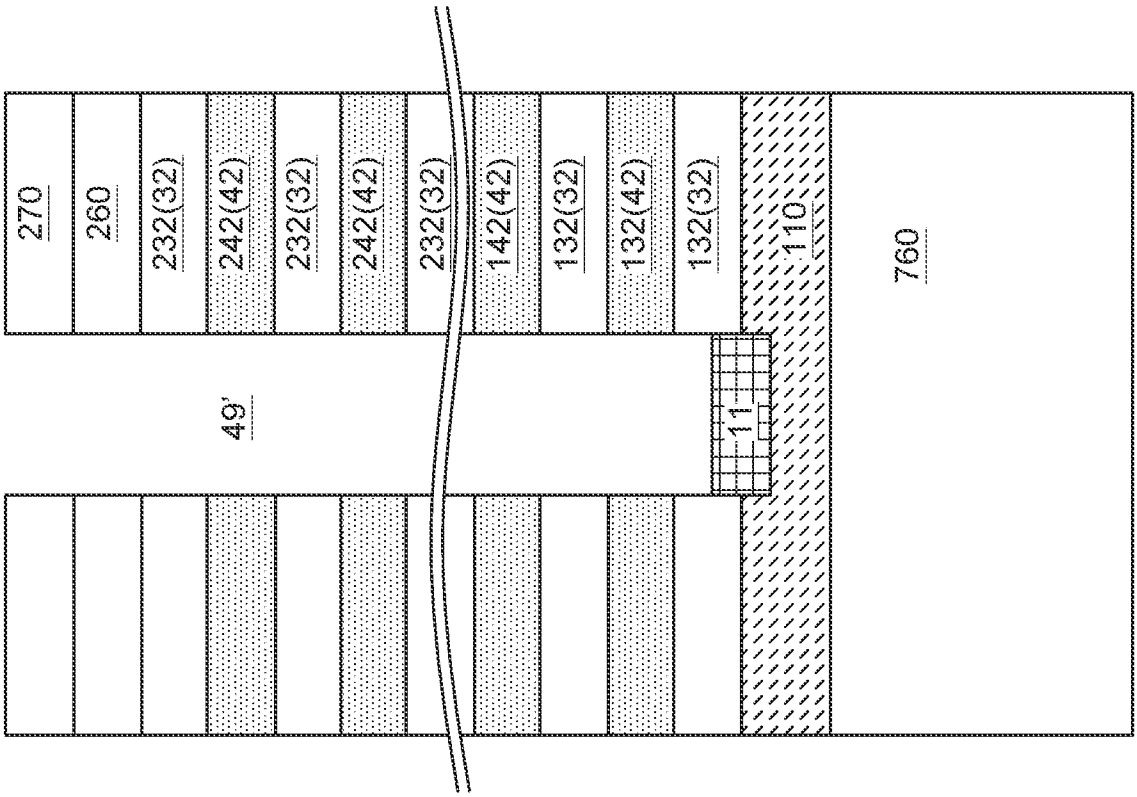


FIG. 16A

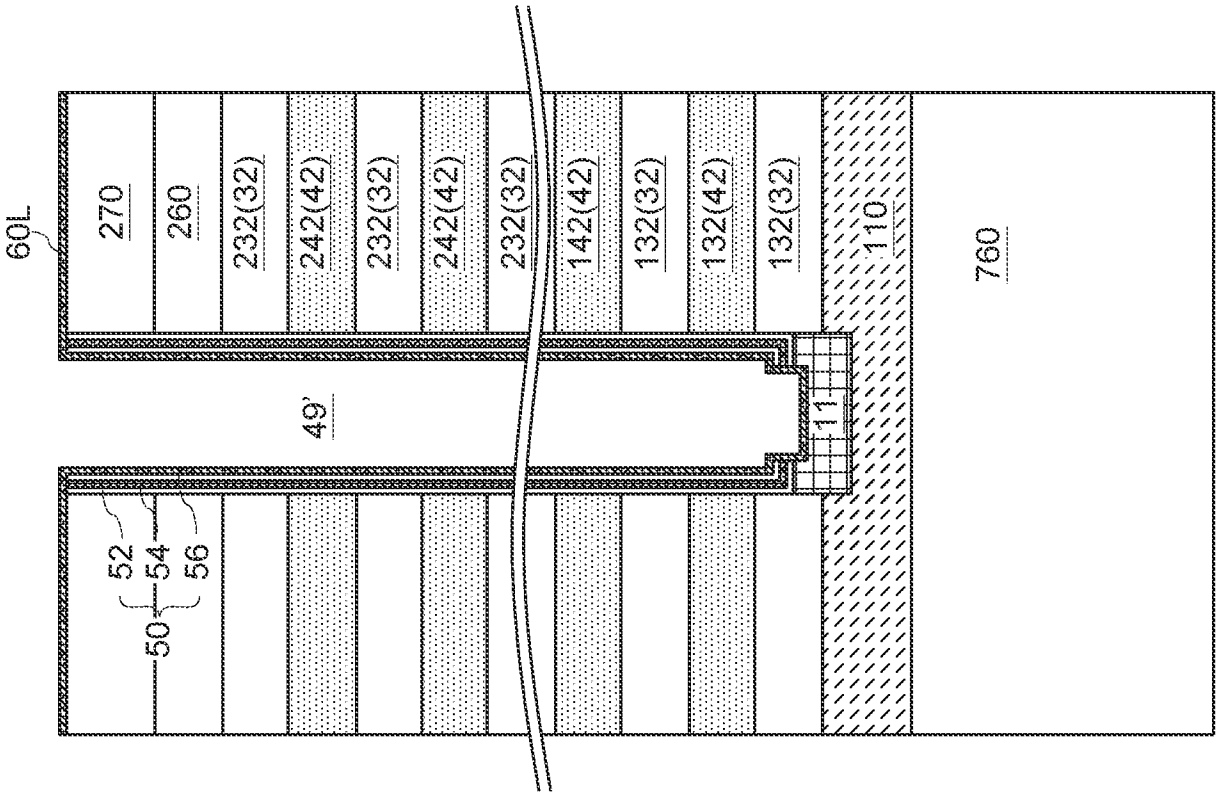


FIG. 16D

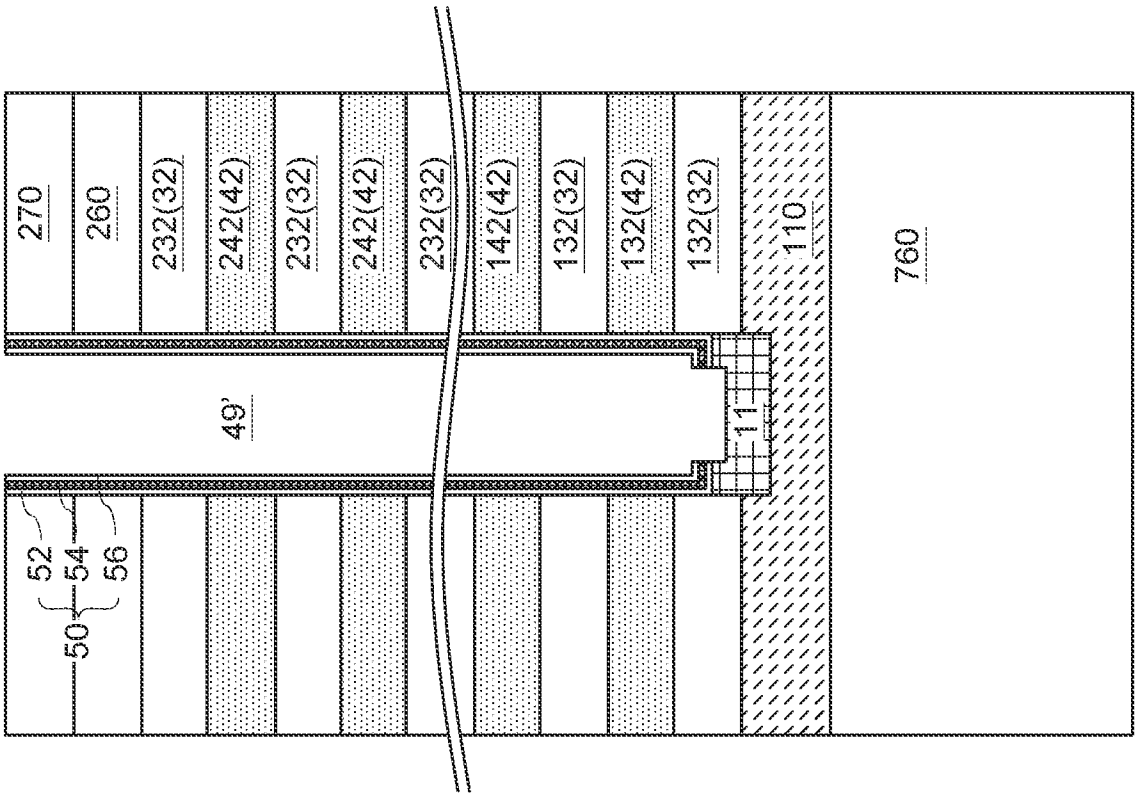


FIG. 16C

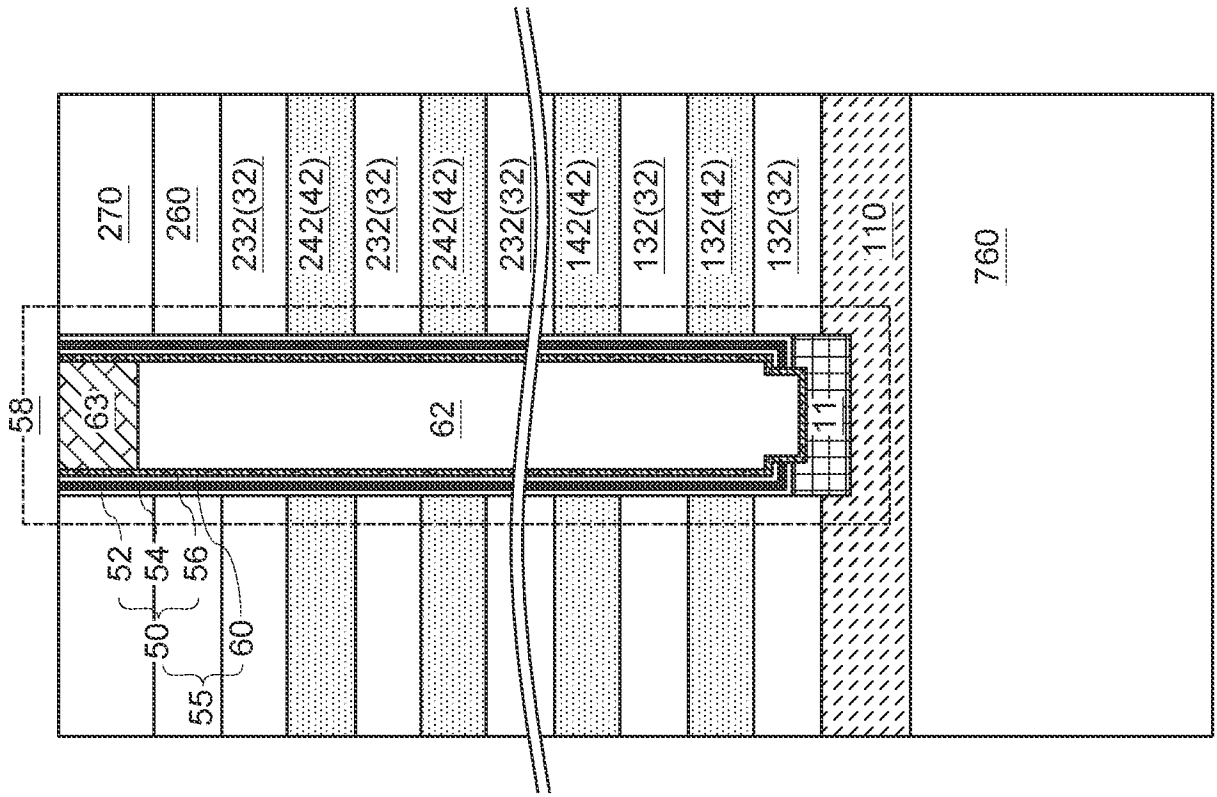


FIG. 16F

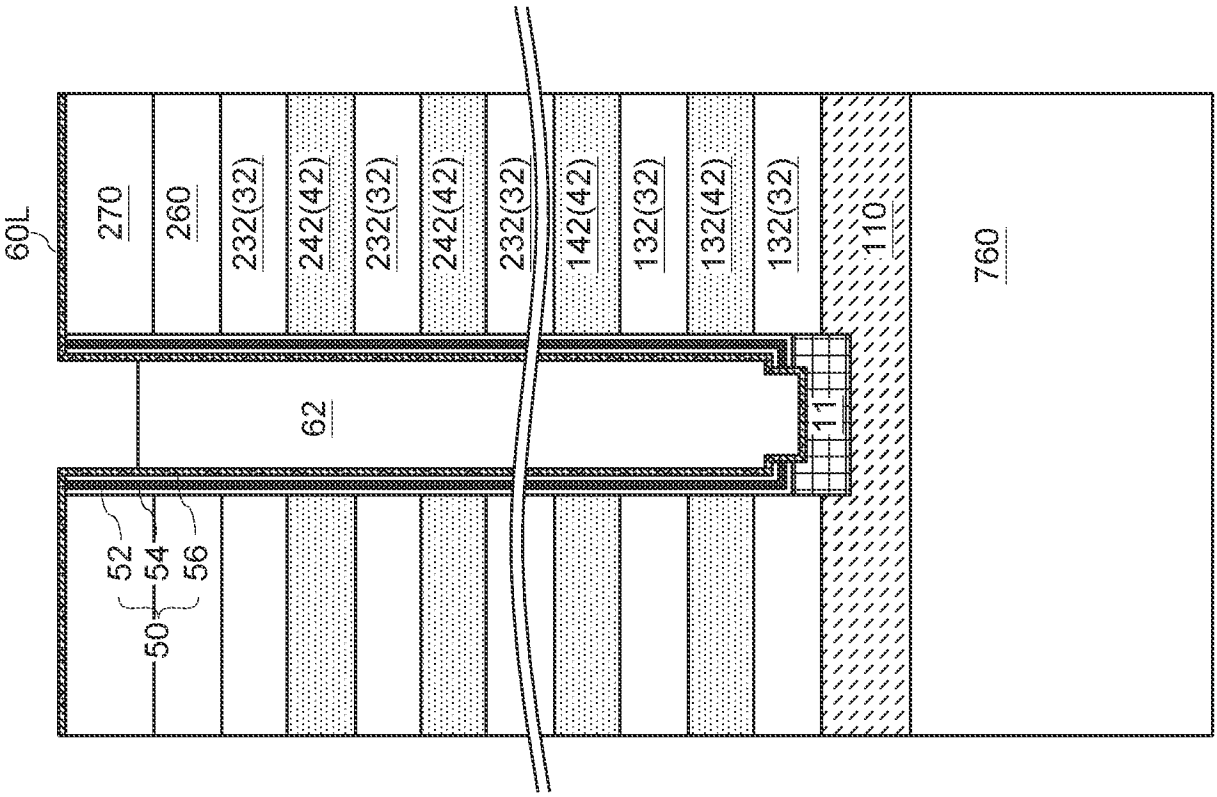


FIG. 16E

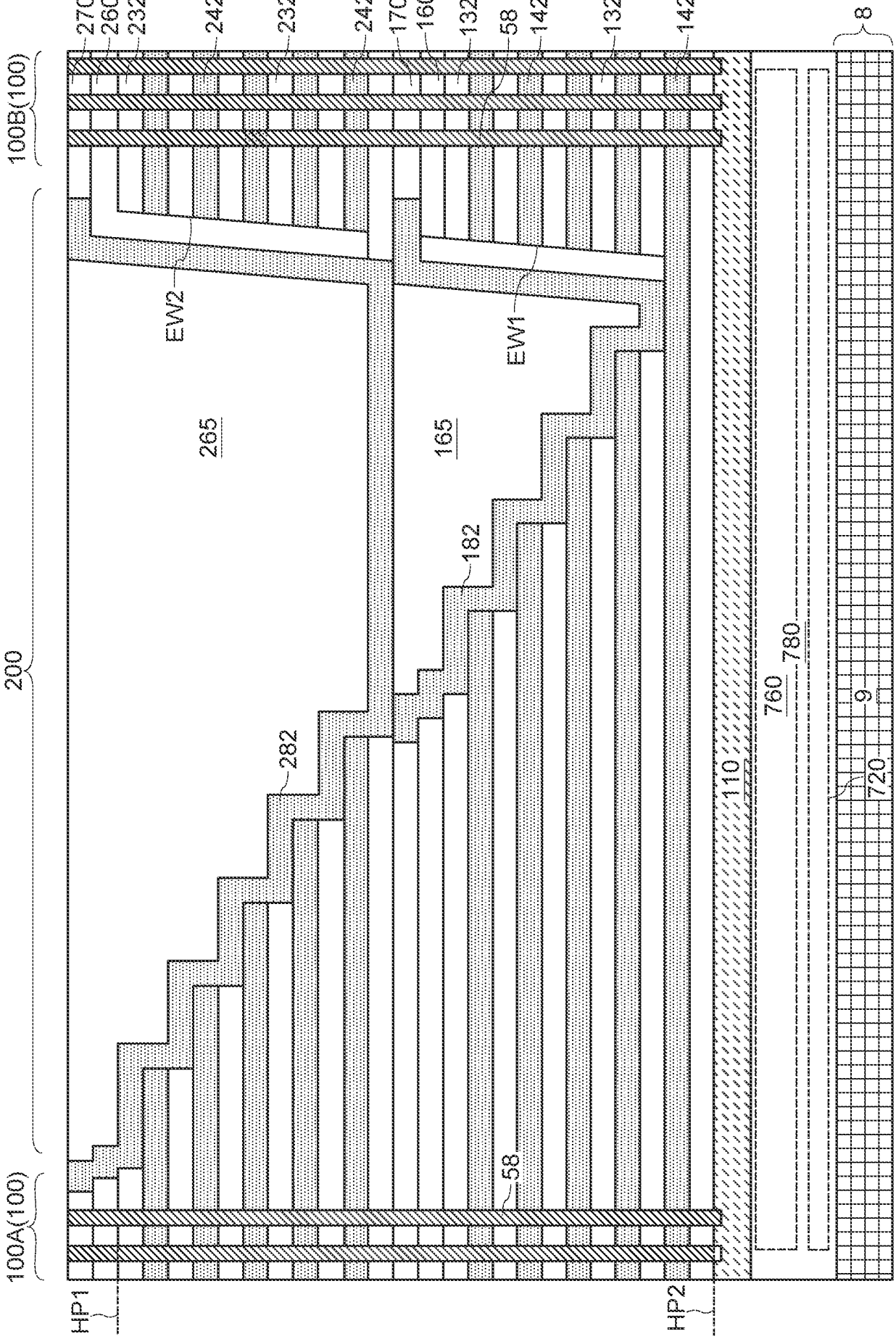

270
260
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
58
142(42)
132(32)
142(42)
8
100B(100)
200
100A(100)
EW2
EW1
265
165
182
282
58
110
760
780
9
720
HP1
HP2

FIG. 17A

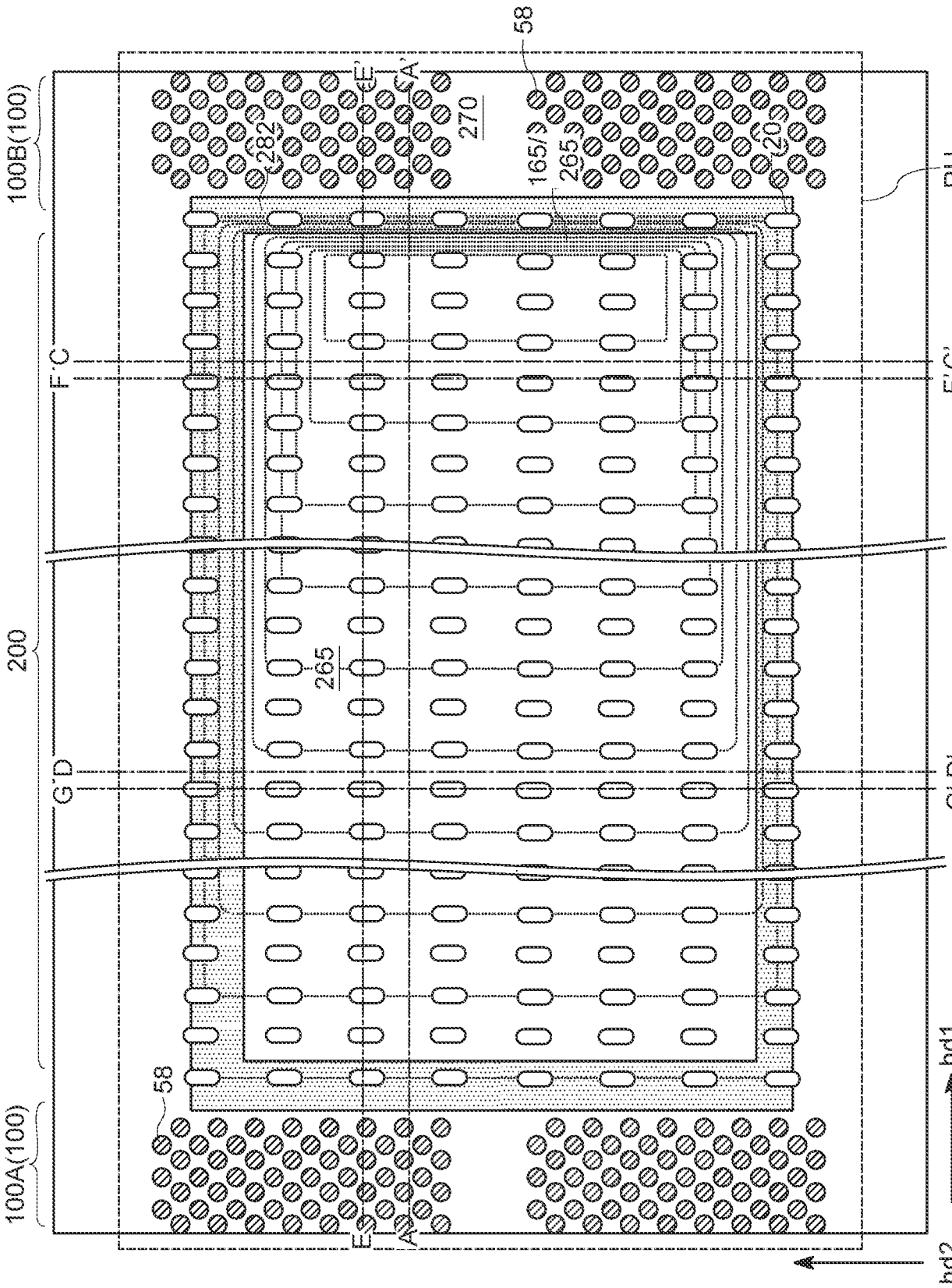
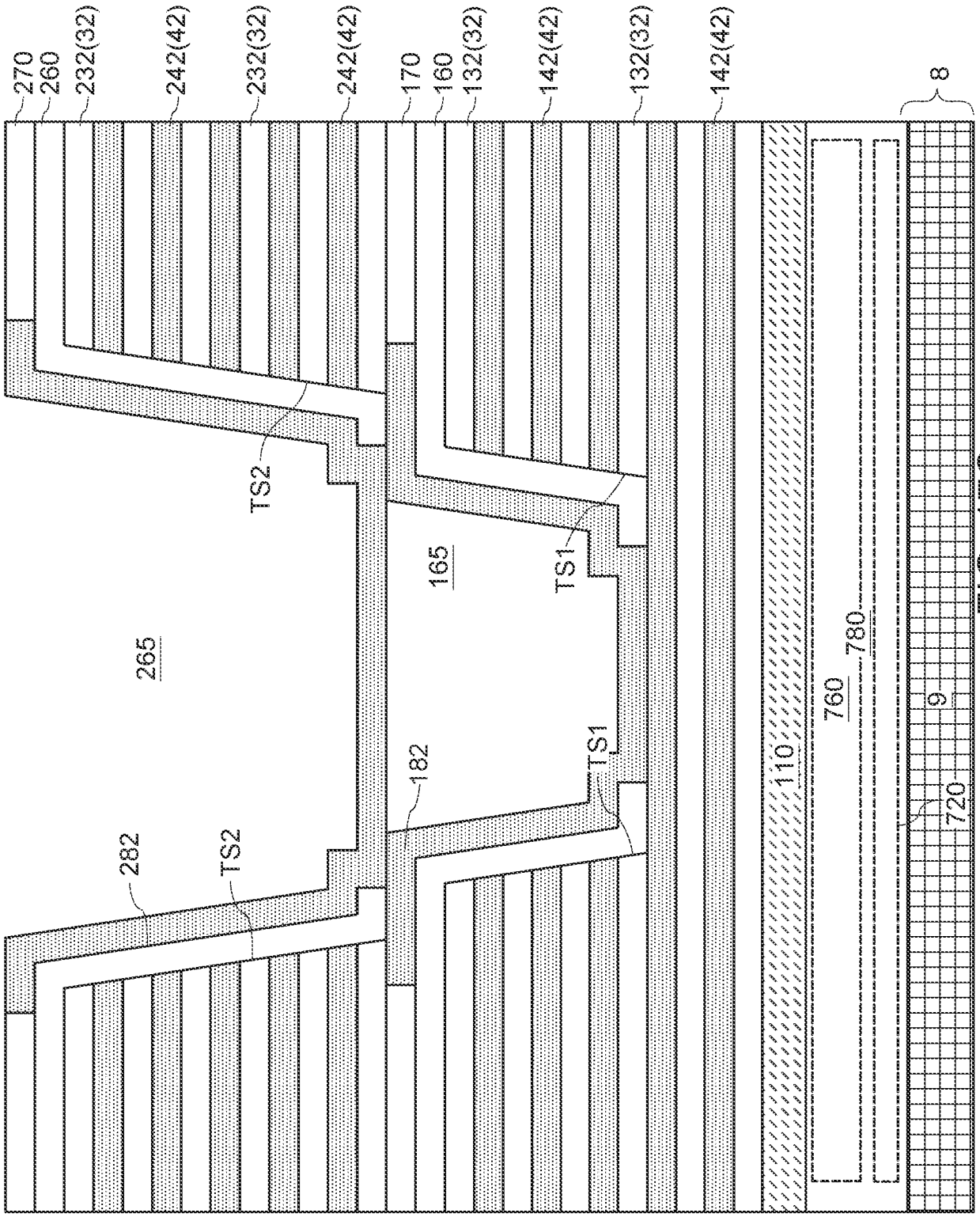

58
E
E'
A
A'
270
282
165/9
265
200
RU
100B(100)
F'C'
200
265
G'D'
58
100A(100)
E
A
hd1
hd2

FIG. 17B


270
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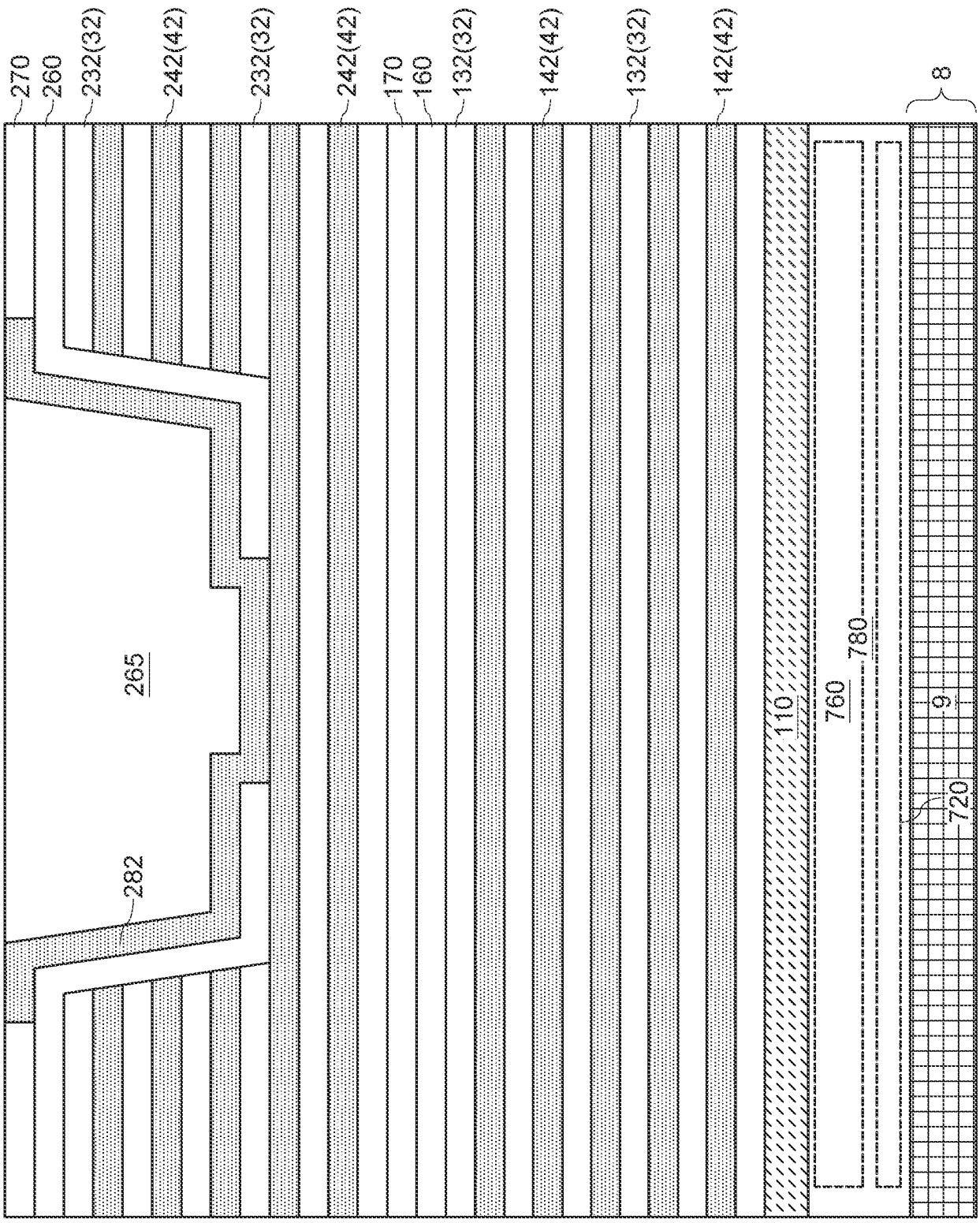
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
8
TS2
165
TS1
265
780
760
9
110
182
TS1
720
282
TS2

FIG. 17C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232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
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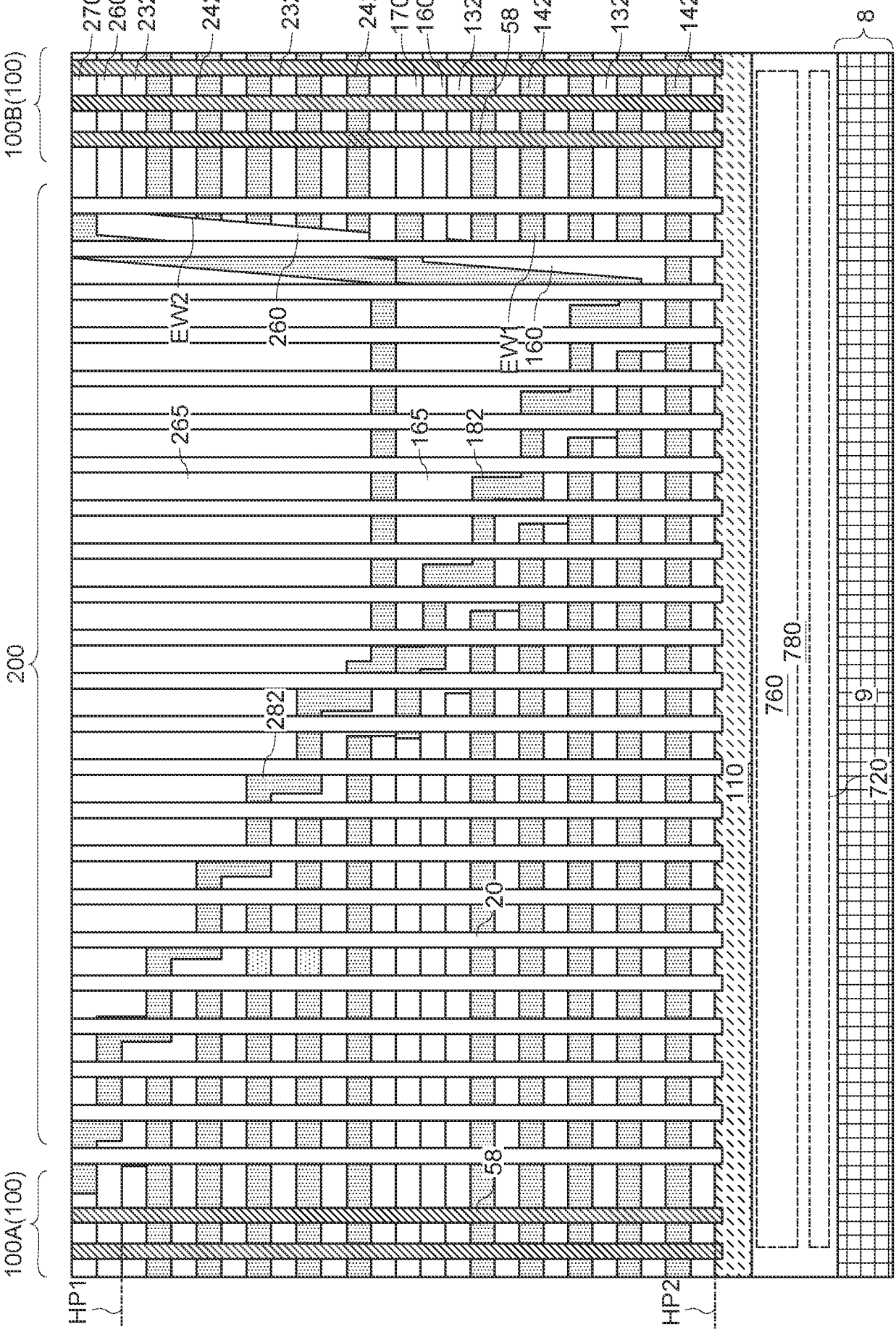
265
282
110
760
780
9
720

FIG. 17D


270
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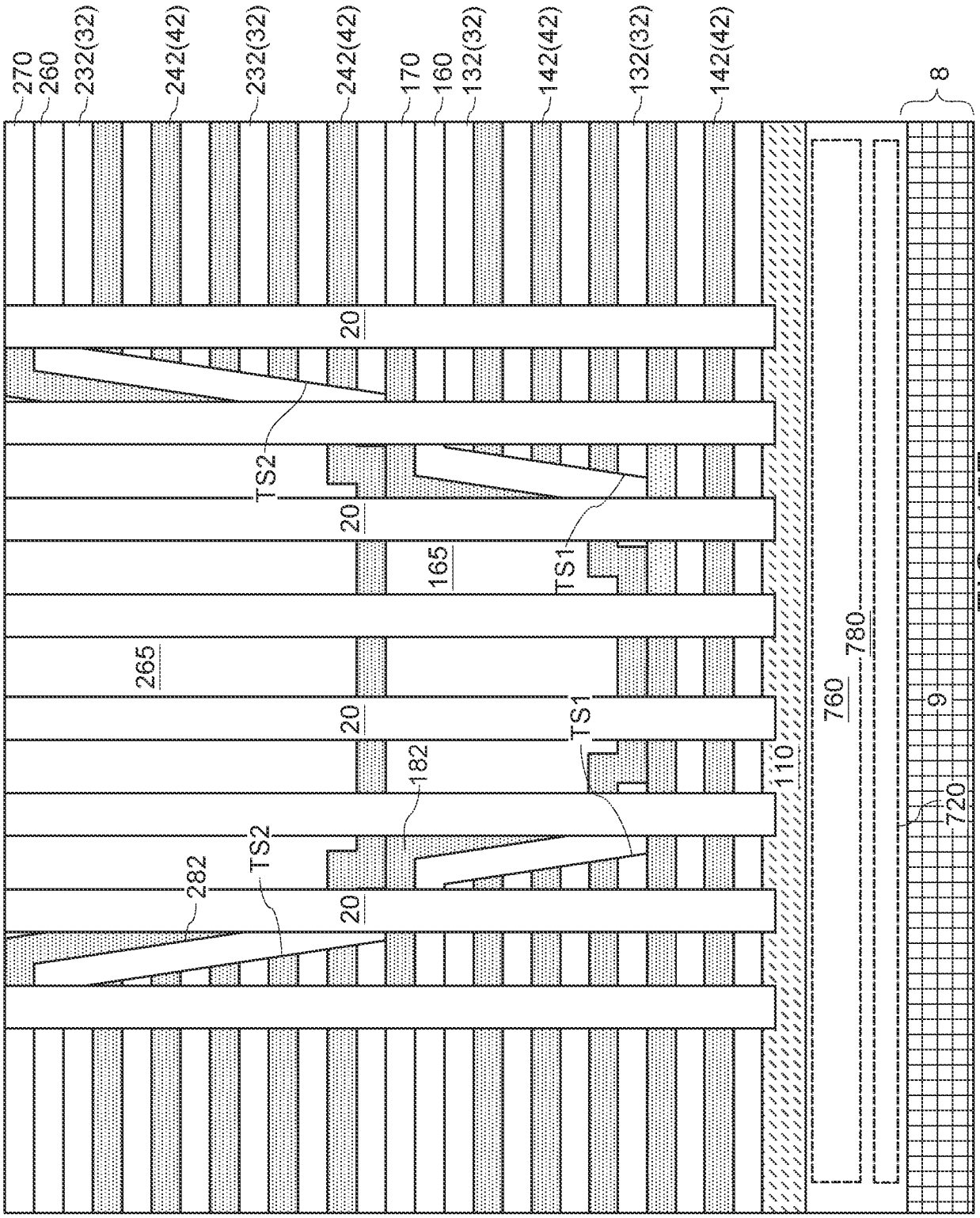
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
58
142(42)
132(32)
142(42)
8
100B(100)
200
100A(100)
EW2
260
EW1
160
265
165
182
282
110
20
58
760
780
9
720
HP1
HP2

FIG. 17E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260
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
8
20
TS2
20
165
TS1
265
780
760
20
TS1
9
182
110
720
282
TS2
20

FIG. 17F

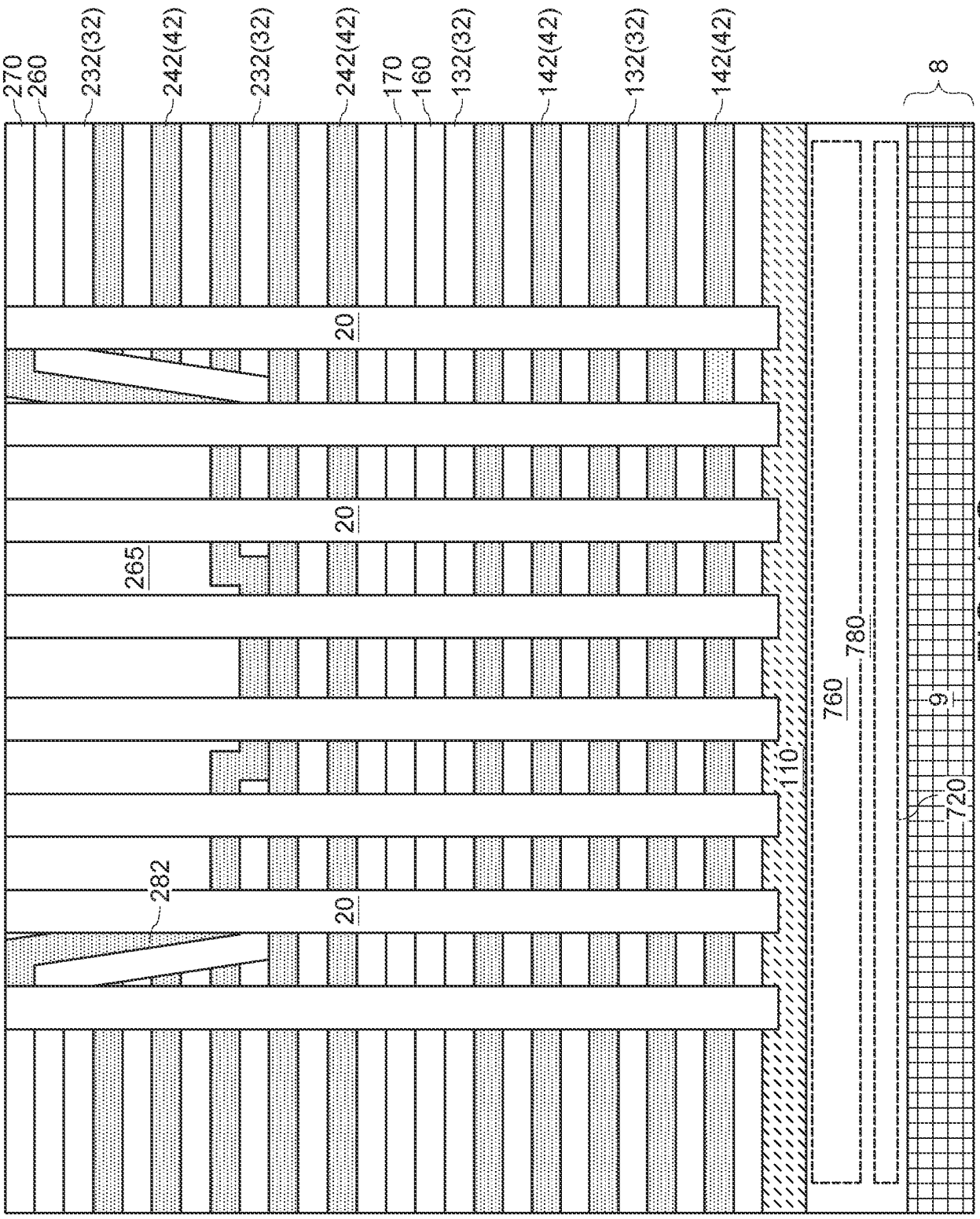
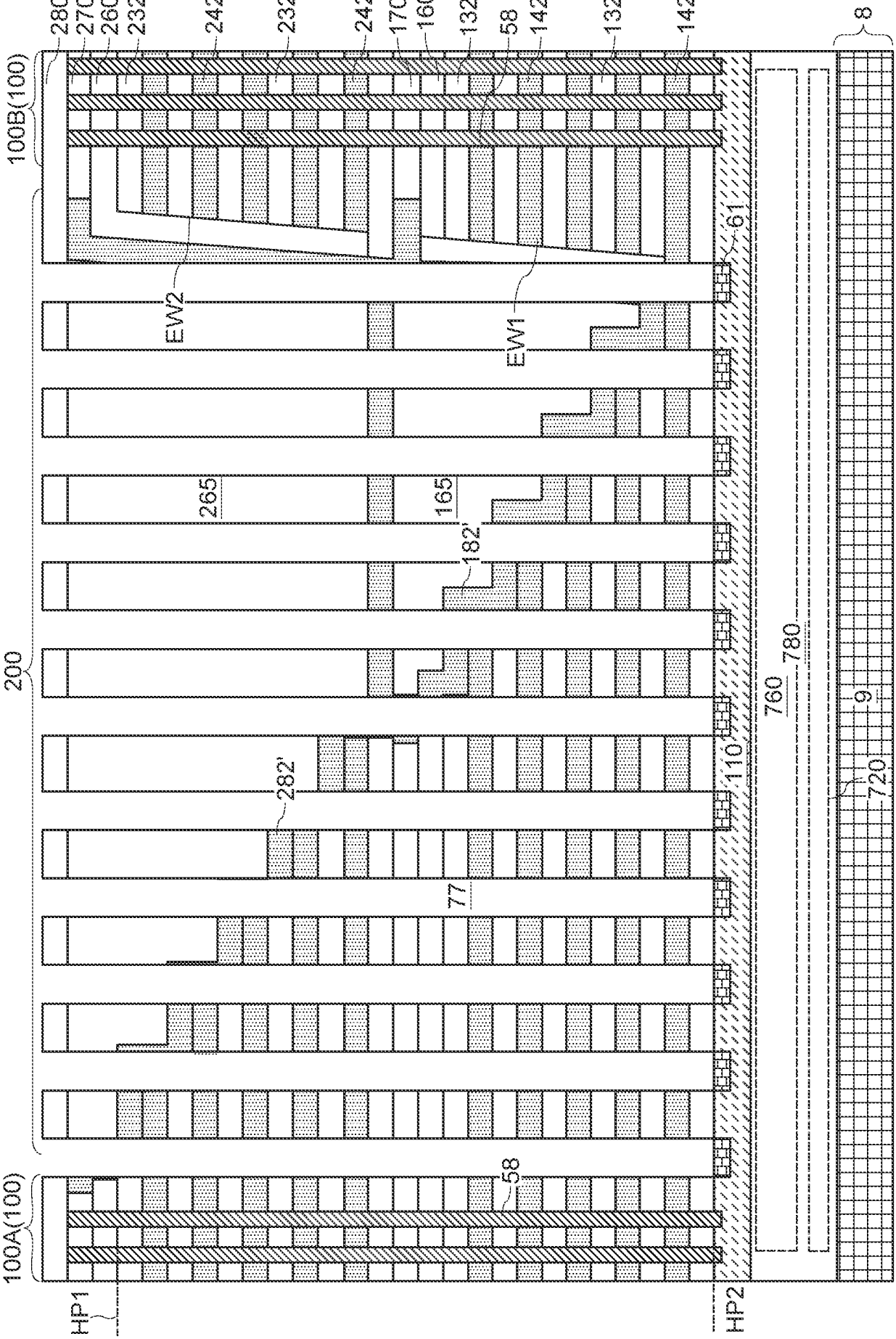

270
260
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
8
20
20
265
20
282
760
780
9
110
720

FIG. 17G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260
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
58
142(42)
132(32)
142(42)
8
100B(100)
61
EW2
EW1
265
165
182'
200
760
780
9
110
720
282'
77
58
100A(100)
HP1
HP2

FIG. 18A

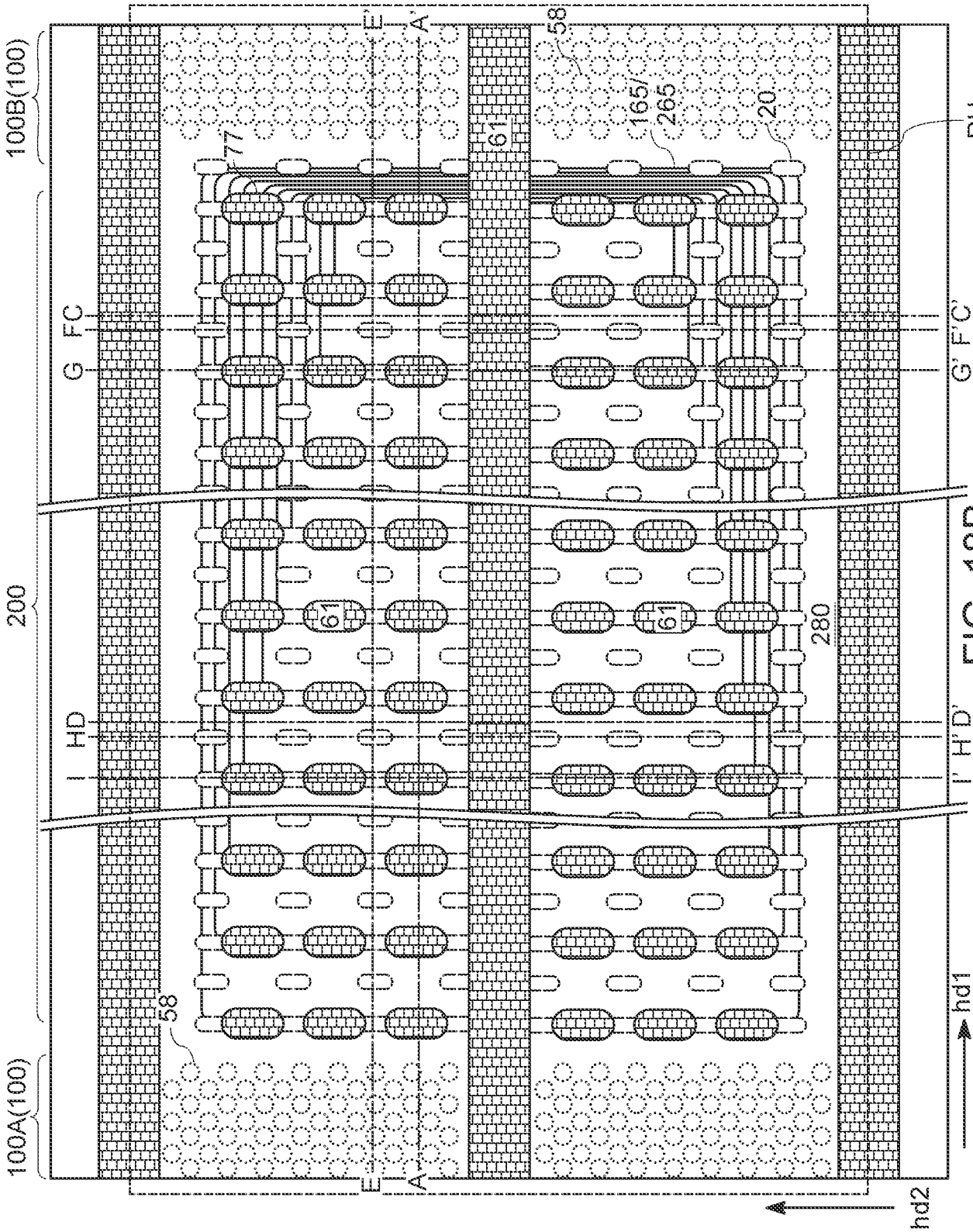
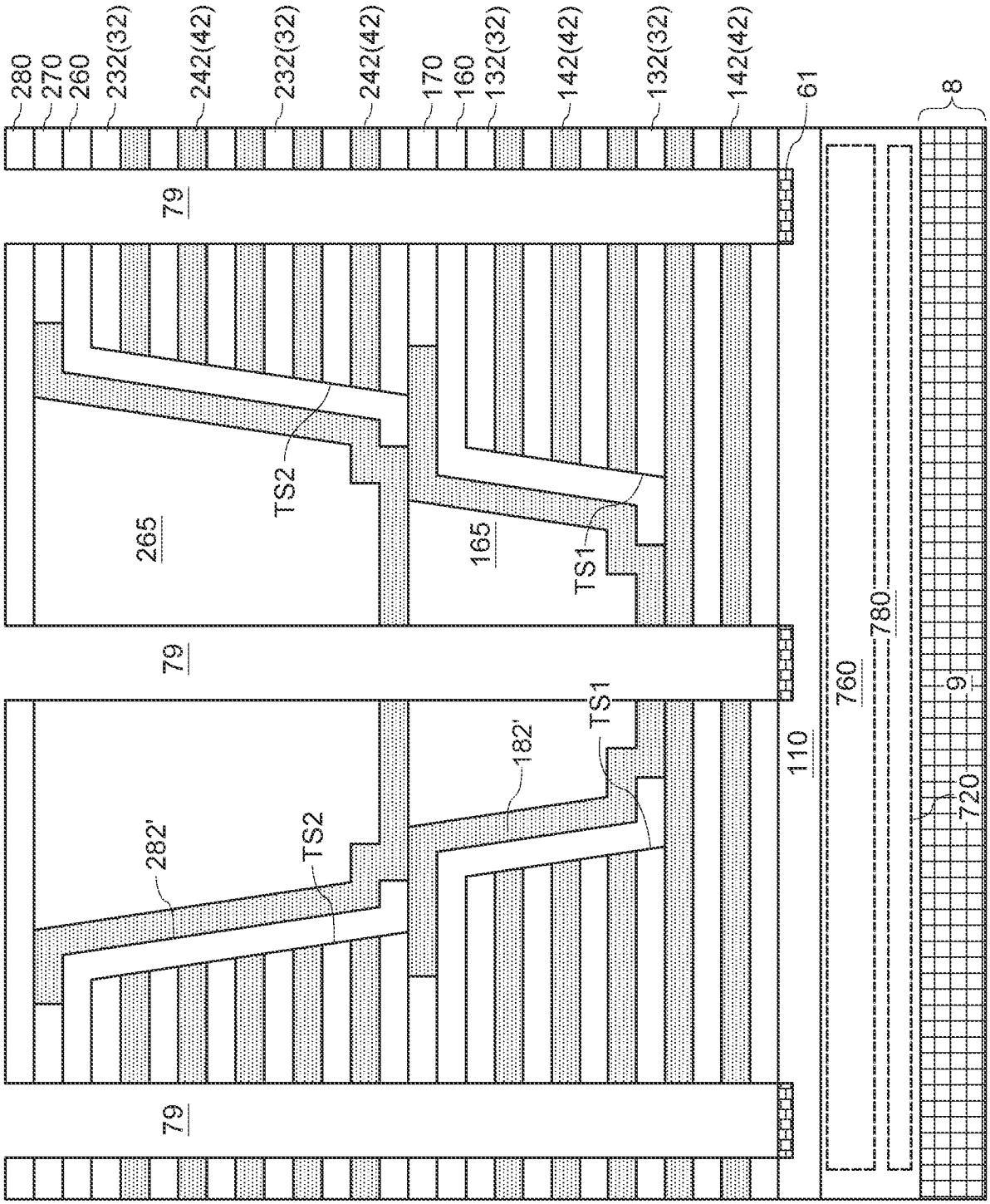

100B(100)
200
100A(100)
E
E'
A
A'
58
61
77
165/265
20
RU
G
FC
G' F'C'
I
HD
I' H'D'
280
hd1
hd2

FIG. 18B


280
270
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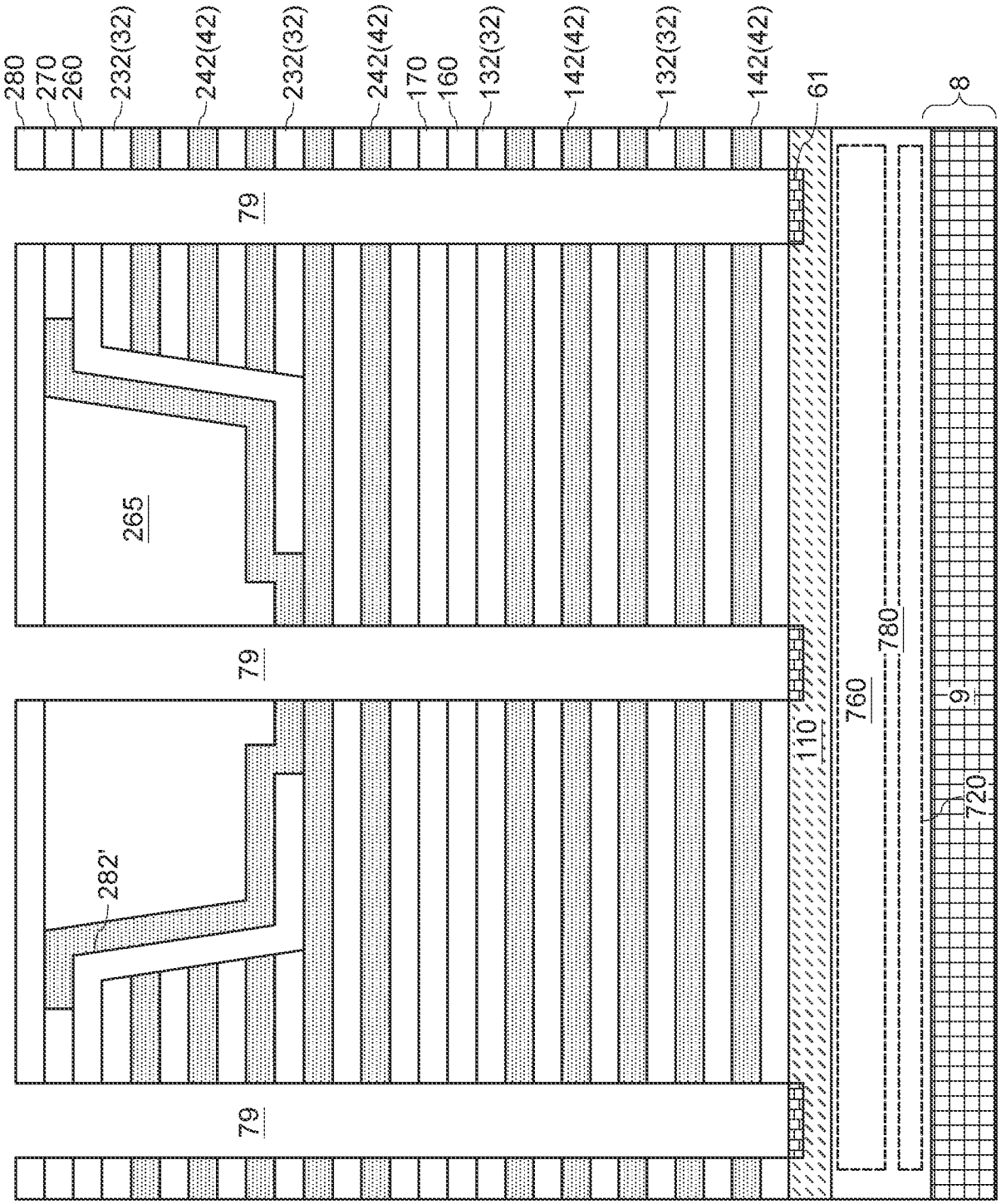
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
61
8
79
265
TS2
165
TS1
79
780
760
9
110
182'
TS1
282'
TS2
720
79

FIG. 18C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270
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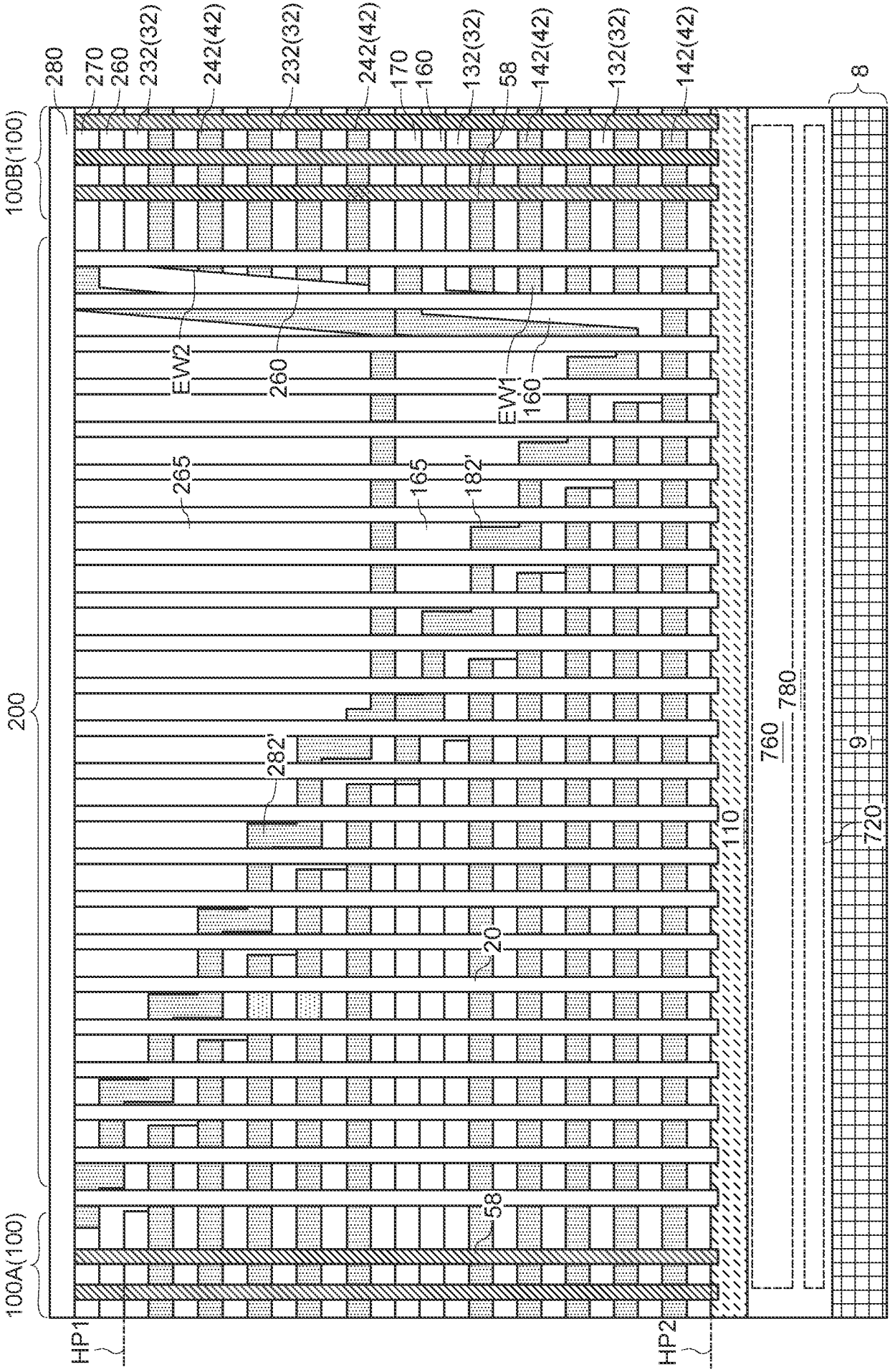
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
61
8
79
265
79
282'
79
110
760
780
9
720

FIG. 18D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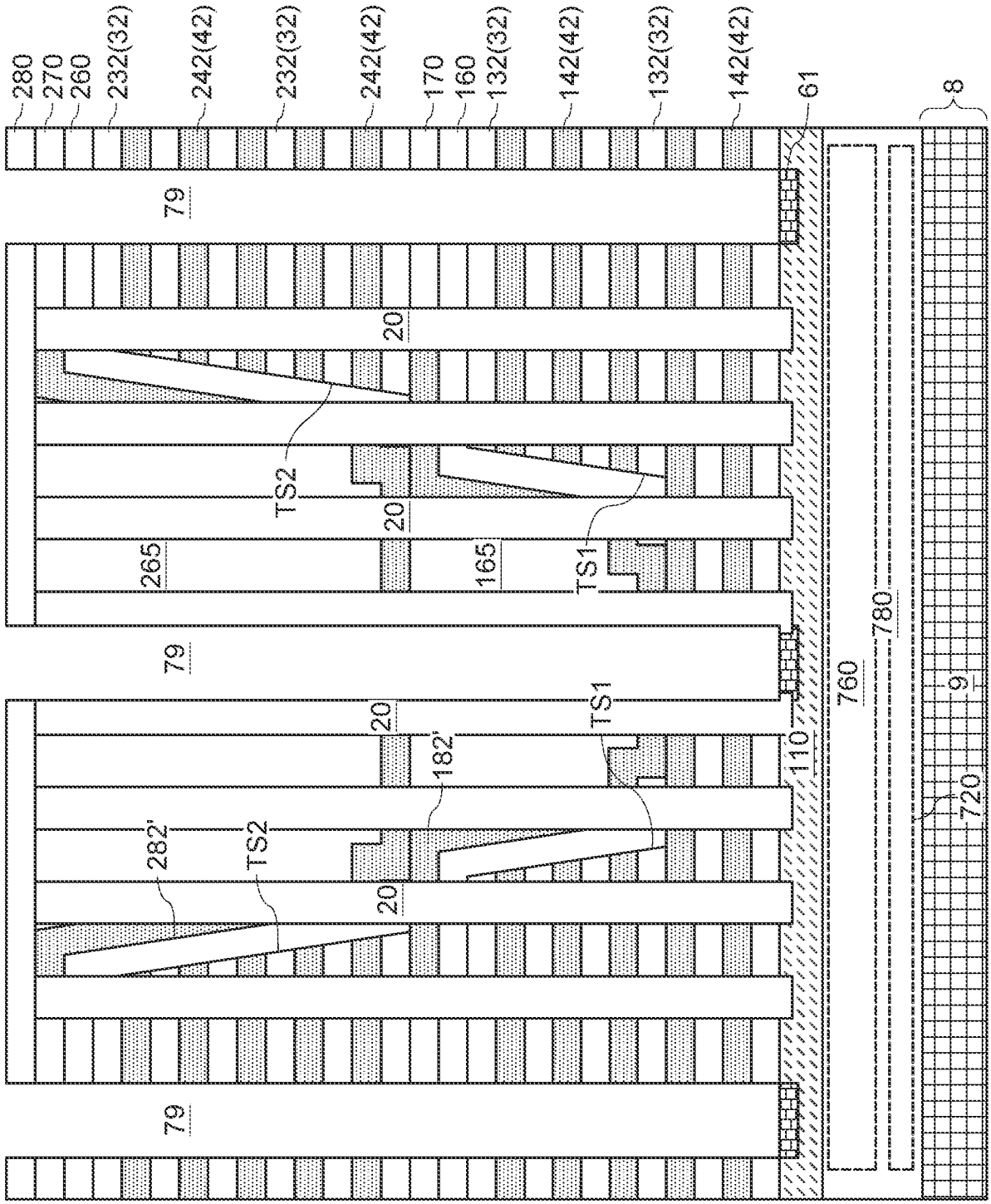
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
58
142(42)
132(32)
142(42)
8
100B(100)
200
100A(100)
EW2
260
EW1
160
265
165
182'
282'
110
20
58
760
780
9
720
HP1
HP2

FIG. 18E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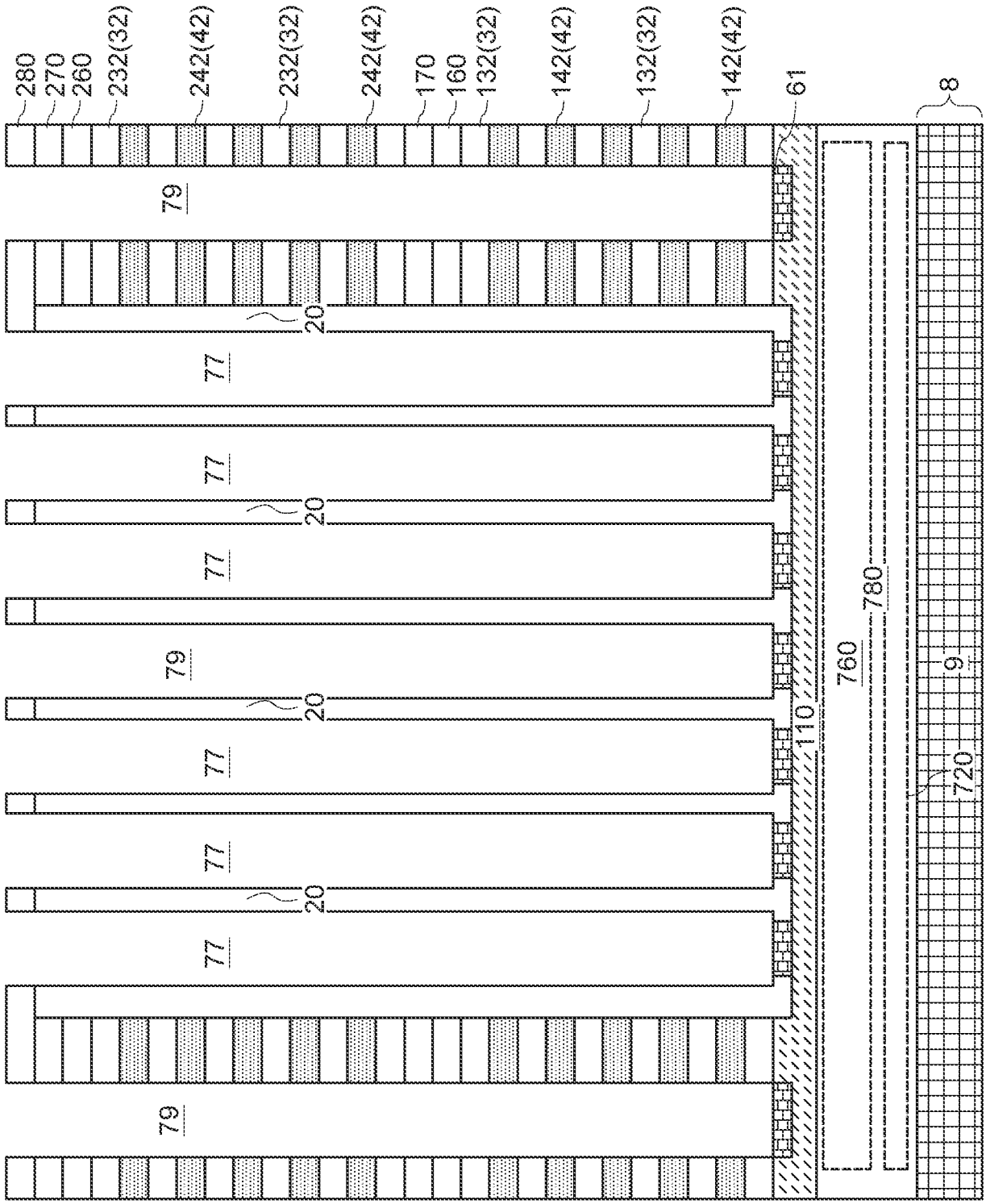
270
260
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
61
8
79
20
TS2
20
265
165
TS1
79
760
780
9
20
TS1
182'
110
720
282'
TS2
20
79

FIG. 18F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270
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232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
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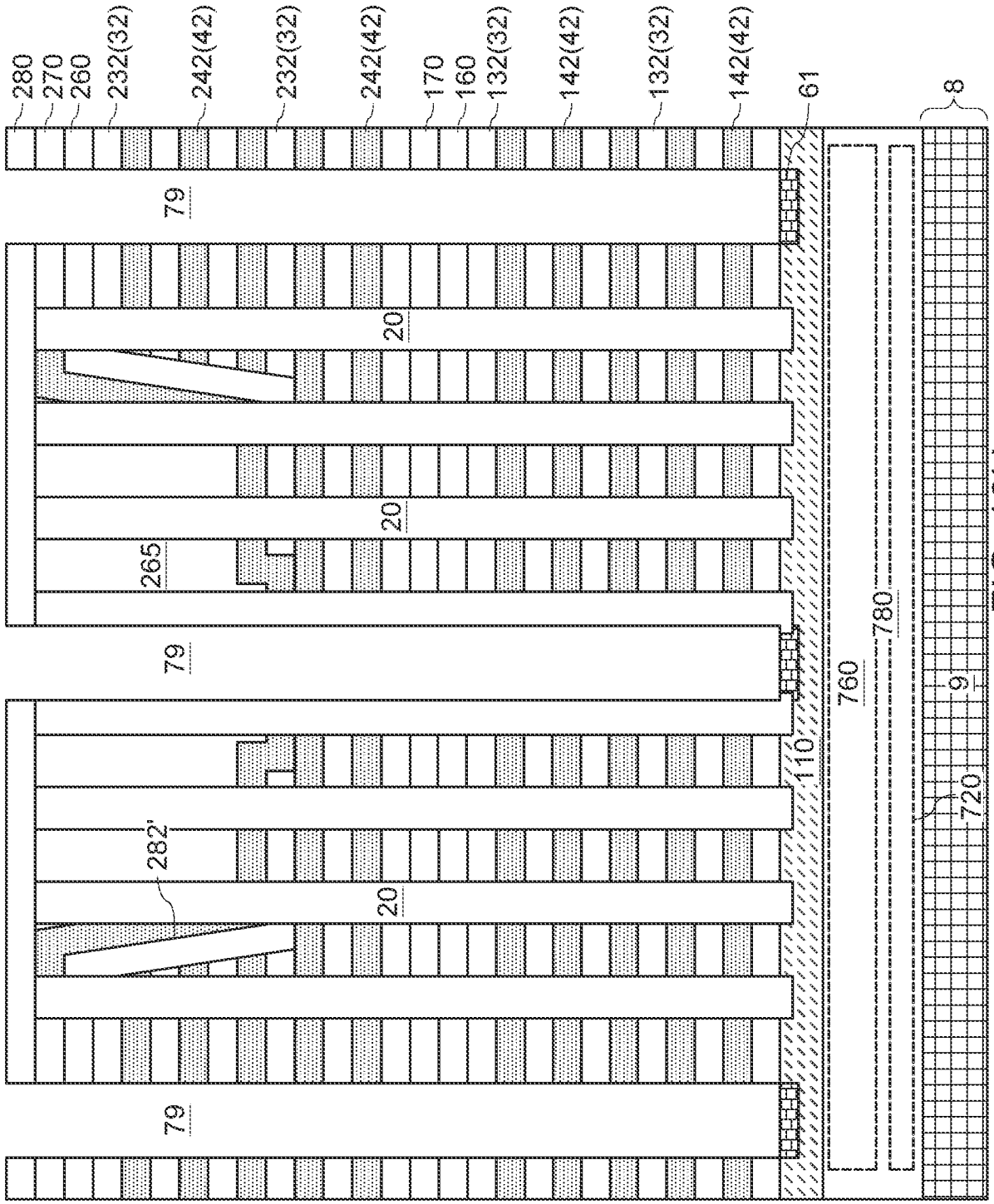
61
8
79
20
77
77
20
77
79
20
77
77
20
77
79
760
780
9
110
720

FIG. 18G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270
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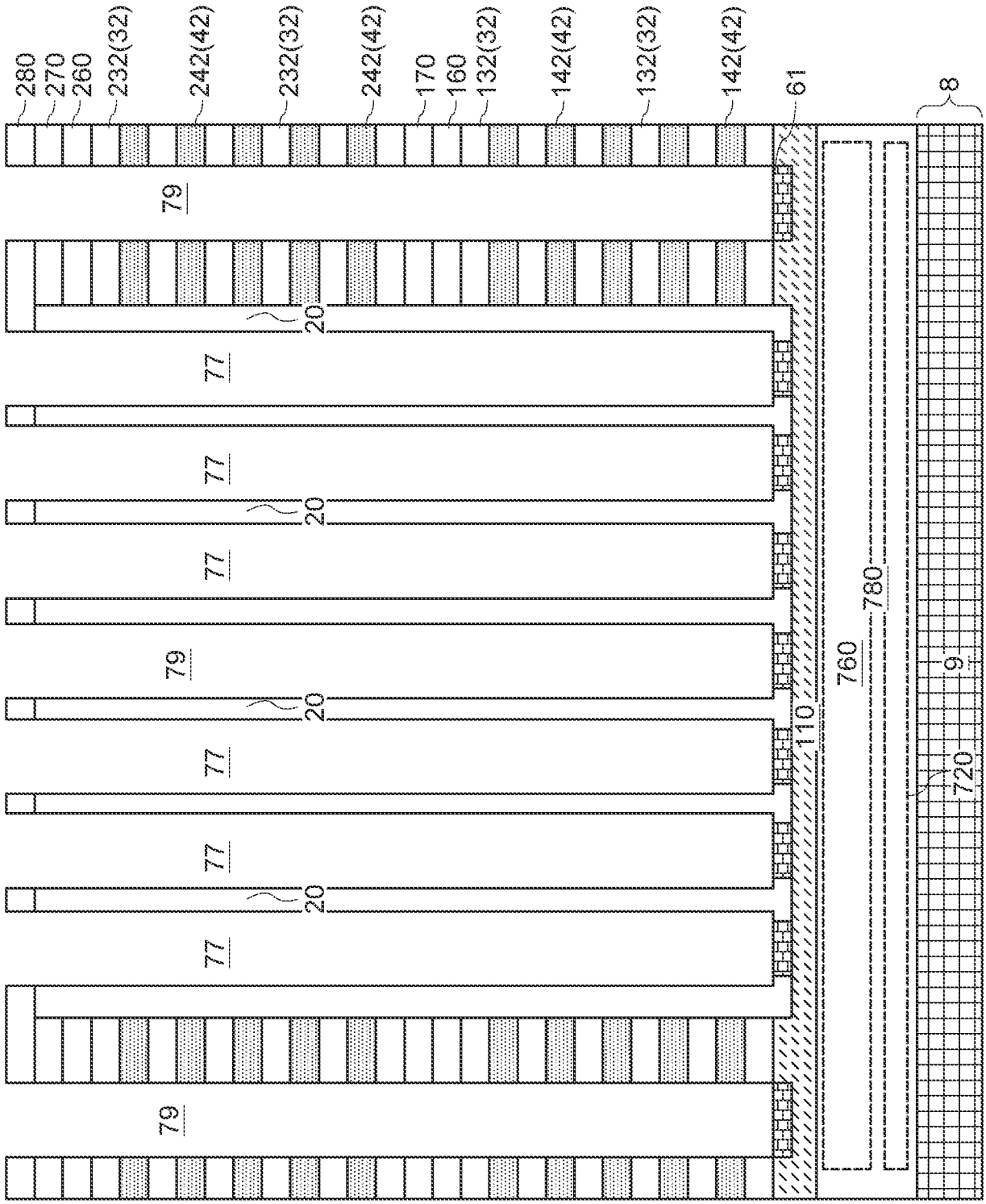
232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
132(32)
142(42)
61
8
79
20
20
265
79
760
780
9
110
720
282'
20
79

FIG. 18H


280
270
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232(32)
242(42)
232(32)
242(42)
170
160
132(32)
142(42)
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142(42)
61
8
79
20
77
77
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77
79
20
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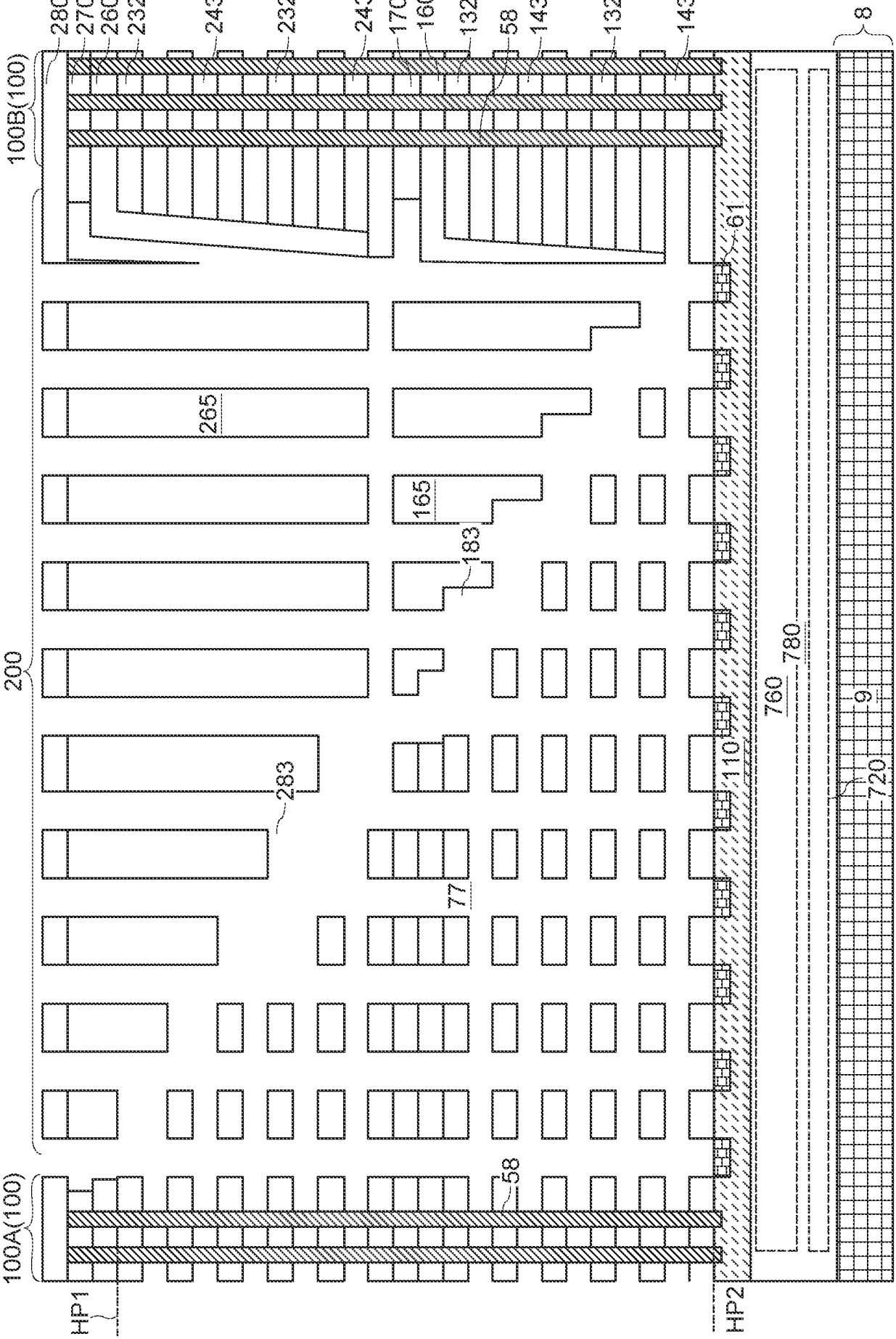
77
20
77
79
760
780
9
110
720

FIG. 18I


280
270
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232(32)
243(43)
232(32)
243(43)
170
160
132(32)
58
143(43)
132(32)
143(43)
8
100B(100)
61
265
165
183
200
760
780
9
110
720
283
77
58
100A(100)
HP1
HP2

FIG. 19A

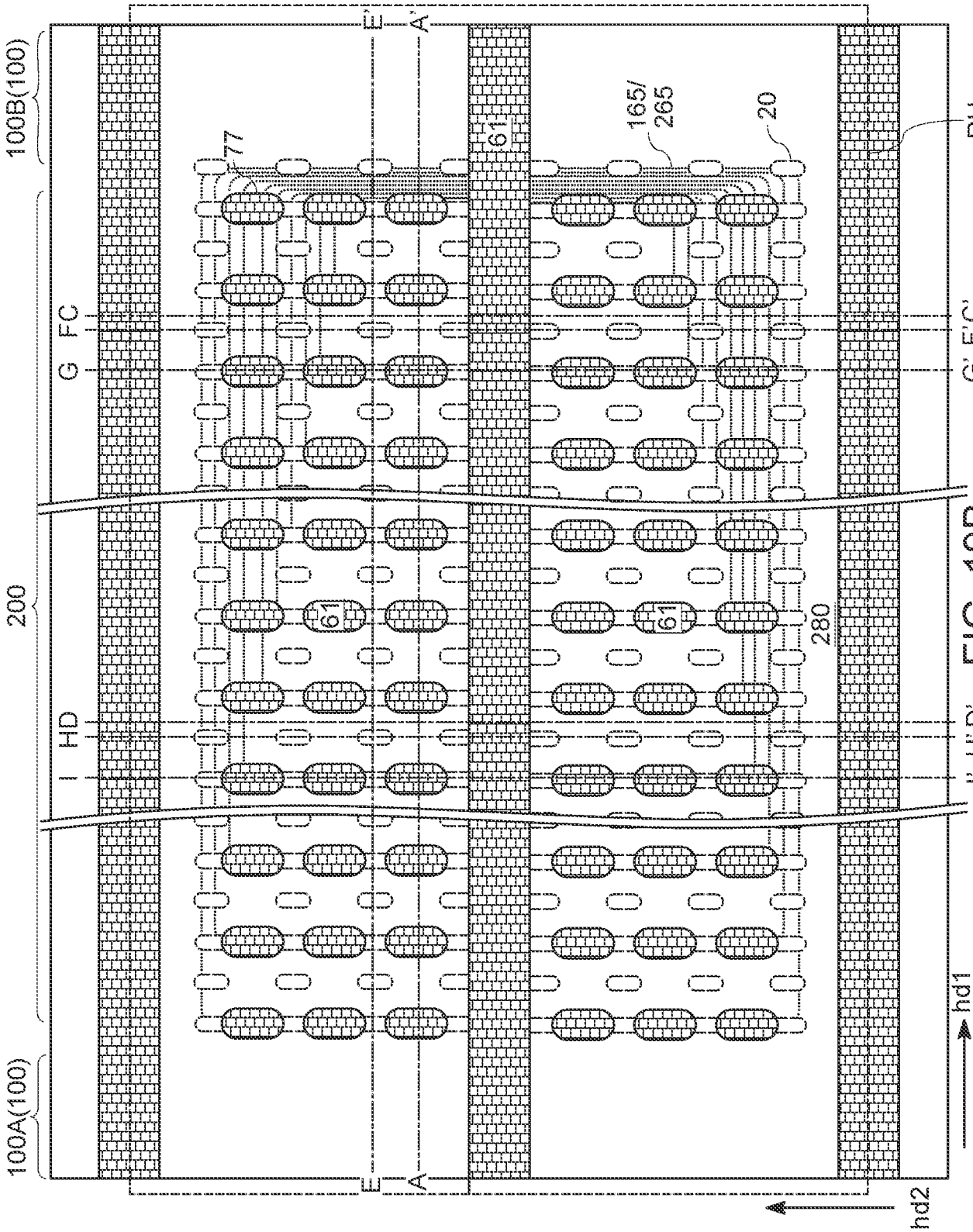
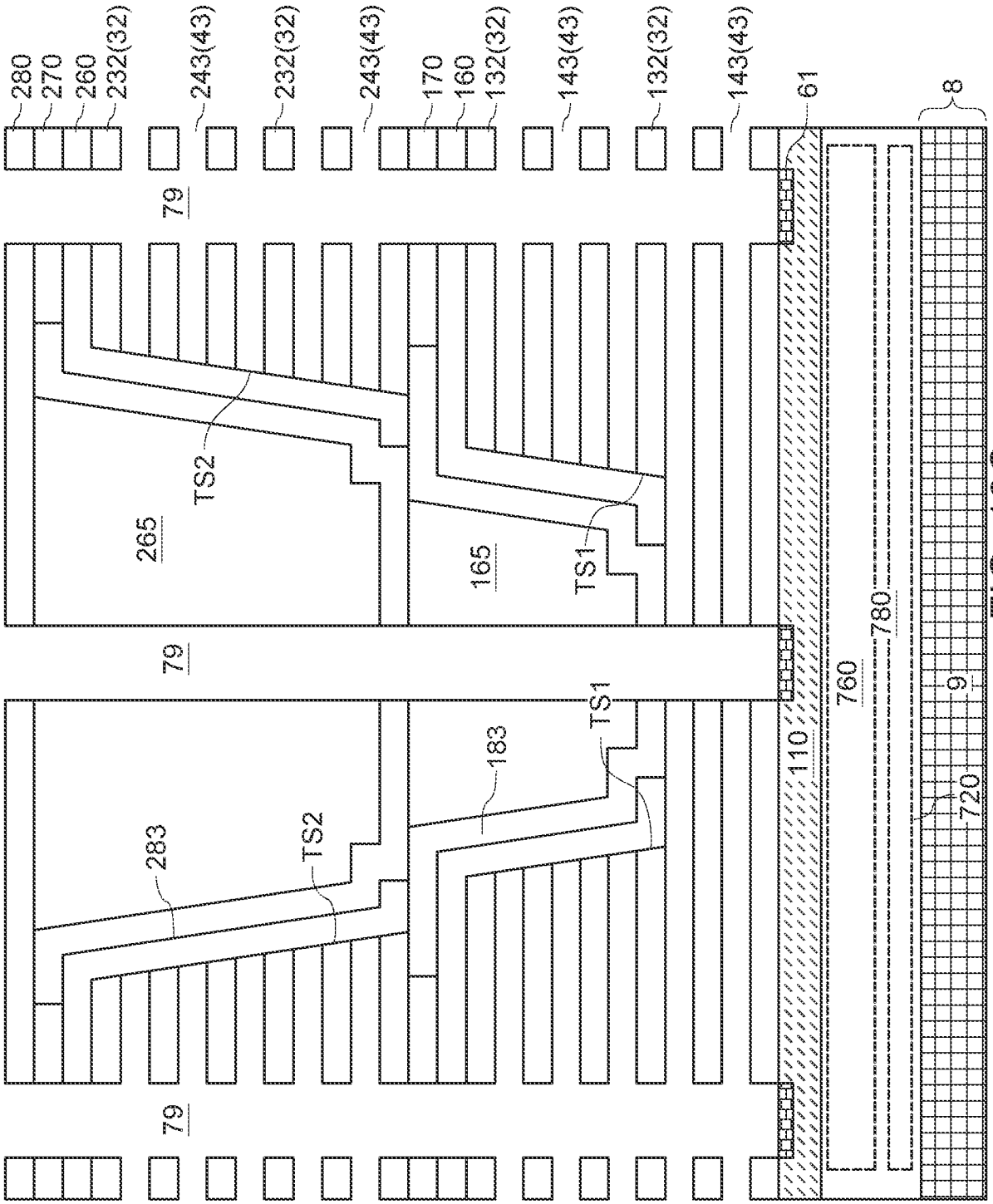

100B(100)
200
100A(100)
E
E'
A
A'
G
FC
G'
F'C'
I
HD
I'
H'D'
77
61
FT
165/
265
20
RU
61
61
280
hd1
hd2

FIG. 19B


280
270
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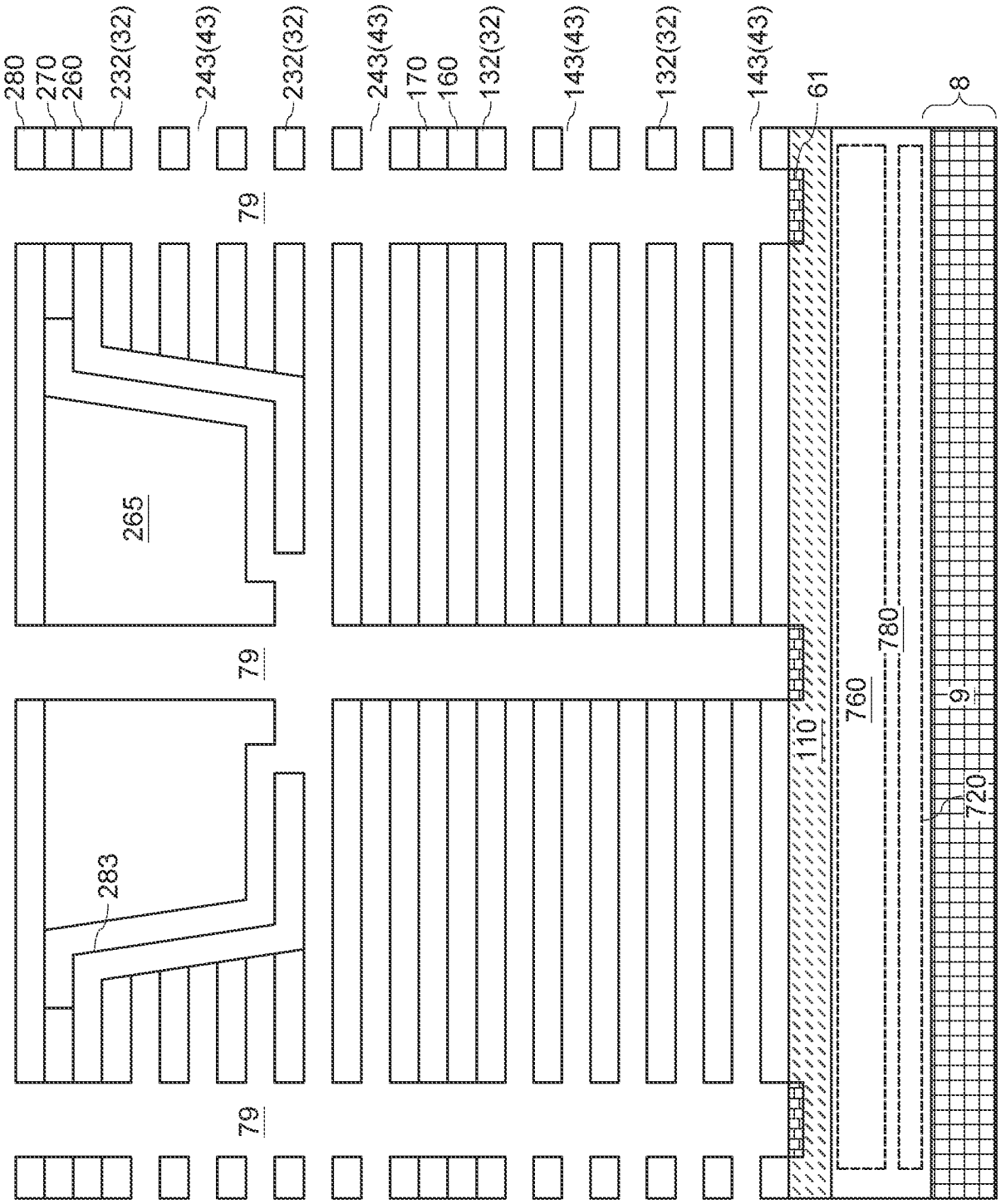
232(32)
243(43)
232(32)
243(43)
170
160
132(32)
143(43)
132(32)
143(43)
61
8
79
TS2
265
165
TS1
780
760
9
110
183
TS1
283
TS2
720
79
79

FIG. 19C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270
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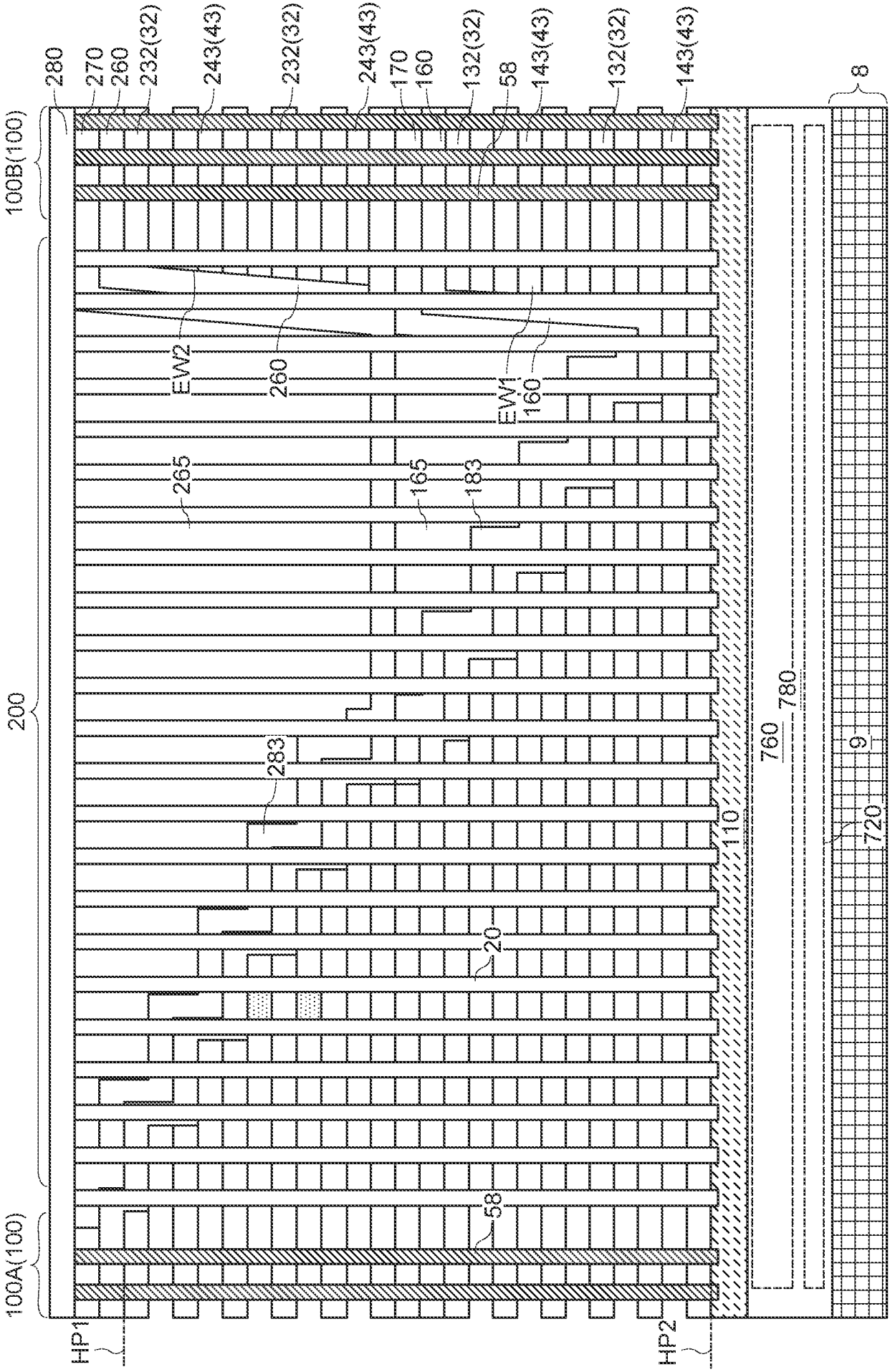
232(32)
243(43)
232(32)
243(43)
170
160
132(32)
143(43)
132(32)
143(43)
61
8
79
265
79
283
79
110
760
780
9
720

FIG. 19D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270
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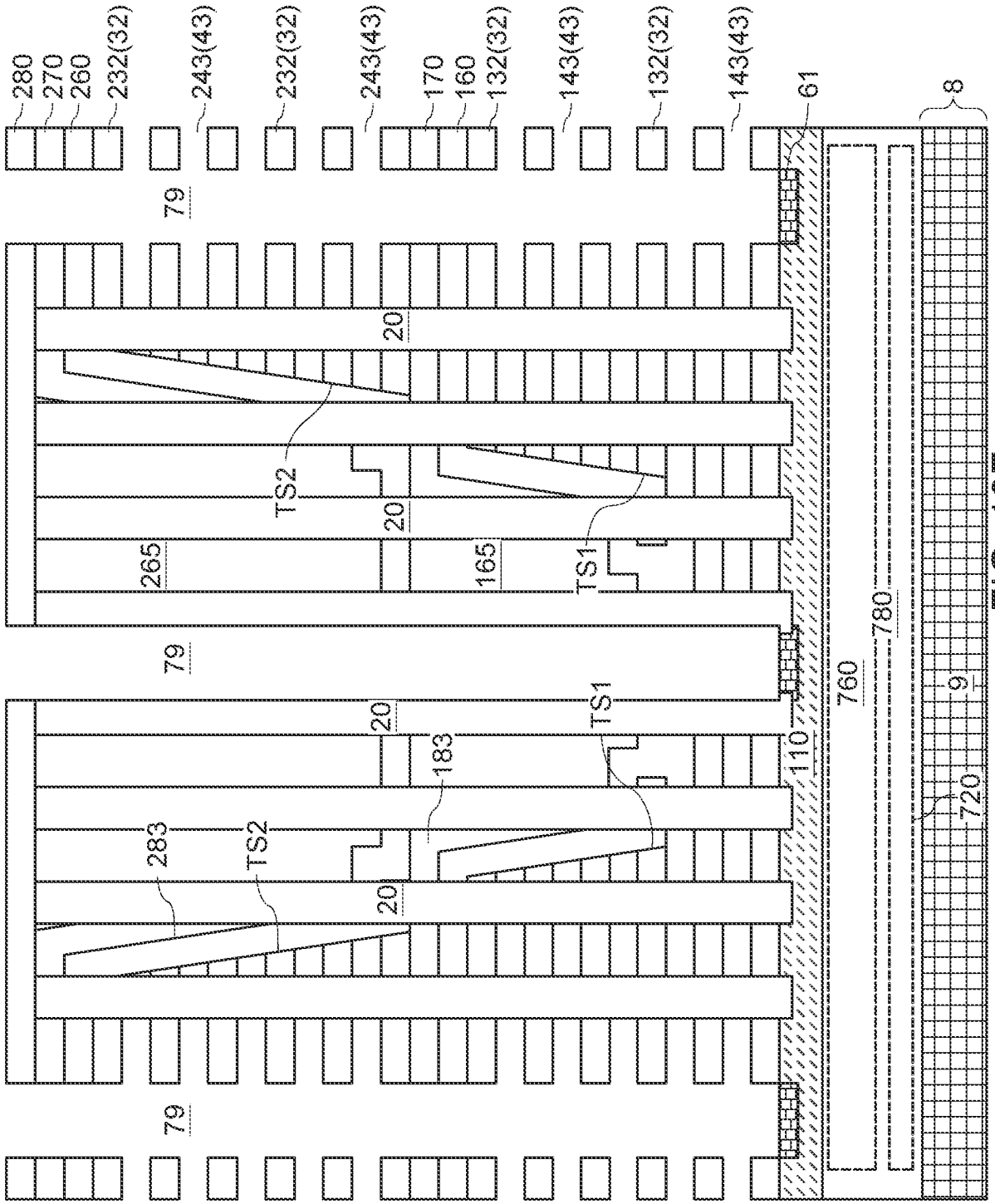
232(32)
243(43)
232(32)
243(43)
170
160
132(32)
58
143(43)
132(32)
143(43)
8
100B(100)
EW2
260
EW1
160
265
165
183
200
283
760
780
9
720
110
20
58
100A(100)
HP1
HP2

FIG. 19E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232(32)
243(43)
232(32)
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170
160
132(32)
143(43)
132(32)
143(43)
61
8
79
20
TS2
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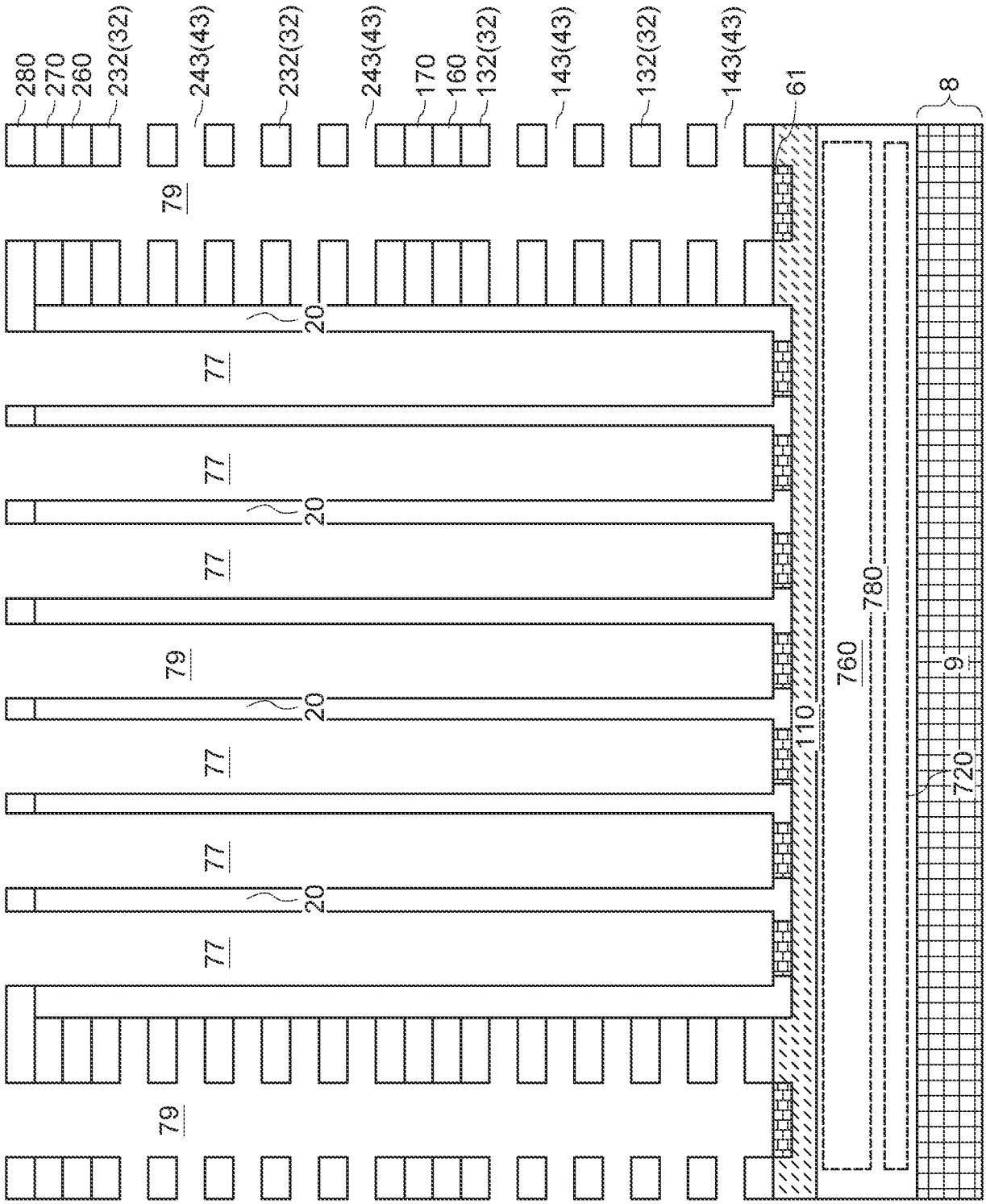
265
165
TS1
79
760
780
9
20
TS1
183
110
720
283
TS2
20
79

FIG. 19F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270
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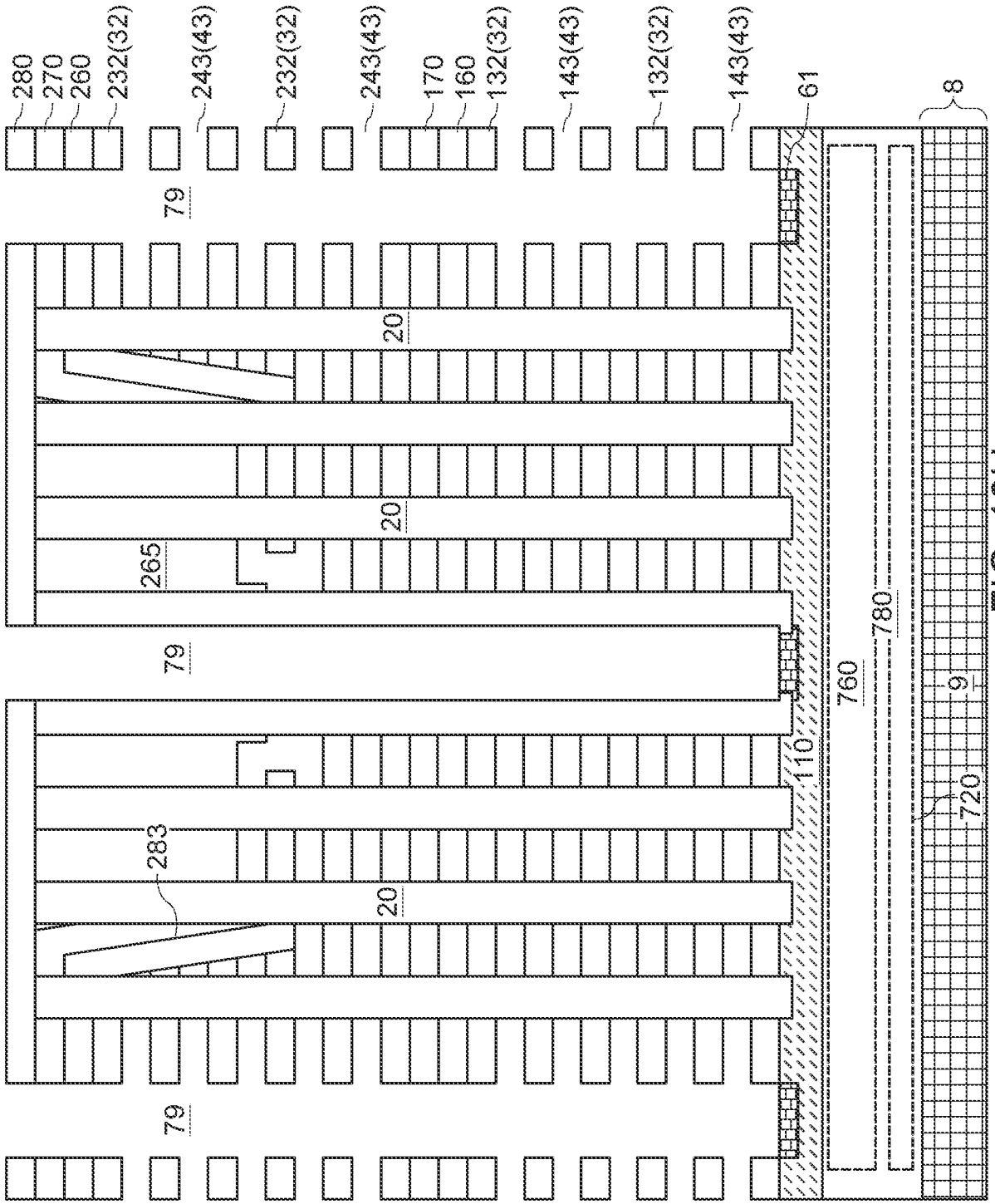
232(32)
243(43)
232(32)
243(43)
170
160
132(32)
143(43)
132(32)
143(43)
61
8
79
20
77
780
760
9
110
720

FIG. 19G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270
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232(32)
243(43)
232(32)
243(43)
170
160
132(32)
143(43)
132(32)
143(43)
61
8
79
20
20
265
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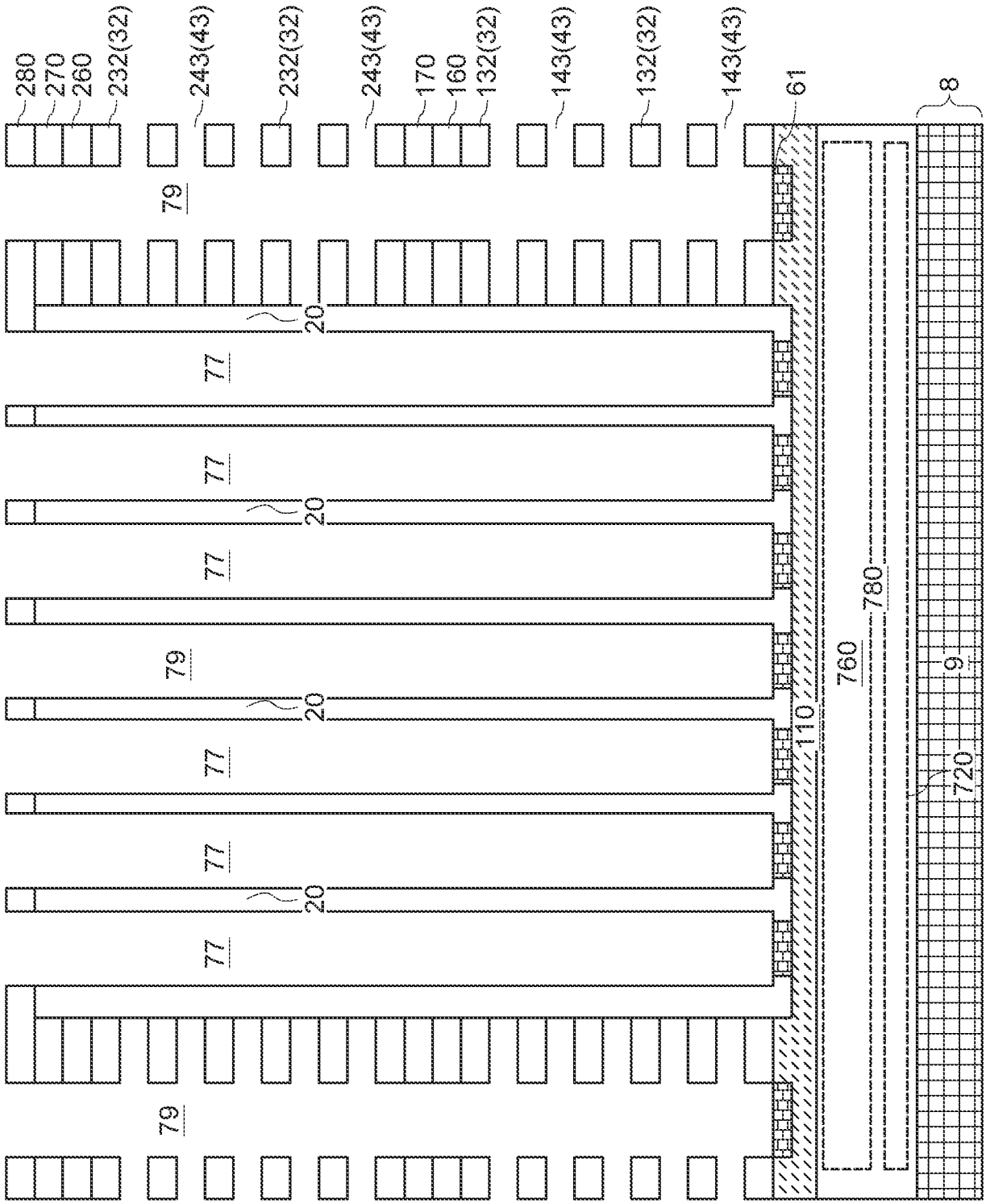
760
780
9
110
720
283
20
79

FIG. 19H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270
260
232(32)
243(43)
232(32)
243(43)
170
160
132(32)
143(43)
132(32)
143(43)
61
8
79
20
77
780
760
9
110
720

FIG. 19I

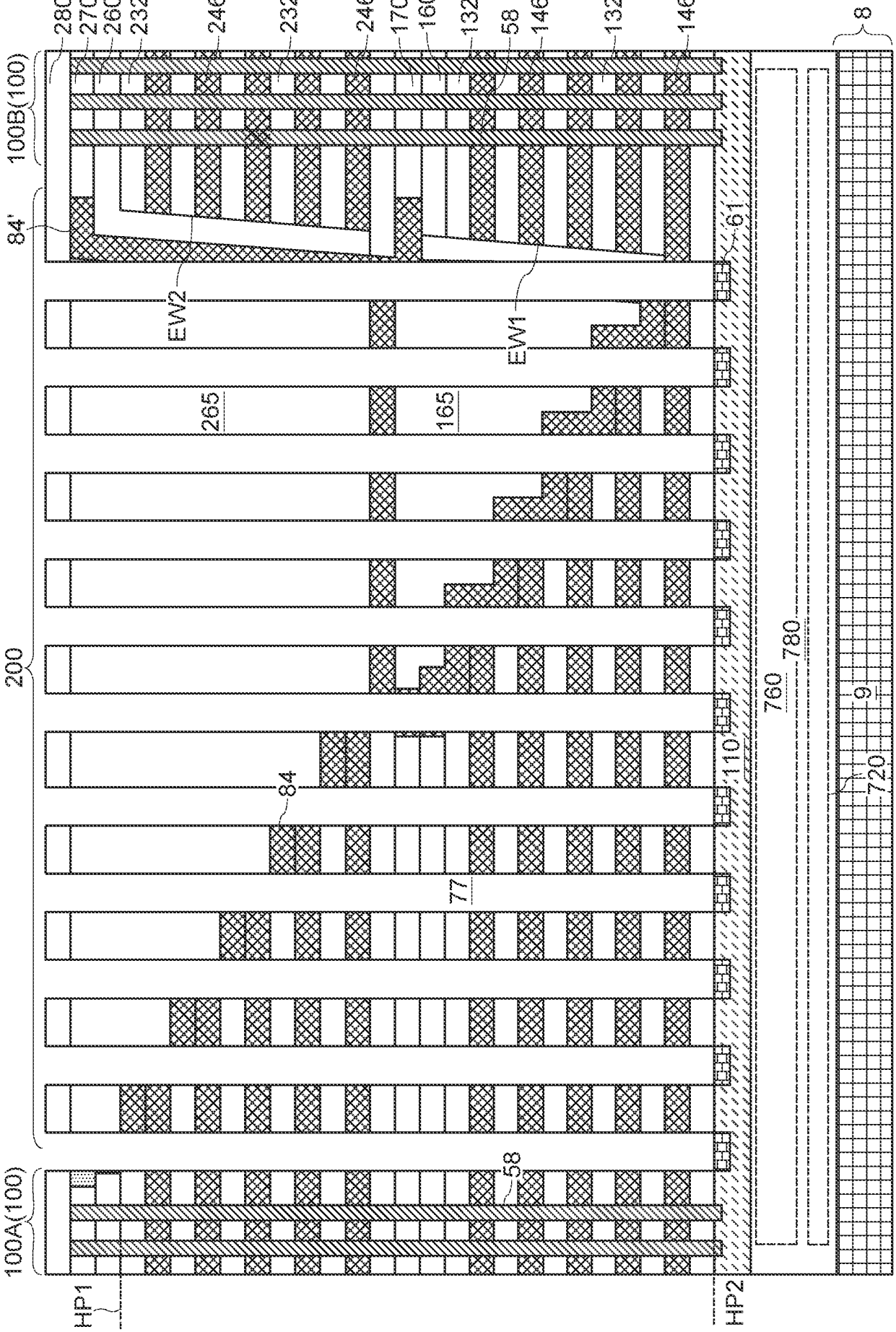

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
58
146(46)
132(32)
146(46)
8
100B(100)
84'
61
EW2
EW1
265
165
200
760
780
9
110
720
84
77
58
100A(100)
HP1
HP2

FIG. 20A

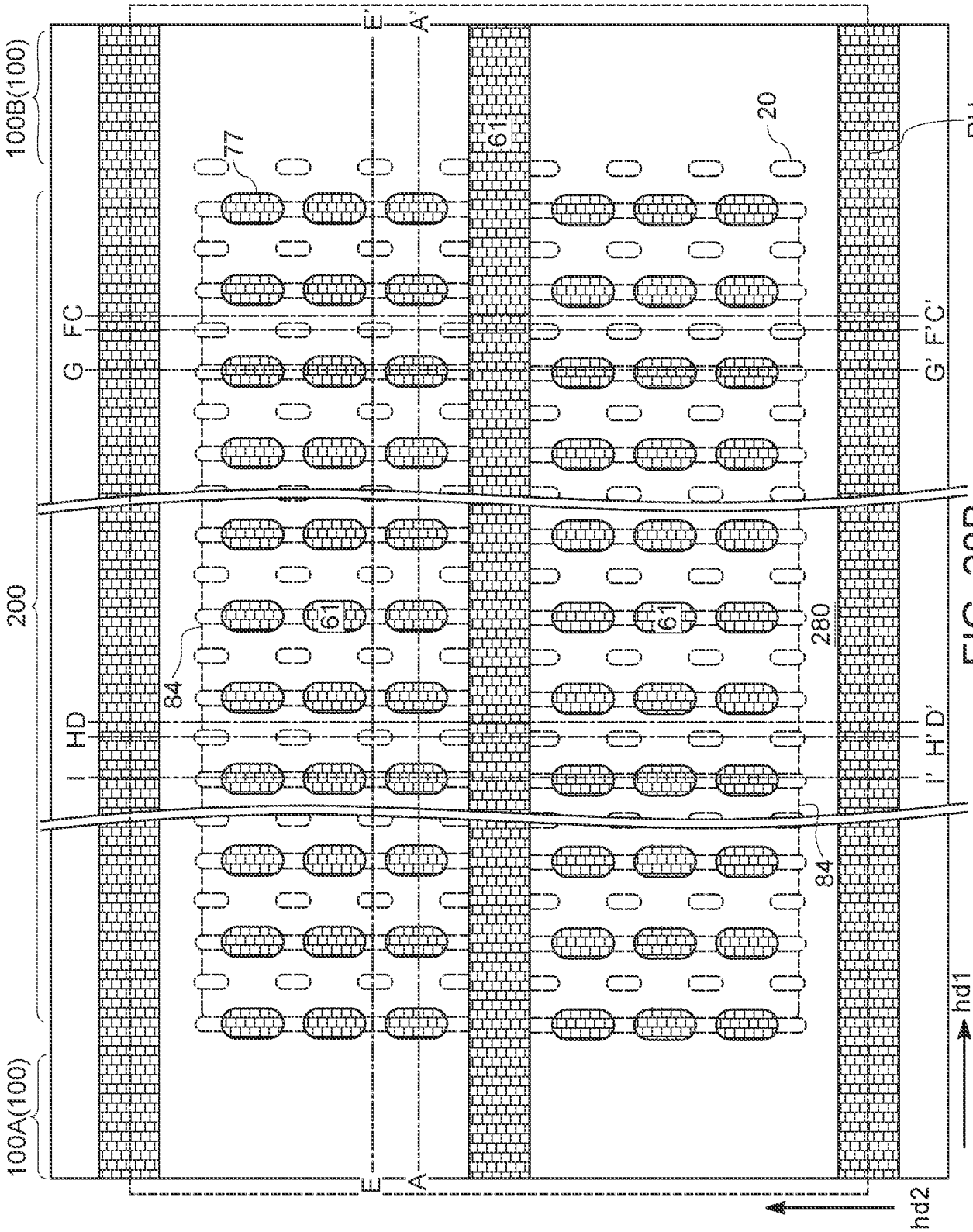

100B(100)
200
100A(100)
E
E'
A
A'
77
61
61
61
20
RU
G
FC
G'
F'C'
I
HD
I'
H'D'
84
84
280
hd1
hd2

FIG. 20B

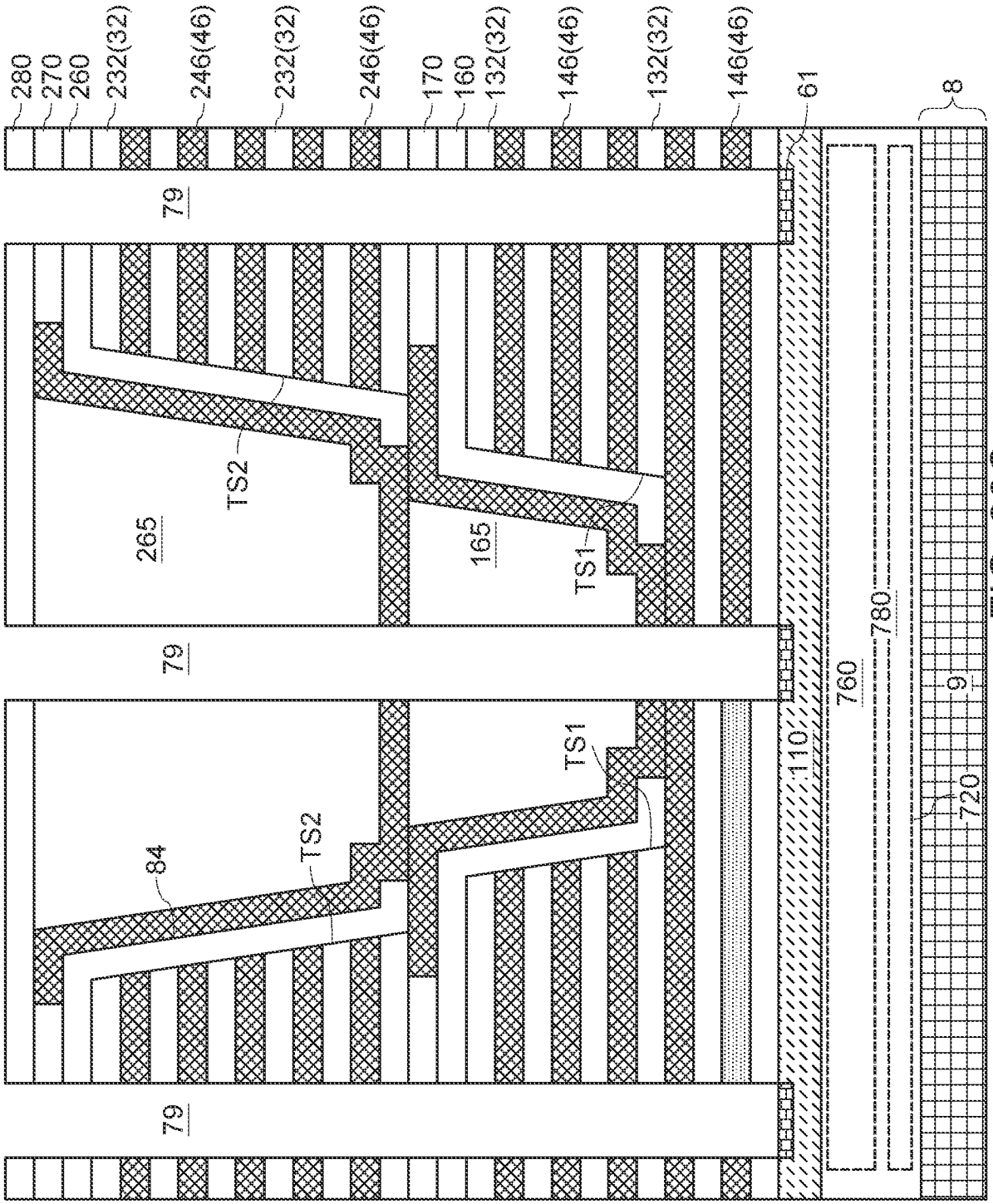
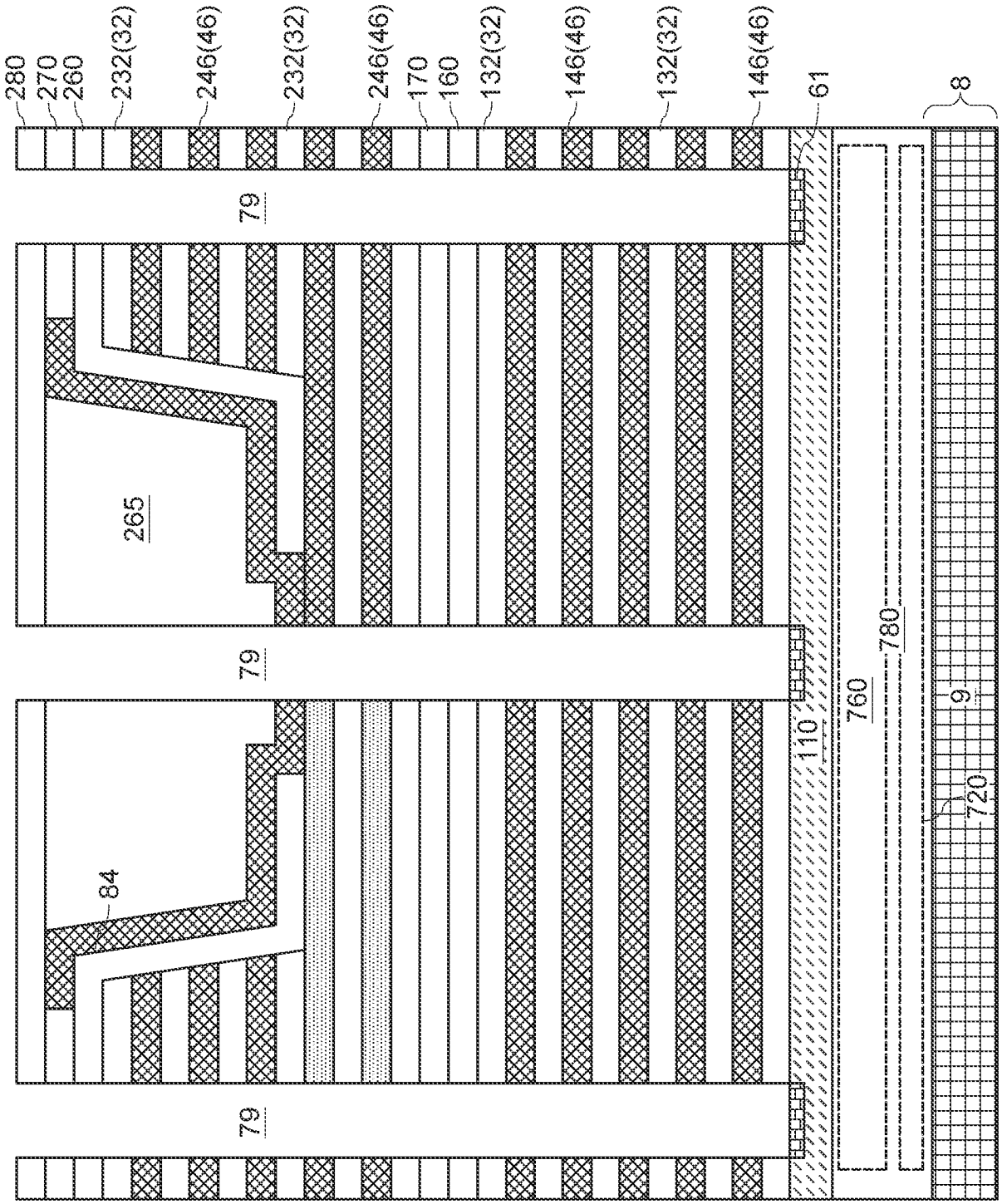

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
79
TS2
265
165
TS1
780
760
9
110
720
84
TS2
TS1
79
79

FIG. 20C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270
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232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
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146(46)
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265
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84
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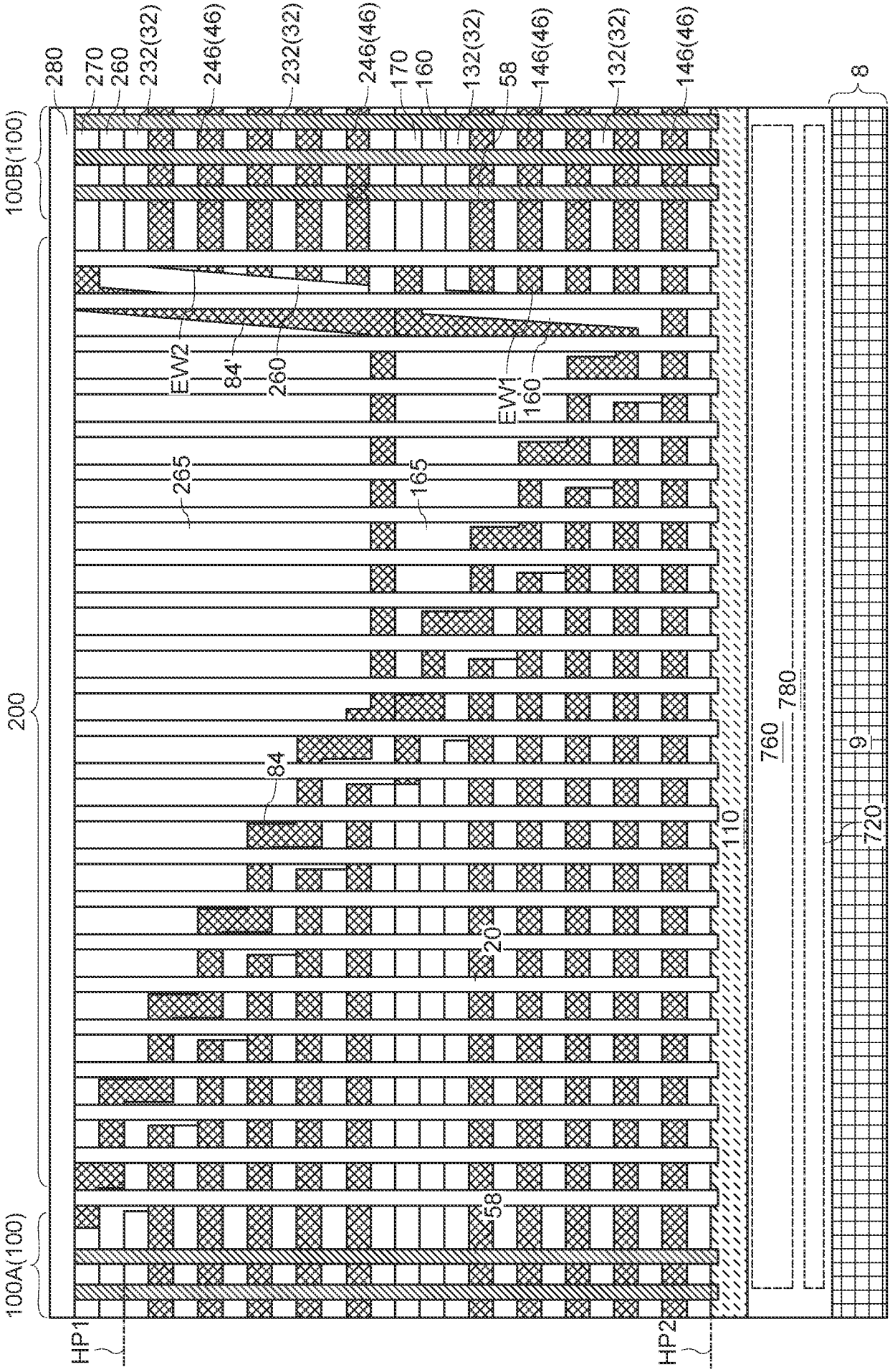
760
780
9
720

FIG. 20D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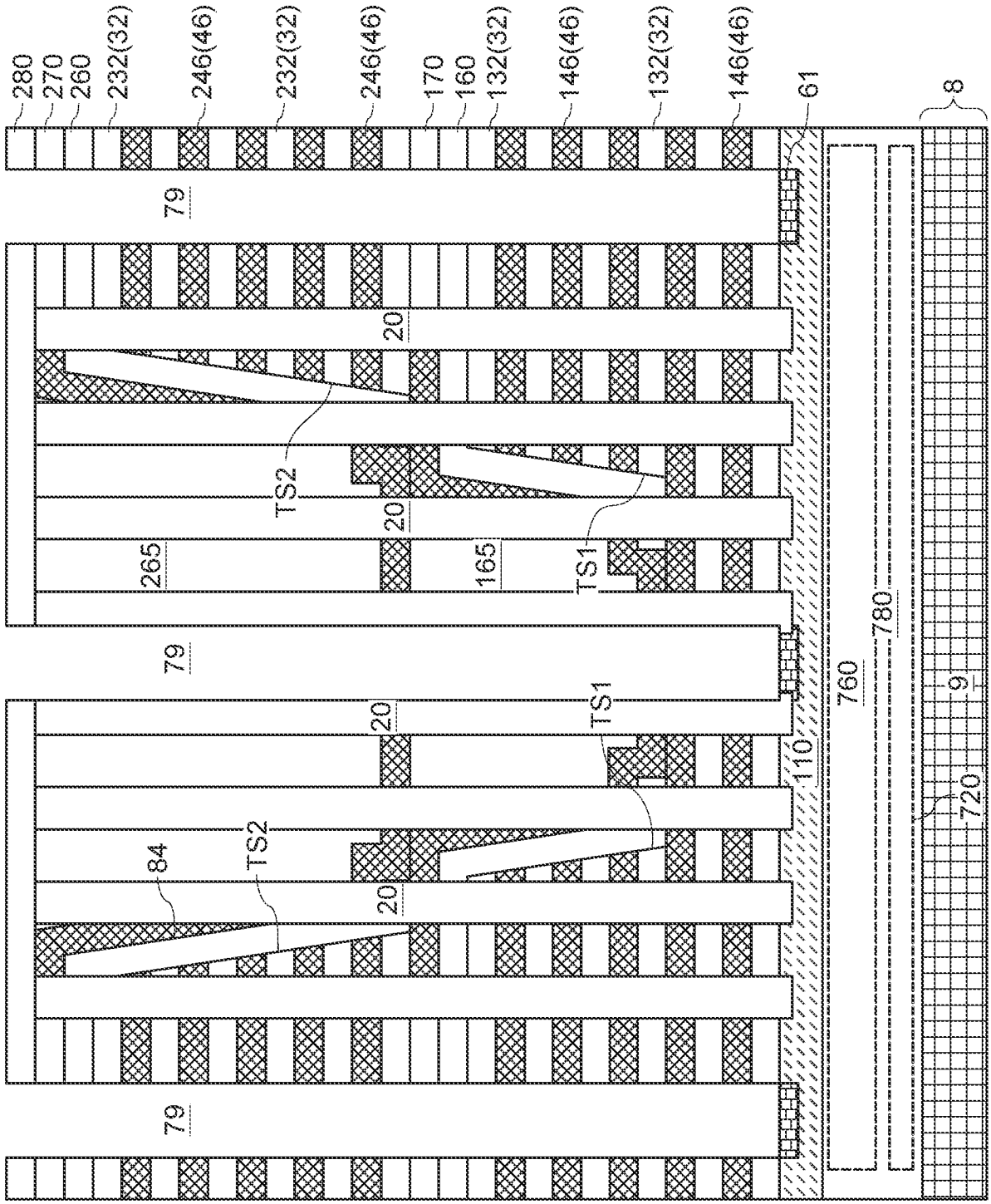
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
58
146(46)
132(32)
146(46)
8
100B(100)
EW2
84'
260
EW1
160
265
165
200
84
110
20
760
780
9
720
58
100A(100)
HP1
HP2

FIG. 20E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232(32)
246(46)
232(32)
246(46)
170
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132(32)
146(46)
132(32)
146(46)
61
8
79
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TS2
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265
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TS1
79
760
780
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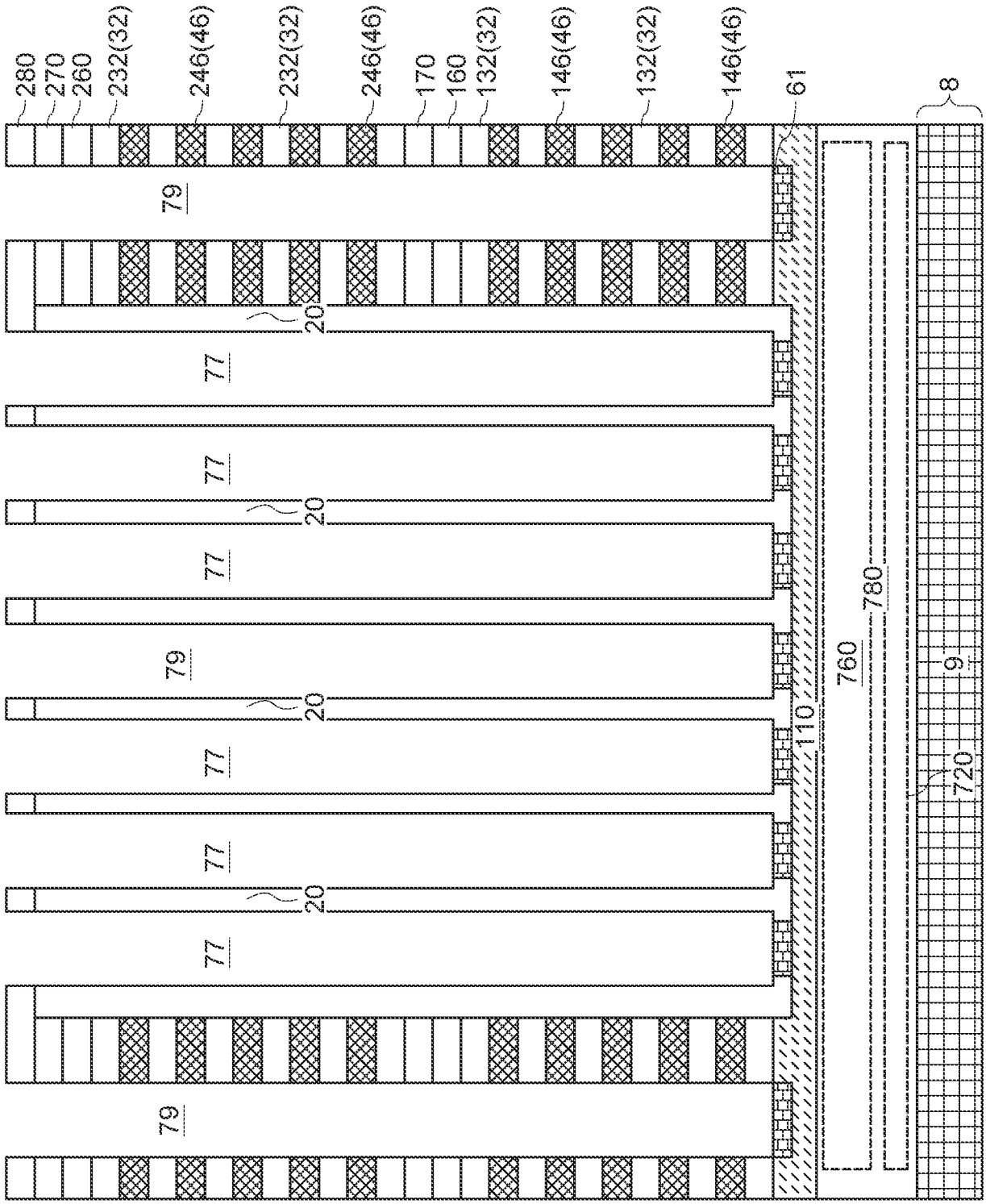
20
TS1
110
720
84
TS2
20
79

FIG. 20F


280
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232(32)
246(46)
232(32)
246(46)
170
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132(32)
146(46)
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146(46)
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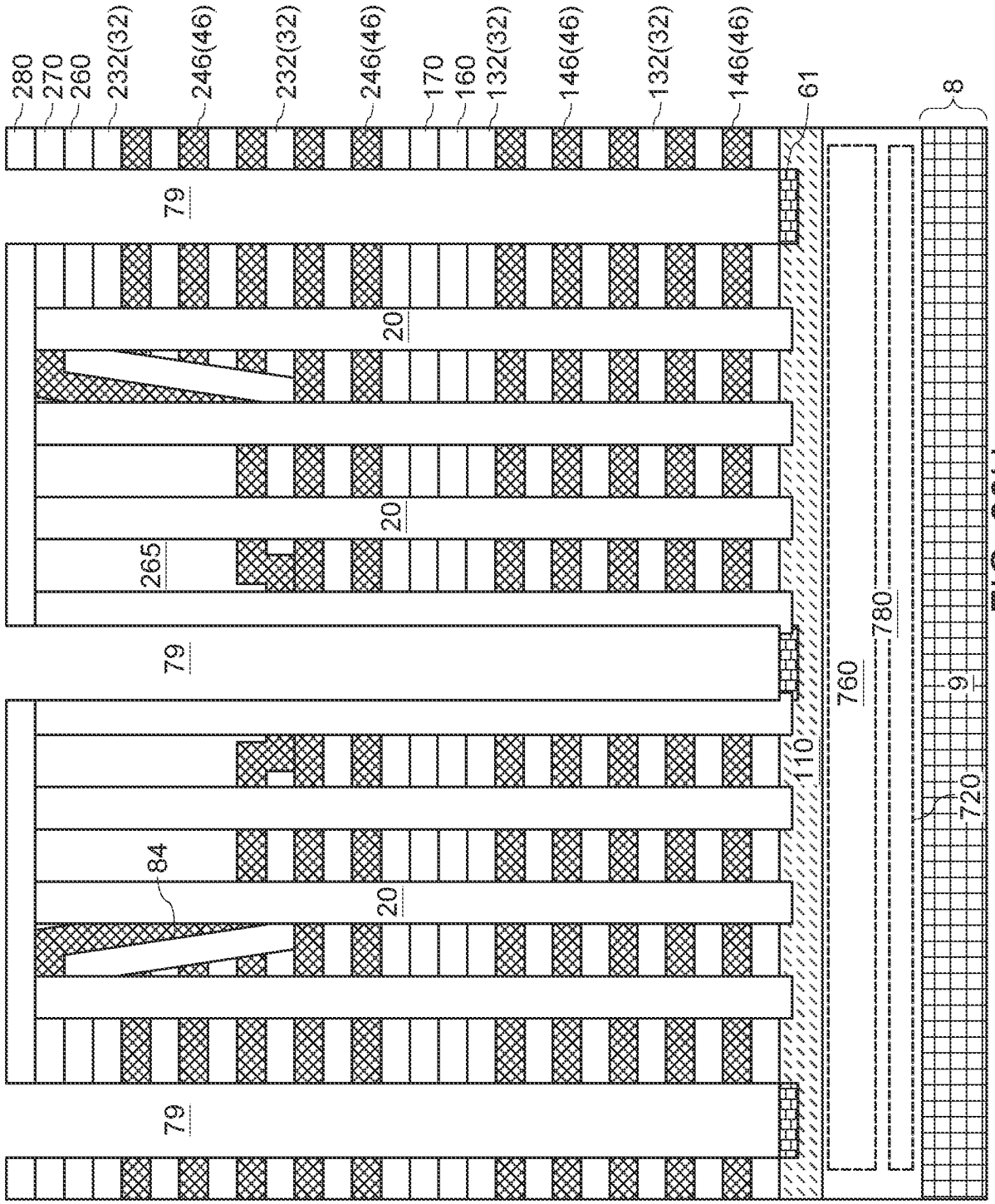
77
79
110
760
780
9
720

FIG. 20G


280
270
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232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
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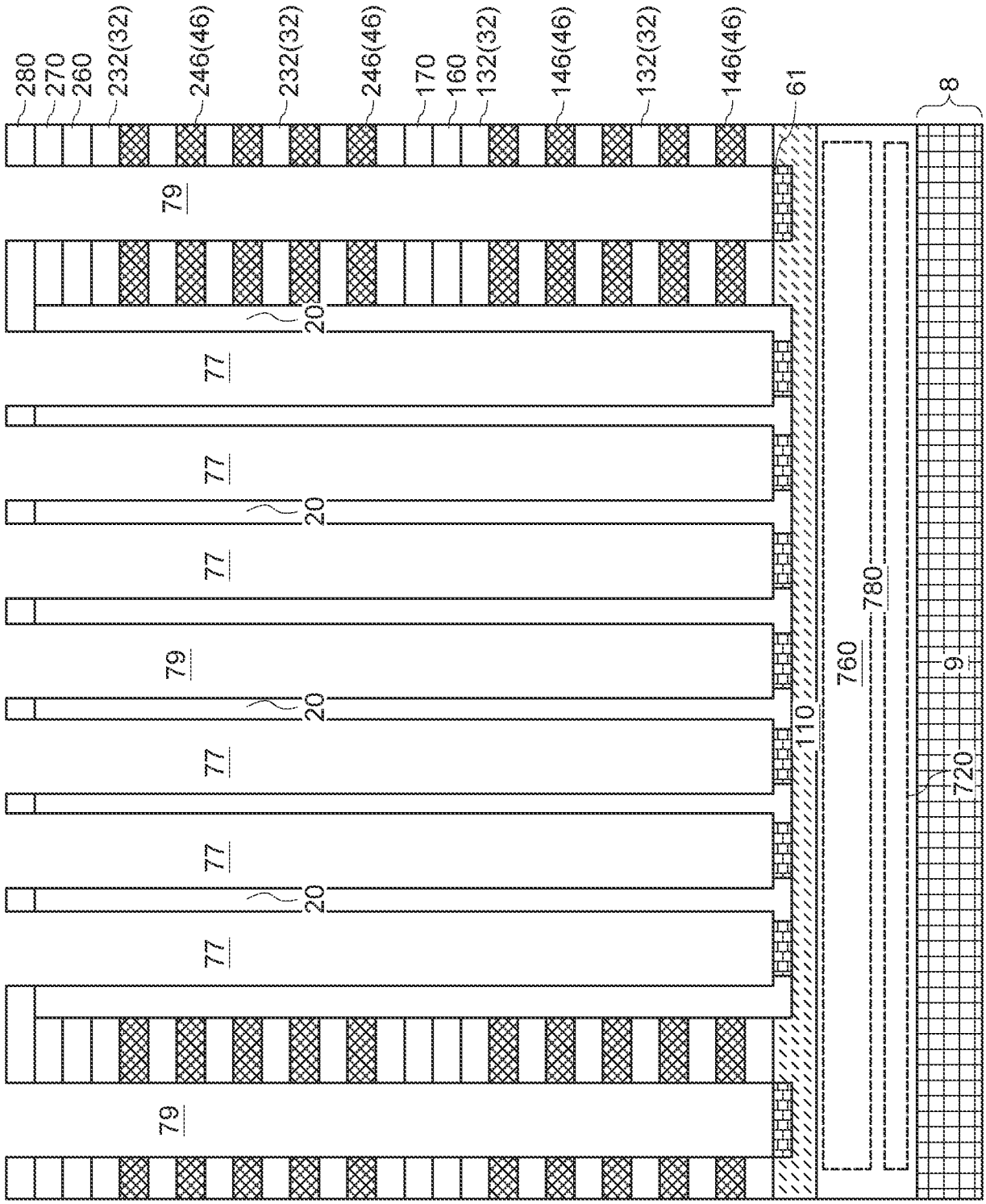
20
265
79
760
780
9
110
720
84
20
79

FIG. 20H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232(32)
246(46)
232(32)
246(46)
170
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132(32)
146(46)
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146(46)
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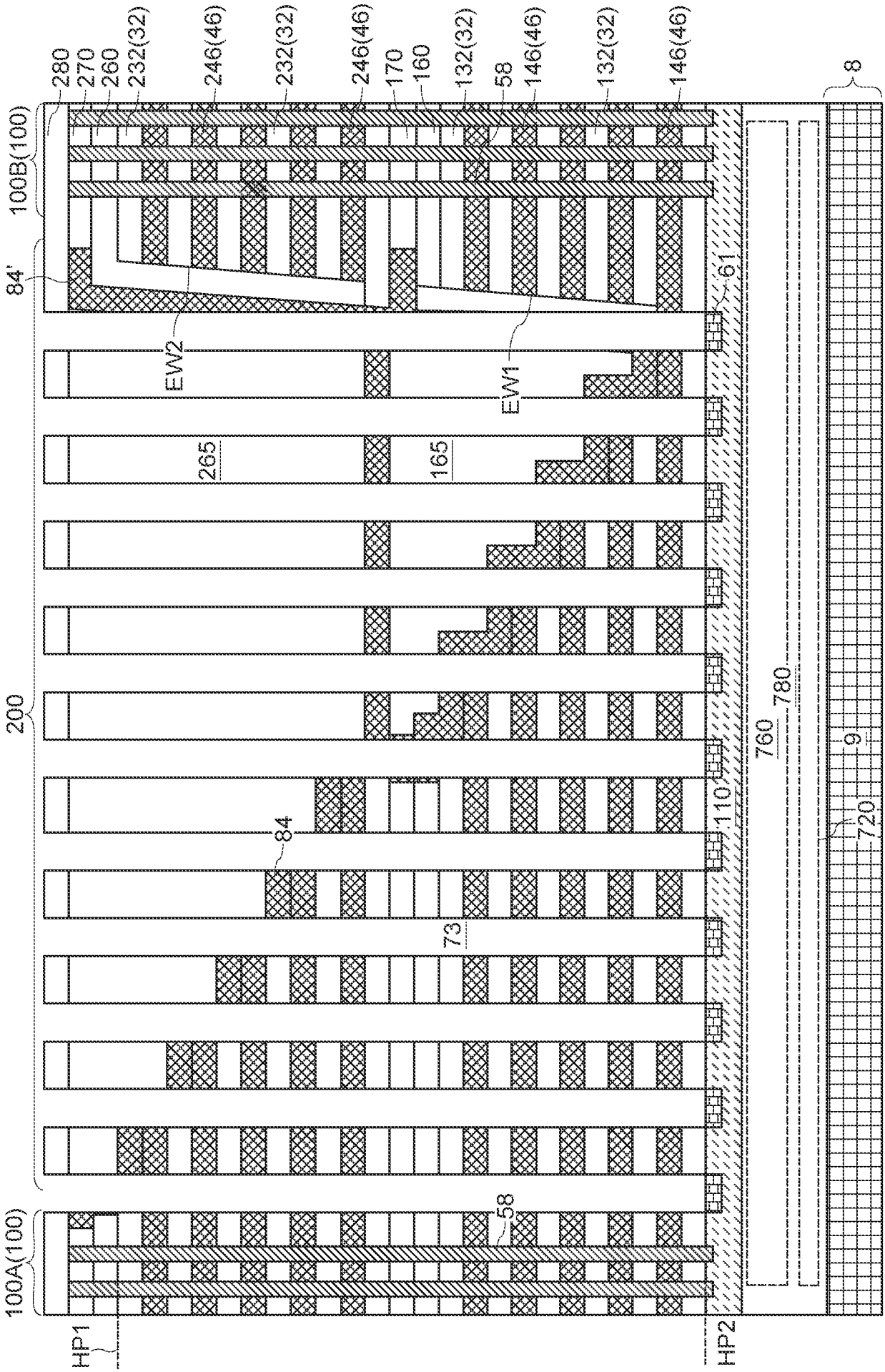
720

FIG. 20I


280
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232(32)
246(46)
232(32)
246(46)
170
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132(32)
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146(46)
132(32)
146(46)
8
100B(100)
84'
61
EW2
EW1
265
165
200
760
780
9
110
720
84
73
58
100A(100)
HP1
HP2

FIG. 21A

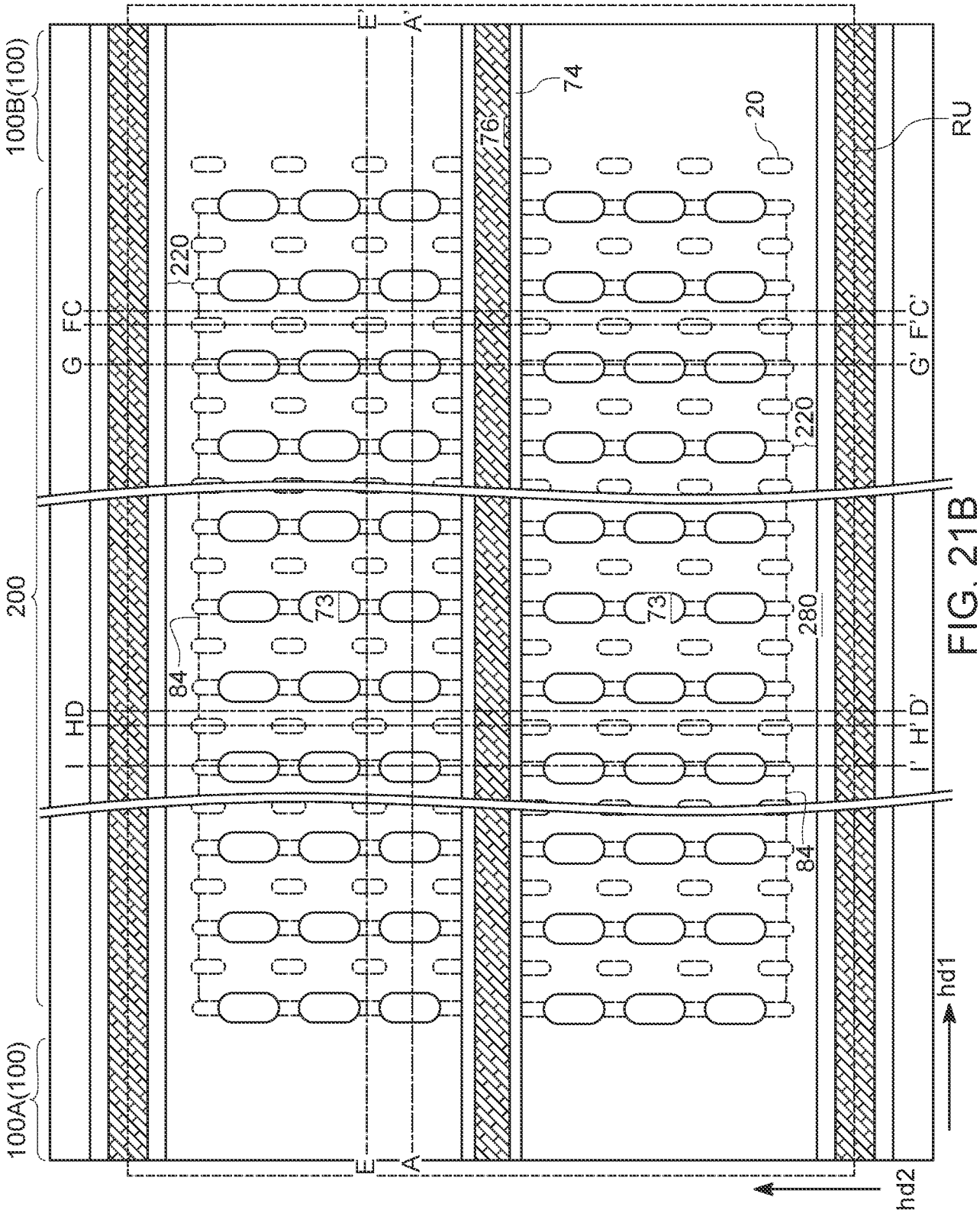
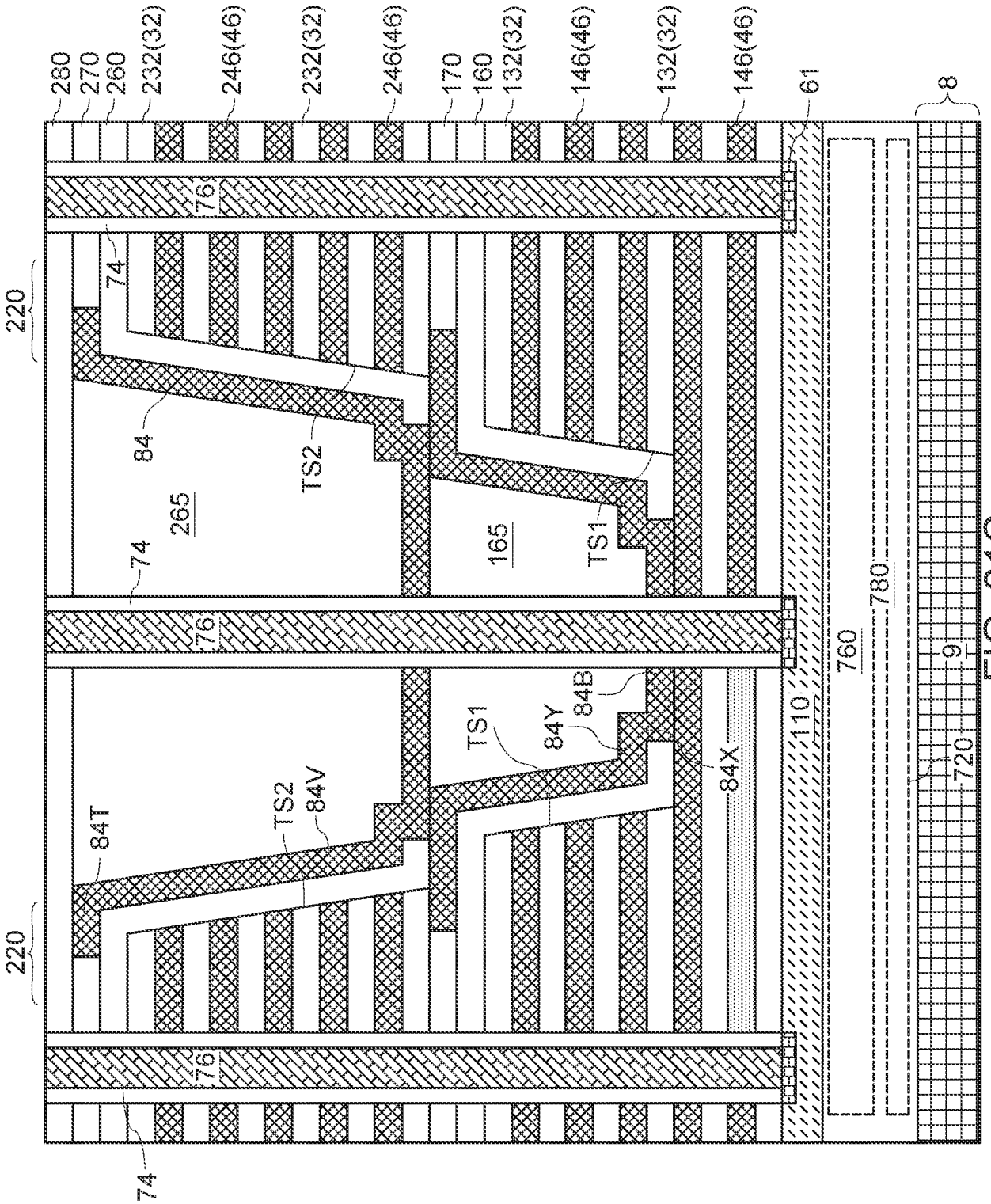

100B(100)
200
100A(100)
E
E'
A
A'
74
76
20
RU
220
G
F
C
G'
F'
C'
220
73
73
280
84
84
I
HD
I'
H'
D'
hd1
hd2

FIG. 21B


280
270
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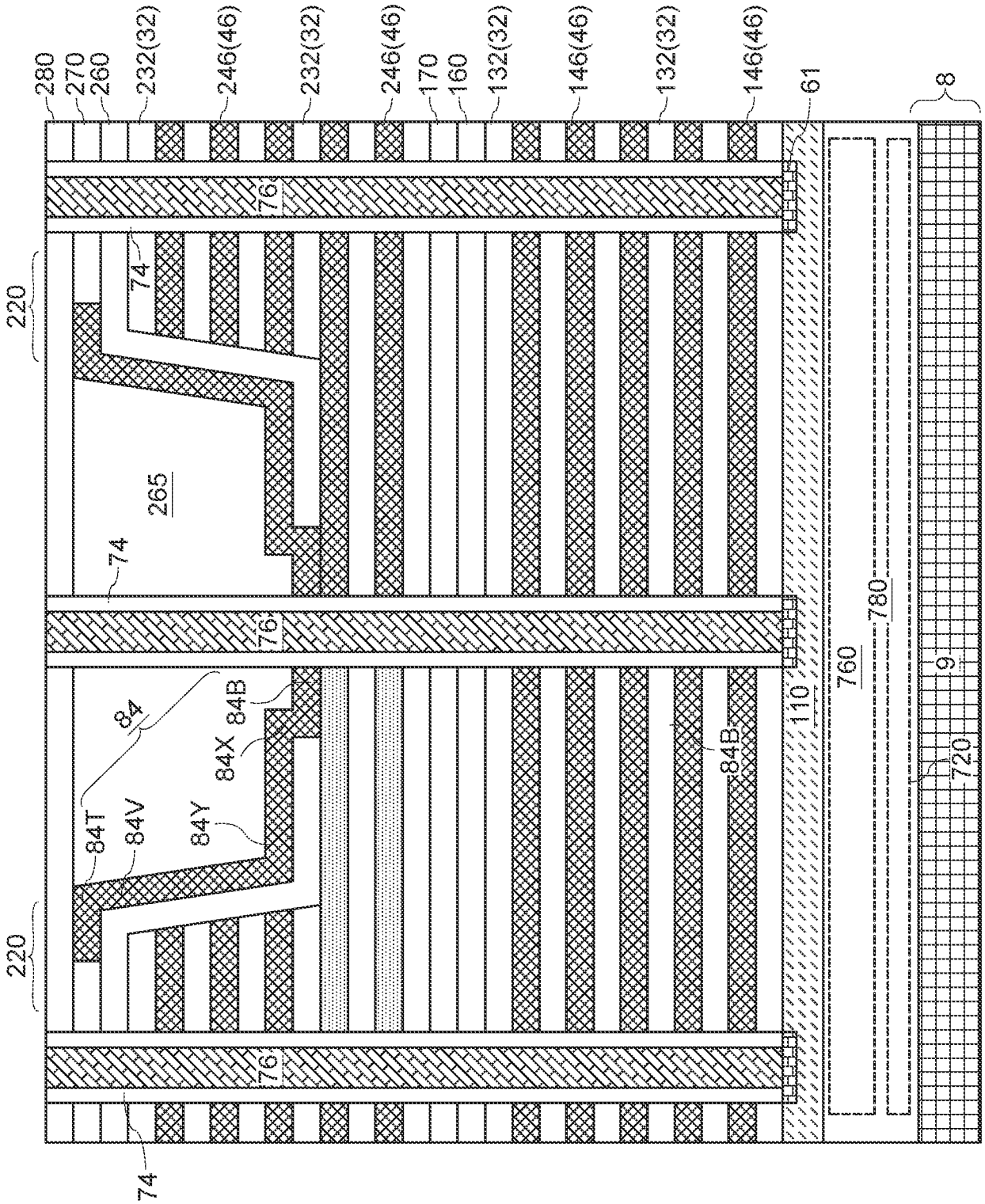
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
220
84
TS2
265
165
TS1
780
760
9
110
84B
84Y
TS1
84X
720
84V
TS2
84T
220
76
74

FIG. 21C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270
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232(32)
246(46)
232(32)
246(46)
170
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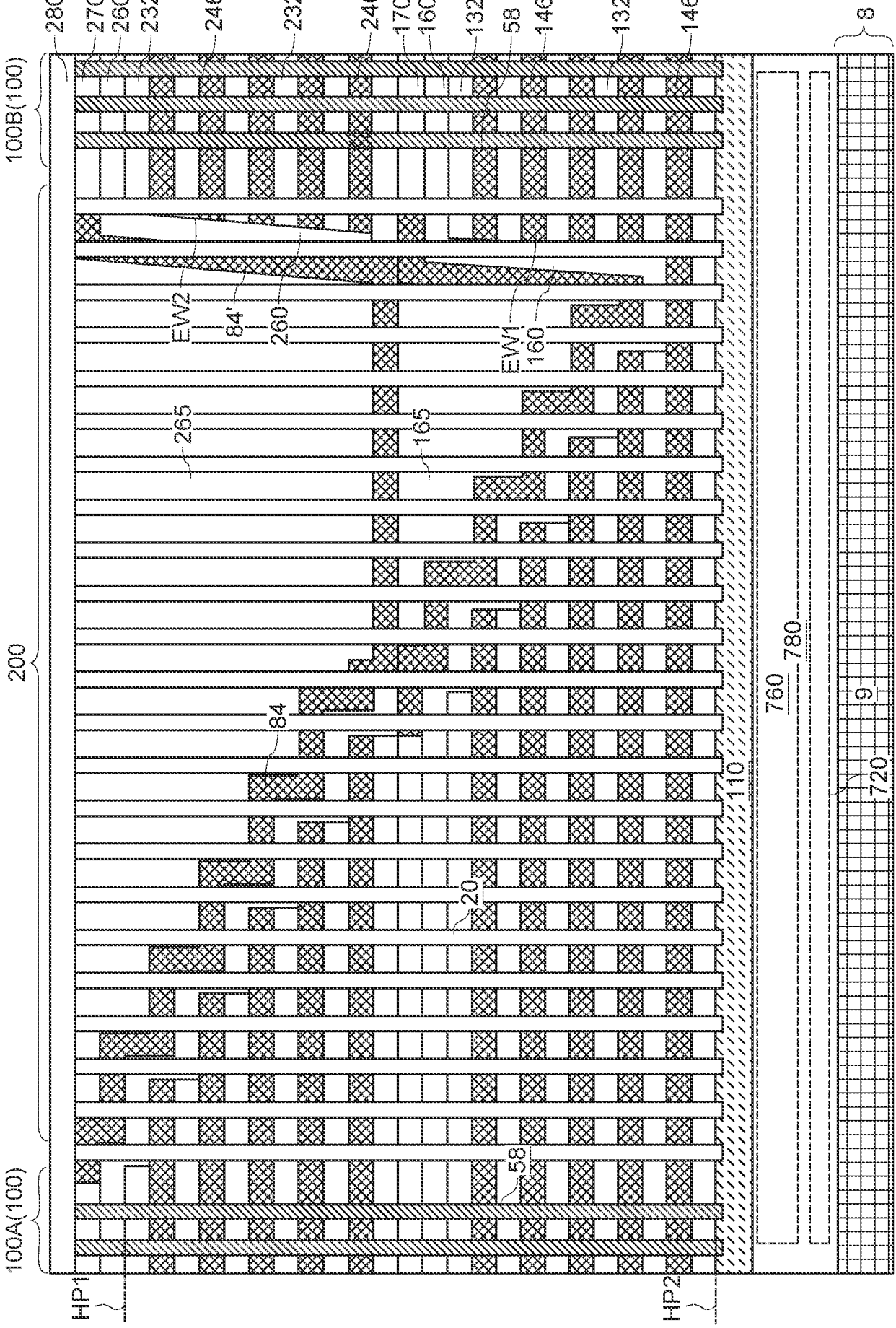
132(32)
146(46)
132(32)
146(46)
61
8
76
74
220
265
84
84B
84X
84T
84V
84Y
110
760
780
9
720

FIG. 21D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232(32)
246(46)
232(32)
246(46)
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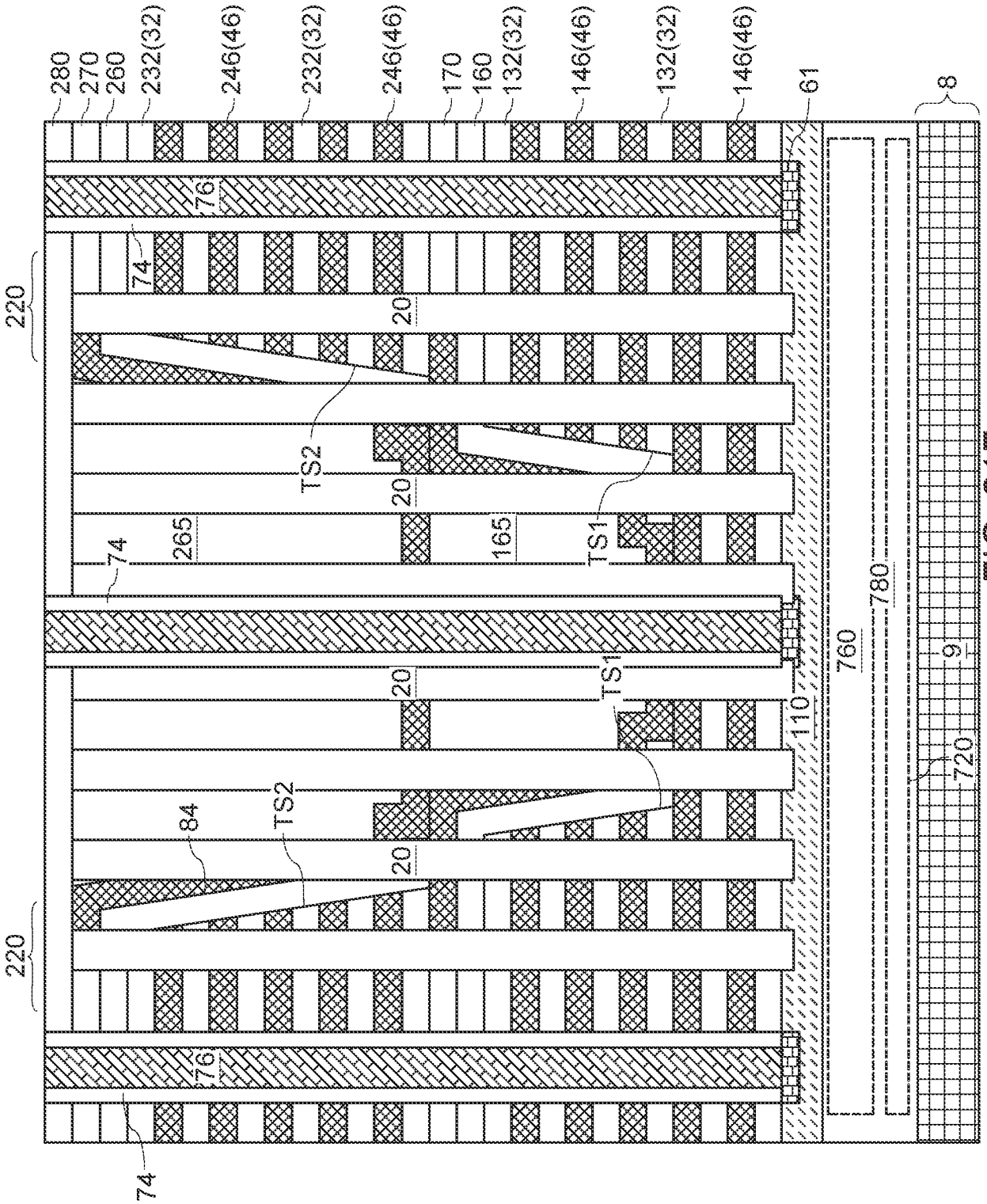
160
132(32)
58
146(46)
132(32)
146(46)
8
100B(100)
EW2
84'
260
EW1
160
265
165
200
84
110
760
780
9
720
20
58
100A(100)
HP1
HP2

FIG. 21E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232(32)
246(46)
232(32)
246(46)
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132(32)
146(46)
132(32)
146(46)
61
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76
74
220
20
TS2
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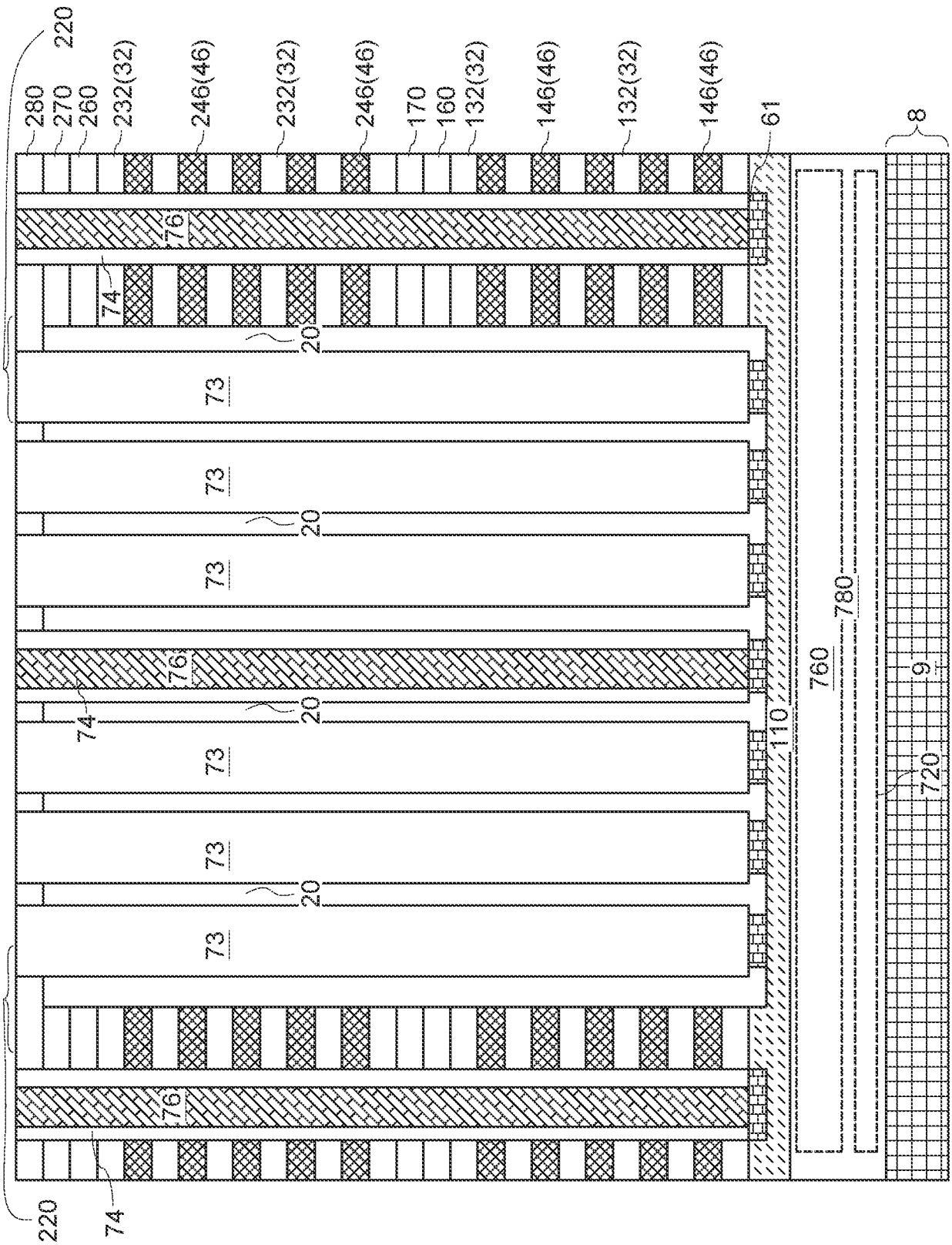
265
165
TS1
74
780
760
9
TS1
110
720
84
TS2
20
220
76
74

FIG. 21F


220
280
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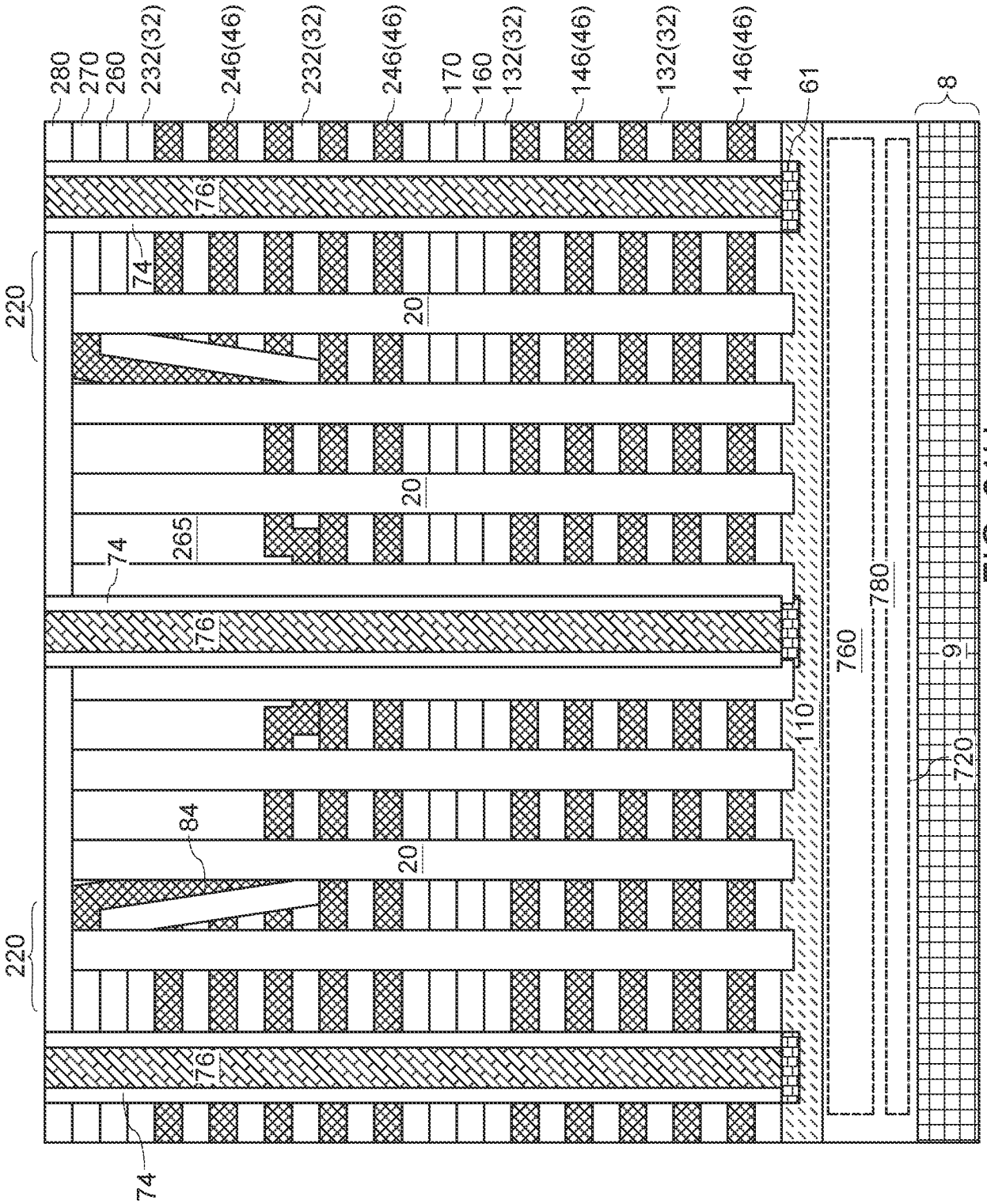
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
20
73
760
780
9
110
720

FIG. 21G


280
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232(32)
246(46)
232(32)
246(46)
170
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132(32)
146(46)
132(32)
146(46)
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76
74
220
20
265
780
760
9
110
720
84

FIG. 21H

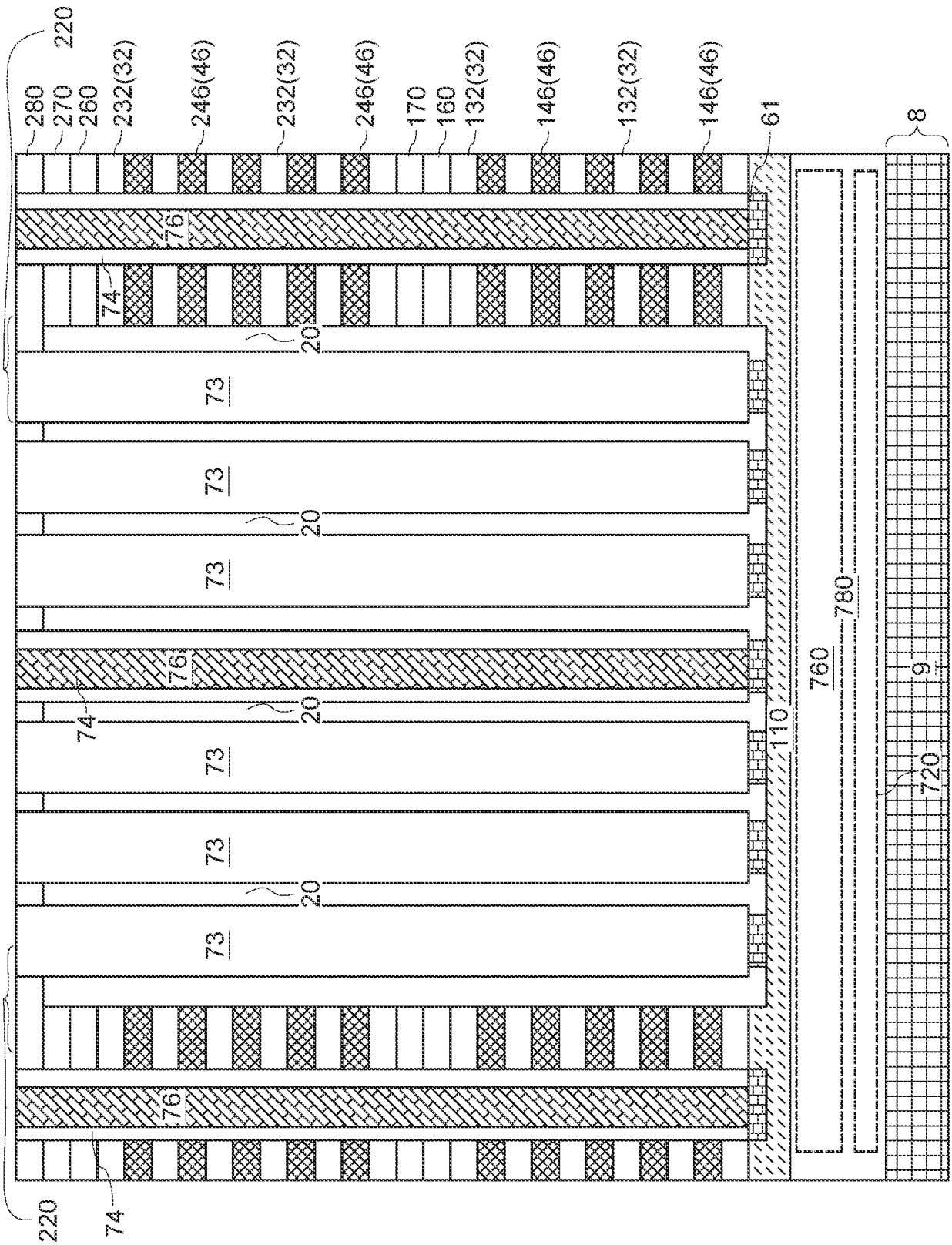

220
280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
20
73
760
780
9
110
720
220
74

FIG. 21I

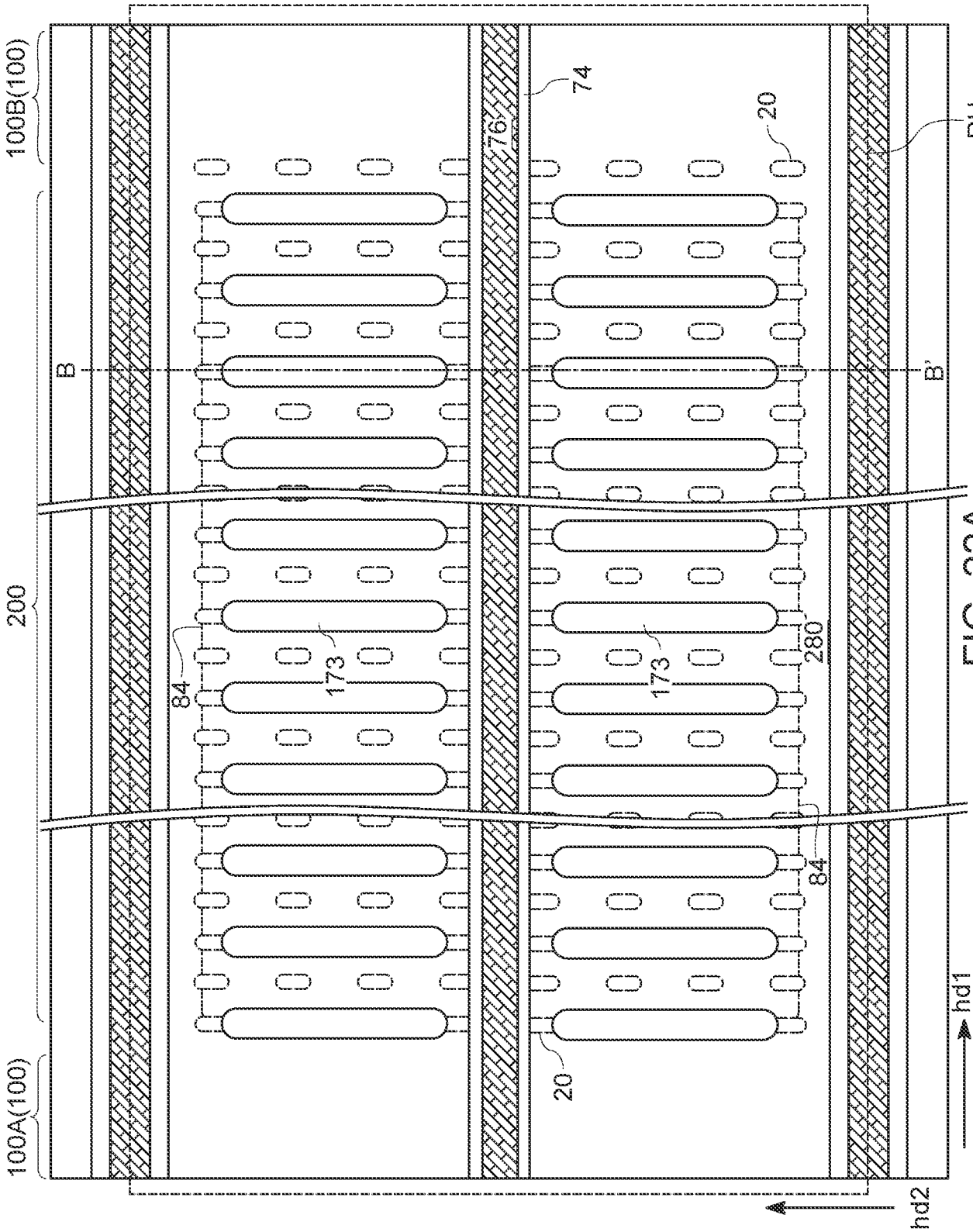
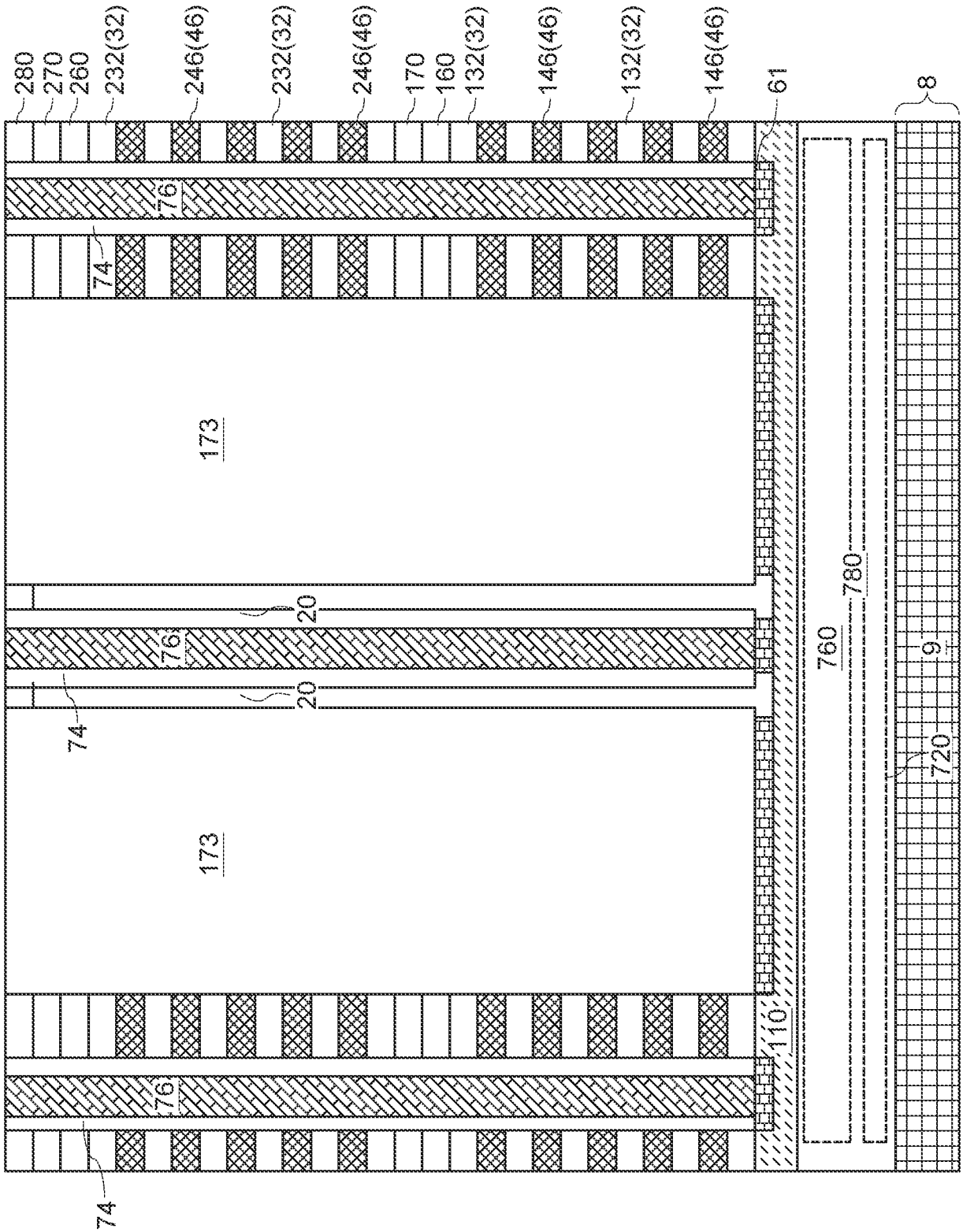


FIG. 22A


280
270
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232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
173
20
760
780
9
720
110

FIG. 22B

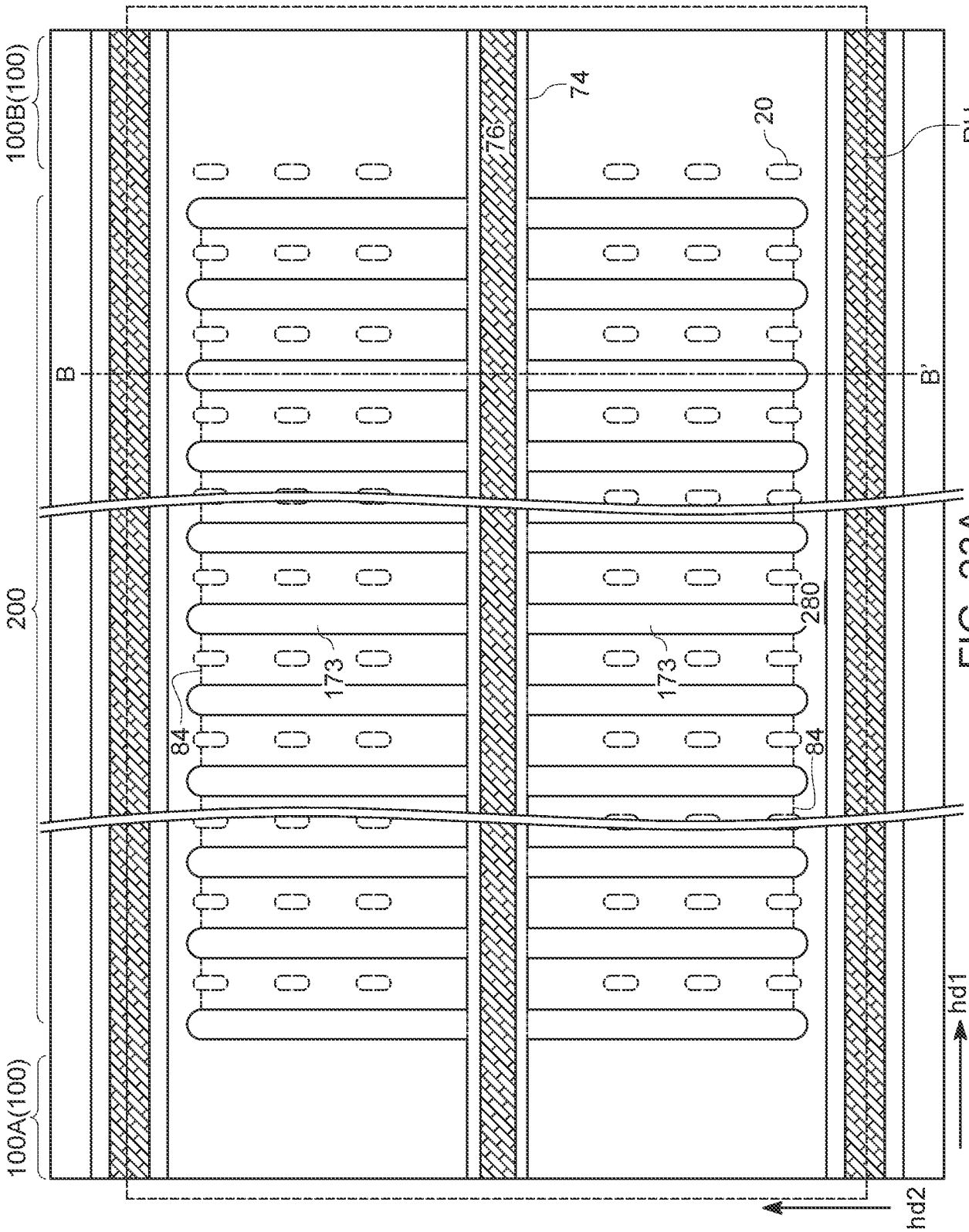


FIG. 23A

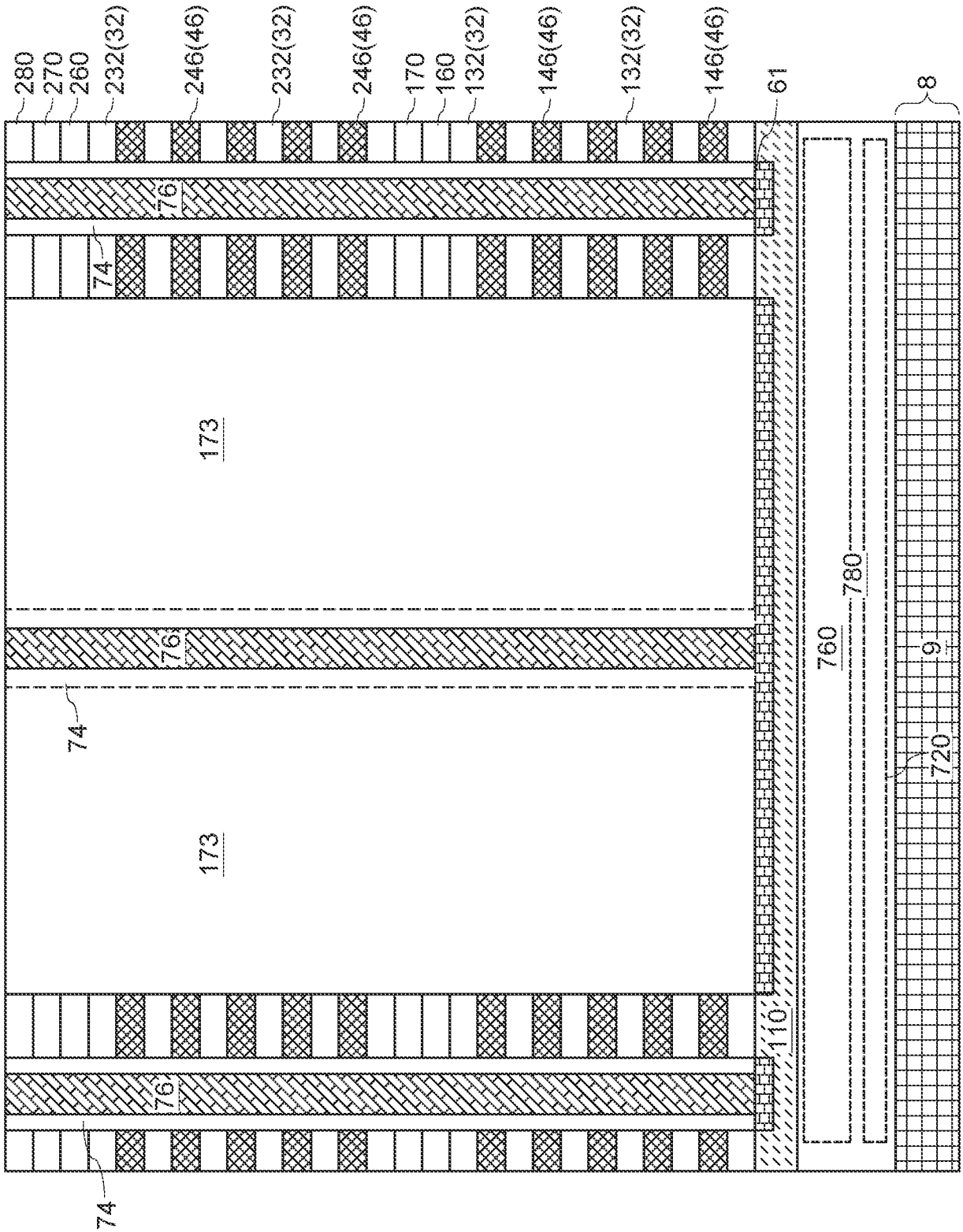

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
173
76
74
173
76
74
110
760
780
9
720

FIG. 23B

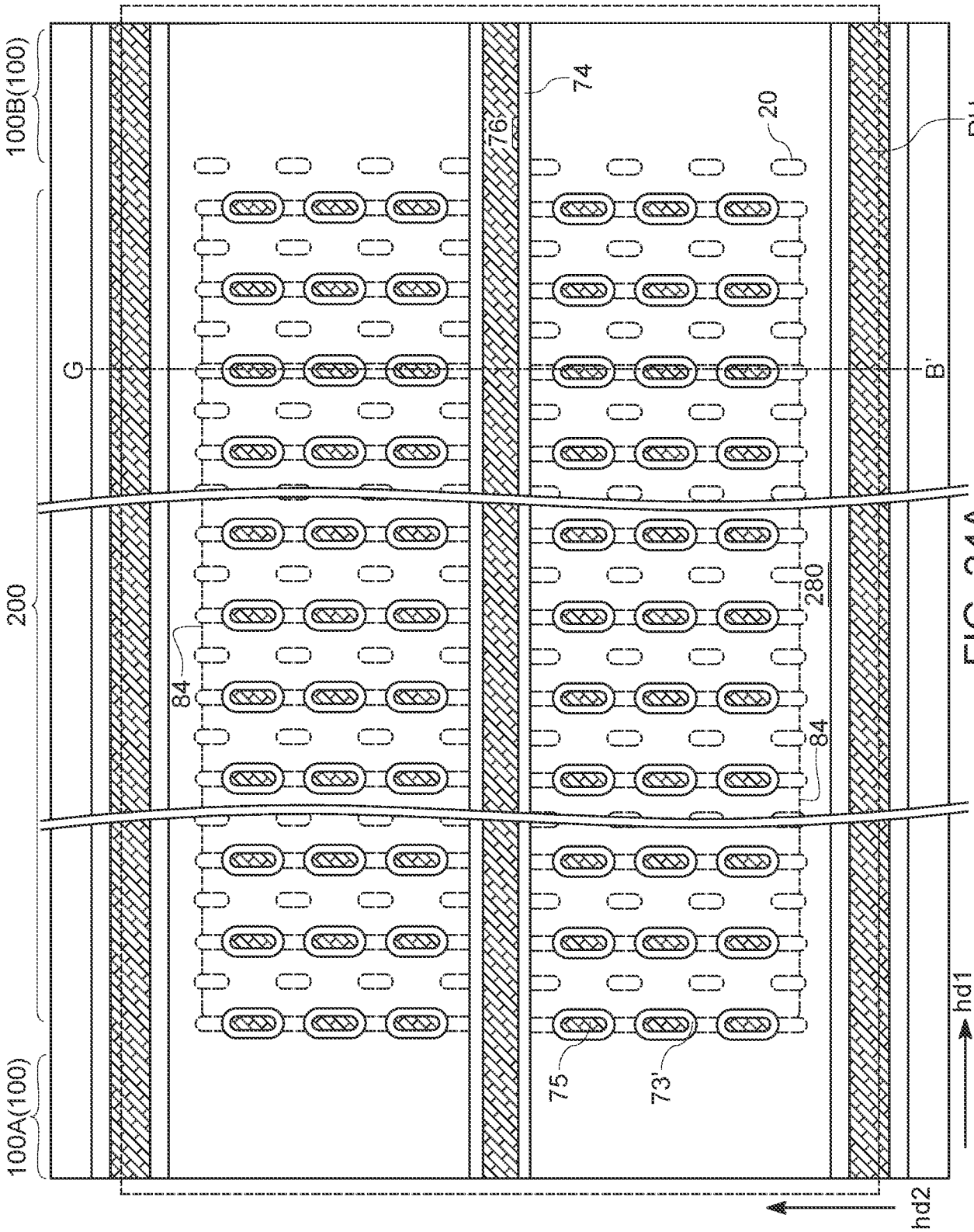


FIG. 24A

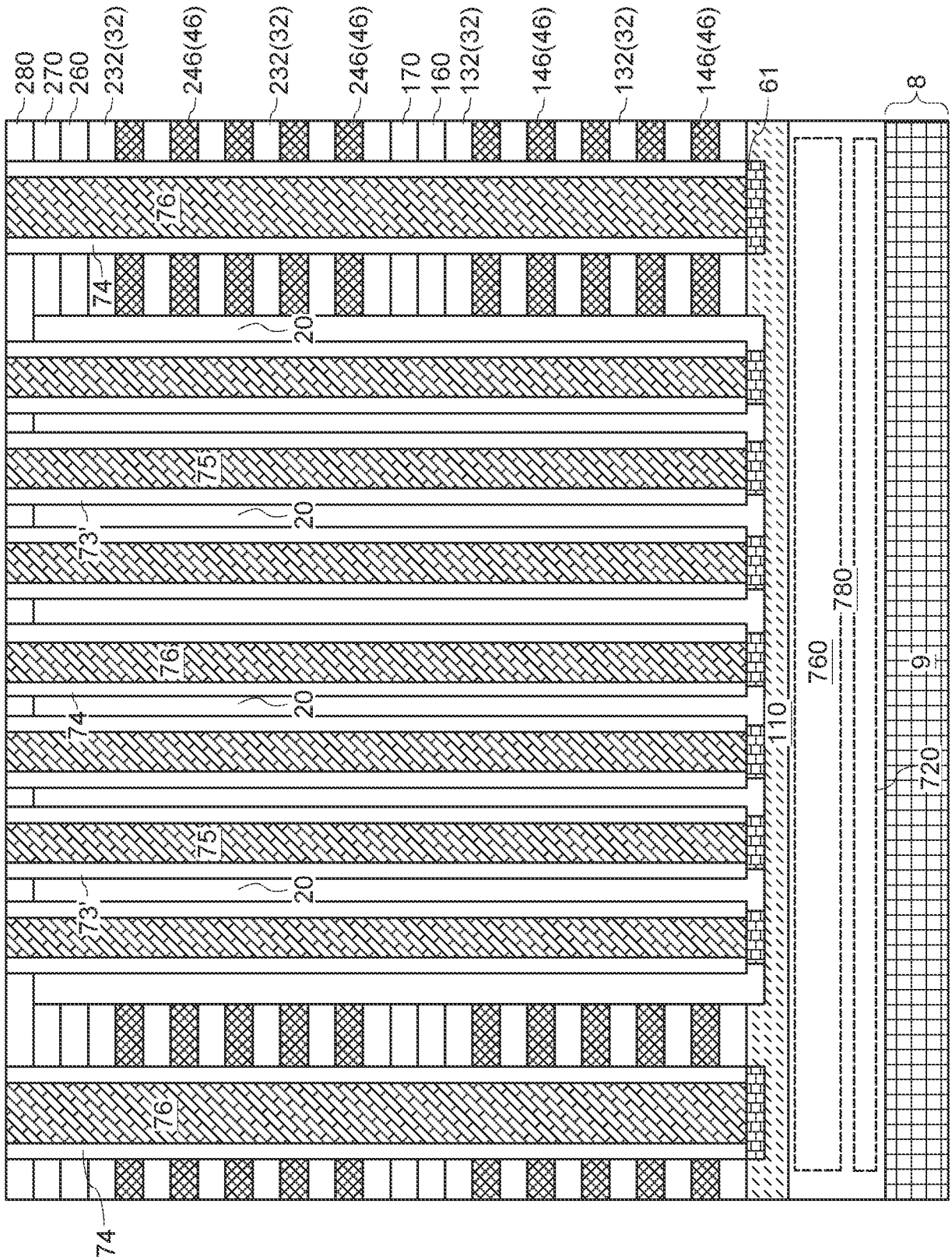

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
20
75
73'
20
76
74
20
75
73'
20
76
74
760
780
9
110
720

FIG. 24B

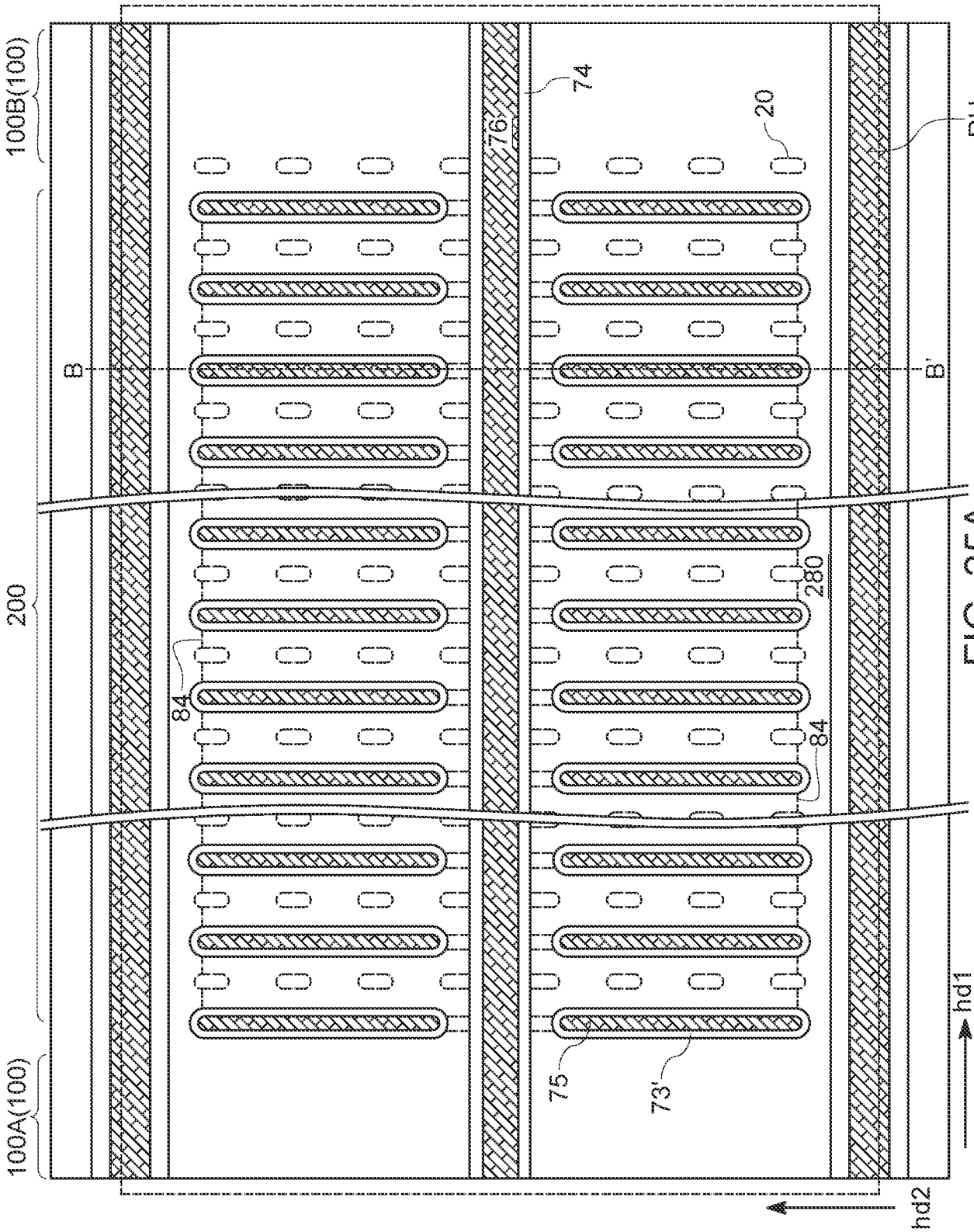


FIG. 25A

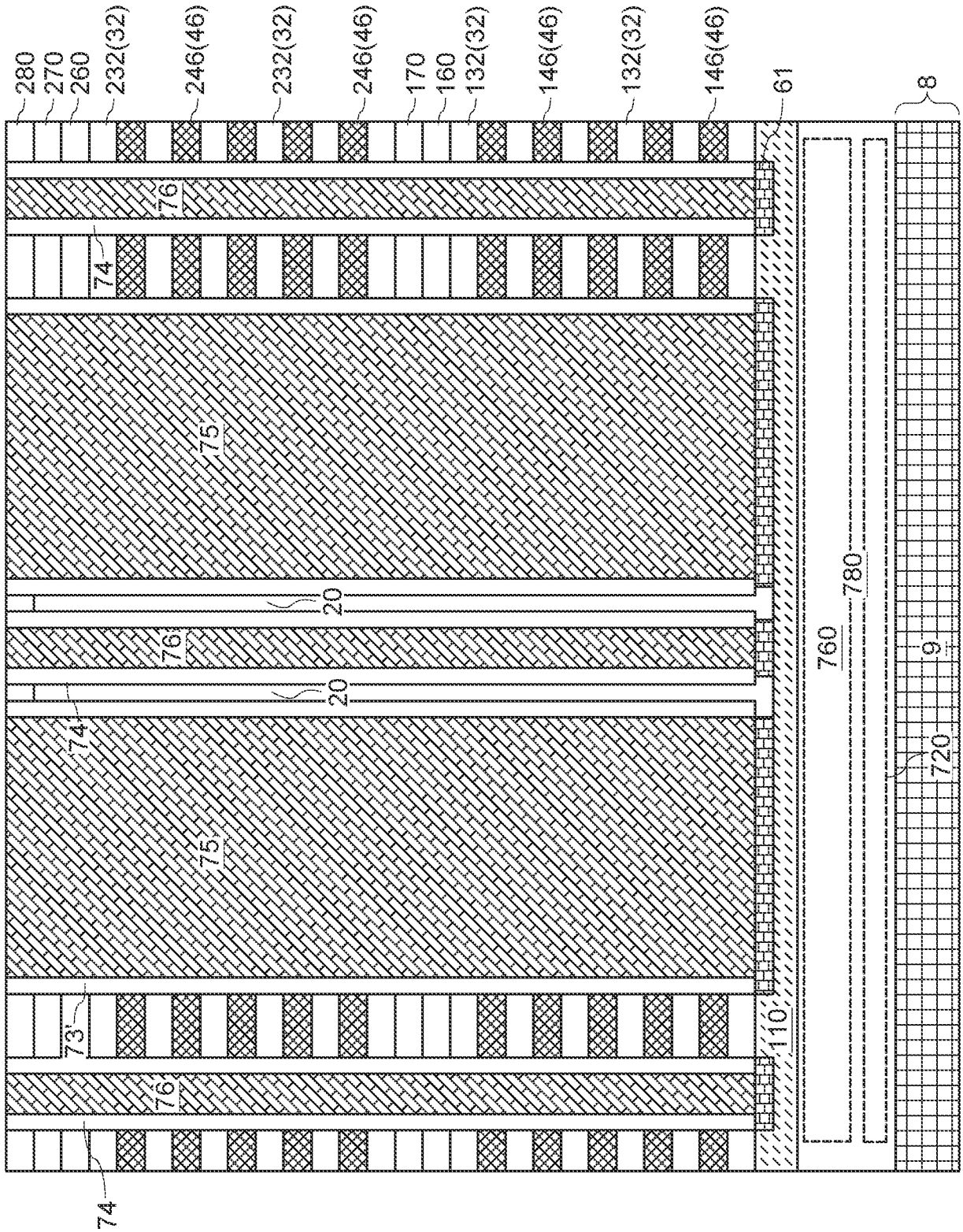

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
75
20
76
20
74
75
73'
76
74
110
760
780
9
720

FIG. 25B

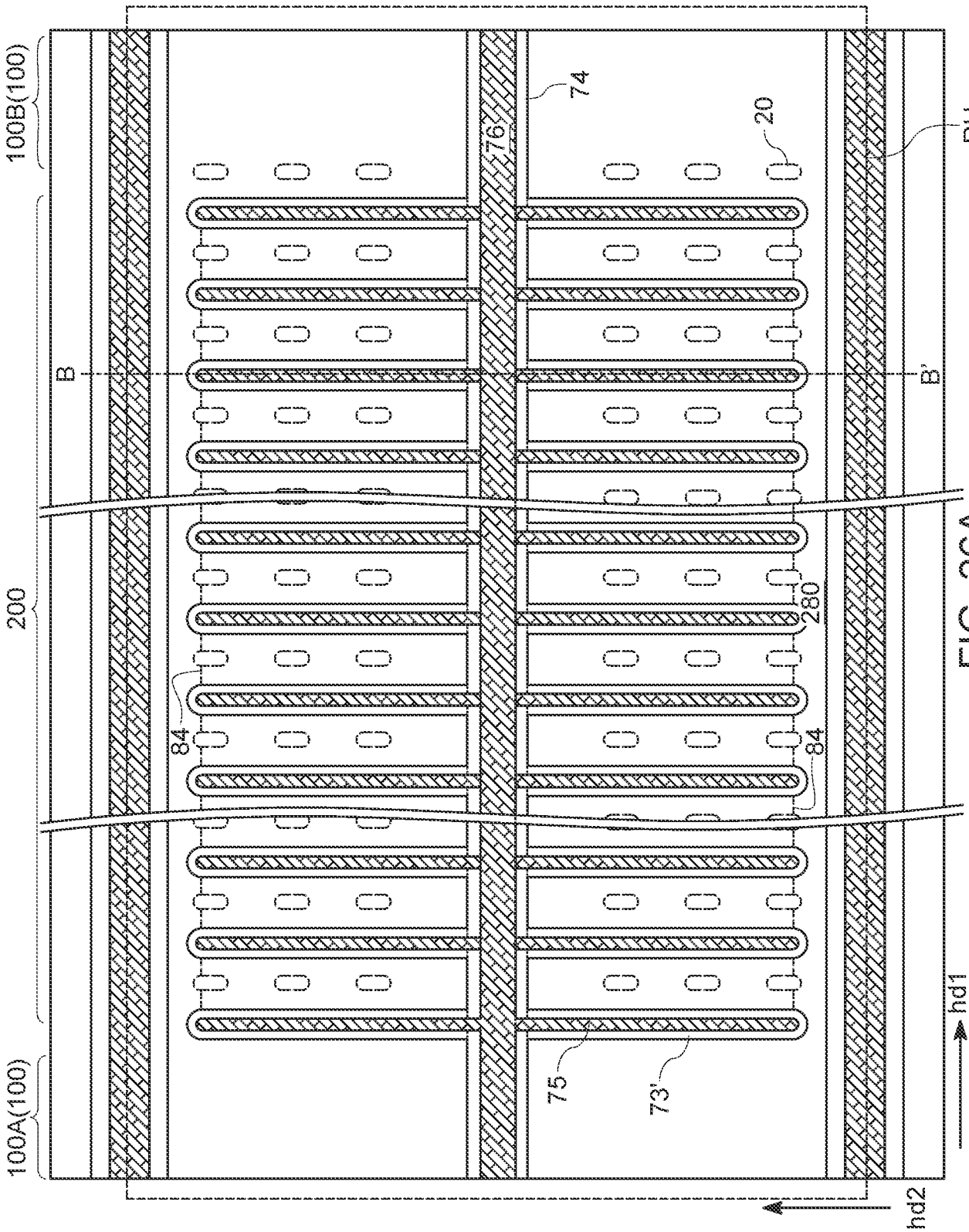


FIG. 26A

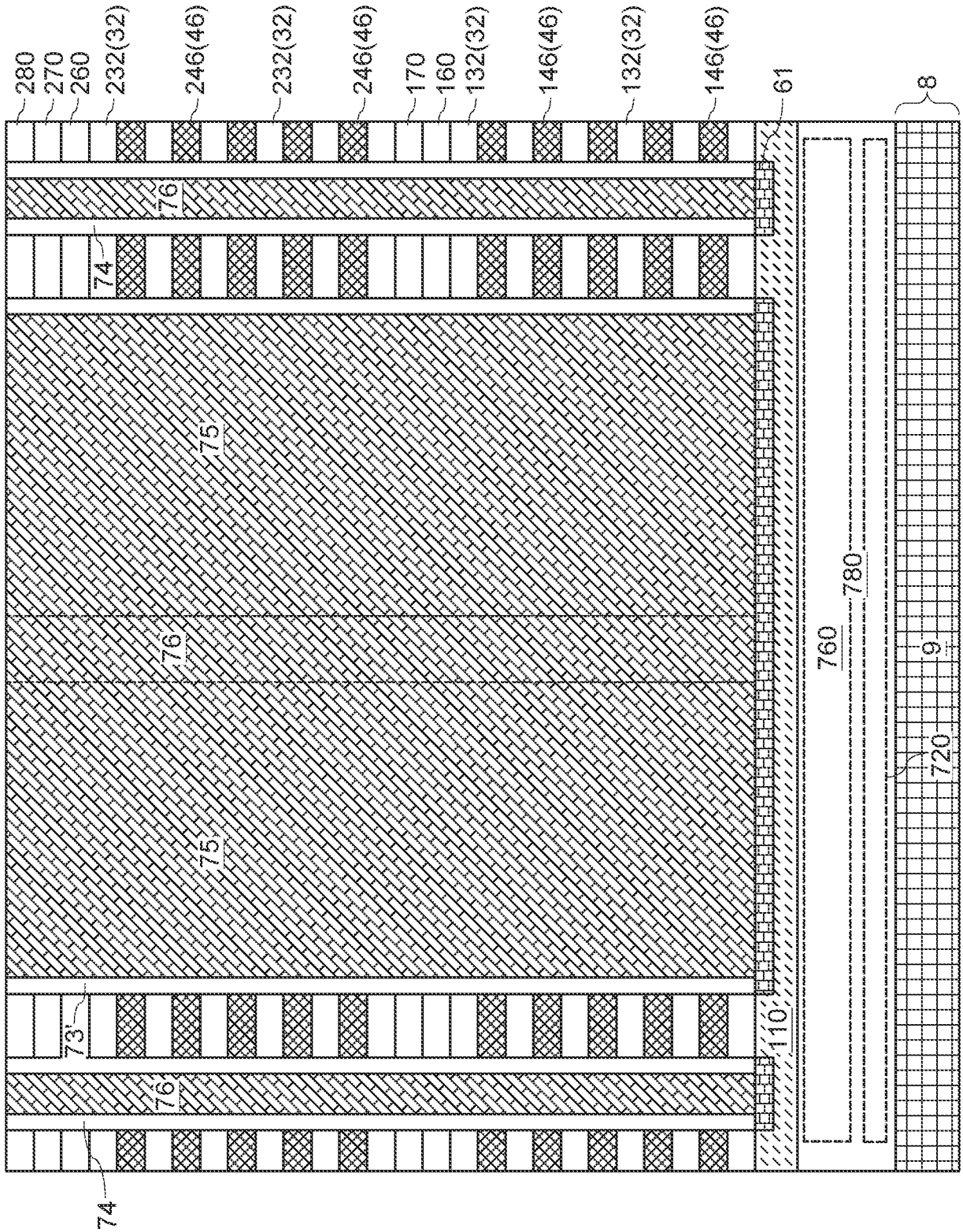

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
75
76
75
73
76
74
110
760
780
9
720

FIG. 26B

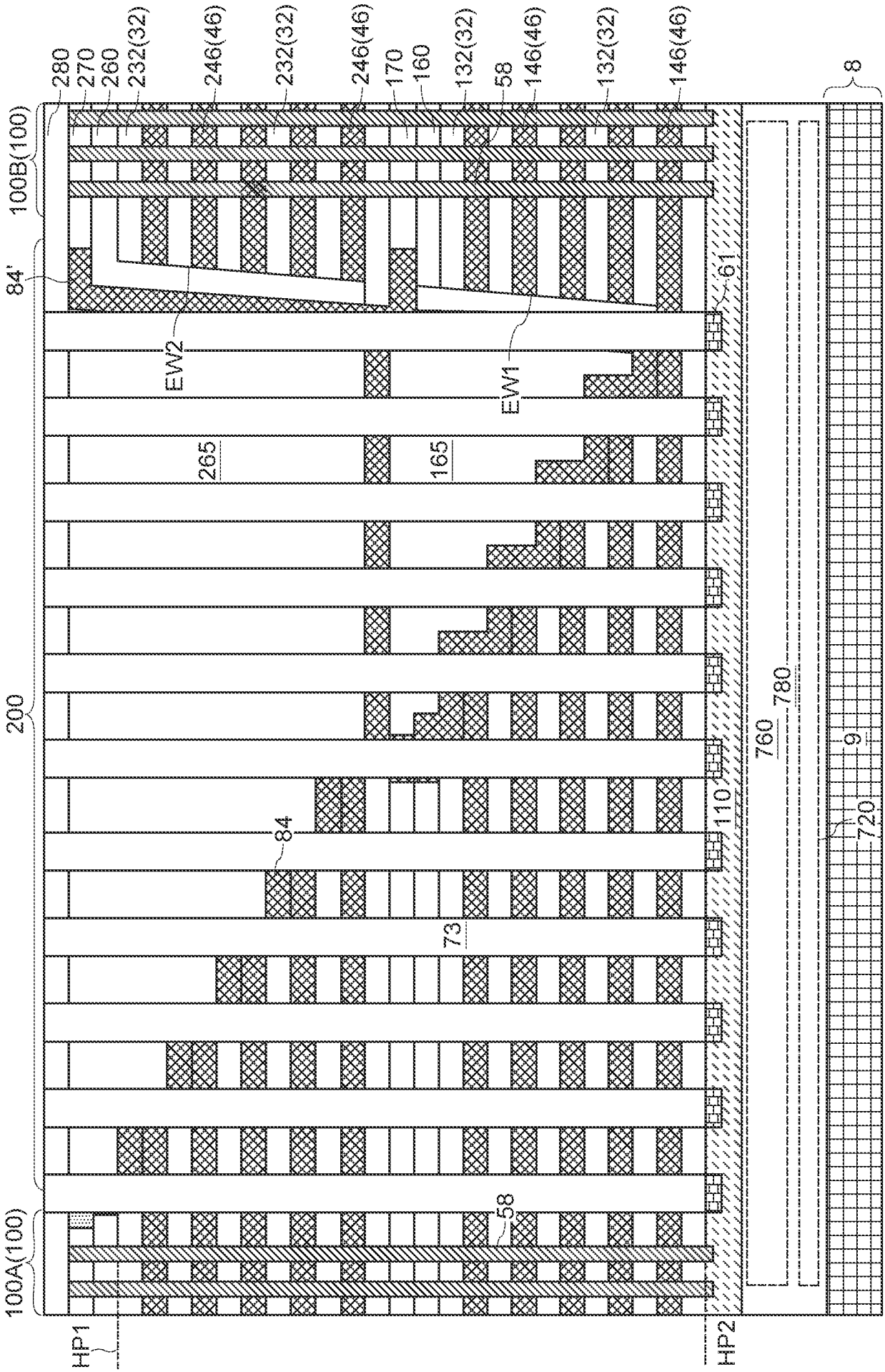

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
58
146(46)
132(32)
146(46)
8
100B(100)
84'
61
EW2
EW1
265
165
200
760
780
9
110
720
84
73
58
100A(100)
HP1
HP2

FIG. 27A

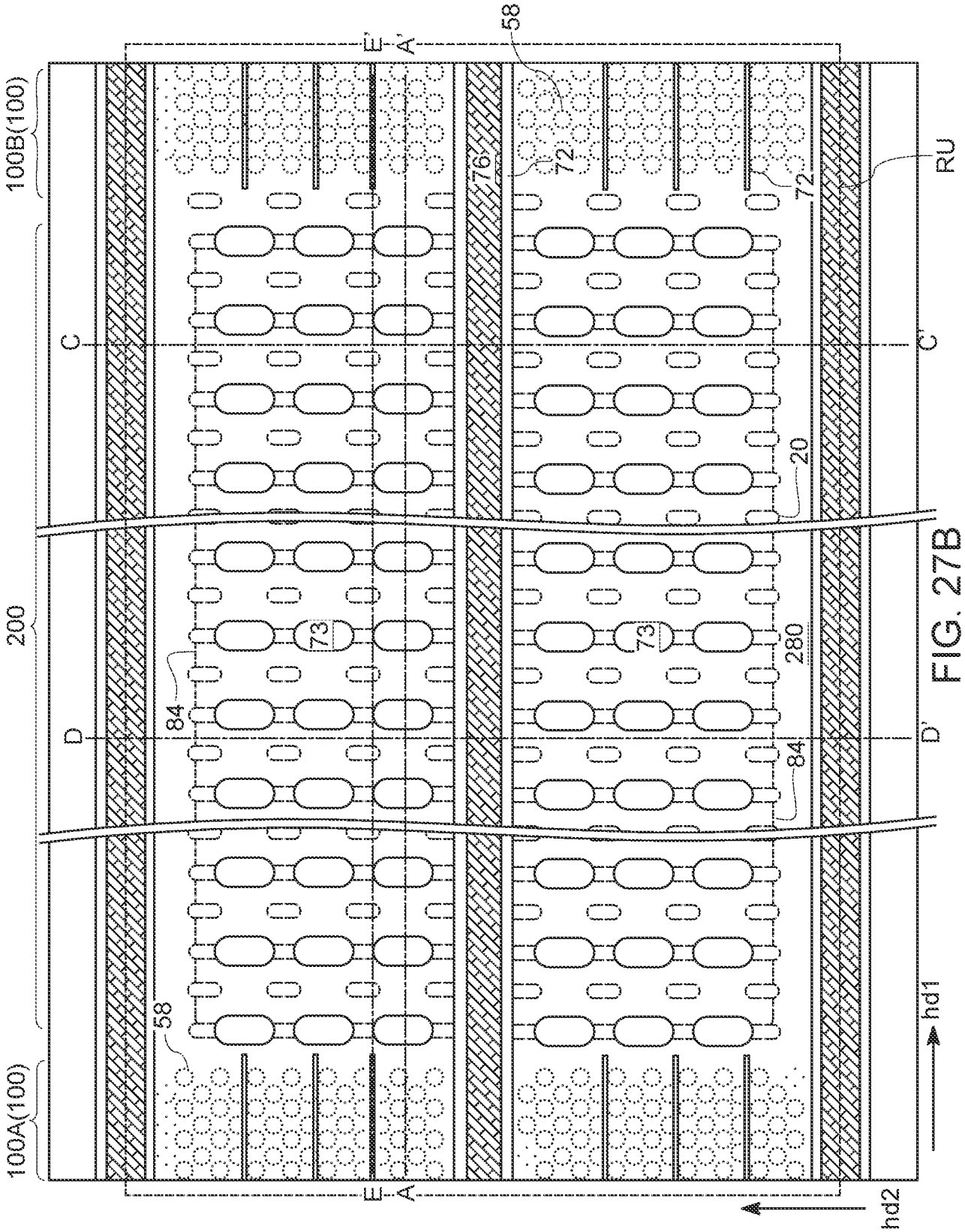
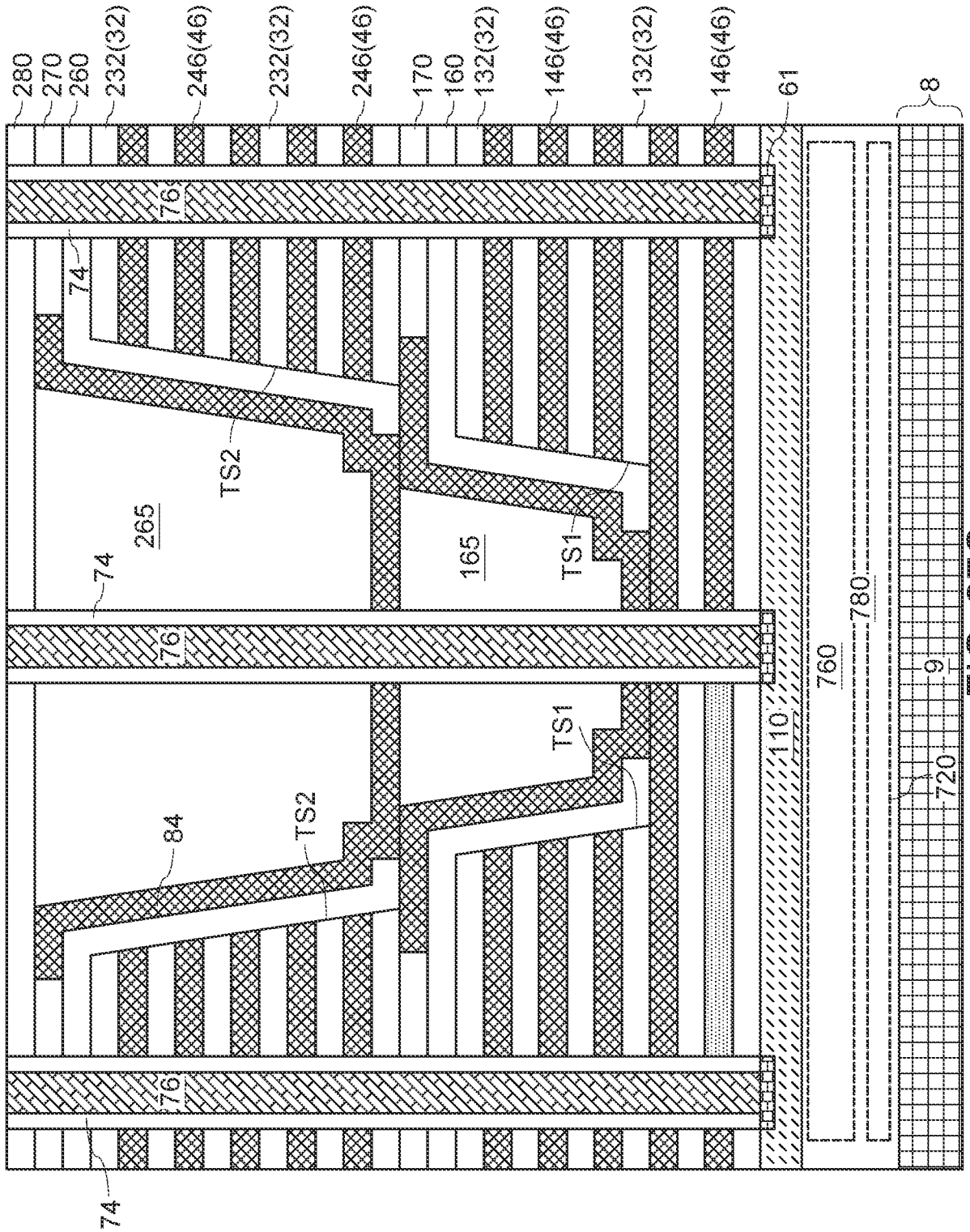

E'
A'
58
100B(100)
76
72
72
RU
C
C'
20
200
73
73
280
84
D
D'
84
58
100A(100)
E
A
hd1
hd2

FIG. 27B


280
270
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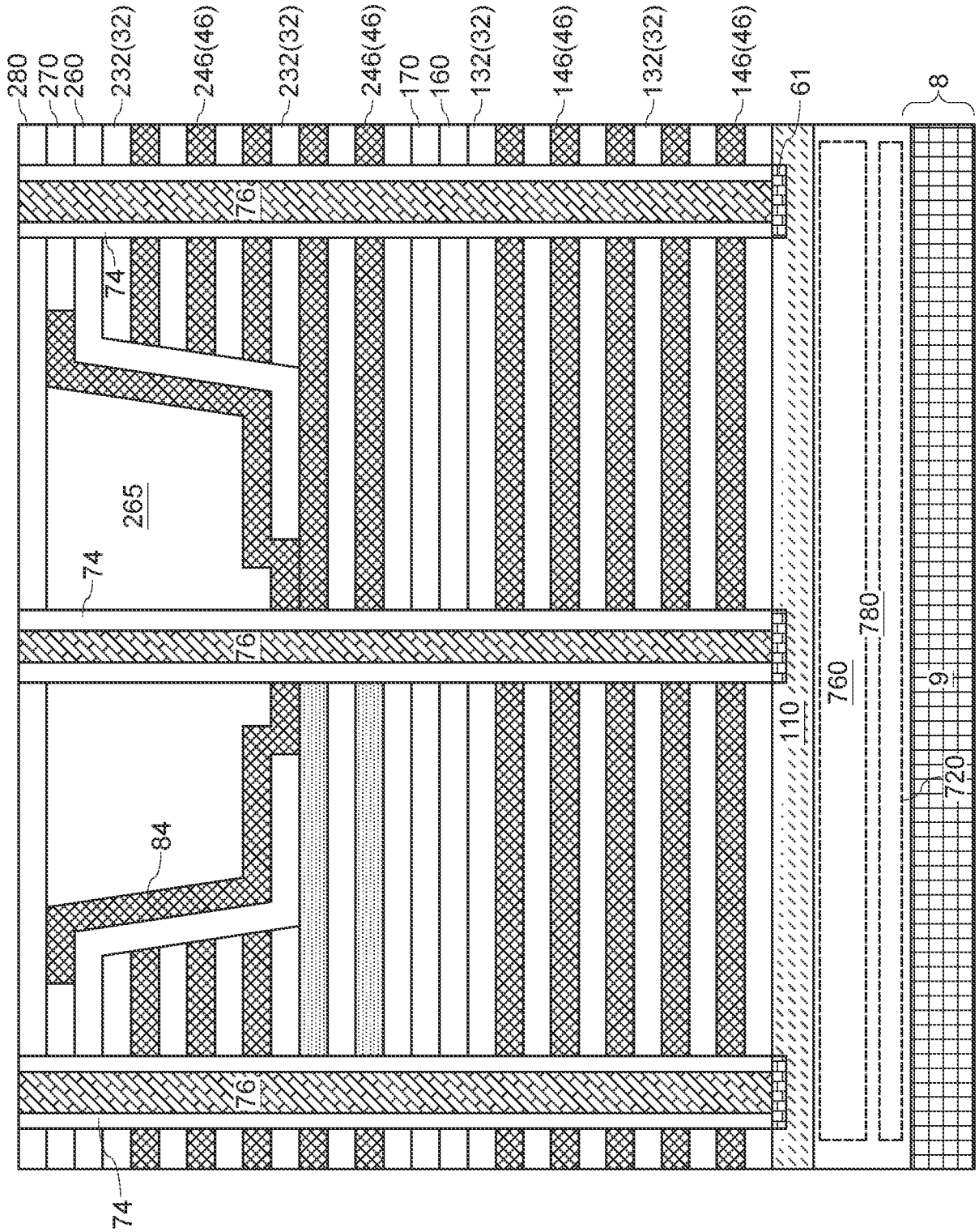
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
TS2
265
165
TS1
74
780
760
9
76
TS1
110
720
84
TS2
76
74

FIG. 27C


280
270
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232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
76
74
265
74
76
84
76
74
110
760
780
9
720

FIG. 27D

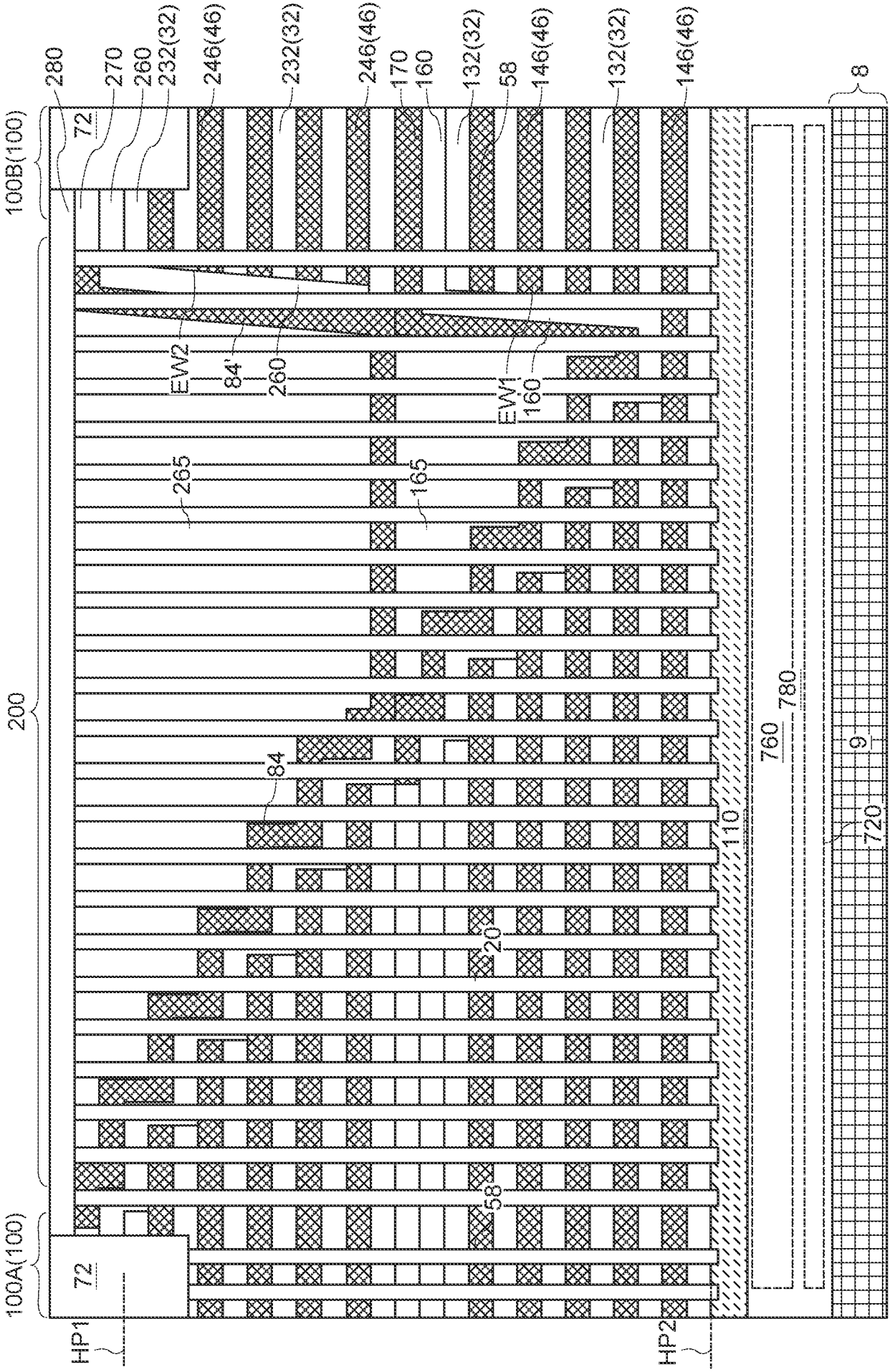

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
58
146(46)
132(32)
146(46)
8
100B(100)
72
EW2
84'
260
EW1
160
265
165
200
84
110
20
760
780
9
720
58
100A(100)
72
HP1
HP2

FIG. 27E

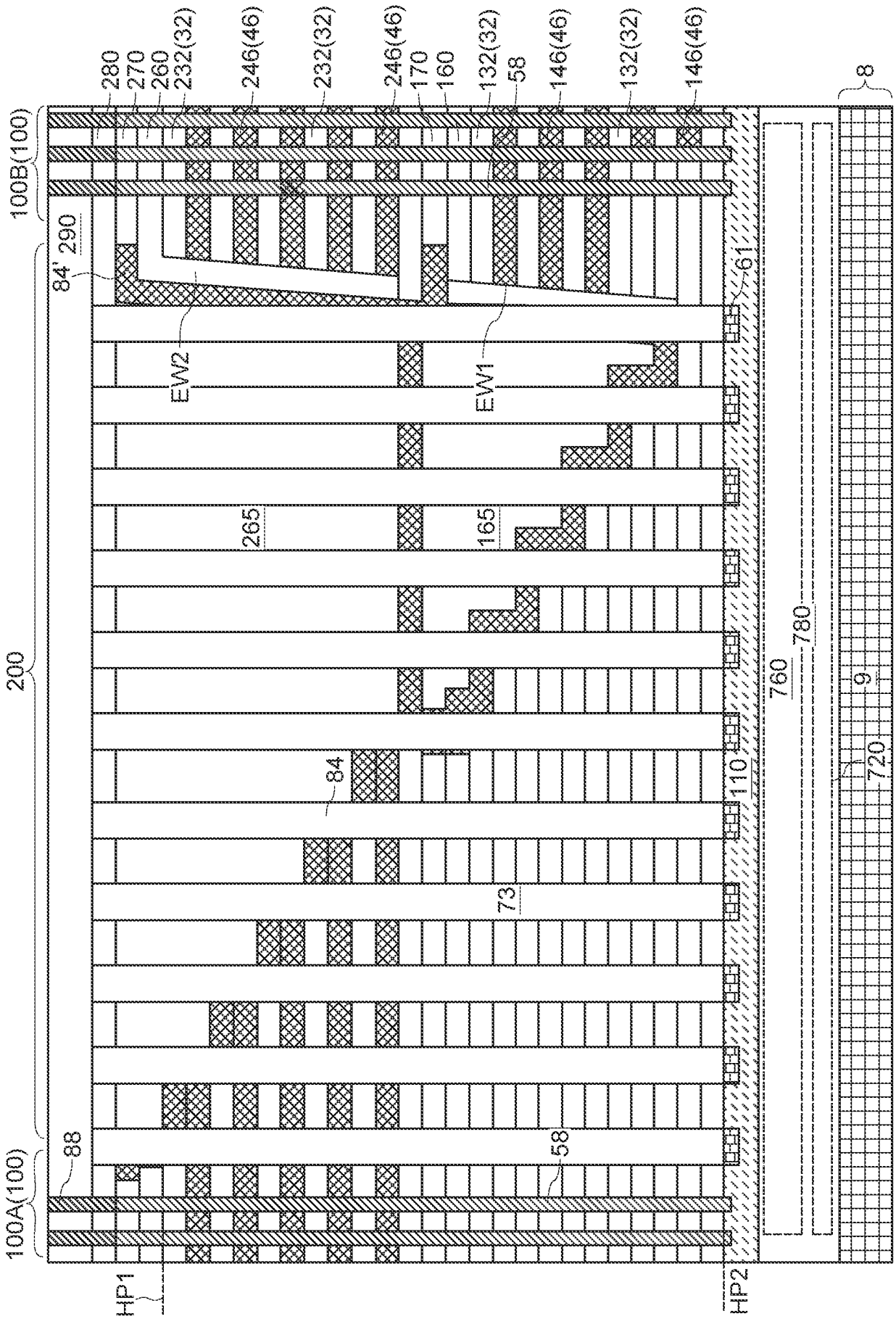

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
58
146(46)
132(32)
146(46)
8
100B(100)
290
84'
61
EW2
EW1
265
165
200
760
780
9
720
84
110
73
88
58
100A(100)
HP1
HP2

FIG. 28A

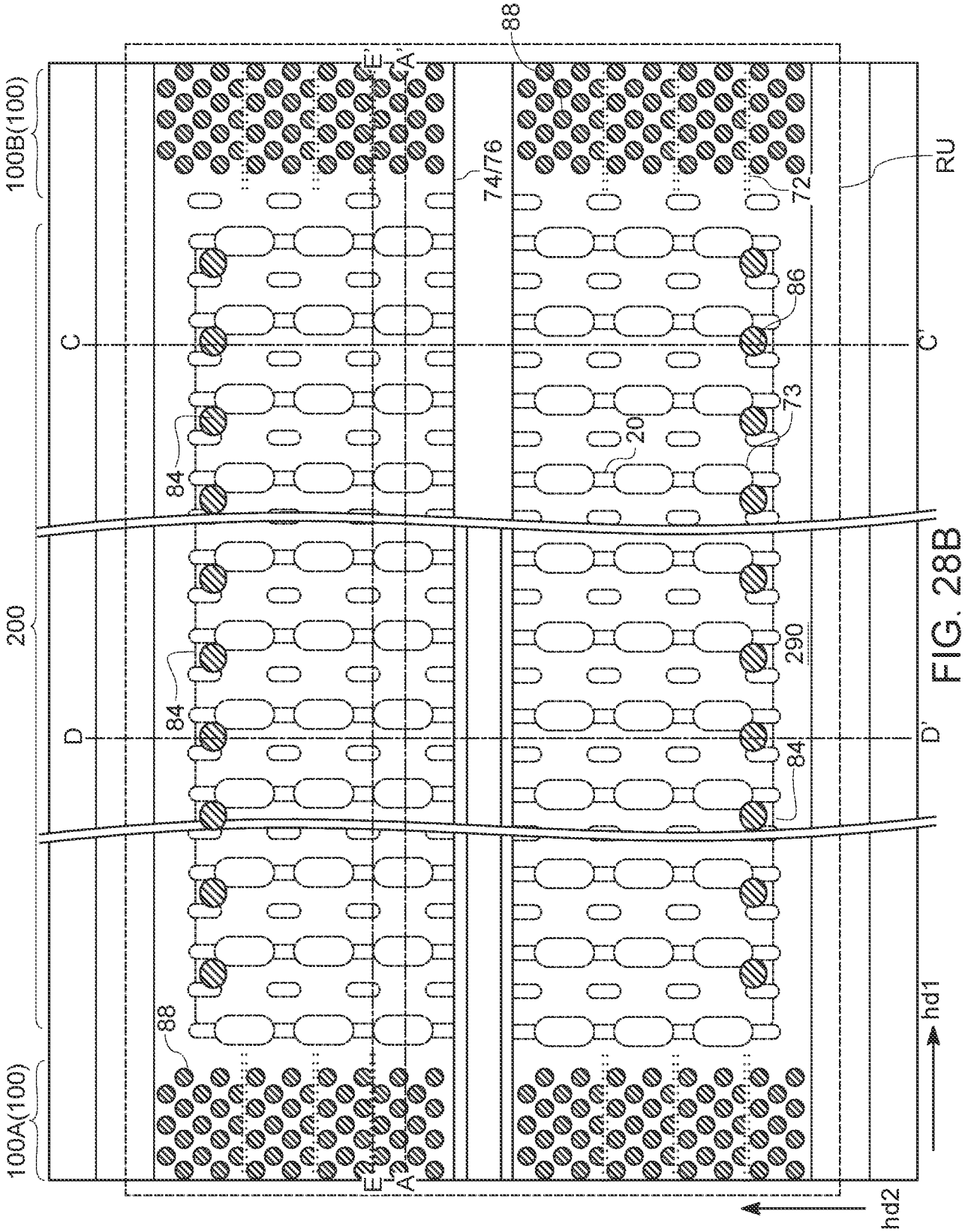

88
E
E'
A
A'
74/76
72
RU
100B(100)
C
C'
86
73
20
84
200
290
D
D'
84
84
88
100A(100)
E
E'
A
A'
hd1
hd2

FIG. 28B

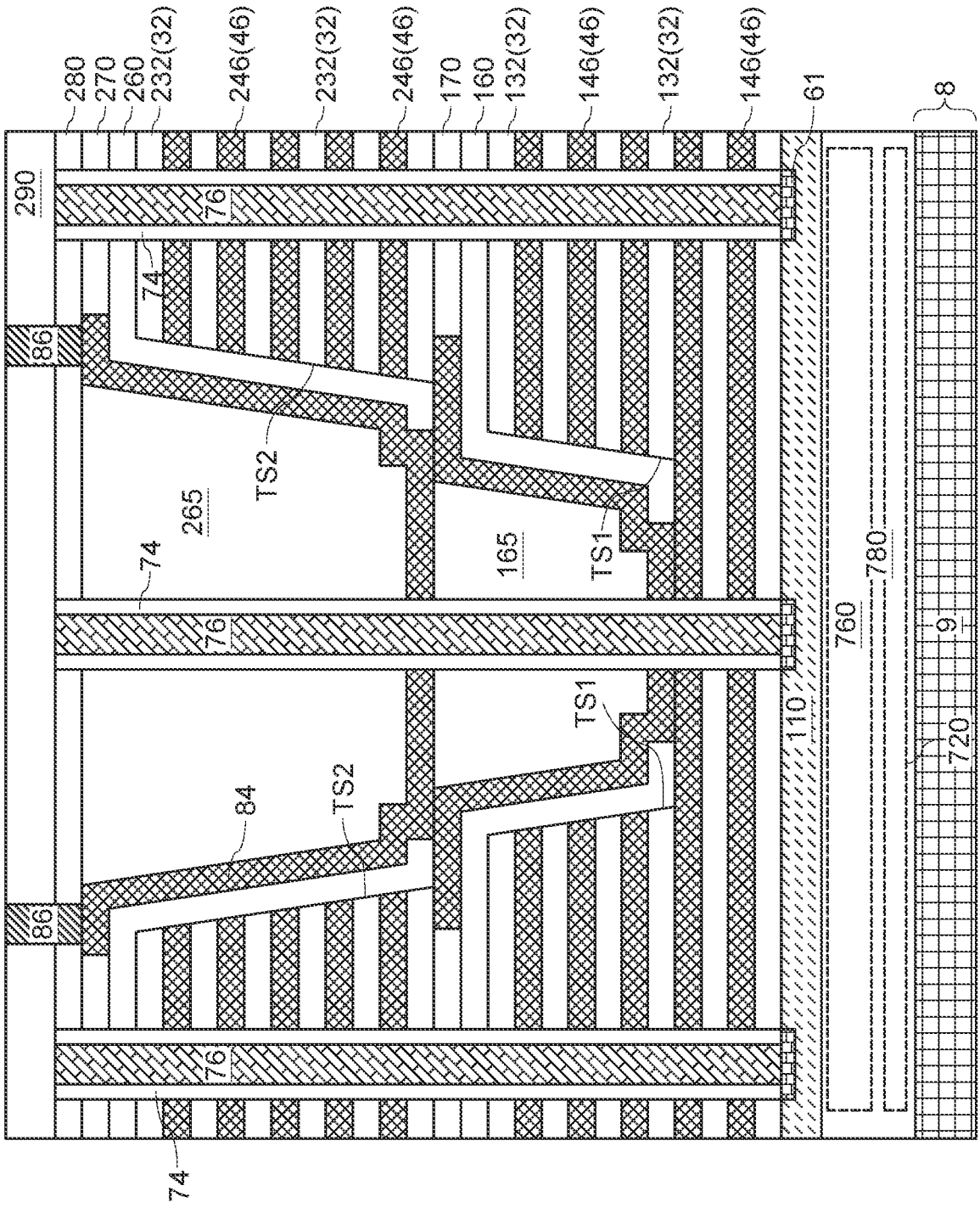

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
290
76
74
86
TS2
265
165
TS1
780
760
9
110
720
84
74

FIG. 28C

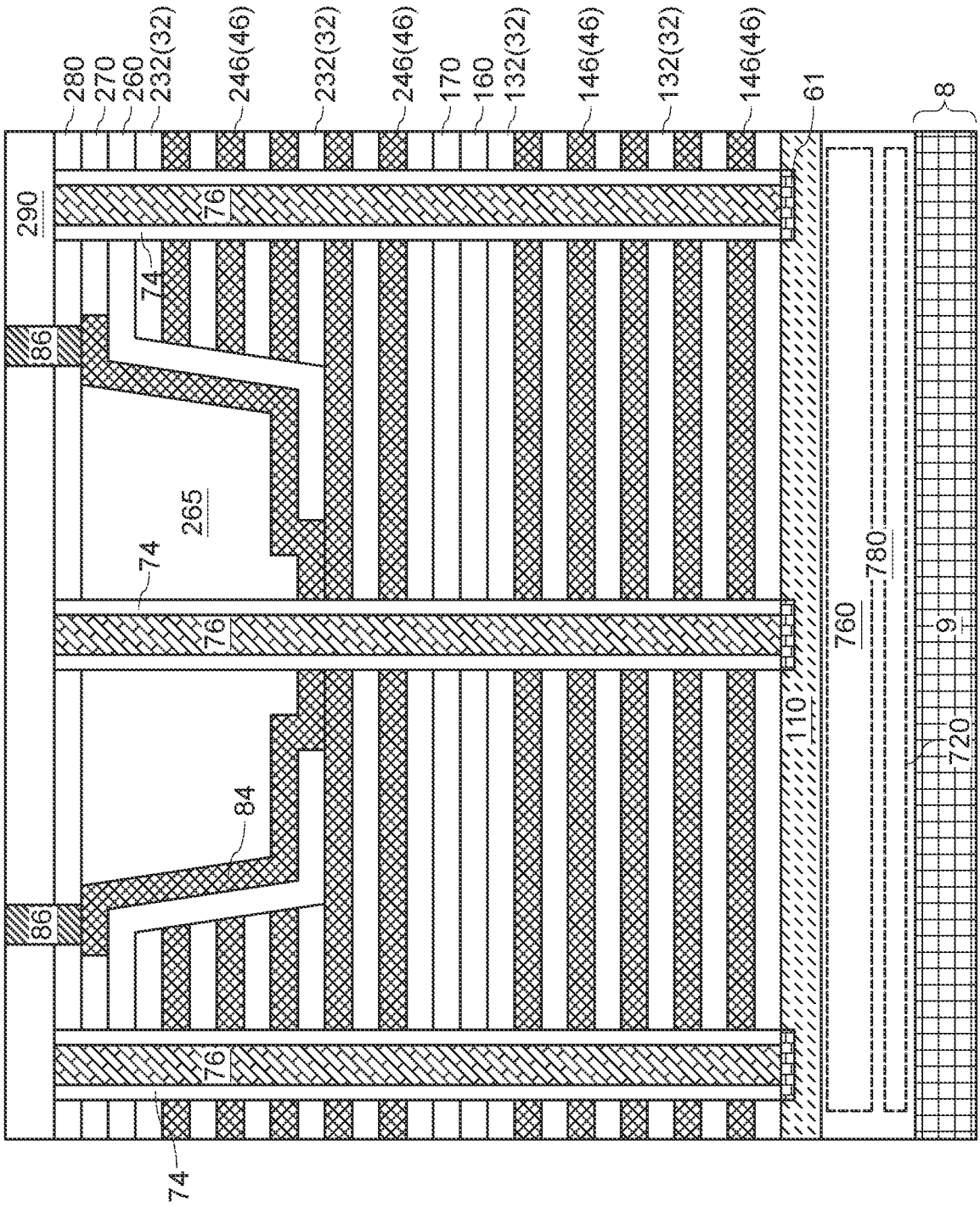
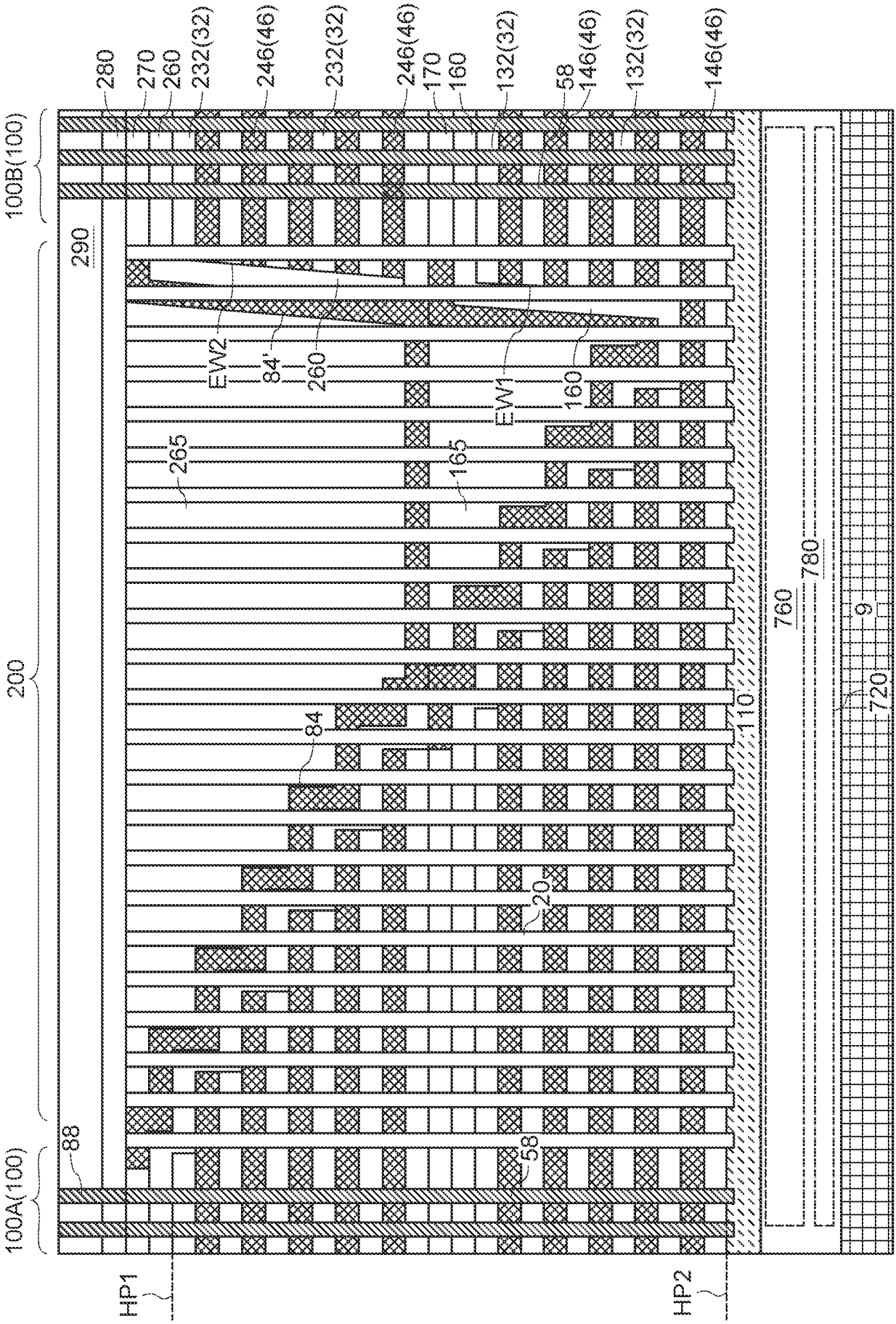

280
270
260
232(32)
246(46)
232(32)
246(46)
170
160
132(32)
146(46)
132(32)
146(46)
61
8
290
76
74
86
265
74
76
84
86
76
74
110
760
780
9
720

FIG. 28D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260
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246(46)
232(32)
246(46)
170
160
132(32)
58
146(46)
132(32)
146(46)
100B(100)
290
EW2
84'
260
EW1
160
265
165
200
84
110
205
760
780
9
720
88
58
100A(100)
HP1
HP2

FIG. 28E

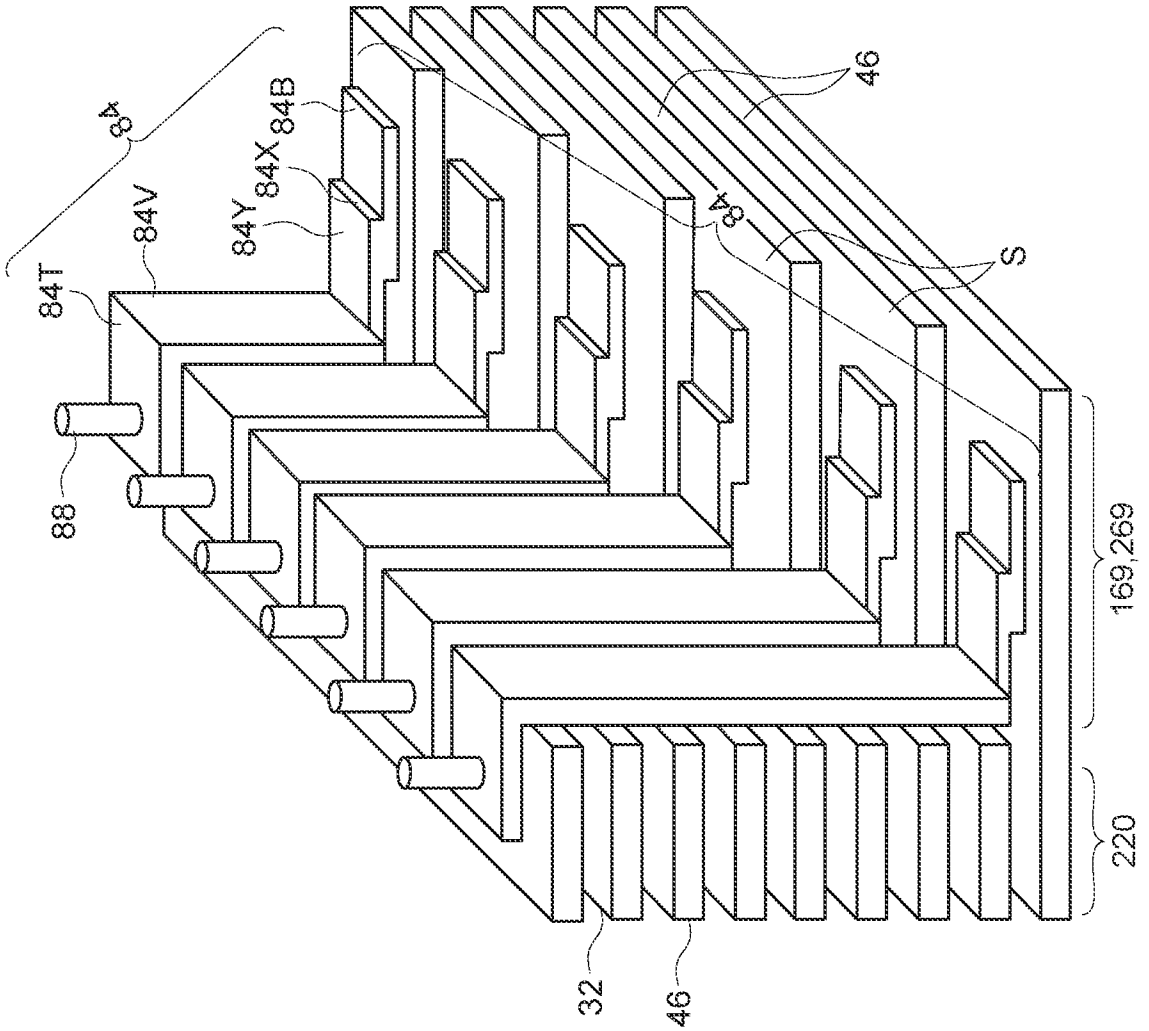

FIG. 28F

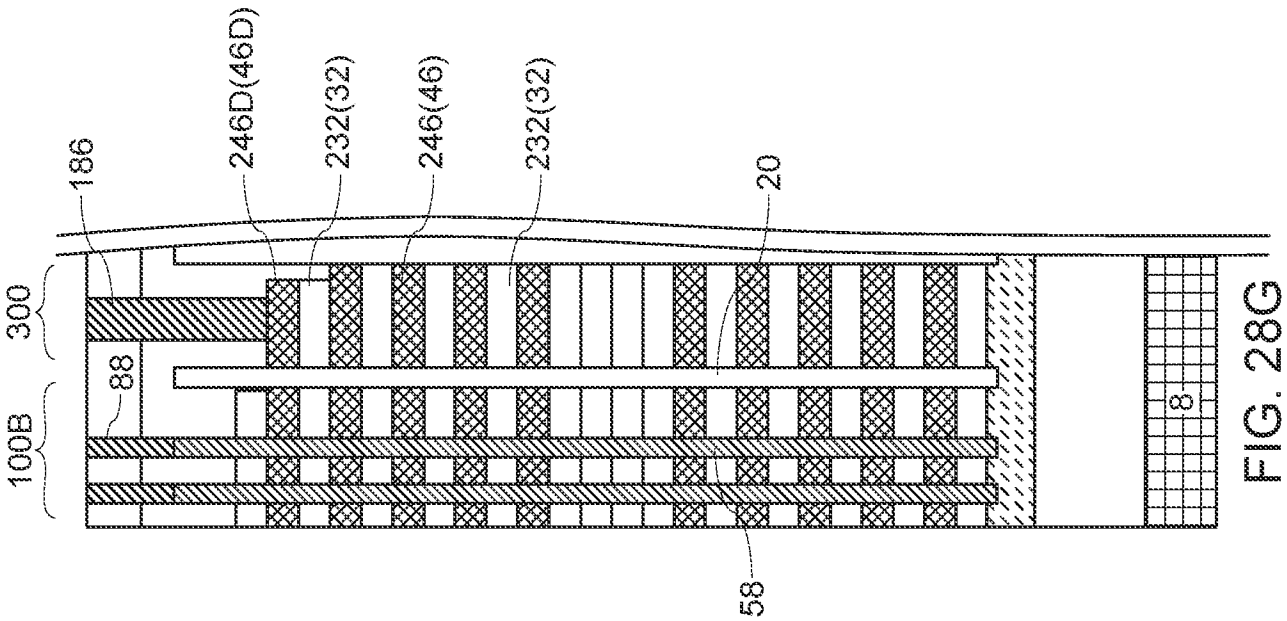

FIG. 28G

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/011257

A. CLASSIFICATION OF SUBJECT MATTER

H10B 43/27(2023.01)i; **H10B 43/35**(2023.01)i; **H10B 43/50**(2023.01)i; **H10B 43/10**(2023.01)i; **H10B 41/27**(2023.01)i; **H10B 41/35**(2023.01)i; **H10B 41/50**(2023.01)i; **H10B 41/10**(2023.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H10B 43/27(2023.01); G11C 11/22(2006.01); H01L 21/48(2006.01); H01L 23/522(2006.01); H01L 27/105(2006.01); H01L 27/11524(2017.01); H01L 27/11556(2017.01); H01L 27/11582(2017.01); H01L 27/11597(2017.01); H10B 69/00(2023.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: tapered sidewall, cavity, stepped surface, insulating liner, electrically conductive strip

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2023-027786 A1 (SANDISK TECHNOLOGIES LLC) 02 March 2023 (2023-03-02) paragraphs [0069], [0098], [0155]; claims 1, 15; and figures 1C, 2-3A, 4A, 7-12A, 14.	1-20
A	US 2021-0407569 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 30 December 2021 (2021-12-30) figures 25A-25D.	1-20
A	KR 10-2017-0139390 A (SAMSUNG ELECTRONICS CO., LTD.) 19 December 2017 (2017-12-19) figure 12.	1-20
A	US 2018-0315758 A1 (ASM IP HOLDING B.V.) 01 November 2018 (2018-11-01) figures 2-10.	1-20
A	US 2023-0023523 A1 (SANDISK TECHNOLOGIES LLC) 26 January 2023 (2023-01-26) paragraph [0235].	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2024	**30 April 2024**

Name and mailing address of the ISA/KR	Authorized officer
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2024/011257

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