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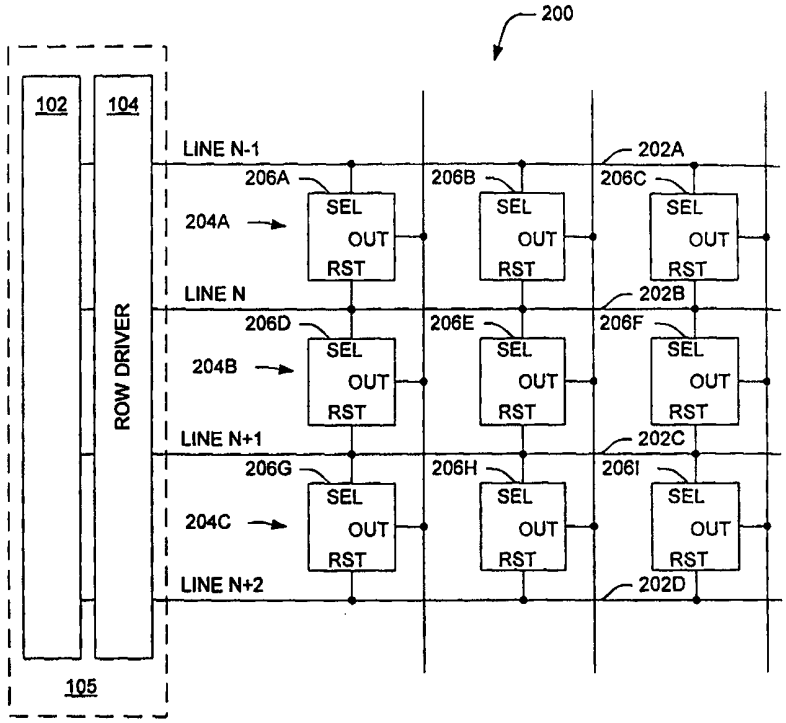
(54) Title: A SINGLE CONTROL LINE FOR PROVIDING SELECT AND RESET SIGNALS TO TWO ROWS OF AN IMAGE SENSOR

(57) Abstract

A digital imaging system, such as an active pixel sensor (APS) system, includes an array of sensors (200) arranged into lines that form rows and columns. Each sensor (206) in the array includes a photosensor that collects electric charge when exposed to light. Each sensor (206) also includes a select circuit (214) that generates an output signal indicating the amount of charge collected by the photosensor during a given time, and a reset circuit (216) that clears collected charge from the sensor (206) at a selected time. The APS system also includes a line decoder circuit (105) that produces select and reset signals and delivers the signals to the select circuits over control lines (202). Each control line (202) connects to two adjacent lines, e.g., rows or columns, of the array (200), delivering a select signal to the image sensors (206) in one of the two lines, and delivering a reset signal to the image sensors (206) in the other line.



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A single control line for providing select and reset signals to two rows of an image sensor

Technological Field

The invention relates to digital imaging devices, such as active pixel sensor and CCD arrays.

Background

Digital imaging devices such as active pixel sensor (APS) and charge-coupled device (CCD) cameras include many image sensors arranged into arrays of columns and rows. Each image sensor collects electrical charge when exposed to light. Control signals provided to the image sensors periodically enable the sensors to transfer the collected charge, or voltage-mode signals derived from the charge, to an imaging circuit.

Summary

The inventor has recognized a desire to reduce a necessary number of control lines for a given application that drive the image sensors in a digital imaging array. One technique for reducing the number of control lines is to provide multiple control signals on lines that are shared by adjacent rows of sensors in the array. Many advantages result, including greater space resolution in the sensor array, reduced interlevel (*e.g.*, metal to polysilicon) contacts in the APS circuit, and higher quantum efficiency for the sensors.

In one aspect, the invention features a digital imaging device that includes a plurality of image sensors arranged into an array of lines including rows and columns. At least one output line connects to the image sensors. A control line connects electrically to at least two different image sensors in two different lines.

The control line delivers a select signal to at least one image sensor in one of the lines and delivers a reset signal to at least one image sensor the other line. The select signal causes the image sensor in the first line to place an output signal on the output line, and the reset signal clears information from the image sensor in the second line.

In another aspect, the invention features a digital imaging system that includes a plurality of image sensors arranged into an array of lines forming rows and columns. Each of the image sensors includes a photosensor that collects electric charge when exposed to light, a select circuit that generates an output signal indicating the amount of electric charge collected by the photosensor, and a reset circuit that removes collected charge from the photosensor. The system also includes a line decoder circuit. This circuit includes a plurality of control lines and a control circuit that delivers select signals and reset signals over the control lines. Each control line connects to image sensors in two lines of the array. Each control line delivers a select signal to the select circuits in one of the two lines and delivers a reset signal to the reset circuits in the other of the two lines.

In another aspect, the invention features a method for use in capturing an image with a plurality of image sensors arranged into an array of lines forming rows and columns. A select signal is delivered to at least one image sensor in a first one of the lines, and a reset signal is delivered to at least one image sensor in a second one of the lines. The select signal and the reset signal are delivered over a single control line. In response to the select signal, an output signal is delivered from the image sensor in the first line, and information is cleared from the image sensor in the

second line.

Other embodiments and advantages are apparent from the following description and from the claims.

Description of the Drawings

FIG. 1 is a schematic diagram of a conventional active pixel sensor (APS) circuit.

FIGS. 2 and 4 are schematic diagrams of two types of conventional active pixel sensors.

FIGS. 3 and 5 are timing diagrams for control signals delivered to the active pixel sensors of FIGS. 2 and 4.

FIG. 6 is a schematic diagram of an APS circuit in which a single control line is shared by two adjacent rows of sensors in the array.

FIGS. 7 and 9 are schematic diagrams of two types of active pixel sensors for use in APS circuits like that of FIG. 6.

FIGS. 8 and 10 are timing diagrams for control signals delivered to the active pixel sensors of FIGS. 7 and 9.

FIG. 11 is a schematic diagram of a logic circuit that drives a shared control line.

Detailed Description

A conventional APS circuit 100 is shown in FIG. 1. In this circuit 100, a timing controller 102 and a row driver 104 together form a control circuit 105 that generates two types of control signals, known as select signals and reset signals, which control the readout of collected charge from each sensor 110A-I in the APS array 115. The control circuit 105 provides two control lines, a select line 106A-C and a reset line 108A-C, for each row 112A-C of sensors in the array 115. Each sensor 110A-I converts the collected charge into a signal and

delivers this signal to one of several column lines 114A-C when the corresponding select line 106A-C is asserted. All collected charge is cleared from the sensor when the corresponding reset line 108A-C is asserted.

FIG. 2 shows a typical active pixel sensor 120. The sensor 120 includes a photosensitive element, *e.g.*, photodiode 122 that collects charge when exposed to light. The charge is delivered at selected times to an output driver 124. The output driver 124 includes two transistors 126, 128 that deliver an output signal to the corresponding column line 130. One of these transistors is a source-follower transistor 126, the source of which connects to a power supply line (Vdd), and the gate of which connects to the cathode of the photodiode 122. The other transistor is a switching transistor 128 that connects the drain of the source-follower transistor 126 to one of the column lines 130. The gate of the switching transistor 128 connects to one of the select lines 132 extending from the control circuit 105.

The sensor 120 also includes a reset transistor 134 connected between the cathode of the photodiode 122 and the power supply line (Vdd). The gate of this transistor 134 connects to one of the reset lines 136 extending from the control circuit.

In operation, charge collected in the photodiode 122 diffuses into the gate of the source-follower transistor 126 and creates an output voltage on the column line 130 when the switching transistor 128 is activated by the select line. The reset transistor 134 begins conducting and thus clears collected charge from the photodiode 122 when the reset line 136 is asserted.

FIG. 3 shows the relative timing of the select and reset signals for two adjacent rows of sensors in the APS array. Each row of sensors has a corresponding select line, which delivers a select pulse 140A-B to each sensor

in the row. Each row also has a corresponding reset line, which delivers a reset pulse 142A-B to each sensor in the row during the corresponding select pulse 140A-B. Charge that collects in the photodiode 122 during the portion of the select pulse 140A-B that follows the reset pulse 142A-B is treated as background noise. The charge that collects in the photodiode during the portion of the select pulse 140A-B that precedes the reset pulse 142A-B is attributable both to background noise and to the incoming image. The difference between the output signals generated during these two time periods indicates how much of the collected charge is attributable to the incoming image. The time interval between the rising or falling edge of the select signal 140A on one select line and the corresponding rising or falling edge of the select signal 140B on an adjacent select line is known as the "row clock period."

FIG. 4 shows another typical APS sensor 145, which acts essentially as a single-stage charge-coupled device (CCD). In this sensor 145, a photogate 144 and a charge transfer gate 146 replace the photodiode of FIG. 2. Four control signals, including a select signal, a reset signal, a photogate (PG) signal, and a charge transfer (TX) signal, are provided for each row of sensors in the array. FIG. 5 shows the relative timing of the select, reset, and PG signals for two adjacent rows of sensors.

FIG. 6 shows an APS circuit 200 in which the number of control lines is reduced by almost a factor of two over conventional APS circuits. Instead of providing separate select and reset lines for each row of sensors, the APS circuit 200 includes control lines 202A, 202B, 202C, respectively associated with each row of sensors. One additional control line 202B is also needed.

The sensors are arranged in an array formed by lines including rows and columns 204A, 204B, 204C. Each

control line 202B, 202C that is connected between two sensor rows 204B, 204C is shared by all of the sensors on those two adjoining rows. In particular, a shared control line 202B delivers a select signal to sensors in one row 204B and delivers a reset signal to sensors in another row 204A.

FIGS. 7 and 9 show alternative image sensors 210, 220 for use in the shared-line APS array 200. A photodiode 212 serves as the image sensing device in one of these sensors 210. A single-stage CCD, embodied as a photogate 222 and a charge transfer transistor 224, serves as the image sensing device in the other sensor 220. The reset circuit structures for these sensors 210, 220 are similar to those for the conventional sensors of FIGS. 2 and 4. However, the switching transistor 214 and the reset transistor 216 do not connect to a separate dedicated select line and a dedicated reset line, as shown in FIGS. 2 and 4. Rather, these transistors 214, 216 connect to shared control lines 218, 219. Each of these delivers both select signals and reset signals to sensors in two rows of the APS array. The single-stage CCD sensor 220 (FIG. 9) also receives a photogate signal (PG) and a charge transfer signal (TX) like those described above.

FIG. 8 shows the relative timing of the control signals on the shared control lines 218, 219 for the sensor 210 of FIG. 7. The upper control line 218 provides one or more select pulses 230 to the switching transistor 214. During the select pulse 230, the lower control line 219 delivers a reset pulse 232 to the reset transistor 216. The collected charge is cleared from the photodiode 212 during the reset pulse 232. The lower control line 219 later provides a select pulse 234 that activates the sensors in another row of the array. The centers of the reset pulse 232 and the select pulse 234 on each shared

control line 219 are separated by a time interval that is equal to approximately one row clock period. In some implementations, the select pulse 230 on one control line 218 is deasserted during the corresponding reset pulse 232 on an adjacent control line 219, as shown by the dashed lines in FIG. 8.

FIG. 10 shows the relative timing of the photogate signal PG and the control signals provided on the shared control lines 218, 219 for the sensor 220 of FIG. 9. The lower control line 219 delivers a reset pulse 242 to the reset transistor, and then the upper control line 218 delivers one or more select pulses 242 to the switching transistor. During the select pulse 242, a photogate pulse 244 is delivered to the photogate 222, during which the photogate 222 transfers charge to the output driver. The lower control line 219 later delivers one or more select pulses 246 to the sensors in another row of the array.

FIG. 11 shows a logic circuit 250 that is used to generate control signals on a shared control line (LINE N). This circuit 250 is added to the conventional control circuit 105 of FIG. 1 to replace a pair of select and reset lines with a single shared control line. The logic circuit 250 receives standard select pulse and row select signals for a particular row N [SELECT(N), ROW_SELECT(N)] from a conventional row driver. The circuit 250 also receives a standard reset pulse for an adjacent row N-1 [RESET(N-1)]. An AND gate 252 receives the SELECT(N) and ROW_SELECT(N) signals as input, and an OR gate 254 receives the RESET(N-1) signal and the output of the AND gate 252 as input. The output of the OR gate drives a control line (LINE N) that is shared by the sensors in row N and row N-1 of the array. The control

line is asserted when both the ROW_SELECT(N) and the SELECT(N) signals are asserted and when the RESET(N-1) signal is asserted.

Other embodiments are within the scope of the following claims. For example, while the invention has been described in terms of an APS array, the invention is useful in other pixel based imaging systems. The invention also is not limited to the use of gated transistors, such as field effect transistors (FETs). Other switching devices, including other types of transistors, such as bipolar junction transistors, are used in some implementations. Also, while this system is described as being used for one control for two rows, it should be understood that the control could be shared between columns instead.

What is claimed is:

1. A digital imaging device comprising:

a plurality of image sensors arranged into an array of lines including rows and columns;

at least one output line connected to the image sensors; and

a control line connected electrically to at least two different image sensors in two different lines and configured to deliver a select signal to at least one image sensor in a first one of the lines and to deliver a reset signal to at least one image sensor in a second one of the lines, where the select signal causes the image sensor in the first line to place an output signal on the output line, and where the reset signal clears information from the image sensor in the second line.

2. The digital image device of claim 1, wherein the lines to which the control line connects are rows.

3. The digital image device of claim 1, wherein the lines to which the control line connects are columns.

4. The digital imaging device of claim 1, wherein the image sensor includes a photosensor, such as a photodiode or a photogate.

5. The digital imaging device of claim 4, wherein the image sensor in the first line includes a select switch connected between the photosensor and the control line and configured to conduct when the select signal is received.

6. The digital imaging device of claim 5, wherein the select switch includes a transistor.

7. The digital imaging device of claim 4, wherein the image sensor in the second line includes a reset switch connected between the photosensor and the control line and configured to conduct when the reset signal is received.

8. The digital imaging device of claim 7, wherein the reset switch includes a transistor.

9. The digital imaging device of claim 1, further comprising a control circuit connected to the control line and configured to produce the reset signal and the select signal.

10. The digital imaging device of claim 9, wherein the control circuit is configured to produce the reset signal before producing the select signal.

11. The digital imaging device of claim 9, wherein the control circuit is configured to produce the reset signal and the select signal separated by a time increment approximately equal to a row clock period of the imaging device.

12. A digital imaging system comprising:

a plurality of image sensors arranged into an array of lines including rows and columns, each image sensor including:

a photosensor configured to collect electric charge when exposed to light;

a select circuit coupled to the photosensor to generate an output signal indicating an amount of electric charge collected by the photosensor; and

a reset circuit coupled to the photosensor to remove collected charge from the photosensor; and

a line decoder circuit including:

a control circuit configured to produce select signals and reset signals; and

a plurality of control lines, each of which is connected to image sensors in two of the lines, and each of which is configured to deliver one of the select signals to the select circuits of image sensors in one of the two lines and to deliver one of the reset signals to the reset circuits of image sensors in the other of the two lines.

13. The digital imaging system of claim 12, wherein the control circuit is configured to generate the reset signal for each control line before generating the select signal for the control line.

14. The digital imaging system of claim 12, wherein the select circuit in each image sensor includes a source-follower transistor coupled to a switching transistor.

15. The digital imaging system of claim 14, wherein the gates of each of the switching transistors in one of the rows are driven by a select signal delivered by one of the control lines.

16. The digital imaging system of claim 14, wherein the source-follower transistor is configured to convert electric charge collected by the photosensor into an output voltage.

17. The digital imaging system of claim 12, wherein the reset circuit in each image sensor includes a switching transistor.

18. The digital imaging system of claim 17, wherein the gates of each of the switching transistors in one of the lines are driven by a reset signal delivered by one of the control lines.

19. The digital imaging system of claim 12, wherein the lines to which each control line connects are rows.

20. The digital imaging system of claim 12, wherein the lines to which each control line connects are columns.

21. A method for use in capturing an image with a plurality of image sensors arranged into an array of lines including rows and columns, the method comprising:

delivering a select signal to at least one image sensor in a first one of the lines and a reset signal to at least one image sensor in a second one of the lines over a single control line;

delivering an output signal from the image sensor in the first one of the lines in response to the select signal; and

clearing information from the image sensor in the second one of the lines in response to the reset signal.

22. The method of claim 21, wherein delivering the output signal from the image sensor in the first line includes delivering the select signal to a select switch in the image sensor and causing the select switch to conduct.

23. The method of claim 21, wherein clearing information from the image sensor in the second line includes delivering the reset signal to a reset switch in the image sensor and causing the reset switch to conduct.

24. The method of claim 21, further comprising delivering the reset signal over the control line before delivering the select signal.

25. The method of claim 21, further comprising delivering the reset signal and the select signal separated by a time increment approximately equal to a row clock period of the array of image sensors.

26. The method of claim 21, wherein the lines to which the control line connects are rows.

27. The method of claim 21, wherein the lines to which the control line connects are columns.

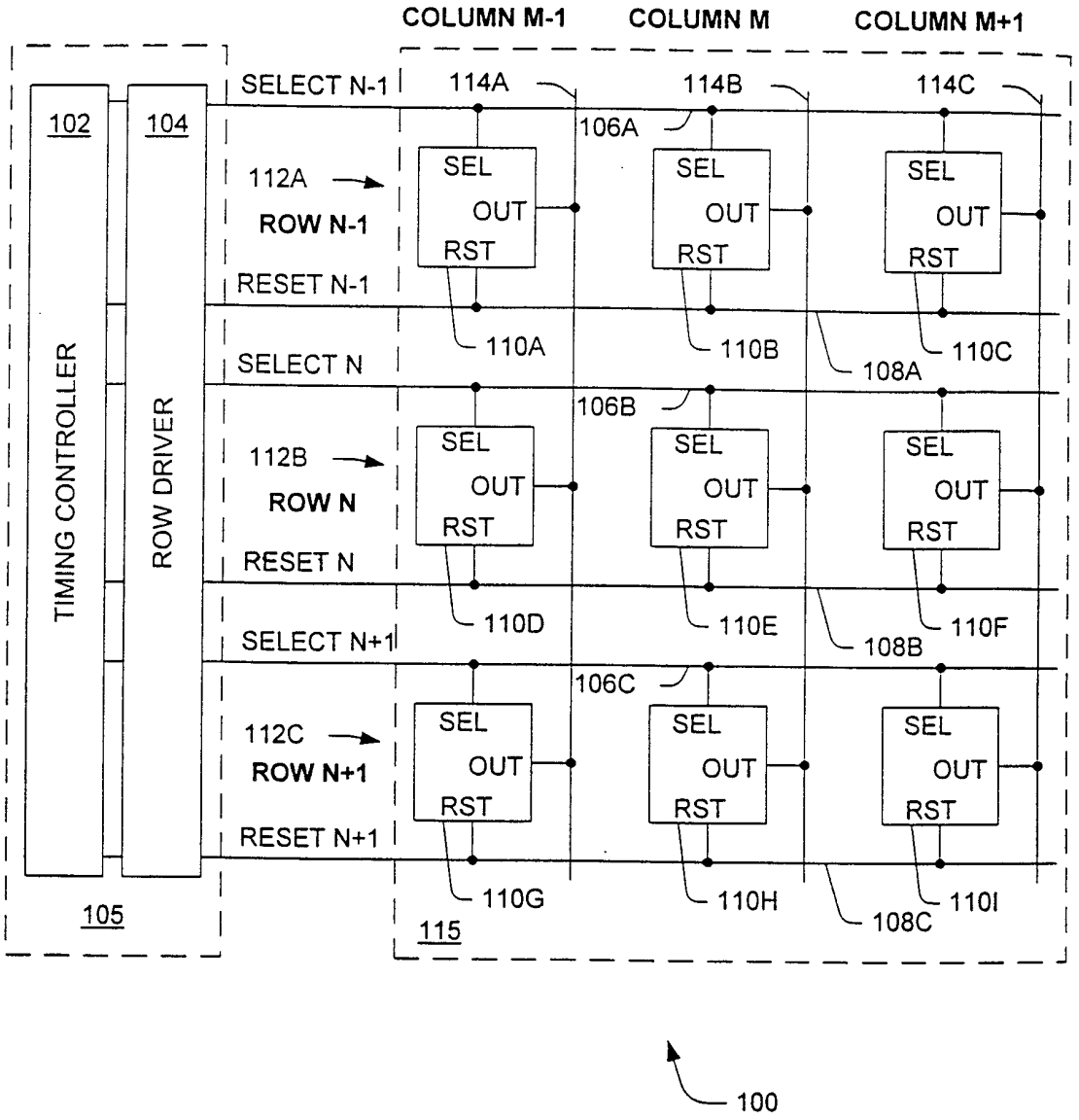
COLUMN M-1
COLUMN M
COLUMN M+1
SELECT N-1
SELECT N
SELECT N+1
RESET N-1
RESET N
RESET N+1
ROW N-1
ROW N
ROW N+1
112A
112B
112C
102
104
105
TIMING CONTROLLER
ROW DRIVER
114A
114B
114C
106A
106B
106C
SEL
OUT
RST
110A
110B
110C
110D
110E
110F
110G
110H
110I
108A
108B
108C
115
100

FIG. 1

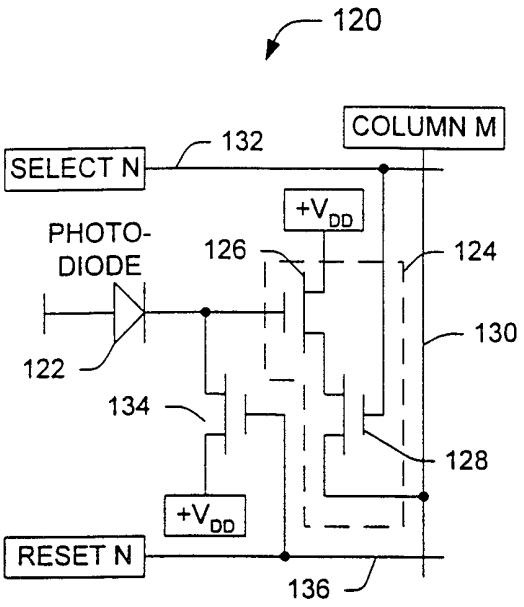

FIG. 2

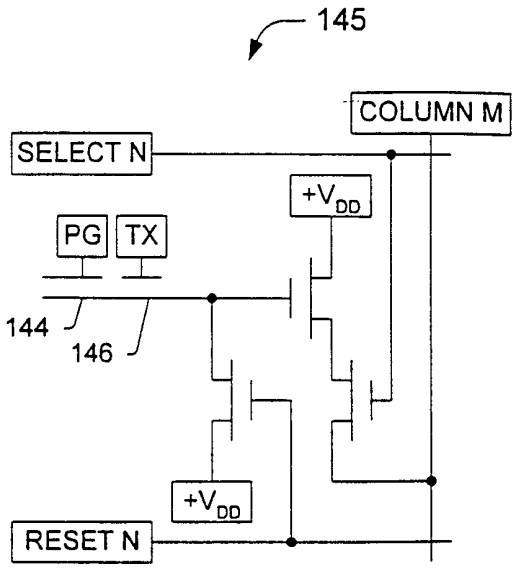

FIG. 4

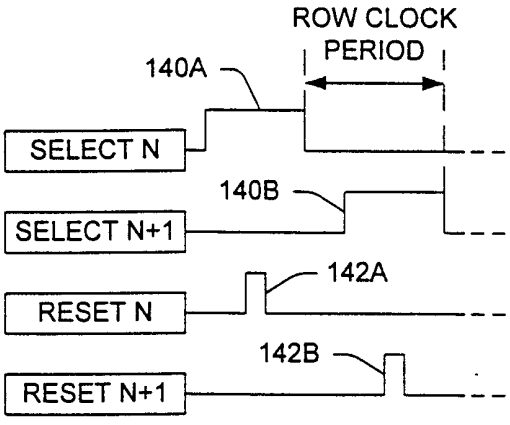

FIG. 3

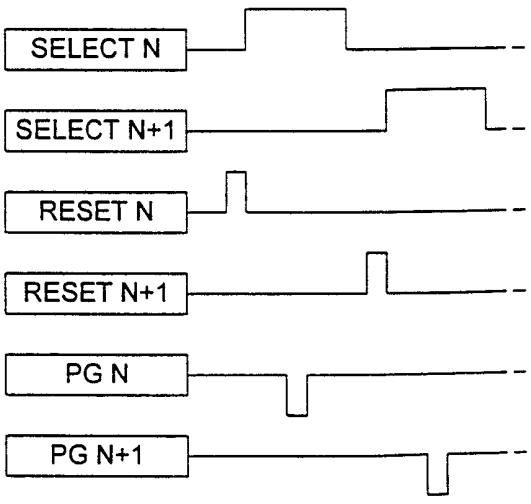

FIG. 5

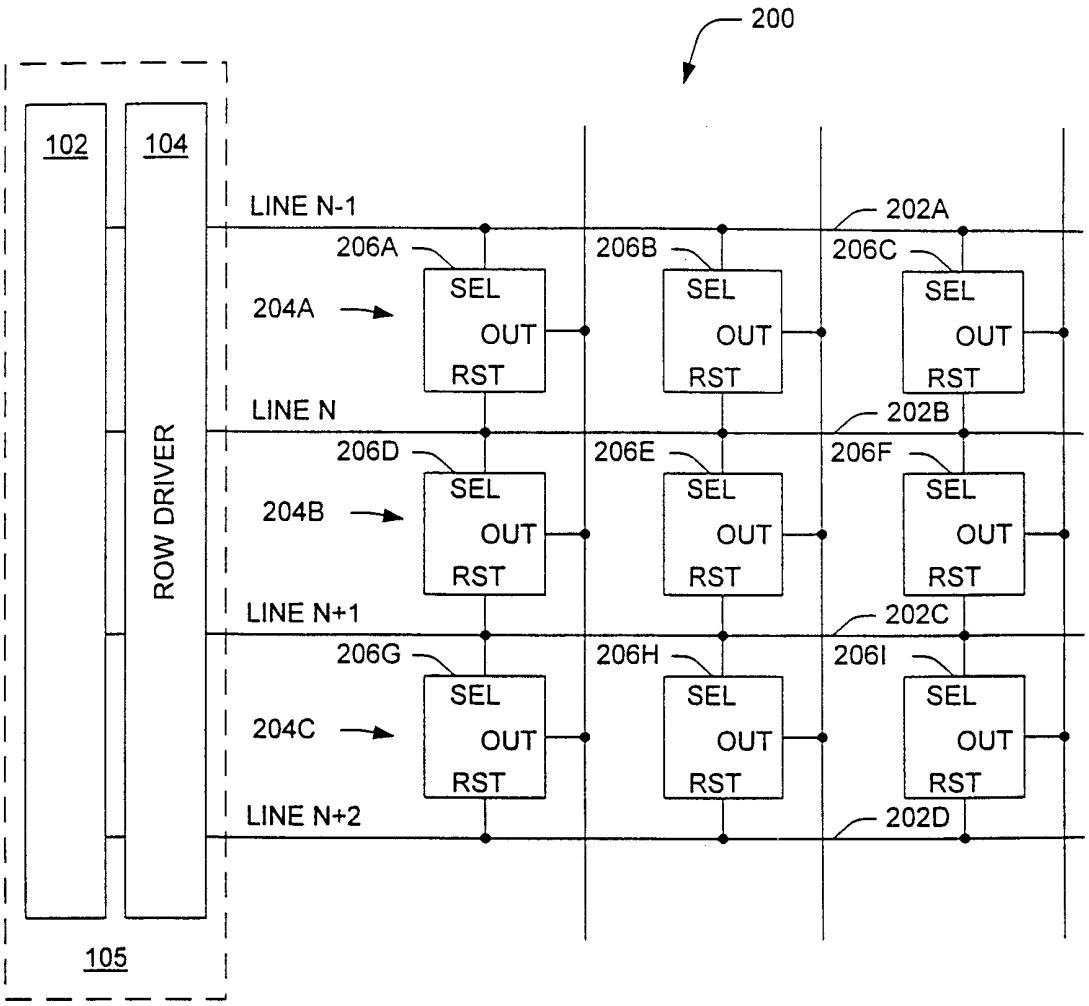
200
102
104
ROW DRIVER
105
LINE N-1
LINE N
LINE N+1
LINE N+2
202A
202B
202C
202D
206A
206B
206C
206D
206E
206F
206G
206H
206I
204A
204B
204C
SEL
OUT
RST

FIG. 6

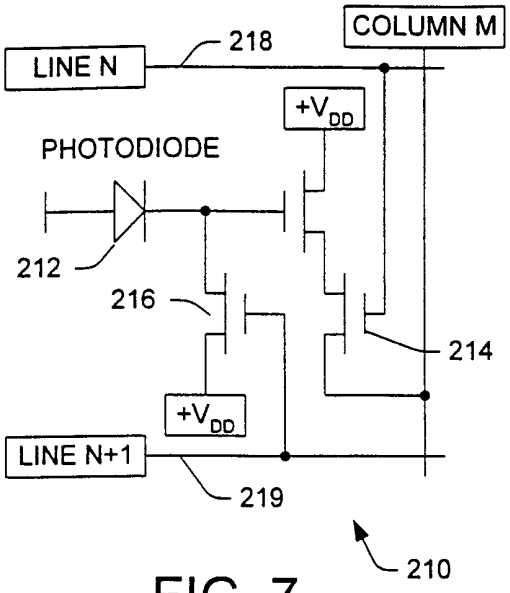

FIG. 7

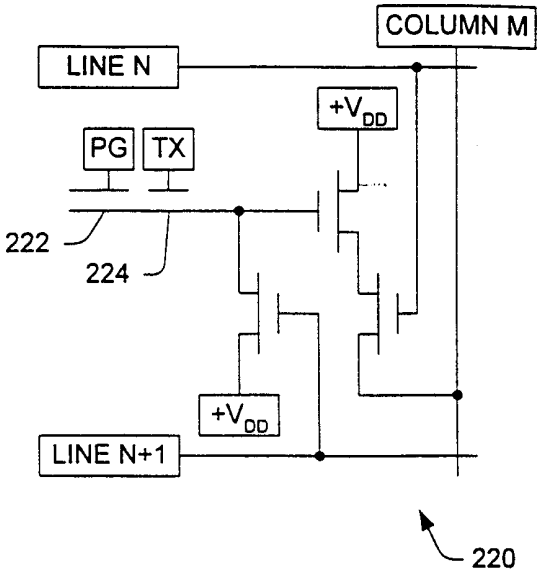

FIG. 9

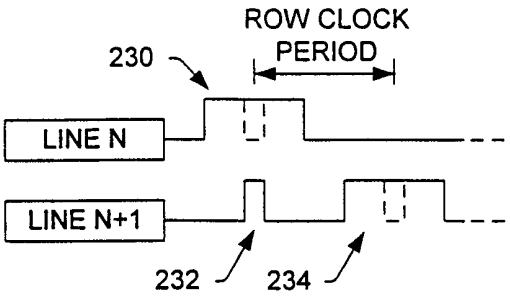

FIG. 8

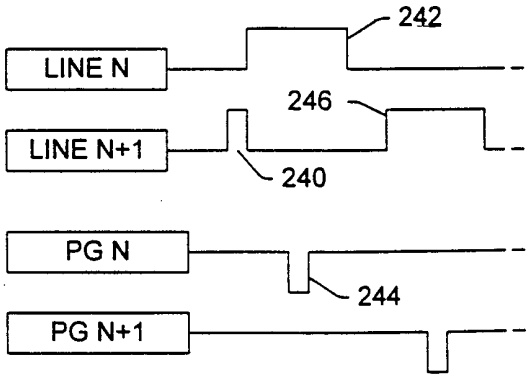

FIG. 10

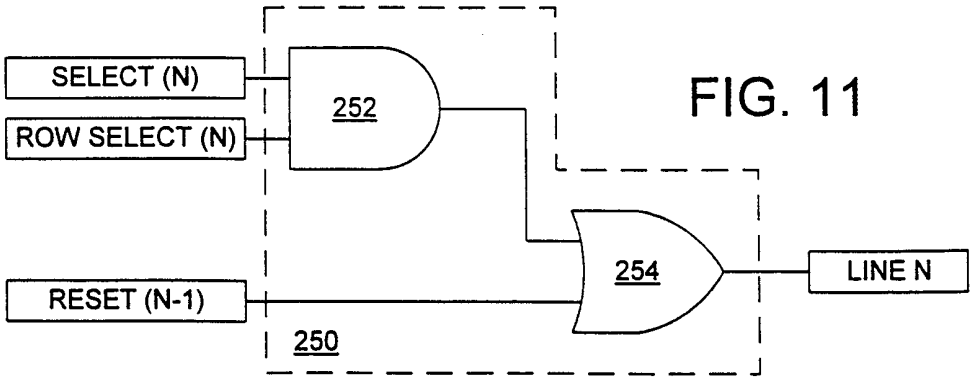

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/03473

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04N 5/335
US CL :250/208.1; 348/294, 302-304, 307-312, 314, 315.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 250/208.1; 348/294, 302-304, 307-312, 314, 315.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,572,257 A (CONRADS et al) 05 November 1996, see entire document.	1-27
A, P	US 5,763,909 A (MEAD et al) 09 June 1998, see entire document.	1-27
A, P	US 5,831,258 A (STREET) 03 November 1998, see entire document.	1-27
A, P	US 5,734,191 A (CHI et al) 31 March 1998, see entire document.	1-27

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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