United States Patent [19]

Doughty

[11] **3,749,837**

[45] **July 31, 1973**

[54] **ELECTRONIC MUSICAL TONE MODIFIER FOR MUSICAL INSTRUMENTS**

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[52] **U.S. Cl.** ..... **179/1 J,** 84/1.01, 84/1.03, 84/1.25

[51] **Int. Cl.** **H04r 3/00,** G10h 1/04

[58] **Field of Search** ..... 84/1.03, 1.25, 1.01, 84/1.24; 331/178; 332/16; 333/29; 179/1 J

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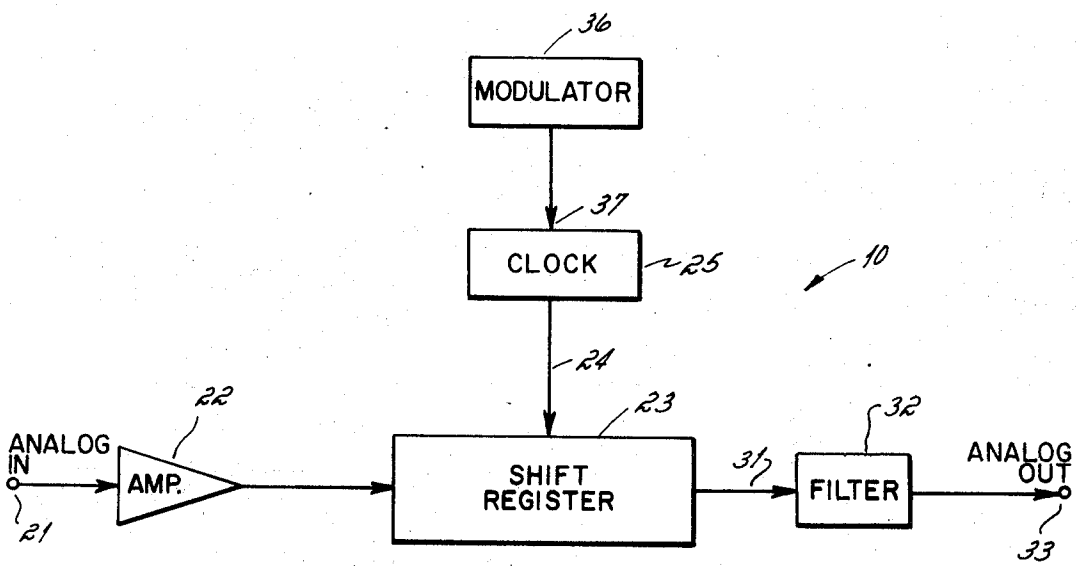
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Assistant Examiner—Stanley J. Witkowski
Attorney—James S. Hight, Donald F. Frei et al.

[57] **ABSTRACT**

A device for electrically modifying a musical tone by frequency modulation to provide effects such as the vibrato effect and the Leslie effect on the musical tone signal. The device employs a shift register through which electrical representations of the magnitude of an input signal are periodically sampled, stored, and shifted progressively through a shift register from the input to the output of the device which delays the signal. The trigger pulses which time the sampling and shifting functions of the device are frequency modulated to vary the time delay imposed, thus effecting a frequency modulation of the delayed input tone at the output of the device. In one embodiment, a digital shift register is employed which stores a digital representation of the magnitude of the signal and is connected between an analog-to-digital convertor at the input of the device and a digital-to-analog converter at the output of the device. Alternatively, a bucket-brigade type analog shift register is employed which directly stores discrete analog representations of sampled input values and shifts them progressively toward the output. Plural channel devices are provided wherein the time delays are modified differently so that when the outputs of the channel are combined, an enhanced effect is provided. In a two channel device, opposite phase relationships of the modulated trigger pulse signals provide a more realistic vibrato effect.

11 Claims, 5 Drawing Figures



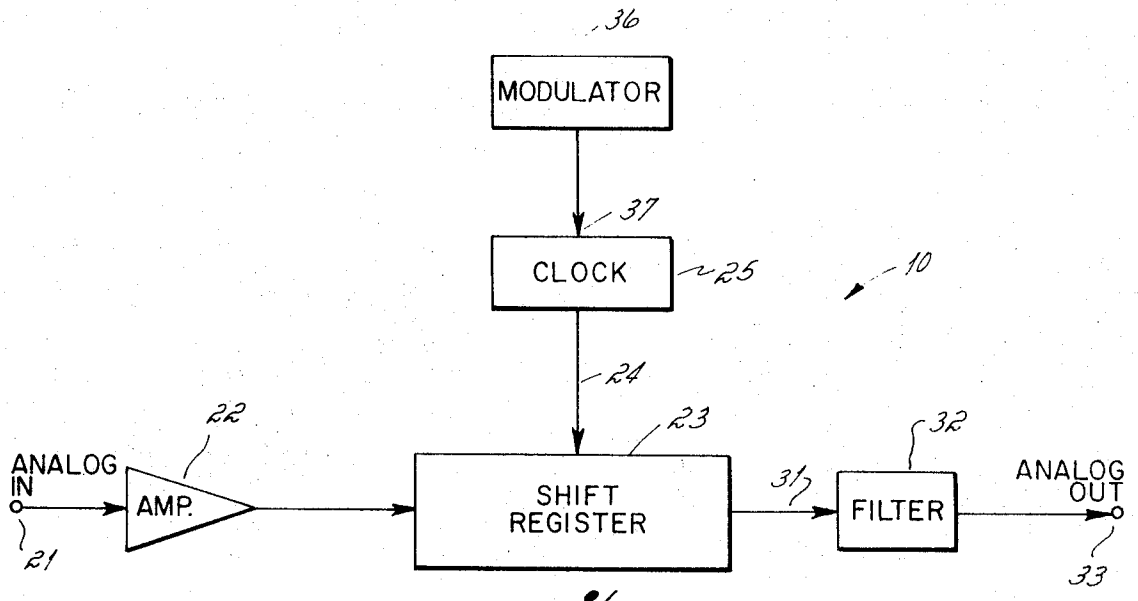

36
MODULATOR
37
CLOCK
25
10
24
22
23
32
ANALOG IN
AMP.
SHIFT REGISTER
31
FILTER
ANALOG OUT
21
33

Fig. 1

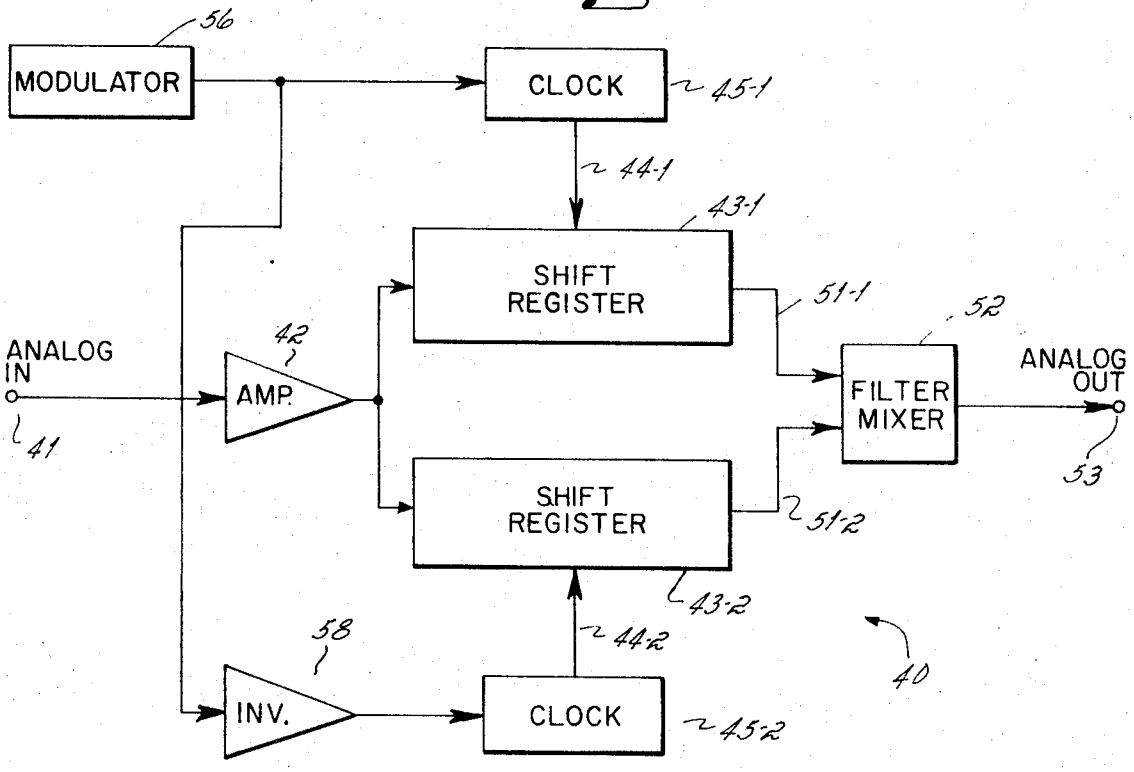

56
MODULATOR
CLOCK
45-1
44-1
43-1
SHIFT REGISTER
51-1
52
42
ANALOG IN
AMP.
FILTER MIXER
ANALOG OUT
41
53
SHIFT REGISTER
51-2
43-2
58
44-2
40
INV.
CLOCK
45-2

Fig. 2

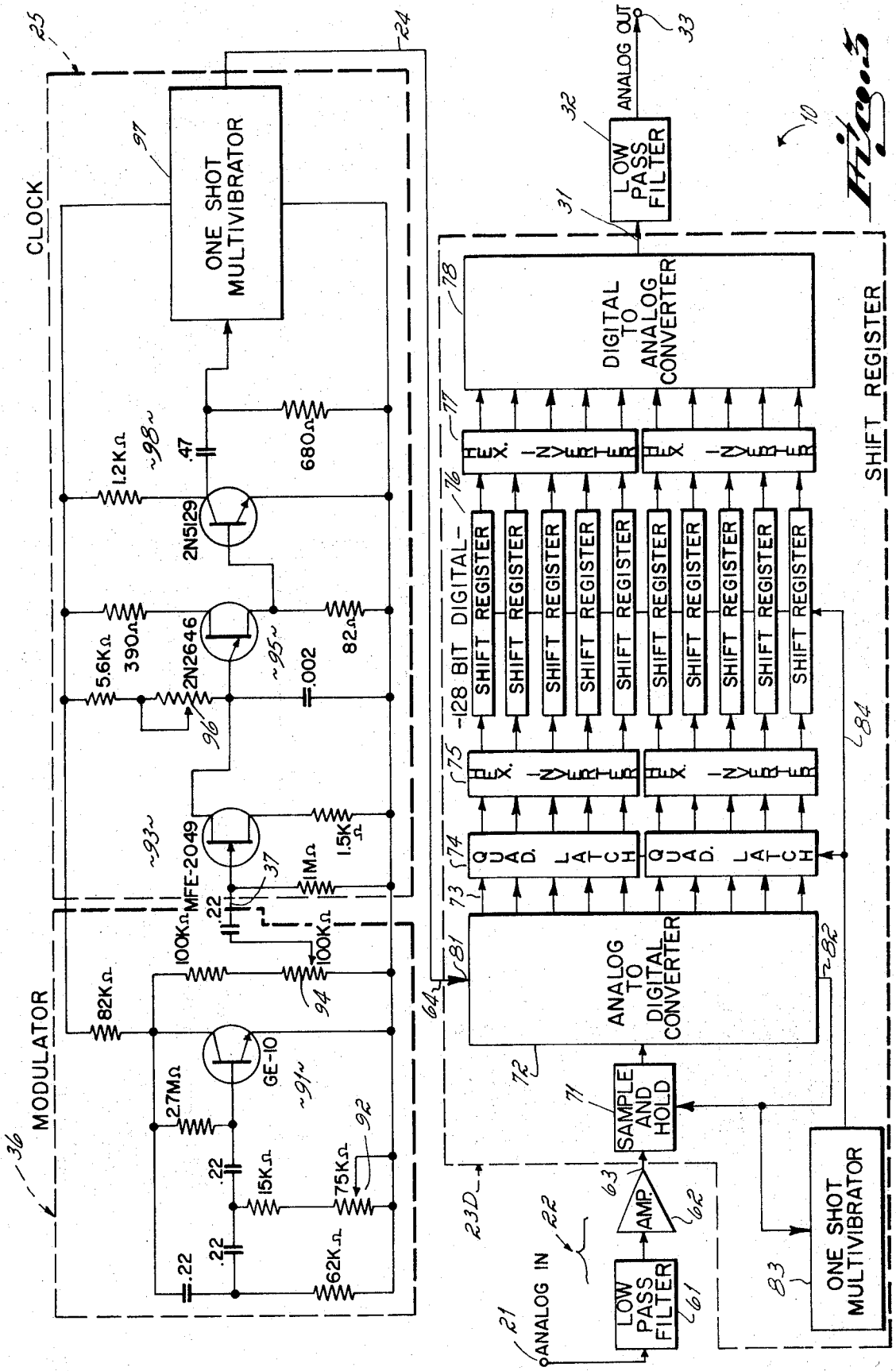
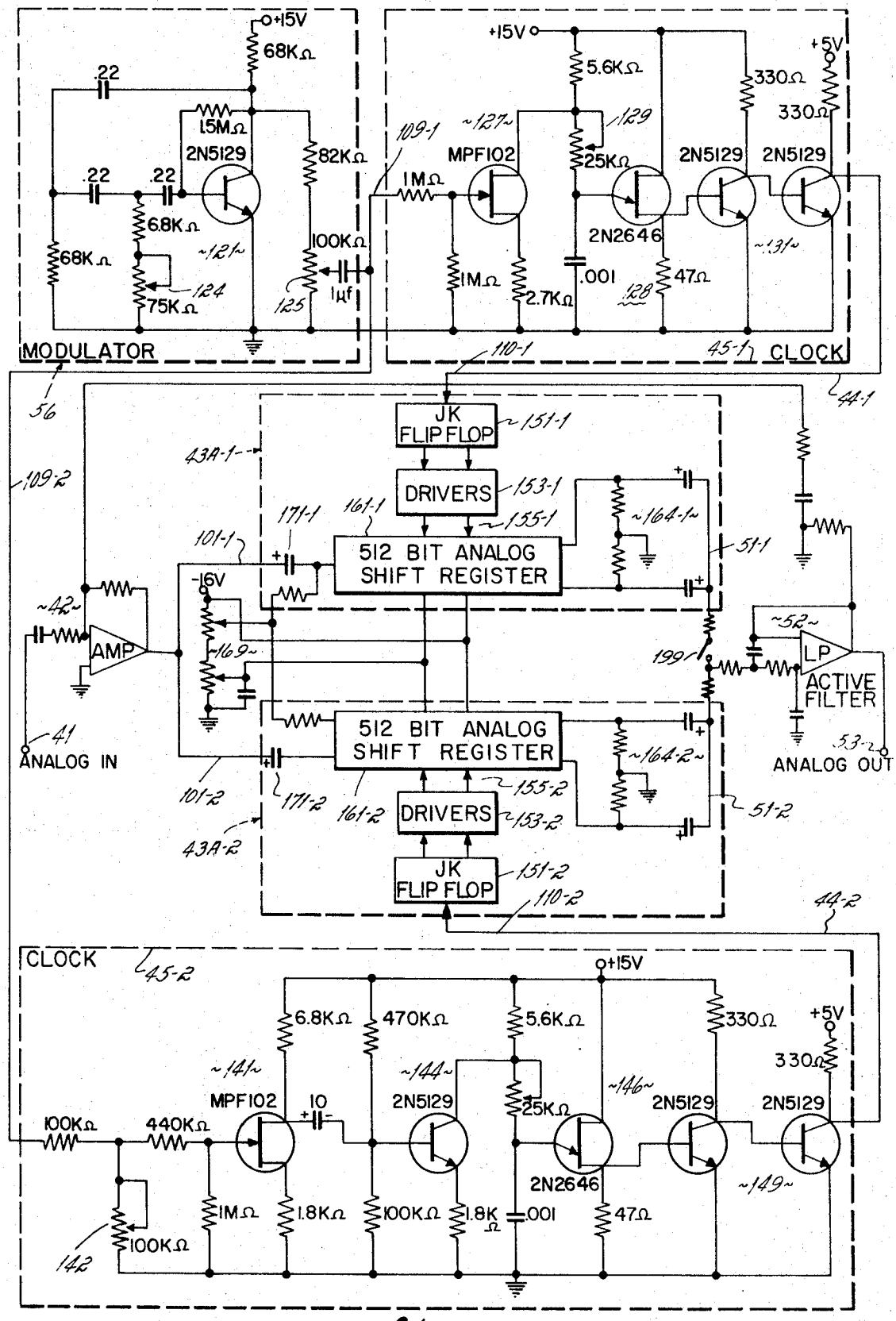

CLOCK
ONE SHOT MULTIVIBRATOR
97
25
24
MODULATOR
36
1.2KΩ
98
.47
680Ω
2N5129
390Ω
5.6KΩ
2N2646
95
82Ω
.002
96
MFE-2049
93
37
1MΩ
1.5KΩ
.22
100KΩ
100KΩ
82KΩ
94
GE-10
91
27MΩ
.22
15KΩ
75KΩ
92
.22
.22
62KΩ
ANALOG OUT
33
32
LOW PASS FILTER
31
10
DIGITAL TO ANALOG CONVERTER
78
MUX
77
76
-128 BIT DIGITAL-
SHIFT REGISTER
MUX
75
QUAD. LATCH
74
73
ANALOG TO DIGITAL CONVERTER
81
82
64
72
SAMPLE AND HOLD
71
SHIFT REGISTER
84
23D
22
ANALOG IN
21
AMP
63
62
LOW PASS FILTER
61
83
ONE SHOT MULTIVIBRATOR

Fig. 3


+15V
68KΩ
.22
1.5MΩ
2N5129
82KΩ
.22
.22
6.8KΩ
68KΩ
~121~
124
75KΩ
100KΩ
125
1μf
MODULATOR
56
109-1
~127~
MPF102
1MΩ
1MΩ
2.7KΩ
5.6KΩ
129
25KΩ
2N2646
.001
128
47Ω
330Ω
+5V
330Ω
2N5129
2N5129
~131~
CLOCK
45-1
110-1
44-1
JK FLIP FLOP
151-1
43A-1
DRIVERS
153-1
155-1
109-2
171-1
161-1
101-1
512 BIT ANALOG SHIFT REGISTER
~164-1~
51-1
-16V
~42~
AMP
~169~
41
ANALOG IN
~52~
LP
ACTIVE FILTER
53-2
ANALOG OUT
199
512 BIT ANALOG SHIFT REGISTER
~164-2~
101-2
171-2
161-2
DRIVERS
155-2
153-2
51-2
43A-2
JK FLIP FLOP
151-2
110-2
44-2
CLOCK
45-2
+15V
6.8KΩ
470KΩ
5.6KΩ
330Ω
+5V
330Ω
~141~
~144~
~146~
MPF102
10
2N5129
25KΩ
2N5129
2N5129
100KΩ
440KΩ
2N2646
~149~
1MΩ
1.8KΩ
100KΩ
1.8KΩ
.001
47Ω
142
100KΩ

40 Fig. 4

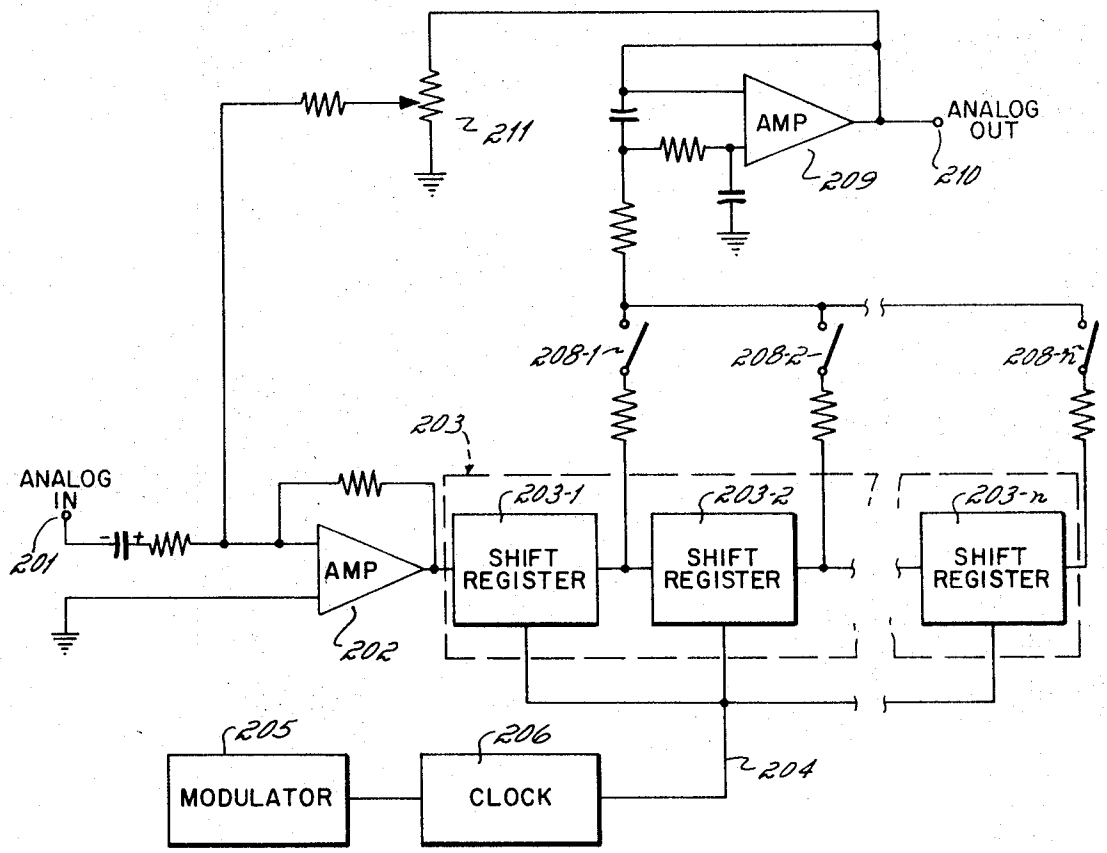

211
AMP
209
ANALOG OUT
210
208-1
208-2
208-n
203
ANALOG IN
201
AMP
202
203-1
SHIFT REGISTER
203-2
SHIFT REGISTER
203-n
SHIFT REGISTER
205
MODULATOR
206
CLOCK
204

Fig. 5

ELECTRONIC MUSICAL TONE MODIFIER FOR MUSICAL INSTRUMENTS

The present invention relates to electronic devices for use with electronic musical instruments and like audio devices. More particularly, the present invention relates to devices for modifying musical tones by, for example, super-imposing low-frequency modulation thereon to produce, for example, vibrato-like effects.

The present invention is most useful in creating musical effects which take the form of sub-audible frequency modulation of audio-frequency signals. Examples of such effects are the vibrato effect and the chorus or Leslie effect. In the vibrato effect, an audio-frequency tone is frequency modulated at usually somewhere between 3 to 12 cycles per second, normally approximately 6 or 7 cycles per second. The use of this effect in connection with electronic musical instruments is for the purpose of simulating more realistically such modulation as it normally occurs in mechanical musical instruments. A similar effect is the Leslie effect in which such low frequency modulation is imposed by utilization of doppler principles usually obtained by mechanical motion of the speakers or audio transducers.

It is a primary objective of the present invention to provide a device which will electronically generate effects of this type in audio frequency electrical signals representative of sound.

Most prior art devices which sought to electronically simulate these effects have provided simple modulators which operate directly to superimpose upon the audio frequency electrical signal a frequency modulation. According to the present invention, this effect is provided through the use of audio signal delay means in which the delay time is varied to provide the frequency modulation sought to be imposed.

Prior art devices have attempted to impose such effects by delay means. One such device is disclosed in Lubow U.S. Pat. No. 3,518,354. The device shown in this patent accepts an audio signal from a signal source and records it upon a rotating storage drum. This signal is stored through a pair of diametrically opposed recording heads. A pick-up head spaced intermediate the recording heads is provided to pick up the recorded signal for transmission to an audio output device. Rotation of the drum at constant frequency will result in delayed version of the output of the input audio signal. The modulated effects are created by varying the speed of rotation of the drum to generate an apparent audio frequency shift in the output signal. Thus, it can be seen that this device employs a mechanical delay concept.

It is a further objective of the present invention to provide a device which will produce certain musical effects through the use of a signal delay which employs a shift register capable of delaying an electrical signal by way of step-by-step progression of discrete sampled values of an analog input wave form. The frequency modulation is imposed by variation of the sampling and shifting rates of the register in causing the values to be shifted from the output of the register through a low pass filter to smooth the output and reproduce a delayed and modulated analog output signal.

Discrete delay methods have not been employed in musical tone modifying devices of this type even though delay devices have generally been available. For example, a discrete analog delay device is disclosed

in McCoy U.S. Pat. No. 2,966,641. This device employs an electro-mechanical scanner having a pair of ganged rotary switches, one of which controls a sampling of an input signal and the other of which controls the readout of the sampled signal. This device employs a plurality of storage capacitors which hold sampled analog signal representations of the signal. This device, however, operates at a constant frequency and provides no modulation.

Other devices have been proposed for synthesizing musical signals from discrete stored values of musical wave forms. One such device is disclosed in Dutsch U.S. Pat. No. 3,515,792. In this device, different wave forms are stored in different digital storage registers and are read out at a selected rate to produce a given musical tone.

The device of the present invention is provided with an input for receiving analog electrical signals and an output for generating the delayed modulated form of the analog signal. The delay in modulation is achieved by providing a shift register connected between the inputs and outputs which operates under the control of a clock. Pulses output from the clock cause the register to sample an instantaneous value of the analog signal at the input and to progressively shift the value along the register toward the output. A modulator is provided for varying the clock output frequency and, therefore, to cause the shifting and sampling to be varied in accordance with the modulation from the modulator. The invention also provides, in a further embodiment, the provision of two shift registers which operate under the control of different clocks. The modulation is such that the pulse frequencies of the clocks will be varied differently so as to generate two signals from the input signal which are then combined at an output to produce an enhanced effect.

The device of the present invention is presented in two specific forms. The first form incorporates the use of a digital shift register. This shift register has at its input an analog-to-digital convertor which transposes the sampled analog input signal to a discrete digital representation of the magnitude of the sampled signal. At the output of the shift register is provided a digital-to-analog convertor which retransforms the delayed digital representation into an analog value which is smoothed in an output filter and delivered at the analog output.

A further embodiment of the invention, and that which is preferred, incorporates an analog shift register which directly stores a discrete representation of a sampled analog value of the magnitude of the input signal and shifts it toward the output at which it is smoothed in a filter and delivered to the output as a delayed and modulated analog signal. The modulation is provided by varying the frequency of a clock supplying trigger pulses to the shift register. Further, the present invention further provides a reverberation effect device having serially connected shift registers and embodying the principles set forth above.

Shift registers of the digital type have long been known and are conventional, and accordingly, need not be described in further detail. Shift registers of the analog type are also presently conventional but have only until recently been employed to a great extent. These registers are typically referred to as the bucket-brigade type and are described in the IEEE Journal of Solid-State Circuits, June 1969, in an article by F. L. J. Sang-

ster and K. Teer entitled, "Bucket-Brigade Electronics — New Possibilities for Delay, Time-Axis Conversion, and Scanning." These devices are also disclosed in the digest technical papers of the 1970 IEEE, International Solid-State Circuits Conference, page 74, in an article by F. L. J. Sangster, entitled "Integrated MOS and Bipolar Analog Delay Lines Using Bucket-Brigade Capacitor Storage."

These and other objectives and advantages of the present invention will be more readily apparent from the following detailed description of the drawings illustrating electronic devices for modifying musical tones and embodying principles of the present invention.

FIG. 1 is a block diagram illustrating a single channel device embodying principles of the present invention.

FIG. 2 is a block diagram illustrating a two channel device embodying principles of the present invention.

FIG. 3 is a schematic diagram of the single channel device of FIG. 1 employing a digital shift register.

FIG. 4 is a schematic diagram of the two channel device of FIG. 2 wherein the shift registers are analog type shift registers.

FIG. 5 is a schematic diagram of a reverberation effect device embodying principles of the present invention.

Referring to FIG. 1, a single channel musical tone modifying device **10** is illustrated in block diagram form. This device includes an input terminal **21** which receives an analog audio frequency electrical signal. The input terminal **21** is connected to the input of an amplifier **22** which may be provided to increase the signal strength and to operate as a filter to limit the band width of the input signal. The output of the amplifier **22** is connected to the input storage element of a shift register **23.** This shift register **23** operates as a delay device for the signal passing therethrough. It includes a plurality of consecutively connected storage elements, each capable of storing an electrical representation of the magnitude of the analog signal from the input **21** at some specific instant in time. The shift register operates under the control of a trigger pulse on line **24** which is connected to the output of a clock circuit **25.** The clock circuit **25** operates to generate a series of periodic pulses on the line **24** at some predetermined frequency. These pulses control the shifting of the values through the register **23.** Also, in response to the pulses on line **24,** a sampling of the analog signal from the amplifier **22** is timed and the sampled value is stored in the first storage element of the shift register **23.** This value will progress, with each subsequent pulse from the line **24,** through the consecutive storage elements of the shift register **23** toward the last storage element of the shift register **23.** The value arriving at the last storage element of the shift register **23** is communicated along an output line **31** through a filter **32.** The filter **32** operates to smooth the discrete values which are successively shifted to the last storage element and to thereby generate a smooth analog signal of audio frequency at an output terminal **33** to which the filter **32** is connected. The signal at the output **33,** when the frequency of the clock **25** is operated at a constant, will be delayed analog representation of the signal at the input **21.**

The device **10** is further provided with a modulator **36** which is operable to generate a low frequency modulating signal to the input **37** of the clock **25.** This frequency is normally, for purposes in which the invention is primarily used, maintained in the range of subaudible frequencies of approximately 3 to 12 cycles per second. This signal operates to frequency modulate the clock **25** so as to vary the frequency of the pulses on line **24** and thus vary the shifting rate and the sampling rate of the shift register **23.** This causes a periodic expansion and compression of the wave passing through the shift register **23** and results in frequency modulation of the delayed signal at the output **33.**

Referring now to FIG. **2,** a two channel device **40** similar to that of FIG. **1** is illustrated in block diagram form. This device includes an input **41** for receiving the analog audio signal which is connected to the input of a band-limiting pre-amplifier **42.** The output of the amplifier **42** is connected to the inputs of respective shift registers **43-1** and **43-2** which partially define the two channels of the device. Each shift register **43** operates under the control of pulses supplied on clock input lines on **44-1** and **44-2** respectively from a respective one of a pair of clocks **45-1** and **45-2.** Each of the shift registers **43-1** and **43-2** operates in the same manner as the shift register **23** of FIG. **1.,** except that the clocks **45-1** and **45-2** are made to operate differently. It is not necessary that the clocks **45-1** and **45-2** operate at the same predetermined frequency. However, in the preferred embodiment this frequency is selected to be the same, or approximately the same, for each clock. In this embodiment, however, it is desired that the modulation of the predetermined frequency be different for each of the channels. In the preferred form this modulation is identical in frequency and deviation but differs only in sign. To achieve this, a single modulator **56** is provided which has its outputs connected to the respective clocks **45-1** and **45-2.** The output to the clock **45-2** is inverted in sign by passage through an inverting amplifier **58.** In this manner, the modulated signal is emitted from each of the channels on respective lines **51-1** and **51-2** in such a manner that the deviation of the modulation is in the opposite direction with respect to the respective predetermined frequencies of the clocks. These modulated signals are passed from lines **51-1** and **51-2** through a filter mixer **52** which blends the two signals on the lines **51-1** and **51-2** to produce an effect which has more desirable audio properties than does the signal from the signal channel device of FIG. **1.** The output of the filter mixer **52** is communicated to the analog output **53** of the device **40.**

Considering the circuitry of the elements set forth in FIGS. **1** and **2** in greater detail, reference is made to FIGS. **3** and **4** which illustrate various forms in which the present invention may be embodied. The diagram of FIG. **3** illustrates the use of a digital shift register provided with analog-to-digital and digital-to-analog convertors and embodied in a single channel circuit **10** such as that of FIG. **1.** FIG. **4** on the other hand discloses analog shift registers embodied in the two channel version of the device **40** shown in FIG. **2.** It will be understood, however, that either the digital or analog shift register versions may be employed in either the single or double channel devices in FIGS. **1** and **2.** The analog shift register, however, is preferred for both applications in that it is far simpler and much more economical than the digital version.

Referring now to the digital shift register version of the single channel device in FIG. **3,** the input **21** is illustrated connected to the input of the preamplifier **22** which is illustrated as composed of a low pass filter **61**

and an amplifier 62. The output of the amplifier 62 is connected to the input 63 of the shift register 23D which is the digital version of the shift register 23 of FIG. 1. The output 31 of the shift register 23D is connected through the filter 32 to the analog output 33. The modulator 36 is illustrated having its output connected to the input 37 of the clock circuit 25. The output of the clock 25 is communicated along the trigger pulse line 24 to the trigger input 64 of the shift register 23D.

The shift register 23D includes a sample and hold circuit 71 having an input connected to the input 63 of the shift register 23D and an output connected to the input of an analog-to-digital converter 72. The sample and hold circuit 71, may, e.g., be a circuit device in accordance with the principles of model SHM-1 manufactured by Varodyne, Inc., Canton, Massachusetts or model NH0023/NH0023C manufactured by National Semiconductor Corp., Santa Clara, California. The analog-to-digital convertor has a plurality of binary outputs 73 which are connected to storage circuits 74. The circuits 74 include flip-flops, one corresponding to each of the outputs 73 for storing binary bit information. These flip-flops are by choice packaged in quad-latch integrated circuits but may be of any other form. The outputs of the flip-flops' circuits 74 are connected through a hexinverter circuit 75 to respective first bit positions of conventional 128 bit binary shift registers 76. The output or last bit positions of the shift registers 76 are connected through hexinverter amplifier circuits 77 to the digital inputs of a digital-to-analog converter 78. The hex inverter circuits 75 and 77 may, e.g., be a circuit device in accordance with the principles of circuit types SN5404 or SN7404 manufactured by Texas Instruments, Inc., Dallas, Texas. The output of the digital-to-analog converter 78, which carries the analog output signal, is connected to the output 31 of the shift register 23D.

The clock input 64 which receives the clock pulses from the pulse line 24 is connected to the clock control input 81 of the analog-to-digital convertor circuit 72. The pulses communicated to this input 81 cause the circuit 72 to perform an analog-to-digital conversion transforming the sampled analog value stored in the sample and hold circuit 71 into binary digital form on the lines 73. When this conversion is complete, an end-of-conversion signal is generated on an output control line 82 of the analog-to-digital convertor 72 to time the sample and hold circuit 71 to sample the next value of the signal from the output of the amplifier 62. The signal on line 82 also energizes a pulse forming one-shot multivibrator 83 which generates a transfer pulse on a line 84 to cause a shifting of the converted value from line 63 as stored in the flip-flop circuit 74 to the first bit position of the shift register 76, and to cause a progressive shifting of each of the electrical representations stored within the storage elements of the shift register 76 to the next successive element along the shift register 76 toward the output side of the register 23D. The values entering the last storage element of the shift register 76 are converted from digital to analog form by the digital-to-analog convertor 78. These values as they appear on line 31 are smoothed by the low pass filter 32 to present the analog signal at the output 33.

The modulator 36 includes a low frequency oscillator circuit 91 which generates a low frequency sine wave in the frequency range of from 3 to 12 cycles per second. The frequency of oscillation of the oscillator 91 is controlled by a potentiometer 92 in the circuit 91. The frequency deviation of the modulator 36 is controlled by the setting of a potentiometer 94.

The clock 25 includes an FET input stage 93 connected between the modulator output 37 and a unijunction transistor oscillator stage 95 which produces a series of pulses at a predetermined given frequency determined by the setting of a potentiometer 96 in the UJT circuit 95. The circuit 95 operates to generate a periodic series of pulses at a frequency of roughly 22 kilohertz. These pulses are fed through a buffer amplifier stage 98 to the input of a one-shot multivibrator 97. The multivibrator 97 shapes the pulses and feeds them to the output pulse line 24. The frequency of the pulses on the output line 24 will be at the predetermined given frequency as set upon the potentiometer 96 with frequency and deviation of modulation as determined by the settings of the potentiometers 92 and 94 respectively of the modulator circuit 36.

In operation, the clock 25 will operate at a predetermined frequency to produce a periodic series of pulses on line 24. These pulses will be frequency modulated in accordance with the setting of the modulator 36 and will proceed to the input 64 of the shift register 23D. Analog audio signals in electrical form communicated from the device input 21 to the shift register input 63 will be continuously presented for sampling at the sample and hold circuit 71. As each pulse enters the input 64 of the shift register 23D, a conversion is made from the analog signal previously held in the sample and hold circuit 71 which is, upon completion of the conversion, caused to shift to the first storage element position of the shift register 76 in response to a trigger pulse initiated by the end of conversion signal from line 82 through the one-shot multivibrator 83 to the line 84 which is connected to the trigger inputs of the flip-flop storage circuits 74 and shift register 76. Simultaneous with the shifting of the stored digital values through the register, the signal from line 82 causes the next value to be sampled from the analog signal at the input 63. As each pulse enters the input 64, the next conversion and sampling and shifting will occur. As the signal emerges from the last storage element of the shift register 76, it is converted back to analog form by the converter 78, whereby a delayed analog signal is reproduced at the output 83.

If the clock frequency on the line 64 is constant, the electrical representations of the stored values which emerge from the shift register 76 and are converted again to analog form will emerge from the shift register 76 at the same rate at which they are stored and sampled. Under this condition, the only difference between the output signal on terminal 33 and the input signal at terminal 21 will be that the output signal is delayed by a time interval which is dependent upon the length or number of storage elements of the shift register 76 and the frequency of the pulses on line 24. But where the clock frequency is varied under control of the modulator 36, the electrical representations which are emerging from the shift register 76, will be at a rate different from that at which they were sampled and stored. This difference is due to the fact that the sampling frequency has changed over the delay interval at which it takes for the stored values to proceed through the shift register 76. Thus, the analog signal which is formed at the output will be either expanded or compressed on a

time basis in relation to the wave form of that signal at the time at which it was sampled and stored, thus resulting in an apparant frequency shift in the output signal.

Referring now to FIG. 4, a two channel device 40 is illustrated which employs analog shift registers. The device 40 includes the analog audio signal input 41 connected through the amplifier circuit 42 to the input 101-1 and 101-2 of the respective shift registers 43A-1 and 43A-2. The outputs 51-1 and 51-2 of the respective shift registers are connected through the filter mixer circuit 52 to the analog output 53.

The modulator 56 has its output connected through lines 109-1 and 109-2 to the input of the clocks 45-1 and 45-2 respectively. The output of the clock 45-1 is connected through the trigger line 44-1 to the input 110-1 of shift register 43A-1 while the output of clock 45-2 is connected through trigger line 44-2 to the input 110-2 of the shift register 43A-2.

The modulator 56 includes a phase shift oscillator circuit 121 which provides the low frequency sine wave modulating signal. The frequency of this signal is determined by the setting of a potentiometer 124. The modulating signal deviation is controlled by a potentiometer 125 in the modulator output.

The clock circuit 45-1 includes an FET input stage 127 connected between the input 109-1 and a unijunction oscillator stage 128. The frequency of oscillation of the clock is determined by the setting of a potentiometer 129 in the oscillator stage. The oscillator stage 128 produces a series of pulses establishing the predetermined clock frequency. As will be explained below, the frequency of the clocks used in the analog shift register version will be twice that of the clock in the digital shift register version of FIG. 3 in the particular circuits illustrated. The output of the oscillator stage 128 is connected through a buffer and driver stage 131 to the output line 44-1.

Similarly, the clock 45-2 includes an FET input stage 141 and is provided with a potentiometer 142 to set the modulator signal voltage so that each clock will deviate the same amount in opposite phases, or alternatively to allow for the different setting of the inputs bias of the two clocks. The output of the FET input and inverter stage 141, which performs the function of the inverter 58 in the block diagram of FIG. 2, is connected through an amplifier circuit 144. This reverses the plurality of the modulation applied to clock 45-2 with respect to that applied to clock 45-1 so that its frequency deviates in the opposite direction from that of clcok 45-1. The clock 45-2 is also provided with a unijunction stage 146 which establishes the predetermined frequency of the clock 45-2 in accordance with the setting of a potentiometer 147. The output of the clock oscillator stage 146 is connected through a buffer and driver stage 149 to pulse output line 44-2.

Each of the pulse output lines 44-1 and 44-2 connects through the respective inputs 110-1 and 110-2 to the trigger input of JK flip-flops 151-1 and 151-2 respectively. The complementary outputs of the flip-flops 151 are connected through driver circuits 153-1 and 153-2 respectively to the trigger inputs 155-1 and 155-2 of analog shift register circuits 161-1 and 161-2 respectively. The driver circuit 153-1 and 153-2 may, e.g. be a circuit device in accordance with the principles of circuit type MH0026/MH0026C manufactured by National Semiconductor Corp., Santa Clara, California The shift registers 161 and 512 bit analog shift registers of the commercially available type manufactured by Amperex. The outputs of the shift registers 161-1 and 161-2 are AC coupled through circuits 164-1 and 164-2 respectively to the shift register outputs 51-1 and 51-2, respectively. The inputs 101-1 and 101-2 of the shift registers 43A-1 and 43A-2 are biased by a biasing circuit 169 to some DC level. The input signals from the inputs 101 are AC coupled through capacitors 171-1 and 171-2 respectively to the inputs of shift registers 161-1 and 161-2.

The operation of the two channel circuit of FIG. 4 is similar to that of the single channel circuit in the FIG. 3 embodiment. Each of the clocks 45-1 and 45-2 produce periodic series of pulses on the lines 44-1 and 44-2 to the shift register clock inputs 110-1 and 110-2, respectively. The flip-flops 151-1 and 151-2 at the shift register clock inputs divide the frequency of the incoming pulses in half, thus requiring that the normal predetermined frequency setting of the clocks 45 be twice that of the setting of the clock 25 in the circuit of FIG. 3. The shift registers 161 operate, upon the occurrence of each pulse from line 44 through terminal 110, to cause a progressive shift of the stored analog electrical representation of the incoming wave form from the input storage element of the shift register toward the output storage element of the shift register and to simultaneously cause a next value output from the amplifier 42 to be sampled and stored at the input storage element of the shift registers 161. When the clock frequencies are constant and equal, the outputs of the lines 51 will be identical and their values will be summed and smoothed at the amplifier stage 52 and passed to the analog output 53. These outputs will be delayed representations of the input signal which has been fed into and passed through each of the shift registers 43 and delayed by some time interval determined by the frequencies of the clocks 45 and the length of the shift registers 161.

Single channel operation is usually employed for vibrato effects while two channel operation provides the chorus of Leslie effect. The switch 199 is provided to select either one or two channel operation.

As the modulating signal from modulator 56 is imposed on each of the clocks 45, the pulse trains on lines 44 will be frequency modulated and, for the same reasons discussed in connection with the circuit of FIG. 3, this frequency modulation will result in a time varying delayed imposed on the signals passing through the shift registers 161. Because of the presence of the inverter stage 141 in the clock 45-2, a positive frequency deviation in the pulse train on line 44-1 will correspond to a negative frequency deviation pulse train on line 44-2. This will cause a decrease in the delay imposed by shift register 161-1 and an increase in the delay imposed by shift register 161-2 resulting in a time expansion of the signal on line 51-1 in relation to the input signal and a time compression of the signal on line 51-2 in relation to the input signal. These will appear as corresponding frequency modulations of opposite deviations in the outputs from the two shift registers and when combined, will provide an effect at the output 53 of an enhanced chorus or Leslie sound. The settings of the two clocks 45 may be varied in different manners to create differing effects at the output 53, and furthermore, separate modulators may be used to differently modulate the clocks in a variety of ways.

In FIG. 5, an echo and reverberation effect circuit is shown embodying the present invention. Here, the analog input 201 connects through the amplifier through the shift register circuit 203. The shift register 203 includes a plurality of n shift registers, either analog or digital, 203-1, . . . , 203-n, all controlled by a common trigger line 204 from the modulator 205 controlled clock 206. The outputs of each shift register 203-1, . . . , 203-n are selectively connectable individually or collectively through switches 208-1, . . . , 208-n. Each of these outputs carries a respective signal of increased delay over the last so that the summed result through the low pass amplifier 209 produces a reverberation effect in the signal at the output 210. Short time delays produce a reverberation effect which can be selected through the switches 208 nearest the input, longer time delays result in an echo effect selectable through the switches 208 nearest the output. Plural connection by switches 208 results in an enhanced effect of the musical tone. Potentiometer 211 controlls the decay time of the effect and, thus the amount of reverberation and the number of times that the echo will repeat.

From the foregoing detailed description of the preferred embodiments of the present invention, it will be apparent that what is provided is a solid state device for imposing certain types of effects resembling the Leslie effect, the vibrato effect, and a reverberation effect on electrical signals representative of musical tones. The devices are suitable for being connected in series with the output stages of electronic musical instruments to which it is desired to provide such effects. The specific circuits disclosed provide shift registers for storing discrete representations of the sampled magnitudes of input wave forms and operate to impose varying delays by controlling the shift rate of the signals passing through the shift registers. These effects are provided in a superior manner than by devices of the prior art. Both one and two channel forms are provided but it will be apparent that these may be combined in any number of channels to provide different effects. Also, both digital and analog shift register forms are disclosed in accordance with the present invention.

What is claimed is:

1. An electronic device for modifying a musical tone comprising:
- an input for receiving an audio frequency analog electrical signal;
- an output;
- a shift register connected between said input and said output;
- said shift register having a plurality of sequentially connected storage elements, each capable of storing a discrete electrical representation of the amplitude of an electrical signal, said plurality of storage elements including a first storage element, a last storage element, and a plurality of intermediate storage elements;
- a clock for generating a periodic series of pulses at a given frequency, said clock being connected to said shift register;
- said first storage element having connected therewith a circuit operable to sample and store the amplitude of said audio frequency electrical signal in response to said pulses from said clock;
- said shift register being operative to sequentially shift stored electrical representations from each storage element to the next consecutive storage element from said first toward said last storage elements in response to said pulses from said clock;
- a filter connected between said last storage element and said output for generating a smooth analog signal from electrical representations sequentially shifted to said last storage element;
- whereby a delayed electrical analog representation of said analog input signal is produced at said output; and
- a modulator for varying said given frequency of said clock;
- whereby a delayed frequency modulated electrical analog representation of said analog input signal is produced at said output.

2. A device according to claim 1 further comprising:
- a second shift register having a plurality of sequentially connected storage elements each capable of storing a discrete electrical representation of the amplitude of an electrical signal, said plurality of storage elements including a first storage element, a last storage element, and a plurality of intermediate storage elements;
- a second clock for generating a periodic series of pulses at a given frequency, said second clock being connected to said second shift register;
- said first storage element of said second shift register being operative to sample and store the amplitude of said audio frequency electrical signal in response to said pulses from said second clock;
- said second shift register being operative to sequentially shift stored electrical representations from each storage element thereof to the next consecutive storage element thereof from said first to said last storage elements thereof in response to said pulses from said second clock;
- said last storage element of said second shift register being connected through said filter to said output; and
- said filter being operable to mix the output of said second shift register with the output from said first recited shift register, and to thereby generate a smoothed electrical signal from the combined electrical representations sequentially shifted to the last storage elements of said shift registers;
- whereby plural combined delay electrical analog representations of said analog input signal are produced at said output.

3. A device according to claim 2 further comprising:
- means for modulating the given frequency of said second clock differently from the given frequency of said first clock.

4. A device according to claim 3 wherein:
- said modulating means are operative to modulate the given frequency of said second clock in opposite relation to the modulation of said first clock.

5. A device according to claim 2 further comprising:
- an inverter connected between said modulator and said second clock for varying said given frequency of said second clock.

6. A device according to claim 1 wherein said shift register comprises:
- a multi-bit digital shift register;
- an analog-to-digital convertor connected between said input and the first storage element of said shift register; and

a digital-to-analog convertor connected between said last storage element of said shift register and said filter.

7. A device according to claim **6** wherein said sample and store circuit includes a sample and hold circuit connected between said input and said analog-to-digital convertor.

8. A device according to claim **1** wherein said shift register comprises:

an analog shift register having storage elements each capable of storing an analog representation of an electrical signal.

9. A device according to claim **1** further comprising:

a second shift register having a plurality of sequentially connected storage elements each capable of storing a discrete electrical representation of the amplitude of electrical signal, said plurality of storage elements including a first storage element, a last storage element, and a plurality of intermediate storage elements;

said first storage element of said second shift register being operative to receive and store the amplitude of the stored electrical representation from the last storage element of said first recited shift register in response to said pulses from said clock;

said second shift register being operative to sequentially shift stored electrical representations from each storage element thereof to the next consecutive storage element thereof from said first to said last storage elements thereof in response to said pulses from said clock;

said last storage element of said second shift register being connected through said filter to said output;

said filter being operable to mix the output of said second shift register with the output from said first recited shift register, and to thereby generate a smoothed electrical signal from the combined electrical representations sequentially shifted to the last storage elements of said shift registers;

whereby plural combined and differently delayed electrical analog representations of said analog input signal are produced at said output.

10. A device according to claim **9** further comprising:

switch means connected in series with each of the inputs of said filter to selectively apply said differently delayed outputs to said filter.

11. A device according to claim **1** further comprising:

circuit means for combining the signal from the input of said shift register with the output from said shift register to produce a combined signal from differently delayed signals whereby an echo or reverberation effect is produced.

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