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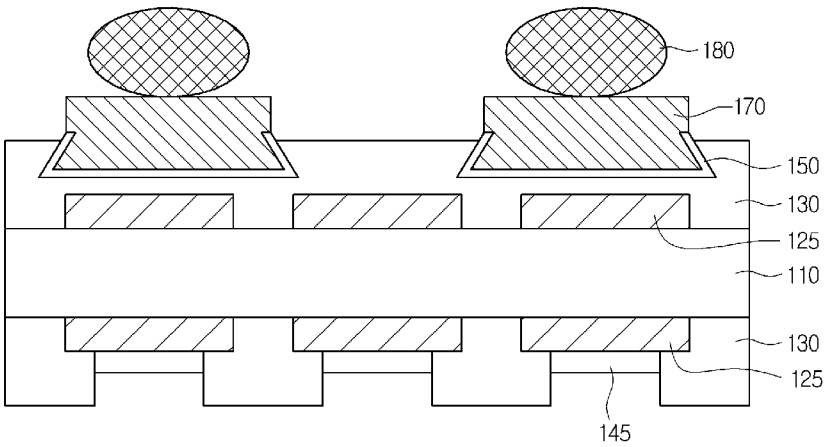
(54) Title: SEMICONDUCTOR PACKAGE SUBSTRATE, PACKAGE SYSTEM USING THE SAME AND METHOD FOR MANUFACTURING THEREOF



(57) Abstract: According to the embodiment, there is provided a semiconductor package substrate including an insulating substrate; a circuit pattern on the insulating substrate; a protective layer on the insulating substrate, the protective layer covering the circuit pattern on the insulating substrate; a pad on the protective layer; and an adhesive member on the protective layer, wherein the pad includes a first pad buried in the protective layer, and a second pad on the first pad, the second pad protruding over the protective layer.

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Description

Title of Invention: SEMICONDUCTOR PACKAGE SUBSTRATE, PACKAGE SYSTEM USING THE SAME AND METHOD FOR MANUFACTURING THEREOF

Technical Field

[1] Embodiments relate to a semiconductor substrate, and more particularly, to a semiconductor substrate for a flash memory, a flash memory using the same and a method of manufacturing the same.

Background Art

[2] As electrical/electronic appliances have been advanced with high performance, technology for attaching a greater number of packages onto a substrate having a limited size has been proposed and studied. However, since it is a rule to mount only one semiconductor chip in a package, there is limitation to obtain a desired capacity.

[3] As a method of increasing a capacity of a memory chip, that is, as a method of achieving high integration, technology of installing a greater number of cells in a limited space has been generally known in the art. However, such a method requires high level technology such as a precise design rule and a lot of development time. Thus, as a method for easily achieving high integration, a stacking technique has been developed and the study for the sacking technique has been currently performed very actively.

[4] To this end, an MCP (Multi Chip Package) technique has been recently utilized.

[5] The MCP is a semiconductor product prepared in the form of one package by stacking several memory chips, so the MCP not only reduces the volume of the semiconductor product, but also increases the data storage capacity, so that the MCP is mainly used in portable electronic equipment such as a mobile phone.

[6] In this case, since several tens of semiconductor chips are stacked to be stably operated while minimizing the thickness thereof, the high level technique is required from the design stage to the production stage.

[7] FIG. 1 is a view showing a package system according to the related art.

[8] Referring FIG. 1, the package system includes a semiconductor package substrate 10, a dummy die 20, and a memory chip 30.

[9] The semiconductor package substrate 10 includes at least one circuit pattern formed on an insulating substrate. A protective layer for protecting the circuit pattern is formed on the circuit pattern (uppermost layer of the semiconductor package substrate 10).

[10] The memory chip 30 may be a nand flash memory chip.

[11] The dummy die 20 is formed between the substrate 10 and the memory chip 30.

[12] The dummy die 20 provides an attaching space for allowing the memory chip 30 to be attached onto the semiconductor substrate 10 while spacing the semiconductor substrate 10 from the memory chip 30.

[13] However, since the package system described above must form the dummy die 20 between the semiconductor substrate 10 and the memory chip 30 for stacking the memory chip 30, an additional process is required in addition to a process for manufacturing the semiconductor substrate 10, so that productivity of a manufacturer is reduced.

[14] Further, since the dummy die 20 is formed of an expensive silicon material, a cost of the entire package system is increased.

[15] In addition, since the silicon dummy die 20 has a predetermined thickness, the entire thickness of the package system is increased.

Disclosure of Invention

Technical Problem

[16] Embodiments provide a semiconductor package substrate having a novel structure, a package system using the same and a method of manufacturing the same.

[17] Further, embodiments provide a semiconductor package substrate which can improve productivity of a package system and reduce the product cost.

[18] The technical objects which will be achieved in the proposed embodiments are not limited to the above, but other technical objects which are not mentioned will be apparently understood to those skilled in the art.

Solution to Problem

[19] According to the embodiment, there is provided a semiconductor package substrate including an insulating substrate; a circuit pattern on the insulating substrate; a protective layer on the insulating substrate, the protective layer covering the circuit pattern on the insulating substrate; a pad on the protective layer; and an adhesive member on the protective layer, wherein the pad includes a first pad buried in the protective layer, and a second pad on the first pad, the second pad protruding over the protective layer.

[20] Further, according to the embodiment, there is provided a package system including a semiconductor package substrate including an insulating substrate, a circuit pattern formed on one surface of the insulating substrate, and a protective layer formed on the insulating substrate while covering the circuit pattern; and a semiconductor chip attached onto the semiconductor package substrate, wherein the semiconductor package substrate comprises: a pad plated on the protective layer; and an adhesive member on the pad, and wherein the semiconductor chip is attached onto the pad form on the semiconductor package substrate by the adhesive member.

[21] Further, according to the embodiment, there is provided a method of manufacturing a package system, the method comprising: forming a circuit pattern on at least one surface of an insulating substrate; forming a protective layer on the insulating substrate to cover the circuit pattern; forming a groove in the protective layer; forming a dry film having an opening of exposing the groove on the protective layer; forming a pad to fill the groove of the protective layer and the opening of the dry film; and forming an adhesive member on the pad.

Advantageous Effects of Invention

[22] According to the embodiments, the copper pad and the adhesive member are formed on the semiconductor package substrate without using the expensive dummy die, so that the productivity of the package system may be improved and the product cost may be reduced.

[23] Further, according to the embodiments, since the pad is formed by using a plurality of stack structure having mutually different widths, the adhesive strength of the pad to the adhesive member can be improved, so that the reliability of the semiconductor package substrate can be improved.

[24] Further, according to the embodiments, since a portion of the pad is buried in the protective layer and the buried portion of the pad has the protrusion shape, the adhesive strength between the pad and the protective layer is increased, so that the reliability of the semiconductor package substrate can be improved.

[25] Further, according to the embodiments, it is possible to achieve a fine pitch by using the copper ball instead of an expensive dummy die.

[26] Further, according to the embodiments, since the second adhesive member is formed by using the copper core solder ball 188, a high standoff height can be maintained even after the reflow process, so that the reliability of the semiconductor package substrate can be improved.

Brief Description of Drawings

[27] FIG. 1 is a view showing a package system according to the related art.

[28] FIG. 2 is a view showing a semiconductor package substrate according to the first embodiment.

[29] FIG. 3 is a view showing a detailed structure of the pad depicted in FIG. 2.

[30] FIGS. 4 to 17 are views illustrating a method of manufacturing a semiconductor package substrate depicted in FIG. 3 in the process sequence.

[31] FIG. 18 is a view showing a semiconductor package substrate according to the second embodiment.

[32] FIG. 19 is a view showing a detailed structure of the pad depicted in FIG. 18.

[33] FIGS. 20 to 25 are views illustrating a method of manufacturing a semiconductor

package substrate depicted in FIG. 18 in the process sequence

[34] FIGS. 26 and 27 are views showing a package system according to the embodiment.

[35] FIG. 28 is a view to compare a package system according to the embodiment with a package system according to the related art.

Mode for the Invention

[36] The embodiment of the disclosure will be described in detail with reference to accompanying drawings, so that those skilled in the art to which the disclosure pertains can easily realize the embodiment. However, the disclosure can be realized in various modifications, and is not limited to the embodiment.

[37] In the following description, when a predetermined part includes a predetermined component, the predetermined part does not exclude other components, but may further include other components if there is a specific opposite description.

[38] The thickness and size of each layer shown in the drawings may be exaggerated, omitted or schematically drawn for the purpose of convenience or clarity. In addition, the size of elements does not utterly reflect an actual size. The same reference numbers will be assigned the same elements throughout the drawings.

[39] In the description of the embodiments, it will be understood that, when a layer (or film), a region, or a plate is referred to as being on or under another layer (or film), another region, or another plate, it can be directly or indirectly on the other layer (or film), region, plate, or one or more intervening layers may also be present. Such a position of the layer has been described with reference to the drawings.

[40] According to a semiconductor package substrate of the embodiment, the copper pad and the adhesive member are formed on the semiconductor package substrate by using hybrid bump technology without using the expensive dummy die, so that the productivity of a package system may be improved and the product cost may be reduced. Further, since the pad is formed by using a plurality of stack structure having mutually different widths, the adhesive strength of the pad to the adhesive member may be improved, so that the reliability of the semiconductor package substrate may be improved. In addition, since a portion of the pad is buried in the protective layer and the buried portion of the pad has the protrusion shape, the adhesive strength between the pad and the protective layer is increased, so that the reliability of the semiconductor package substrate may be improved.

[41] FIG. 2 is a view showing a semiconductor package substrate according to the first embodiment.

[42] Referring to FIG. 2, a semiconductor package substrate 100 includes an insulating substrate 110, a circuit pattern 125 formed on at least one surface of the insulating substrate 110, a protective layer 130 formed on the insulating substrate 110 to protect

the circuit pattern 125, a first adhesive member 145 formed on the circuit pattern 125 formed on the surface opposite to the surface of the insulating substrate 110 on which a semiconductor chip 300 (which will be described below) is mounted, a pad 170 formed on the protective layer 130 formed on a top surface of the insulating substrate 110, and a second adhesive member 180 formed on the pad 170.

[43] One portion of the pad 170 is buried in the protective layer 130, and the other portion protrudes over a surface of the protective layer 130.

[44] Hereinafter, the semiconductor package substrate 100 according to the first embodiment will be described in detail.

[45] The insulating substrate 110 may include a thermosetting polymer substrate, a thermoplastic polymer substrate, a ceramic substrate, an organic/inorganic composite substrate or an impregnated fiberglass substrate. If the insulating substrate 110 includes polymer resin, the insulating substrate 110 may include epoxy insulating resin. In addition, the insulating substrate 110 may include polyimide resin.

[46] The circuit pattern 125 is formed on at least one surface of the insulating substrate 110.

[47] The circuit pattern 125 may be formed of a conductive material and may be formed by simultaneously patterning thin copper layers formed on both surfaces of the insulating substrate 110.

[48] The circuit pattern 125 may be formed of alloy including copper and a roughness may be formed on a surface of the circuit pattern 125.

[49] The protective layer 130 is formed on the insulating substrate 110 to coat the circuit pattern 125 formed on the top surface of the insulating substrate 110 and expose a portion of the circuit pattern 125 formed on the bottom surface of the insulating substrate 110.

[50] The protective layer 130, which is for protecting the surfaces of the insulating substrate 110, is formed on the entire surfaces of the insulating substrate 110 and has an opening (not shown) which opens the surface of the circuit pattern 125, that is, the surface of a stack structure of the circuit pattern 125 formed on the bottom surface.

[51] The protective layer 130 may include at least one layer formed of one of SR (Solder Resist), oxide and Au.

[52] A first adhesive member 145 is formed on the surface of the circuit pattern 125 exposed through the protective layer 130.

[53] The first adhesive member 145 is formed to attach a conductive ball for packaging with a separate substrate in the subsequent process.

[54] The pad 170 is formed on the protective layer 130.

[55] The pad 170 is formed on the protective layer 130 which coats the entire surface of the circuit pattern 125, and does not make contact with the insulating substrate 110 or

the circuit pattern 125.

[56] The pad 170 may be formed of a conductive material such as copper.

[57] The pad 170 is formed on the protective layer 130 for the purpose of attaching the semiconductor chip 300 onto the semiconductor package substrate 100 in future.

[58] That is, although a dummy die having a silicon material is formed on the semiconductor package substrate separately form the manufacture of the semiconductor package substrate 100 in order to attach the semiconductor chip 300 in the related art, the pad 170 is formed on the protective layer 130 in the semiconductor package manufacturing process instead of the dummy die in the embodiment.

[59] FIG. 3 is a view showing a detailed structure of the pad depicted in FIG. 2.

[60] Referring to FIG. 3, the pad 170 includes a first pad 172 which is buried in the protective layer 130 and both sides of which have a protrusion shape, and a second pad 174 which is formed on the first pad 172 and protrudes over the surface of the protective layer 130.

[61] The first pad 172 is buried in the protective layer 130, so that the adhesive strength between the pad 170 and the protective layer 130 is improved.

[62] At this time, the first pad 172 is formed to have an upper width B and a lower width A different from each other.

[63] In more detail, the upper width B of the first pad 172 is narrower than the lower width A of the first pad 172. That is, the first pad 172 has a shape in which a width is gradually narrowed upward, and thus, both sides of the first pad 172 have a protrusion shape.

[64] As described above, the first pad 172 is buried in the protective layer 130 and has the protrusion shape of which the upper and lower widths are different from each other, so that the adhesive strength between the entire structure of the pad 170 and the protective layer 130 is improved.

[65] The second pad 174 is an upper portion of the first pad 172 and protrudes over the surface of the protective layer 130.

[66] The upper and lower widths of the second pad 174 are equal to each other.

[67] At this time, the upper and lower portions of the second pad 174 have the same width at that of the upper portion of the first pad 172.

[68] Since the second pad 174 protrudes over the protective layer 130, the semiconductor chip 300 is easily attached onto the semiconductor package substrate 100 by the second adhesive member 180 formed later.

[69] Again, referring to FIG. 2, the second adhesive member 180 is formed on the pad 170.

[70] The second adhesive member 180 is formed on the pad 170, so that the adhesive strength between the semiconductor chip 300 and the semiconductor package substrate

100 is provided.

[71] The second adhesive member 180 may be formed of a general solder ball. To the contrary, the second adhesive member 180 may be formed by using adhesive paste or a copper core solder ball.

[72] Further, the adhesive paste may include a conductive material. When the adhesive paste is formed of conductive material, the adhesive paste may include a conductive material selected from the group consisting of Ag, cu, Au, Al, carbon nano-tube and combination thereof.

[73] According to the embodiment described above, the copper pad and the adhesive member are formed on the semiconductor package substrate without using the expensive dummy die, so that the productivity of a package system may be improved and the product cost may be reduced.

[74] Further, according to the embodiment, since the pad is formed in a plurality of stack structure having mutually different widths through hybrid bump technology, the adhesive strength of the pad to the adhesive member is improved, so that the reliability of the semiconductor package substrate may be improved.

[75] Further, according to the embodiment, since a portion of the pad is buried in the protective layer and the buried portion of the pad has the protrusion shape, the adhesive strength between the pad and the protective layer is increased, so that the reliability of the semiconductor package substrate may be improved.

[76] FIGS. 4 to 17 are views illustrating a method of manufacturing a semiconductor package substrate depicted in FIG. 3 in the process sequence.

[77] First, as shown in FIG. 4, the insulating substrate 110 is prepared and a metallic layer 120 is laminated on at least one surface of the insulating substrate 110.

[78] At this time, when the insulating substrate 110 is an insulation layer, the lamination structure of the insulation layer and the metallic layer 120 may be conventional CCL (Copper Clad Laminate).

[79] Further, the metallic layer 120 may be formed on the insulating substrate 110 through an electroless plating scheme. When the metallic layer 120 is formed through the electroless plating scheme, a roughness is formed to the surface of the insulating substrate 110, so that the electroless plating may be smoothly performed.

[80] The insulating substrate 110 may include epoxy resin or polyimide resin without using an expensive ceramic material having high thermal conductivity. The insulating substrate 110 may be a copper foil of a thin film including copper of high thermal conductivity and or low resistance.

[81] Next, as shown in FIG. 5, the circuit pattern 125 is formed by etching the metallic layer 120 formed on the top and bottom surfaces of the insulating substrate 110 in a predetermined pattern.

[82] At this time, the circuit pattern 125 may be formed by performing the etching through a photolithography process or a laser process in which a pattern is directly formed by using a laser.

[83] Further, the circuit pattern 125 may be formed at each of upper and lower portions of the insulating substrate 110. To the contrary, the circuit pattern 125 may be formed only at the upper portion of the insulating substrate 110.

[84] Next, as shown in FIG. 6, the protective layer 130, in which the circuit pattern 125 is buried, is formed at the upper and lower portions of the insulating substrate 110.

[85] The protective layer 130, which is for the purpose of protecting the surface of the insulating substrate 110 or the circuit pattern 125, may include at least one layer formed by using at least one of solder resist, oxide or Au.

[86] Next, as shown in FIG. 7, the protective layer 130 formed at the lower portion of the insulating substrate 110 is processed, such that the surface of the circuit pattern 125 formed at the bottom surface of the insulating substrate 110 is exposed.

[87] That is, the protective layer 130 formed at the lower portion of the insulating substrate 110 is processed by using a laser, such that an opening 140 of exposing the surface of the circuit pattern 125 formed below the insulating substrate 110 is formed.

[88] According to the laser process, optical energy is concentrated on a surface of a material, so that a portion of the material can be cut in a desirable form by melting and evaporating the portion of the material, and a complex form of a material can be easily processed through a computer program. In addition, a complex material hard to be cut can be processed.

[89] In addition, according to the laser process, a material can be cut to a diameter of 0.005 mm. In addition, according to the laser process, an allowable process thickness range is wide.

[90] For the laser process, an yttrium aluminum garnet (YAG) laser, a CO2 laser, or a UV laser preferably is used. The YAG laser is a laser to process both of a copper foil layer and an insulating layer, and the CO2 layer is a laser to process only an insulating layer.

[91] It is preferable to form the opening having a small diameter by using the UV laser in the laser process.

[92] Further, the opening 140 may be formed such that only a portion of the circuit pattern 125 is exposed.

[93] In other words, the opening 140 may be formed to have a width narrower than that of the circuit pattern 125, so that only an edge region of the circuit pattern 125 may be protected by the protective layer 130.

[94] Next, as shown in FIG. 8, the first adhesive member 145 is formed on the circuit pattern 125 exposed through the opening 140.

[95] The first adhesive member 145 may be formed by coating adhesive paste on the

circuit pattern 125 exposed through the opening 140 by using the protective layer 130 as a mask.

[96] In order to attach other substrate (not shown) onto the semiconductor package substrate 100, the first adhesive member 145 is used for the purpose of attaching the solder ball which provides the adhesive strength between the semiconductor package substrate 100 and other substrate.

[97] Next, as shown in FIG. 9, a groove 135 is formed in the protective layer 130 formed above the insulating substrate 110.

[98] At this time, the groove 135 is formed to have upper and lower widths which are different from each other.

[99] That is, the groove 135 is formed to have the upper and lower widths different from each other through an expose energy control.

[100] At this time, the groove 135 is formed such that the upper width is narrower than the lower width.

[101] That is, the groove 135 has a protrusion shape having a width which is gradually narrowed upward.

[102] Next, as shown in FIG. 10, a plating seed layer 150 is formed on the protective layer 130 formed on the insulating substrate 110.

[103] The plating seed layer 150 is formed not only on the top surface of the protective layer 130 but also on the inner wall of the groove 135.

[104] The plating seed layer 150 may be formed through a chemical copper plating scheme.

[105] The chemical copper plating scheme may include a degreasing process, a soft corrosion process, a preliminary catalytic treatment process, a catalytic treatment process, an activation process, an electroless plating scheme, and an anti-oxidation treatment process.

[106] Further, the copper plating is classified into a heavy copper plating of 2 ㎛ or more, a medium copper plating of 1~2 ㎛, and a light copper plating of 1 ㎛ or less. The plating seed layer 150 is formed through the medium copper plating or the light copper plating to satisfy a thickness of 0.5~1.5 ㎛.

[107] Next, as shown in FIG. 11, the dry film 160 is formed on the plating seed layer 150.

[108] The dry film 160 may have the opening 165 for opening a portion corresponding to a region in which the pad 170 is formed.

[109] At this time, the dry film 160 surrounds the entire surface of the plating seed layer 150, and thus, the opening 165 may be formed to open the region in which the pad 170 is formed.

[110] Further, the opening 165 of the dry film 160 has an upper width and a lower width equal to each other. In addition, the upper and lower widths of the opening 165 are

equal to the upper width of the groove 135.

[111] Next, as shown FIG. 12, the groove 135 formed in the protective layer 130 and the opening 165 formed in the dry film 160 are filled with the pad 170.

[112] The pad 170 may be formed by electroplating metal such as copper using the plating seed layer 150 as a seed layer.

[113] Thus, a portion of the pad 170 has a shape corresponding to the groove 135 and the other portion of the pad 170 has a shape corresponding to the opening 165.

[114] Next, as shown in FIG. 13, the dry film 160 is delaminated.

[115] Next, as shown in FIG. 14, the plating seed layer 150, which is formed on a region except for the region in which the pad 170 is formed, is removed.

[116] A portion of the plating seed layer 150 exists at a lower portion of the pad 170. Thus, the entire structure of the pad 170 includes the plating seed layer 150.

[117] The pad 170 including the plating seed layer 130 is formed on the protective layer 130 through the method described above.

[118] That is, the pad 170 includes a first pad 172 which is buried in the protective layer 130 and of which both sides have a protrusion shape, and a second pad 174 which is formed on the first pad 172 and protrudes over the surface of the protective layer 130.

[119] The first pad 172 is buried in the protective layer 130, so that the adhesive strength between the pad 170 and the protective layer 130 is improved.

[120] In this case, the first pad 172 has a shape corresponding to the groove 135, so that an upper width B and a lower width A of the first pad 172 are different from each other.

[121] In more detail, the first pad 172 is formed to allow the upper width B to be narrower than the lower width A. That is, the first pad 172 has a shape of which a width is gradually narrowed upward, and thus, both sides of the first pad 172 have a protrusion shape.

[122] As described above, the first pad 172 is buried in the protective layer 130 and has the protrusion shape of which the upper and lower widths are different from each other, so that the adhesive strength between the entire structure of the pad 170 and the protective layer 130 is improved.

[123] The second pad 174 is an upper portion of the first pad 172 and protrudes over the surface of the protective layer 130.

[124] The second pad 174 has a shape corresponding to the opening 165, so that an upper width and a lower width of the second pad 174 are equal to each other.

[125] At this time, the upper and lower portions of the second pad 174 have the same width at that of the upper portion of the first pad 172.

[126] Since the second pad 174 protrudes over the protective layer 130, the semiconductor chip 300 is easily attached onto the semiconductor package substrate 100 by the second adhesive member 180 formed later.

[127] Next, as shown in FIG. 15, the second adhesive member 180 is formed on the pad 170.

[128] The second adhesive member 180 according to the first embodiment may be prepared as a solder ball or a micro ball.

[129] The second adhesive member 180 may be formed on the pad 170 through flux printing, ball printing, reflow, deflux and coining.

[130] To the contrary, as shown in FIG. 16, the second adhesive member 18 may be formed by coating the adhesive paste 182 on the pad 170.

[131] In addition, as shown in FIG. 17, the second adhesive member may be formed on the pad 170 by using a copper core solder ball 188 including a copper ball 184 and a solder 186 surrounding a peripheral surface of the copper ball 184.

[132] According to the embodiment described above, the copper pad and the adhesive member are formed on the semiconductor package substrate by using hybrid bump technology without using the expensive dummy die, so that the productivity of a package system may be improved and the product cost may be reduced.

[133] Further, according to the embodiment, since the pad is formed in the plurality of stack structure having mutually different widths by using hybrid bump technology, the adhesive strength of the pad to the adhesive member is improved, so that the reliability of the semiconductor package substrate may be improved.

[134] Further, according to the embodiment, since a portion of the pad is buried in the protective layer and the buried portion of the pad has the protrusion shape, the adhesive strength between the pad and the protective layer is increased, so that the reliability of the semiconductor package substrate may be improved.

[135] Further, as described above, since the second adhesive member is formed by using the copper core solder ball 188, a high standoff height may be maintained even after the reflow process, so that the reliability of the semiconductor package substrate may be improved.

[136] FIG. 18 is a view showing a semiconductor package substrate according to the second embodiment.

[137] Referring to FIG. 16, a semiconductor package substrate 200 according to the second embodiment includes an insulating substrate 210, a circuit pattern 225 formed on at least one surface of the insulating substrate 210, a protective layer 230 formed on the insulating substrate 210 to protect the circuit pattern 225, a first adhesive member 245 formed on the circuit pattern 225 formed on the surface opposite to the surface of the insulating substrate 210 on which a semiconductor chip 300 (which will be described below) is mounted, a pad 270 formed on the protective layer 230 formed on a top surface of the insulating substrate 210, and a second adhesive member 280 formed on the pad 270.

[138] The pad 270 includes a first pad 272 buried in the protective layer 230 and a second pad 274 formed on the first pad 272.

[139] The insulating substrate 210 may include a thermosetting polymer substrate, a thermoplastic polymer substrate, a ceramic substrate, an organic/inorganic composite substrate or an impregnated fiberglass substrate. If the insulating substrate 210 includes polymer resin, the insulating substrate 210 may include epoxy insulating resin. In addition, the insulating substrate 210 may include polyimide resin.

[140] The circuit pattern 225 is formed on at least one surface of the insulating substrate 210.

[141] The circuit pattern 225 may be formed of a conductive material and may be formed by simultaneously patterning thin copper layers formed on both surfaces of the insulating substrate 210.

[142] The circuit pattern 225 may be formed of alloy including copper and a roughness may be formed on a surface of the circuit pattern 225.

[143] The protective layer 230 is formed on the insulating substrate 210 to coat the circuit pattern 225 formed on the top surface of the insulating substrate 210 and expose a portion of the circuit pattern 225 formed on the bottom surface of the insulating substrate 210.

[144] The protective layer 230, which is for protecting the surfaces of the insulating substrate 210, is formed on the entire surfaces of the insulating substrate 210 and has an opening (not shown) which opens the surface of the circuit pattern 225, that is, the surface of a stack structure of the circuit pattern 225 formed on the bottom surface.

[145] The protective layer 130 may include at least one layer formed of one of SR (Solder Resist), oxide and Au.

[146] A first adhesive member 245 is formed on the surface of the circuit pattern 225 exposed through the protective layer 230.

[147] The first adhesive member 245 is formed for the purpose of attaching a conductive ball to separately package it together with a substrate in future.

[148] The pad 270 is formed on the protective layer 230.

[149] The pad 270 is formed on the protective layer 230 which coats the entire surface of the circuit pattern 225, and does not make contact with the insulating substrate 210 or the circuit pattern 225.

[150] The pad 170 may be formed of a conductive material such as copper.

[151] The pad 270 is formed on the protective layer 230 for the purpose of attaching the semiconductor chip 300 onto the semiconductor package substrate 200 in future.

[152] FIG. 19 is a view showing a detailed structure of the pad depicted in FIG. 18.

[153] Referring to FIG. 19, the pad 270 includes a first pad 272 which is buried in the protective layer 230 and has both sides having a protrusion shape, and a second pad

274 which is formed on the first pad 272 and protrudes over the surface of the protective layer 230.

[154] The first pad 272 is buried in the protective layer 230, so that the adhesive strength between the pad 270 and the protective layer 230 is improved.

[155] At this time, the first pad 272 is formed to have an upper width B and a lower width A different from each other.

[156] In more detail, the first pad 272 is formed to allow the upper width B to be narrower than the lower width A. That is, the first pad 272 has a shape of which a width is gradually narrowed upward, and thus, both sides of the first pad 272 have a protrusion shape.

[157] As described above, the first pad 272 is buried in the protective layer 130 and has the protrusion shape of which the upper and lower widths are different from each other, so that the adhesive strength between the entire structure of the pad 270 and the protective layer 230 is improved.

[158] The second pad 274 is an upper portion of the first pad 272 and protrudes over the surface of the protective layer 230.

[159] The upper and lower widths of the second pad 274 are equal to each other.

[160] The upper and lower portions of the second pad 274 have the width narrower than that of the upper portion of the first pad 272.

[161] Since the second pad 274 protrudes over the protective layer 230, the semiconductor chip 300 is easily attached onto the semiconductor package substrate 200 by the second adhesive member 280 formed later.

[162] The width of the second pad 272 is formed to be narrower than the upper width of the first pad 272, so that the adhesive strength between the pad 270 and the protective layer 230 is improved.

[163] That is, in the second embodiment, the first and second pads 272 and 274 are formed in order to attach the semiconductor chip 300. The width of the second pad 274 is narrower than the upper width of the first pad 272, so that the adhesive strength of the second adhesive member 280 may be enhanced.

[164] The second adhesive member 280 is formed on the second pad 274.

[165] The second adhesive member 280 is formed on the second pad 274, so that the adhesive strength between the semiconductor chip 300 and the semiconductor package substrate 200 is provided.

[166] The second adhesive member 280 may be formed of a general solder ball. To the contrary, the second adhesive member 280 may be formed by using adhesive paste or a copper core solder ball.

[167] Further, the adhesive paste may include a conductive material. When the adhesive paste is formed of conductive material, the adhesive paste may include a conductive

material selected from the group consisting of Ag, cu, Au, Al, carbon nano-tube and combination thereof.

[168] According to the embodiment describe above, the copper pad and the adhesive member are formed on the semiconductor package substrate without using the expensive dummy die, so that the productivity of a package system may be improved and the product cost may be reduced.

[169] FIGS. 20 to 25 are views illustrating a method of manufacturing a semiconductor package substrate depicted in FIG. 18 in the process sequence.

[170] First, as shown in FIG. 20, the insulating substrate 210 is prepared and a metallic layer 220 is laminated on at least one surface of the insulating substrate 210.

[171] At this time, when the insulating substrate 210 is an insulation layer, the lamination structure of the insulation layer and the metallic layer 220 may be conventional CCL (Copper Clad Laminate).

[172] Further, the metallic layer 220 may be formed on the insulating substrate 210 through an electroless plating scheme. When the metallic layer 120 is formed through the electroless plating scheme, a roughness is formed to the surface of the insulating substrate 210, so that the electroless plating may be smoothly performed.

[173] The insulating substrate 210 may include epoxy resin or polyimide resin without using an expensive ceramic material having high thermal conductivity. The insulating substrate 210 may be a copper foil of a thin film including copper of high thermal conductivity and or low resistance.

[174] Next, the circuit pattern 225 is formed by etching the metallic layer 220 formed on the top and bottom surfaces of the insulating substrate 210 in a predetermined pattern.

[175] At this time, the circuit pattern 225 may be formed by performing the etching through a photolithography process or a laser process in which a pattern is directly formed by using a laser.

[176] Next, the protective layer 230, in which the circuit pattern 225 is buried, is formed at the upper and lower portions of the insulating substrate 210.

[177] The protective layer 230, which is for the purpose of protecting the surface of the insulating substrate 210 or the circuit pattern 225, may include at least one layer formed by using at least one of solder resist, oxide or Au.

[178] Next, the protective layer 230 formed at the lower portion of the insulating substrate 210 is processed, such that the surface of the circuit pattern 225 formed at the bottom surface of the insulating substrate 210 is exposed.

[179] Then, the first adhesive member 245 is formed on the exposed circuit pattern 225.

[180] In order to attach other substrate (not shown) onto the semiconductor package substrate 200, the first adhesive member 245 is used for the purpose of attaching the solder ball which provides the adhesive strength between the semiconductor package

substrate 200 and other substrate.

[181] Then, a groove 235 is formed in the protective layer 230 formed above the insulating substrate 210.

[182] Here, upper and lower widths of the groove 235 are different from each other.

[183] That is, the groove 235 is formed to have the upper and lower widths different from each other through an expose energy control.

[184] At this time, the groove 235 is formed such that the upper width is narrower than the lower width.

[185] That is, the groove 235 has a protrusion shape having a width which is gradually narrowed upward.

[186] Then, a plating seed layer 250 is formed on the protective layer 230 formed on the insulating substrate 210.

[187] The plating seed layer 250 is formed not only on the top surface of the protective layer 230 but also on the inner wall of the groove 235.

[188] The plating seed layer 250 may be formed through a chemical copper plating scheme.

[189] The chemical copper plating scheme may include a degreasing process, a soft corrosion process, a preliminary catalytic treatment process, a catalytic treatment process, an activation process, an electroless plating scheme, and an anti-oxidation treatment process.

[190] Next, as shown in FIG. 21, the dry film 260 is formed on the plating seed layer 250.

[191] The dry film 260 may have the opening 265 for opening a portion corresponding to a region in which the pad 270 is formed.

[192] At this time, the dry film 260 surrounds the entire surface of the plating seed layer 250, and thus, the opening 265 may be formed to open the region in which the pad 270 is formed.

[193] Further, the opening 265 of the dry film 260 has an upper width and a lower width equal to each other. In addition, the upper and lower widths of the opening 265 are narrower than the upper width of the groove 235.

[194] Next, as shown FIG. 22, the groove 235 formed in the protective layer 230 and the opening 265 formed in the dry film 260 are filled with the pad 270.

[195] The pad 270 may be formed by electro plating metal such as copper using the plating seed layer 250 as a seed layer.

[196] Thus, a portion of the pad 270 has a shape corresponding to the groove 235 and the other portion of the pad 270 has a shape corresponding to the opening 265.

[197] Next, as shown in FIG. 23, the dry film 260 is delaminated.

[198] Next, as shown in FIG. 24, the plating seed layer 250, which is formed on a region except for the region in which the pad 270 is formed, is removed.

[199] At this time, a portion of the plating seed layer 250 exists below the pad 270. Thus, the entire structure of the pad 170 includes the plating seed layer 250.

[200] The pad 270 including the plating seed layer 230 is formed on the protective layer 230 through the method described above.

[201] That is, the pad 270 includes a first pad 272 which is buried in the protective layer 230 and has both sides having a protrusion shape, and a second pad 274 which is formed on the first pad 272 and protrudes over the surface of the protective layer 230.

[202] The first pad 272 is buried in the protective layer 230, so that the adhesive strength between the pad 270 and the protective layer 230 is improved.

[203] At this time, the first pad 272 is formed to have an upper width B and a lower width A different from each other.

[204] In more detail, the first pad 272 is formed to allow the upper width B to be narrower than the lower width A. That is, the first pad 272 has a shape of which a width is gradually narrowed upward, and thus, both sides of the first pad 272 have a protrusion shape.

[205] As described above, the first pad 272 is buried in the protective layer 230 and has the protrusion shape of which the upper and lower widths are different from each other, so that the adhesive strength between the entire structure of the pad 170 and the protective layer 230 is improved.

[206] The second pad 274 is an upper portion of the first pad 272 and protrudes over the surface of the protective layer 230.

[207] The upper and lower widths of the second pad 274 are equal to each other.

[208] The upper and lower portions of the second pad 274 have the width narrower than that of the upper portion of the first pad 272.

[209] Since the second pad 274 protrudes over the protective layer 230, the semiconductor chip 300 is easily attached onto the semiconductor package substrate 200 by the second adhesive member 280 formed later.

[210] The width of the second pad 272 is formed to be narrower than the upper width of the first pad 272, so that the adhesive strength between the pad 270 and the semiconductor chip 300 is improved.

[211] Next, as shown in FIG. 25, the second adhesive member 280 is formed on the pad 270.

[212] The second adhesive member 280 may be formed of a solder ball or a micro ball. To the contrary, the second adhesive member 280 may be formed of an adhesive paste or a copper core solder ball including a copper ball and a solder surrounding a peripheral surface of the copper ball.

[213] According to the embodiment described above, the copper pad and the adhesive member are formed on the semiconductor package substrate by using hybrid bump

technology without using the expensive dummy die, so that the productivity of a package system may be improved and the product cost may be reduced.

[214] Further, according to the embodiment, since the pad is formed in the plurality of stack structure having mutually different widths by using hybrid bump technology, the adhesive strength of the pad to the adhesive member is improved, so that the reliability of the semiconductor package substrate may be improved.

[215] Further, according to the embodiment, since a portion of the pad is buried in the protective layer and the buried portion of the pad has the protrusion shape, the adhesive strength between the pad and the protective layer is increased, so that the reliability of the semiconductor package substrate may be improved.

[216] FIGS. 26 and 27 are views showing a package system according to the embodiment.

[217] Referring to FIG. 26, the package system includes a semiconductor package substrate 100 and a memory chip 300 formed on the semiconductor package substrate 100.

[218] The memory chip 300 may be a nand flash memory chip.

[219] At this time, the memory chip 300 is attached onto the semiconductor package substrate 100 with the pad 170 and the second adhesive member 180 which are formed on the semiconductor package substrate 100.

[220] As described above, in order to attach the memory chip 300, separately from the process of fabricating the semiconductor package substrate 100, the memory chip 300 is attached onto the pad 170 and the second adhesive member 180, which are formed during the process of fabricating the semiconductor package substrate 100, by using hybrid bump technology without forming an expensive dummy die.

[221] Further, a portion of the pad 100 has the protrusion shape and is buried in the protective layer 130, so that high reliability may be obtained in the ball shear test and ball pull test which are factors to determine the reliability of the pad.

[222] FIG. 28 is a view to compare a package system according to the embodiment with a package system according to the related art.

[223] Referring to FIG. 28, according to the related art, an expensive dummy die 20 is formed on a package substrate 10, so that a memory chip 30 is formed on the dummy die 20.

[224] Thus, a process of fabricating a package system according to the related art is substantially divided into 3 steps.

[225] In the first step of the 3 steps, the package substrate 10 is fabricated.

[226] Then, in the second step, the dummy die 20 is formed on the package substrate 10. At this time, the first and second steps are not achieved at a time, but performed with several steps due to the process characteristics.

[227] Finally, in third step, the semiconductor chip 30 is formed on the dummy die 20.

[228] However, according to the embodiment, the memory chip 300 is attached onto the

pad 170 and the second adhesive member 180 by using hybrid bump technology.

[229] Thus, the process of fabricating a package system according to the embodiment is divided into 2 steps.

[230] In the first step of the 2 steps, the package substrate 100 is fabricated. In this time, the step of fabricating the package substrate 100 includes the step of forming the pad 170 and the second adhesive member 180 by using hybrid bump technology.

[231] Then, in the second step, the memory chip 300 is attached onto the pad 170 and the second adhesive member 180 by using hybrid bump technology.

[232] As describe above, according to the embodiment, by using hybrid bump technology without using an expensive dummy die, the memory chip 300 is attached onto the pad 170 and the second adhesive member 180, so that the fabrication cost may be reduced and in addition, the fabrication process may be simplified.

[233] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

[Claim 1] A semiconductor package substrate comprising:
an insulation substrate;
a circuit pattern on the insulation substrate;
a protection layer on the insulation substrate, the protection layer covering the circuit pattern on the insulation substrate;
a pad on the protection layer; and
an adhesive member on the protection layer,
wherein the pad includes a first pad buried in the protection layer, and a second pad on the first pad, the second pad protruding over the protection layer.

[Claim 2] The semiconductor package substrate of claim 1, wherein the first pad has a shape of a protrusion having a lower width and an upper width different from each other.

[Claim 3] The semiconductor package substrate of claim 2, wherein the first pad has a width gradually narrowed upward.

[Claim 4] The semiconductor package substrate of claim 1, wherein the second pad has a shape of a column having a lower width and an upper width equal to each other.

[Claim 5] The semiconductor package substrate of claim 4, wherein the second pad has a width equal to the upper width of the first pad.

[Claim 6] The semiconductor package substrate of claim 4, wherein the second pad has a width narrower than the upper width of the first pad.

[Claim 7] The semiconductor package substrate of claim 1, wherein the adhesive member provides an adhesive strength between the pad and a semi-conductor chip attached onto the pad.

[Claim 8] The semiconductor package substrate of claim 1, wherein the first pad further includes a plated seed layer formed at a lower portion of the first pad.

[Claim 9] The semiconductor package substrate of claim 1, wherein the adhesive member includes one of a solder ball, a micro ball, an adhesive paste and a copper core solder ball.

[Claim 10] The semiconductor package substrate of claim 1, wherein the protection layer includes one of solder resister, oxide and Au.

[Claim 11] The semiconductor package substrate of claim 1, wherein the firs pad makes contact with the protection layer without making contact with the circuit pattern and the insulation substrate.

[Claim 12] A package system comprising:
a semiconductor package substrate including an insulation substrate, a circuit pattern formed on one surface of the insulation substrate, and a protection layer formed on the insulation substrate while covering the circuit pattern; and
a semiconductor chip attached onto the semiconductor package substrate,
wherein the semiconductor package substrate comprises:
a pad plated on the protection layer; and
an adhesive member on the pad, and
wherein the semiconductor chip is attached onto the pad form on the semiconductor package substrate by the adhesive member.

[Claim 13] The package system of claim 12, wherein the pad includes a first pad buried in the protection layer, and
a second pad on the first pad, the second pad protruding over a surface of the protection layer.

[Claim 14] The package system of claim 13, wherein the first pad has a width gradually narrowed upward.

[Claim 15] The package system of claim 13, wherein the second pad has a shape of a column having a lower width and an upper width equal to each other.

[Claim 16] The package system of claim 15, wherein the second pad has a width equal to or narrower than the upper width of the first pad.

[Claim 17] The package system of claim 12, wherein the adhesive member includes one of a solder ball, a micro ball, an adhesive paste and a copper core solder ball.

[Claim 18] The package system of claim 12, wherein the protection layer includes one of solder resister, oxide and Au.

[Claim 19] The package system of claim 12, wherein the firs pad makes contact with the protection layer without making contact with the circuit pattern and the insulation substrate.

[Claim 20] A method of manufacturing a package system, the method comprising:
forming a circuit pattern on at least one surface of an insulation substrate;
forming a protection layer on the insulation substrate to cover the circuit pattern;
forming a groove in the protection layer;
forming a dry film having an opening of exposing the groove on the protection layer;

forming a pad to fill the groove of the protection layer and the opening of the dry film; and

forming an adhesive member on the pad.

[Claim 21] The method of claim 20, wherein the forming of the groove includes forming the groove for opening a top surface of the protection layer, and

wherein the groove includes an upper width and a lower width different from each other.

[Claim 22] The method of claim 21, wherein the forming of the groove includes forming the groove having a shape of a protrusion with a width gradually narrowed upward.

[Claim 23] The method of claim 22, wherein the forming of the dry film includes forming the dry film having an opening with a shape of a column having an upper width and a lower width equal to each other.

[Claim 24] The method of claim 23, wherein a width of the opening is equal to or narrower than an upper width of the groove.

[Claim 25] The method of claim 24, wherein the forming of the pad includes:

forming a first pad to fill the groove, the first pad having a shape corresponding to the shape of the groove; and

forming a second pad to fill the opening, the second pad having a shape corresponding to the shape of the opening.

[Claim 26] The method of claim 24, wherein the forming of the pad includes forming the pad on the protection layer such that the pad makes contact with the protection layer without making contact with the insulation substrate and the circuit pattern.

[Claim 27] The method of claim 25, further comprising:

forming a plated seed layer on the protection layer having the groove,

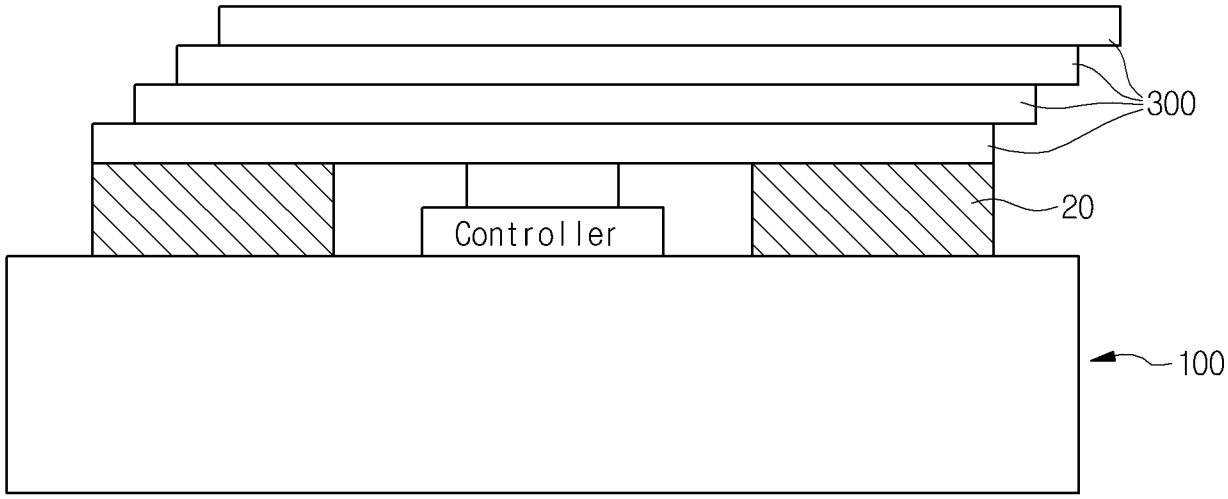
wherein the first pad is formed on a lower portion and a side portion thereof with the plated seed layer.

[Claim 28] The method of claim 20, wherein the forming of the adhesive member includes forming at least one of a solder ball, a micro ball, an adhesive paste and a copper core solder ball on the pad.

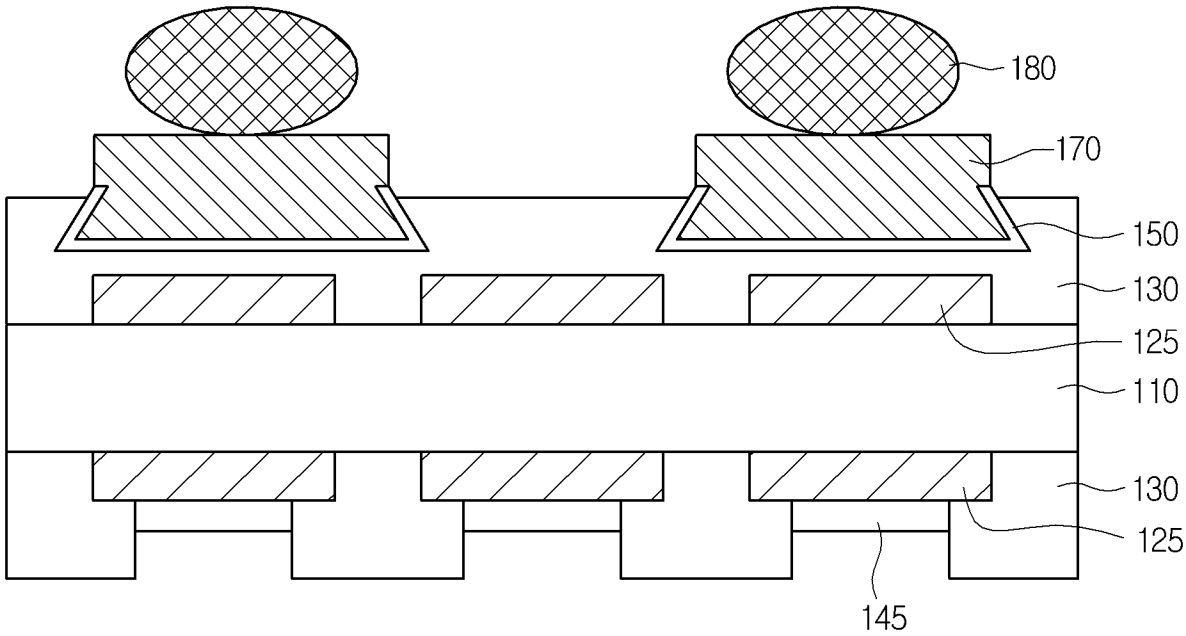
[Claim 29] The method of claim 20, further comprising:

attaching a semiconductor chip onto the adhesive member

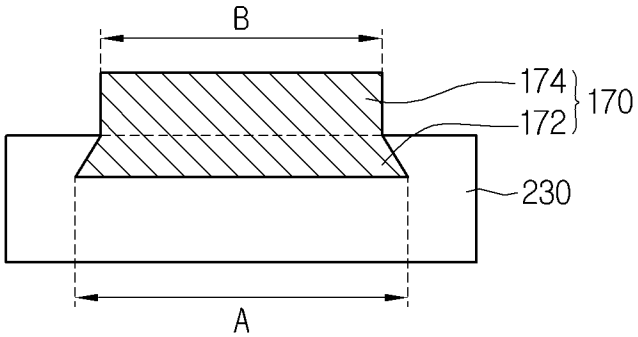
[Fig. 1]



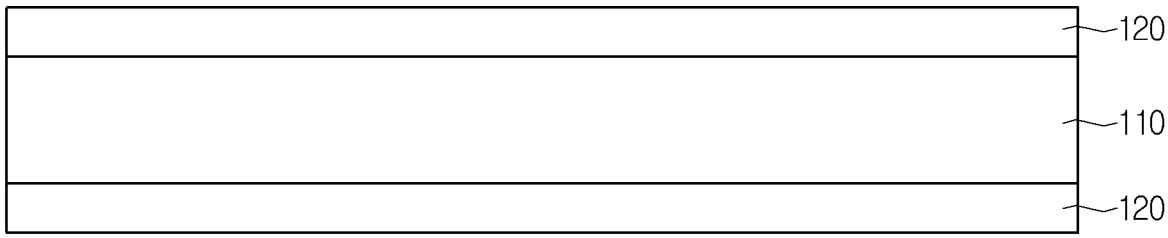
[Fig. 2]



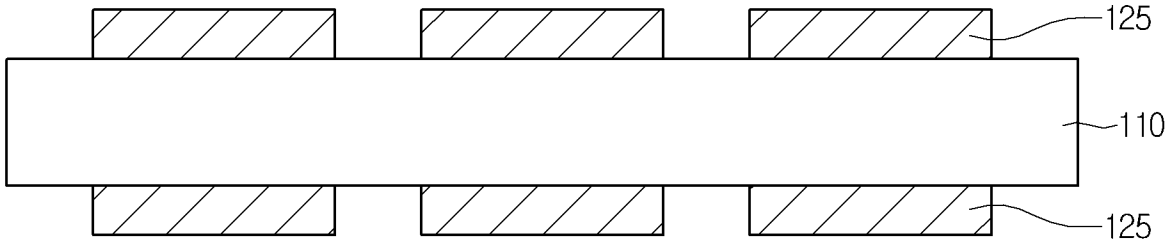
[Fig. 3]



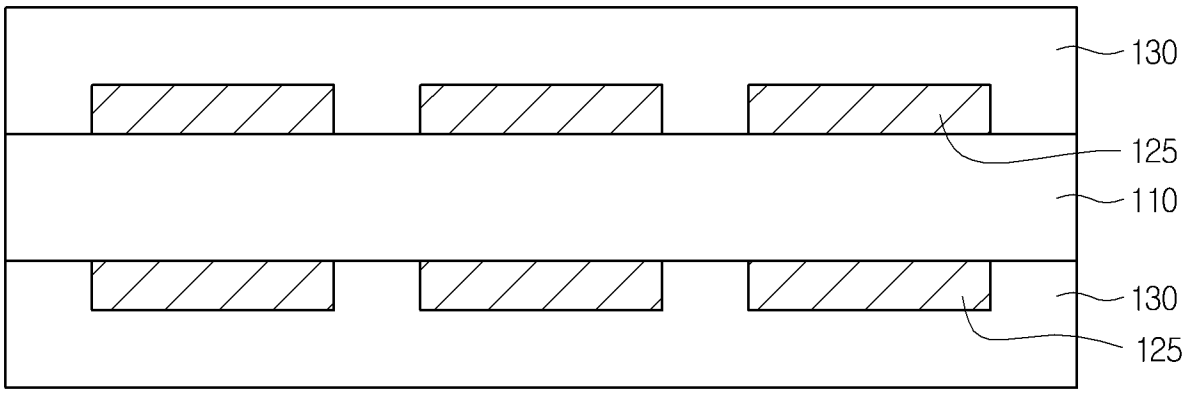
[Fig. 4]



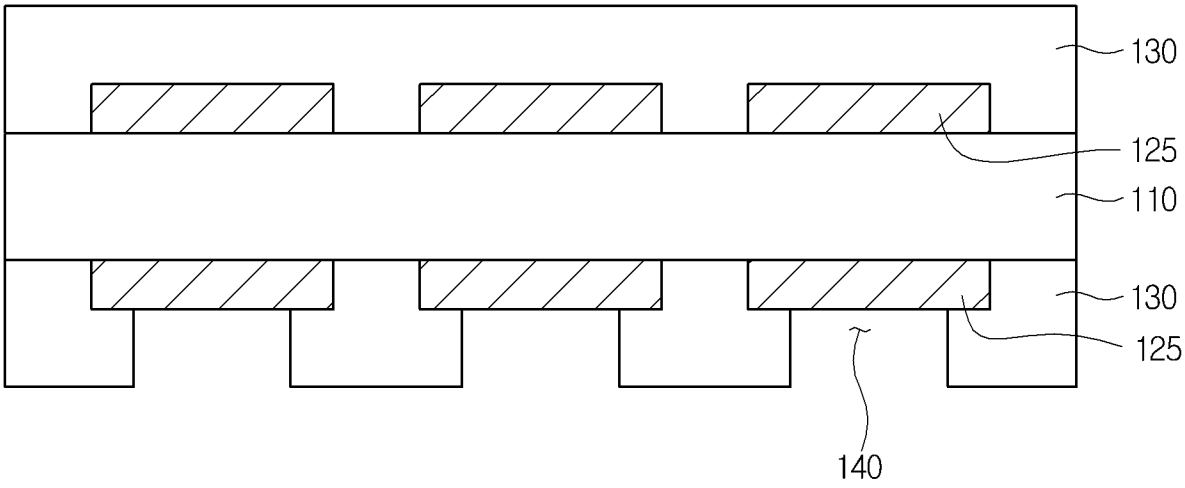
[Fig. 5]



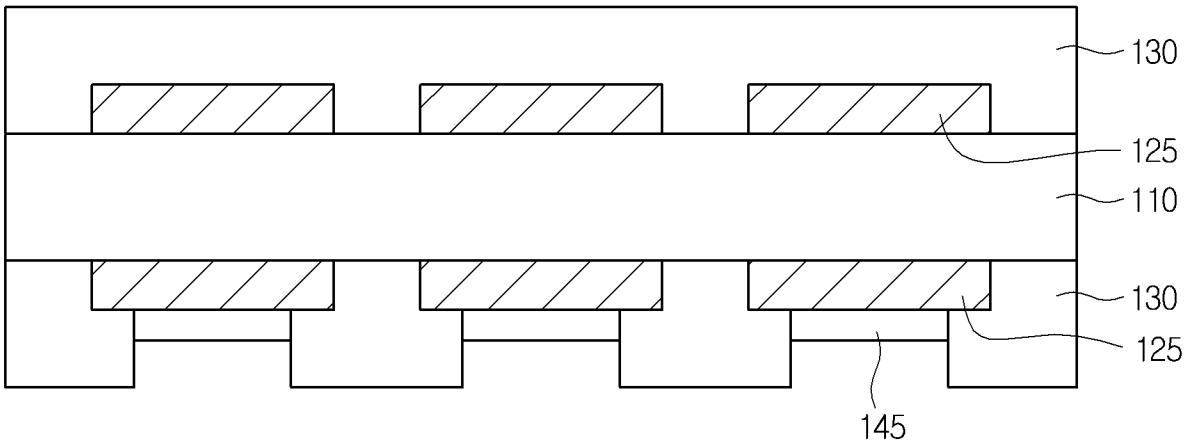
[Fig. 6]



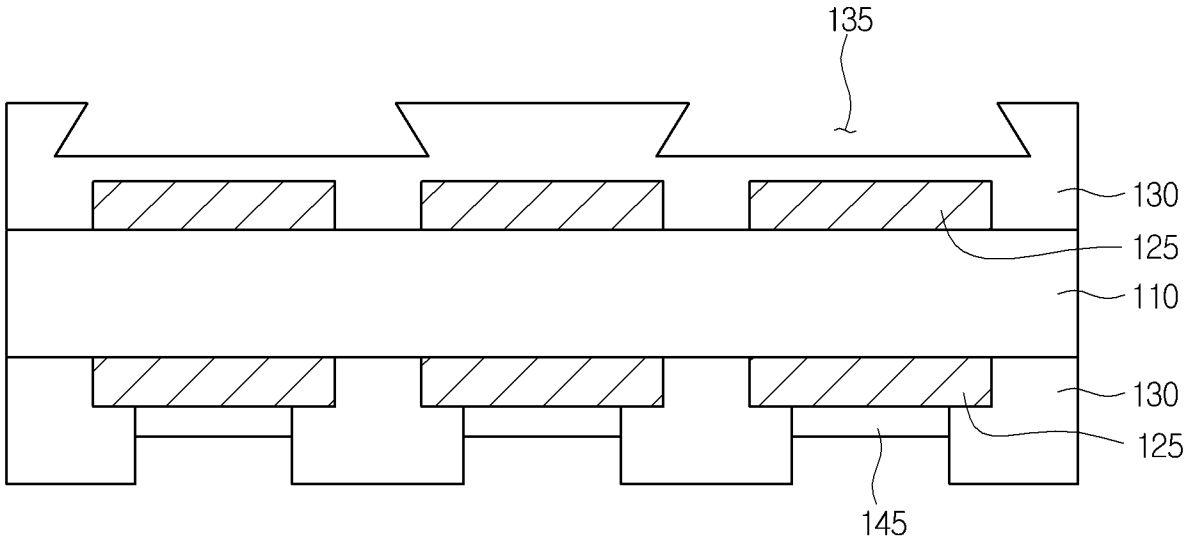
[Fig. 7]



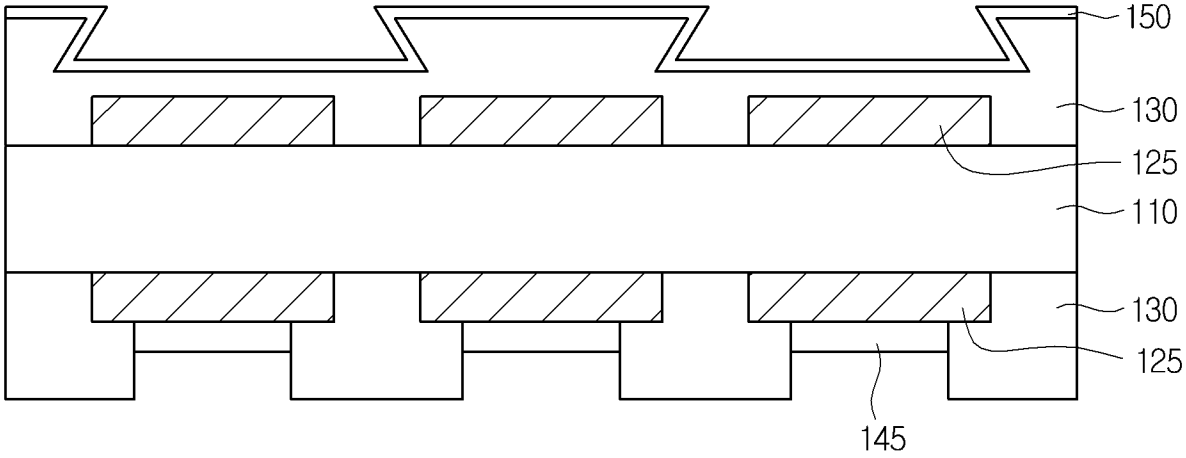
[Fig. 8]



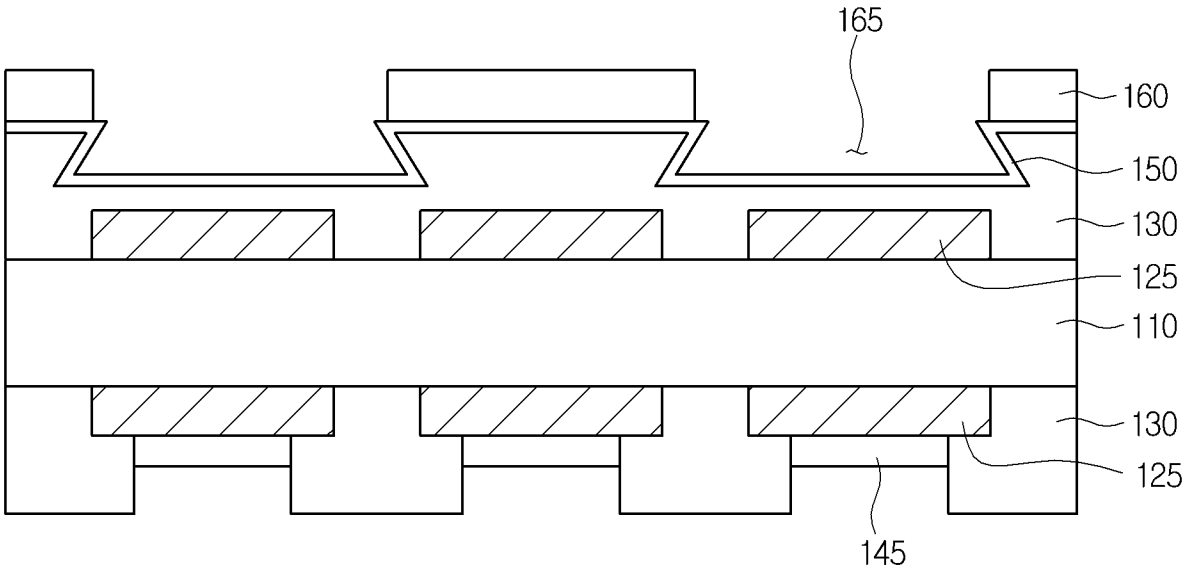
[Fig. 9]



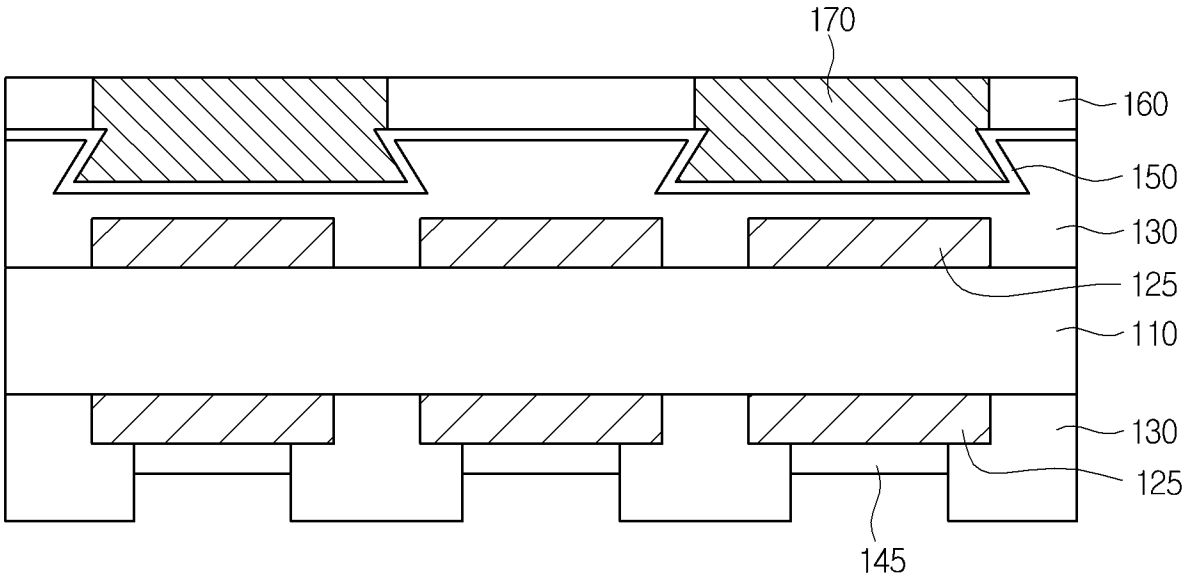
[Fig. 10]



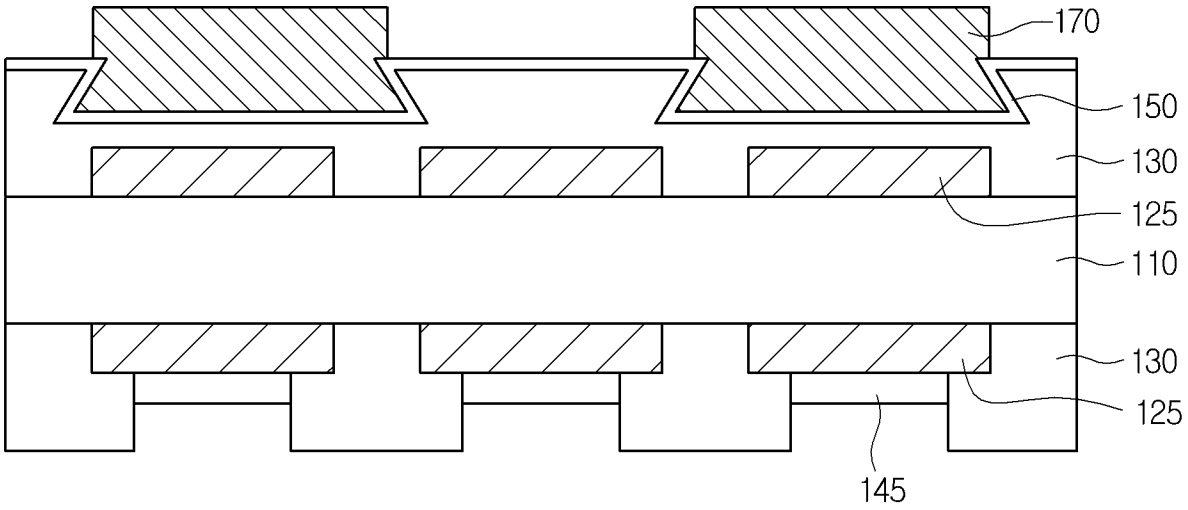
[Fig. 11]



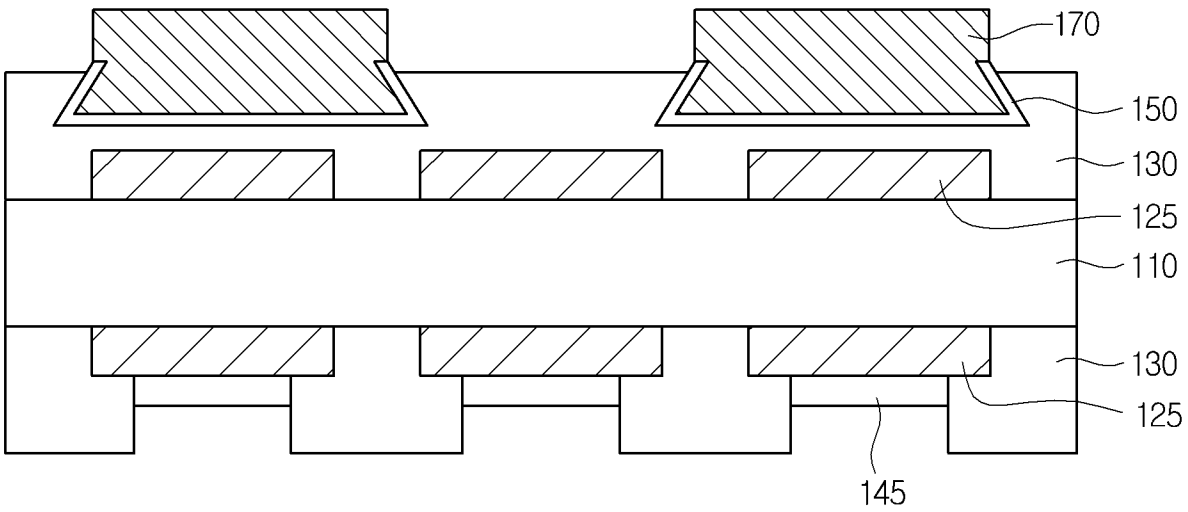
[Fig. 12]



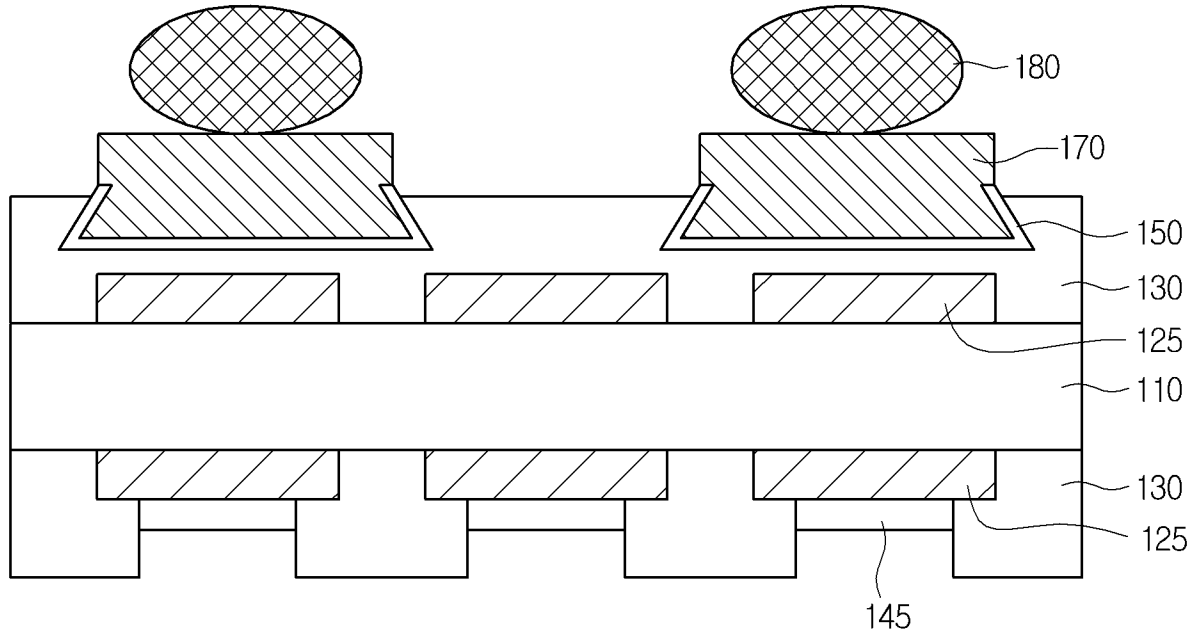
[Fig. 13]



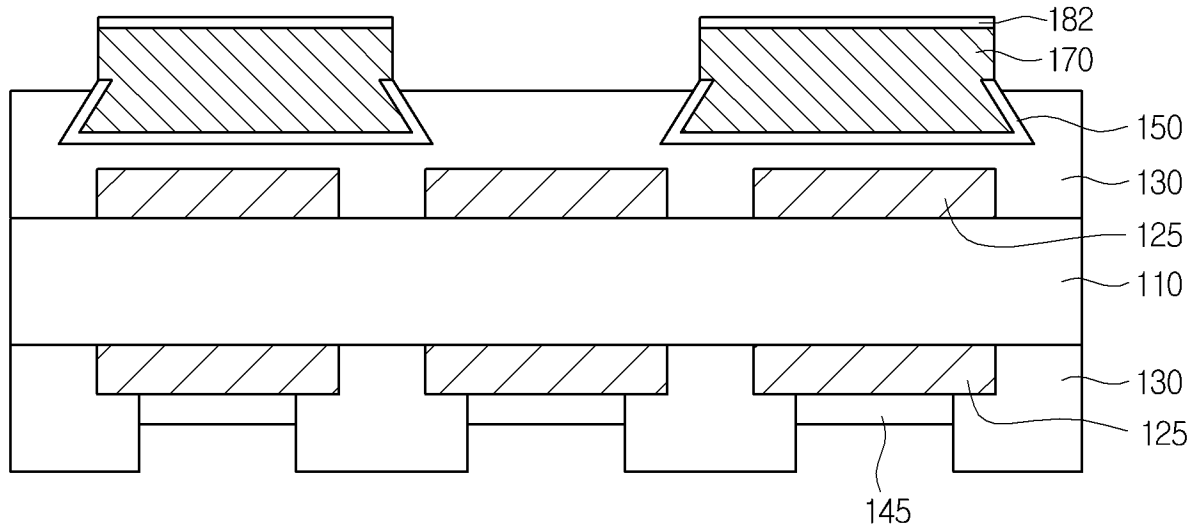
[Fig. 14]



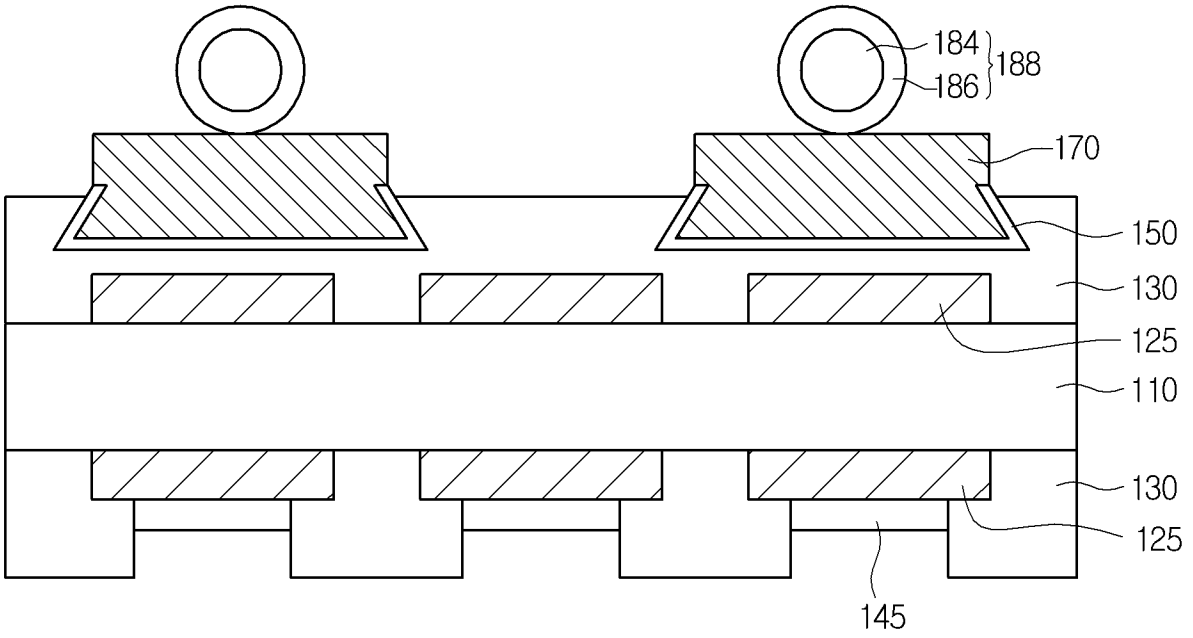
[Fig. 15]



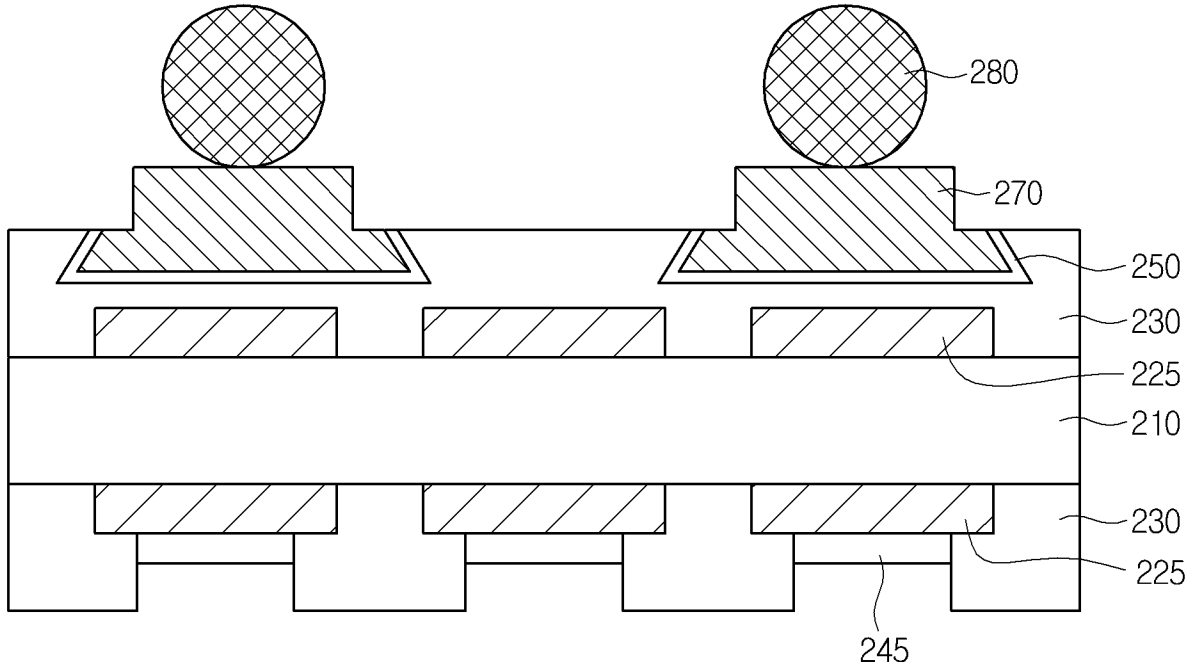
[Fig. 16]



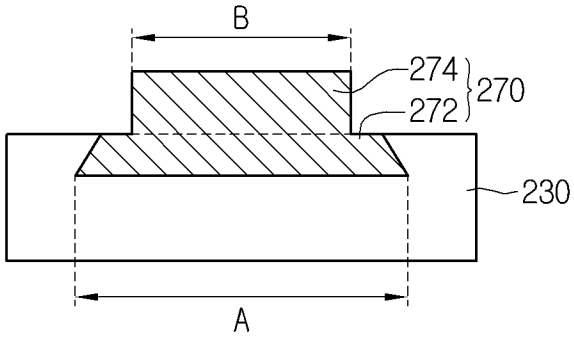
[Fig. 17]



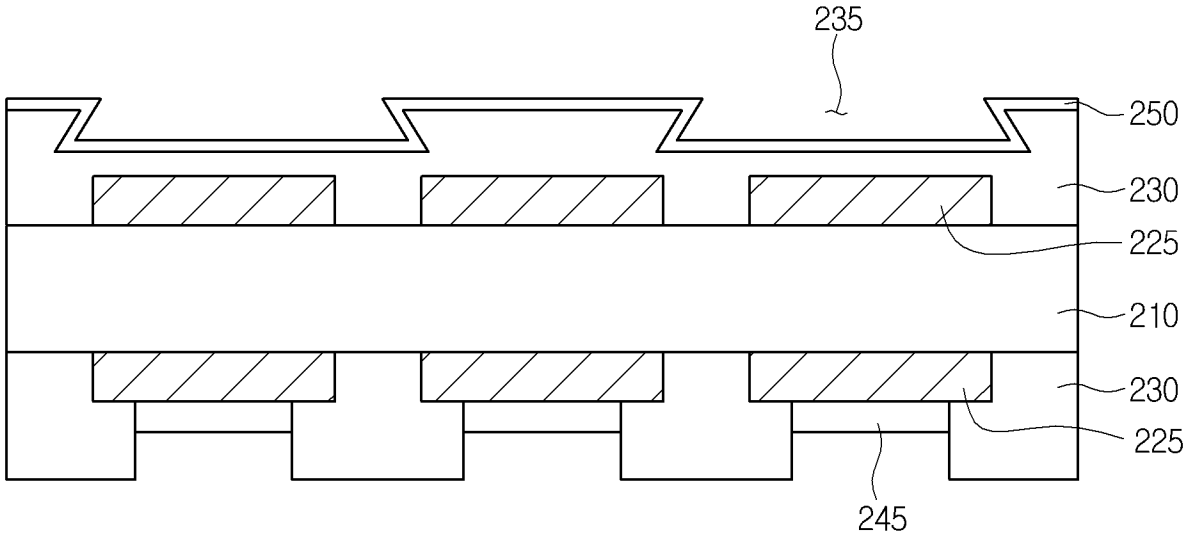
[Fig. 18]



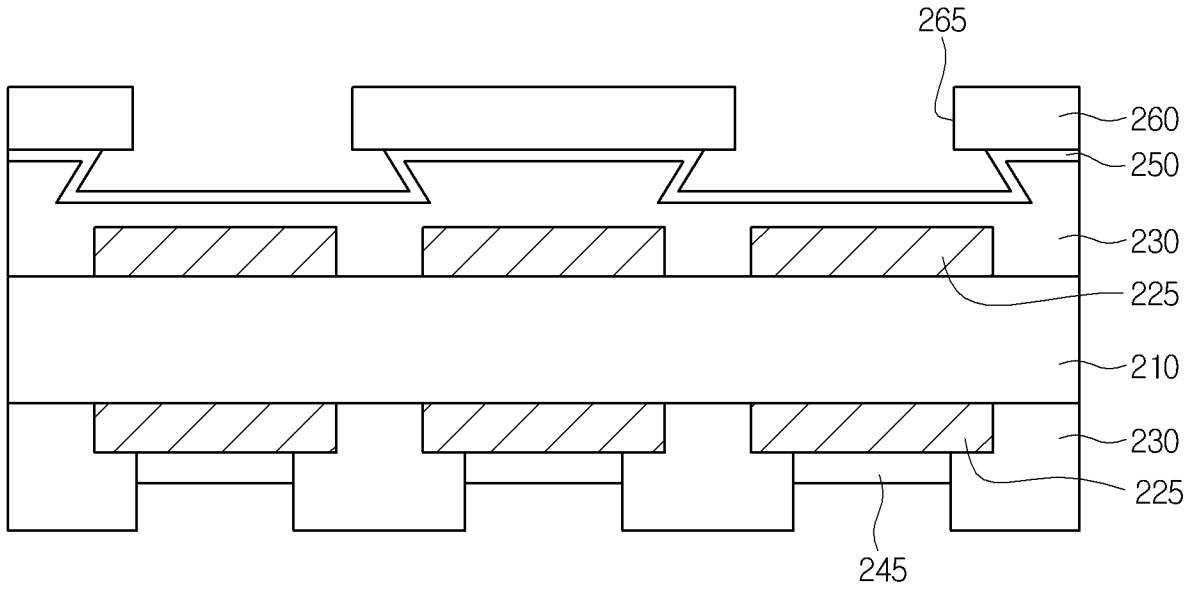
[Fig. 19]



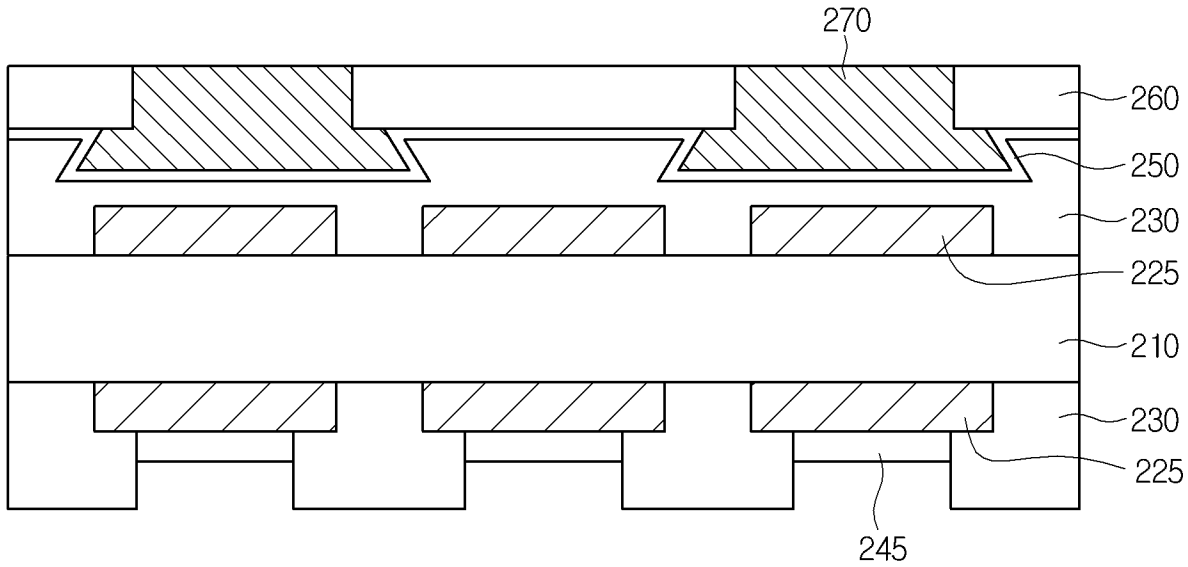
[Fig. 20]



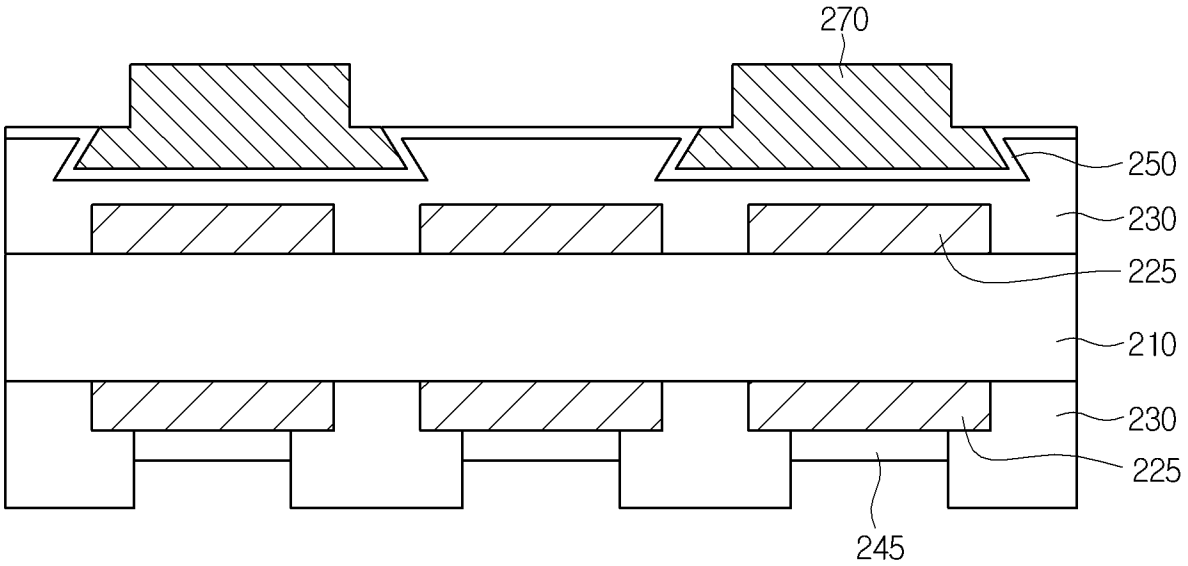
[Fig. 21]



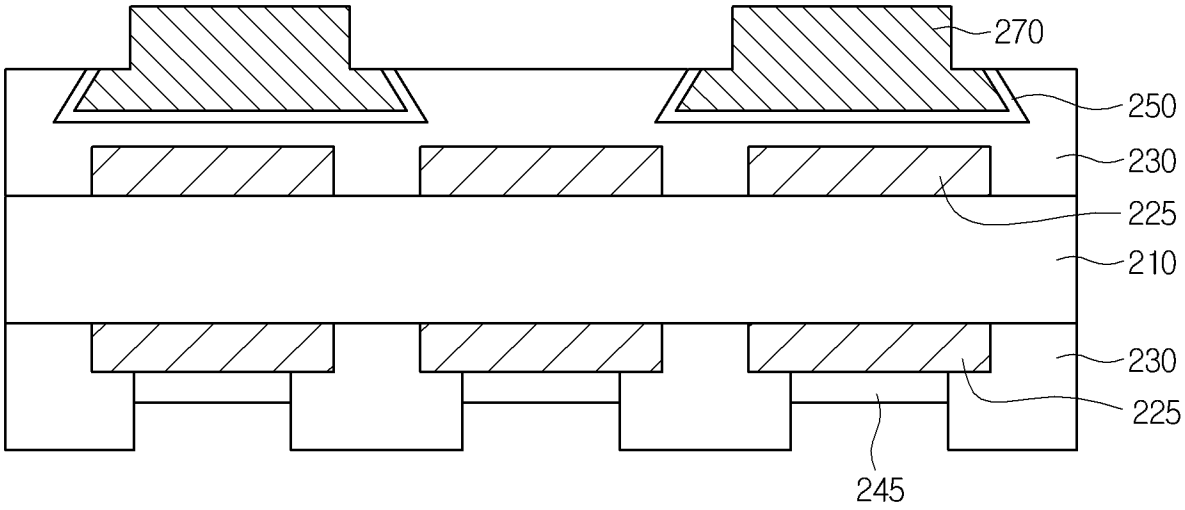
[Fig. 22]



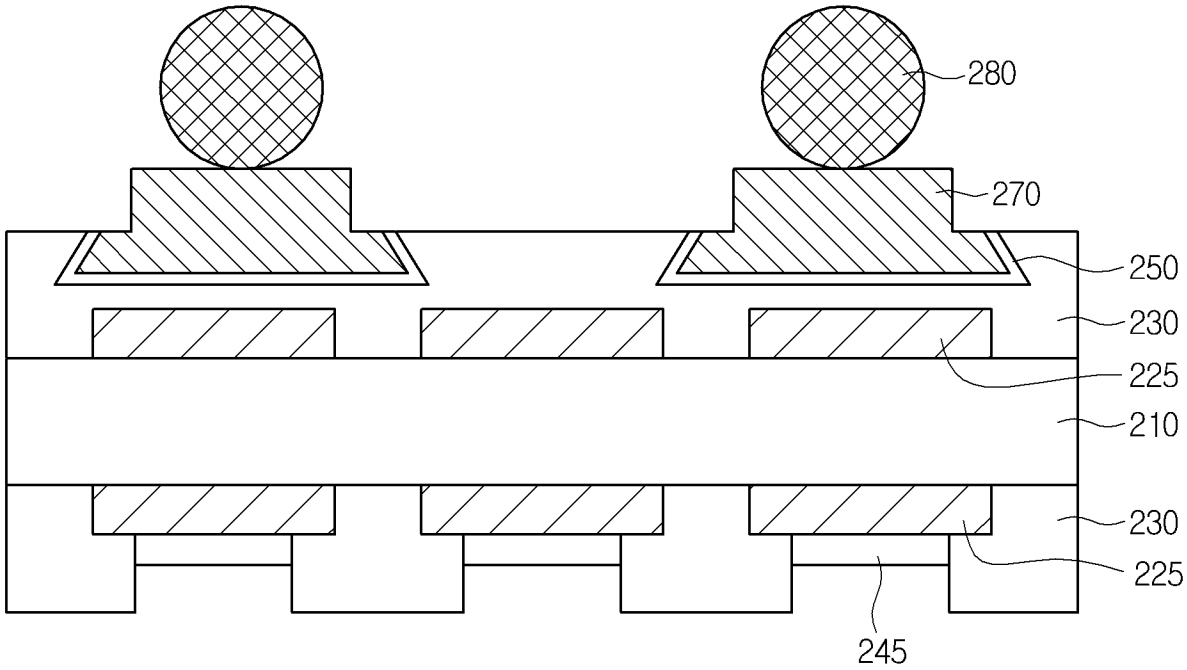
[Fig. 23]



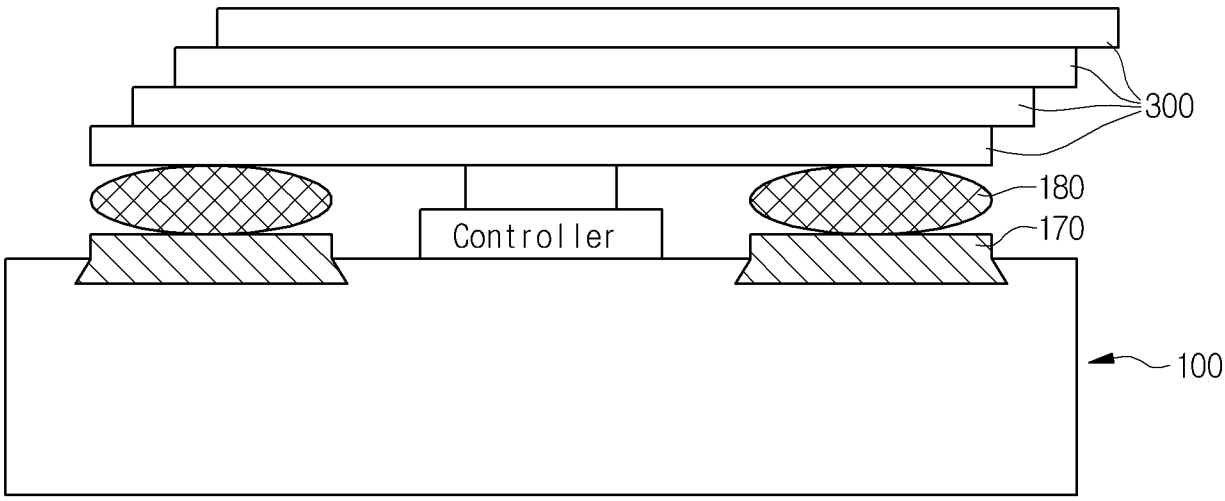
[Fig. 24]



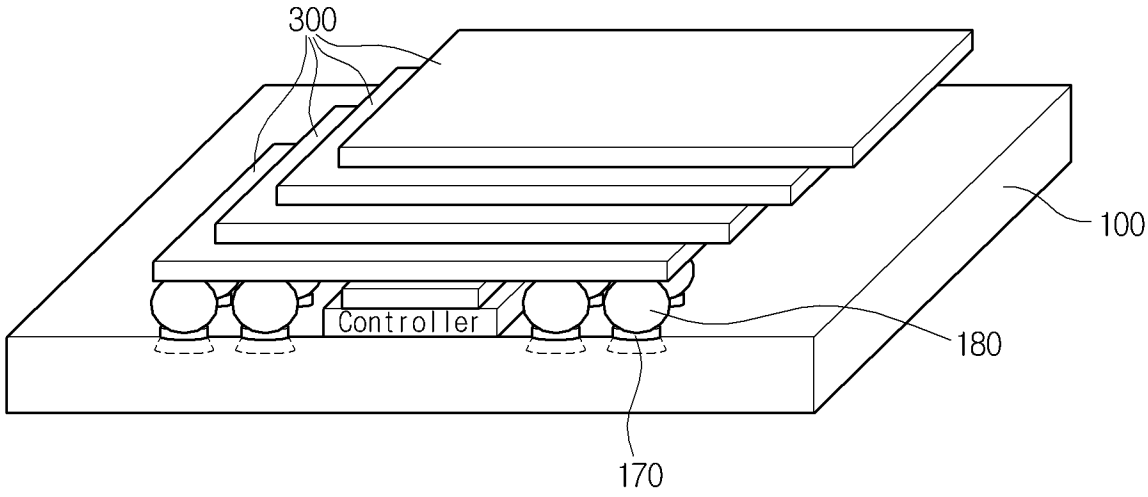
[Fig. 25]



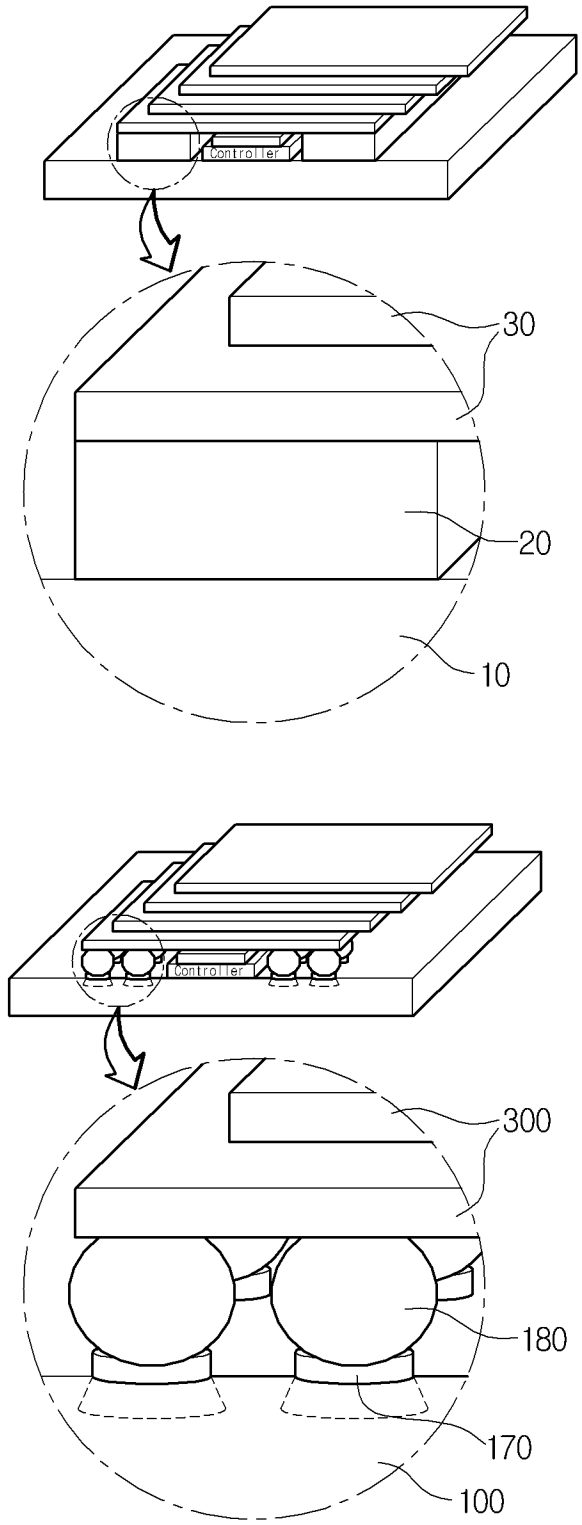
[Fig. 26]



[Fig. 27]



[Fig. 28]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2013/004579

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/12(2006.01)i, H01L 23/15(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/12; H01L 21/60; H01L 21/56; H01L 23/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: "package, substrate, pattern, protective layer, pad"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2006-0085464 A (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 27 July 2006 See claims 1-5; and figures 1-5; and pages 2-4.	1-19
A		20-29
Y	KR 10-2006-0094248 A (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 29 August 2006 See claims 1-12; and figures 1-7; and pages 3-7.	1-19
A		20-29
Y	KR 10-2000-0002962 A (SAMSUNG ELECTRONICS CO., LTD.) 15 January 2000 See claims 1-34; and figures 1-7; and pages 2-4.	20-29
A		1-19
Y	KR 10-2011-0029466 A (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 23 March 2011 See claims 1-9; and figures 1-4; and pages 5-10.	20-29
A		1-19

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 October 2013 (24.10.2013)	**24 October 2013 (24.10.2013)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2013/004579

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2006-0085464 A	27/07/2006	None	
KR 10-2006-0094248 A	29/08/2006	None	
KR 10-2000-0002962 A	15/01/2000	None	
KR 10-2011-0029466 A	23/03/2011	None	