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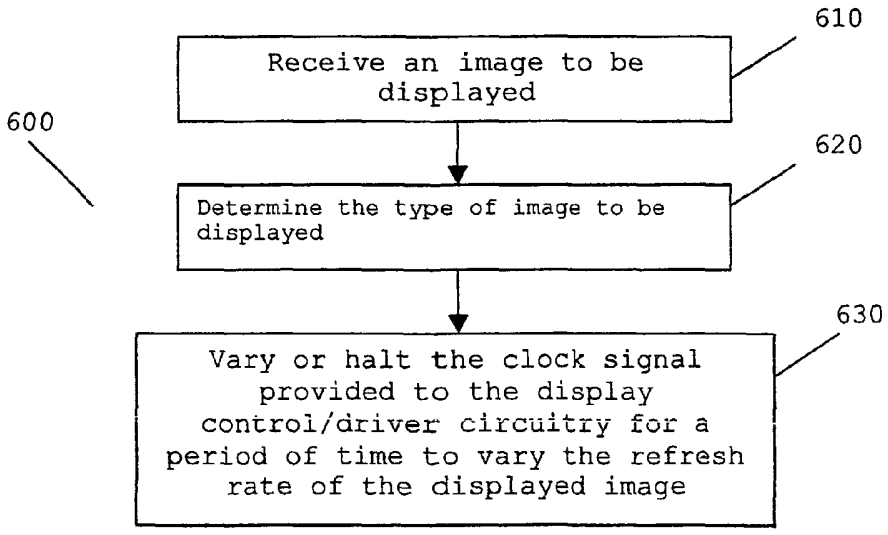
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for the following designation US*

[Continued on next page]

(54) Title: IMAGE OR VIDEO DISPLAY DEVICE AND METHOD OF CONTROLLING A REFRESH RATE OF A DISPLAY



(57) Abstract: A video or image display device (100) includes a display (110) for displaying an image and display refresh circuitry (200), operably coupled to the display (110), to refresh an image on the display (110). A processor (108), operably coupled to the display (110) and display refresh circuitry (200), processes a received image to determine an image type to be displayed. The processor (108) then varies or halts a clock signal provided to the display refresh circuitry dependent upon the image being displayed.This provides the advantage that the refresh rate is varied or halted in response to the type of image being displayed, to constantly minimise the power consumption of the display device without noticeable flickering of the display device.

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IMAGE OR VIDEO DISPLAY DEVICE AND METHOD OF CONTROLLING A REFRESH RATE OF A DISPLAY

Field of the Invention

This invention relates to a method of reducing power consumption of a display. The invention is applicable to, but not limited to, display devices used in battery powered apparatus, such as personal digital assistants (PDAs) or mobile phones, where battery power to operate and refresh the display is limited.

Background of the Invention

Future generation mobile and fixed communication systems are expected to provide the capability for video and image transmission as well as the more conventional voice and data services. As such, video and image services for communication devices will become more prevalent, and improvements in video/image compression technology are likely to be needed in order to satisfy the anticipated consumer demand within the available communication bandwidth.

Furthermore, as mobile users wish to access ever more services whilst on the move, such as text strings, text messages, email, images and/or video, similar improvements are required for display technologies. Given the current user trend towards desiring smaller, lighter and more portable wireless communication devices, the improvement to displays is considered a particularly key market differentiator for portable communication device manufacturers.

For hand-held battery-powered equipment, it is important to minimize power consumption in order to prolong battery life between recharging operations. Colour thin film transistor (TFT) liquid crystal displays (LCDs) are increasingly being used in such equipment. In such displays, power consumption depends mainly on properties such as:

(i) Refresh rate;

(ii) Colour balance; and

(iii) The amount of image data (pixel) detail to be displayed.

When an LCD panel displays an image, the image fades with time. Therefore, it is necessary for the image to be refreshed in order for it to remain clear. Therefore, the pixel data is constantly, and cyclically, being retrieved from memory, provided to the LCD and used to refresh the image one pixel at a time.

It is known that the refresh rate of a display must be set to be sufficiently high for the human eye not to perceive the difference in the image before and after it is refreshed. Otherwise visible flickering of the image occurs.

Therefore, there is a need for providing a portable communication device having a display and a method of reducing the refresh rate of a display, in particular when displaying a static image, such that the power consumption of the display, and display driver circuitry, is reduced.

Statement of Invention

In accordance with a first aspect of the present invention, there is provided a method of refreshing an image on a display device, as claimed in Claim 1.

In accordance with a second aspect of the present invention, there is provided an image or video communication device, as claimed in Claim 5.

In accordance with a third aspect of the present invention, there is provided a display driver for controlling a refresh rate of a display device, as Claimed in claim 7.

In accordance with a fourth aspect of the present invention, there is provided a video or image display device, as claimed in Claim 8.

In accordance with a fifth aspect of the present invention, there is provided a display driver for controlling the refresh rate of a display device, as claimed in Claim 12.

Further aspects of the invention are as claimed in the dependent claims.

In summary, the present invention provides a means of varying or halting a clock provided to display refresh circuitry to halt or vary a refresh rate of a display, dependent upon the type of image being displayed. In this manner, when the display does not need to be refreshed based on the image being displayed a reduction

in the overall power consumption of the display device can be achieved.

Thus, by halting the refresh operation of the control/driver circuit for a period of time, the length of a refresh cycle is increased, thereby reducing the refresh rate.

Brief Description of the Drawings

Exemplary embodiments of the present invention will now be described, with reference to the accompanying drawings, in which:

FIG. 1 shows a block diagram of a battery-powered wireless subscriber unit adapted to support the inventive concepts of the preferred embodiments of the present invention.

FIG. 2 shows a block diagram of a preferred display driver arrangement of the subscriber unit of FIG. 1.

FIG. 3 shows a graphical illustration of a display refresh operation.

FIG. 4 shows timing diagrams of a subscriber unit used to support the inventive concepts of the preferred embodiments of the present invention.

FIG. 5 shows a block diagram of part of a processor system that handles the provision of clock signals, in accordance with an enhanced embodiment of the present invention.

FIG. 6 shows a flowchart of a preferred process of adapting a refresh rate of a display, in accordance with an preferred embodiment of the present invention.

Description of Preferred Embodiments

In summary, the inventor of the present invention has recognised that, at present, no distinction is made as to the refresh rates for different images being displayed. Hence, the same refresh rate is used for both static images and moving pictures. Notably, a static, i.e. fixed, image does not require as high a refresh rate as, for example, a moving picture such as a video clip or the like. This results in the display being refreshed more than is needed when a static image is being displayed. Such a refresh rate consumes unnecessary power.

The preferred embodiment of the present invention is described with reference to a portable cellular phone. However, it is within the contemplation of the present invention that the inventive concepts described herein are equally applicable to any other video or image display device, such as a personal data assistant (PDA), a portable or mobile radio, a laptop computer or a wirelessly networked personal computer (PC) or indeed any other digital device having a display to support video/image transmissions.

Referring first to FIG. 1, there is shown a block diagram of a cellular subscriber unit 100 adapted to support the inventive concepts of the preferred embodiments of the present invention. The subscriber unit 100 contains an

antenna 102 preferably coupled to a duplex filter, antenna switch or circulator 104 that provides isolation between receiver and transmitter chains within the subscriber unit 100.

The receiver chain, as known in the art, includes scanning receiver front-end circuitry 106 (effectively providing reception, filtering and intermediate or base-band frequency conversion). The scanning front-end circuit 106 is serially coupled to a signal processing function 108. An output from the signal processing function 108 is provided to a suitable output device 110, such as a screen or flat panel liquid crystal display. The screen or flat panel display 110 includes a display driver circuit 111.

Each time an image on the screen or flat panel display 110 is to be refreshed, each pixel within the display device is typically refreshed.

The receiver chain also includes received signal strength indicator (RSSI) circuitry 112, which in turn is coupled to a controller 114 for maintaining overall subscriber unit control. A timer 118 is operably coupled to the controller 114 to control the timing of operations (including transmission or reception of time-dependent signals) within the cellular subscriber unit 100. The controller 114 is also coupled to the scanning receiver front-end circuitry 106 and the signal processing function 108 (generally realised by a DSP) for receiving a transmitted video or image signal.

The controller 114 may therefore receive bit error rate (BER) or frame error rate (FER) data from recovered information.

In accordance with the preferred embodiment of the present invention, the interaction between the microprocessor 108 and the output device 110 and display driver circuit 111 has been adapted to reduce power consumption of the respective elements. The reduction in power consumption is achieved by the microprocessor 108 determining, or being informed, of the type of image, for example static or video, to be displayed on the display 110. In response to the determination, or information, the microprocessor adapts or halts a refresh operation of the display, thereby reducing power consumption of the respective devices used in the refresh operation.

One example of determining a type of image to be displayed would be to simply identify the image by the file type (e.g. bitmap being a static image and MPEG being a video clip etc.). Alternatively, a default mode could be set to substantially static images, and only when certain applications are running (i.e. those capable of displaying video clips etc.) does the microprocessor revert to a normal refresh operation.

FIG. 2 illustrates a block diagram of a liquid crystal display (LCD) control/driver circuit 200, in accordance with the preferred embodiment of the present invention. A microprocessor, for example the microprocessor 108 of FIG. 1, initialises an LCD controller 140 and a DMA controller 220 by way of control registers 132. The microprocessor 108 manages the contents of image memory

210 via an address bus 134 and a data bus 136. In this regard, in accordance with the preferred embodiment of the present invention, the microprocessor determines the type of image to be displayed.

The LCD controller 140 is also connected to an LCD panel 110 by way of three timing links 142a, 142b, 142c that provide timing signals vertical (V)-sync, horizontal (H)-sync and pixel clock respectively. The DMA controller 220 drives pixel data bus 144, by way of a data latch 240, providing pixel data to the LCD panel 110. The LCD panel 110 includes an LCD display and control circuitry (not shown).

The LCD controller 140 also provides timing control signals to the LCD panel 110, the DMA controller 220 and the data latch 240 to coordinate the retrieval and making available of pixel data. The DMA controller 220 retrieves pixel data for the image to be displayed from the memory device 210 via an address bus and data bus. The pixel data retrieved from the memory is then passed to a data latch 240.

The LCD panel 110 receives the timing signals provided by the LCD controller 140 and, in response to the timing signals, retrieves the data for each pixel. The LCD panel 110 then systematically displays the corresponding image one pixel at a time.

If the image is determined by the microprocessor 108 as being, say, a static, or substantially static (video) image, the microprocessor 108 initiates an adapted image refresh operation. The adapted image refresh operation

includes either temporarily halting timing signals being supplied to the aforementioned devices used in the refresh operation, or reducing the rate of timing signals supplied to these devices so that the refresh rate is reduced.

It will be appreciated that the LCD control/driver circuit 200 illustrated in FIG. 2 is only an example of a suitable LCD driver circuitry apparatus, and that any other suitable circuitry known may alternatively be adapted to facilitate and perform the inventive concepts described herein.

When the LCD panel 110 displays an image, the image fades with time. Therefore, it is necessary for the image to be refreshed in order for it to remain clear. Therefore, the pixel data is constantly, and cyclically, being retrieved from memory, provided to the LCD panel and used to refresh the image one pixel at a time.

It is known that the refresh rate of a display must be set to be sufficiently high for the human eye not to perceive the difference in the image before and after it is refreshed, otherwise flickering occurs. Each time an image is refreshed, generally each pixel within the display device is refreshed, starting at the top left corner 310 and refreshing each pixel row-by-row 320-360, as illustrated in FIG. 3. An exception to this may be when interleaving is used, whereby odd and even lines of pixels are alternately refreshed.

A display refresh operation is preferably controlled in response to a status of particular signal timings 410, as

shown in the graph 400 of FIG. 4. The preferred embodiment of the present invention utilises timing of signals that include vertical synchronisation (V-Sync) 420, horizontal synchronisation (H-Sync) 430, data 440 and pixel clock 450, associated with the display in conjunction with the received video or image signal(s). The frequencies of H-Sync 430 and the pixel clock 450 are multiples of the V-Sync 420 frequency.

The V-Sync signal 420 is used to inform the display device 110 when to commence incorporating the next whole image or commence refreshing portions of the current image. The V-Sync signal 420 essentially controls when the vertical alignment of the refresh operation returns to the top of the display device, as shown by the top left hand corner 310 of FIG. 3. Thus, for the illustrated embodiment, every low pulse of the V-Synch causes the refresh cycle to start at the top again thereby essentially setting a display refresh rate.

The H-Sync signal 430 is used to inform the display device when to begin to refresh the next horizontal line (row) of pixels. Hence, the H-Sync signal 430 controls when the horizontal alignment of the refresh operation returns to the start of a new row, at the left hand side of the screen of the display 110.

The Data signal 440 contains the data for each pixel of the display device. This data is divided into blocks, where each block represents a row on the display device. As shown in FIG. 4, these blocks correspond to the H-Sync timing signal 430. Furthermore, it is envisaged that the data contained in a row is further divided into a series

of pixels, where each pixel is preferably further partitioned into bits that relate to the primary colours red, green and blue.

In accordance with the preferred embodiment of the present invention, the microprocessor 108 monitors a timing signal of a refresh operation of the display. The timing signal monitored is preferably one of V-Sync, H-Sync or Pixel Clock. For the control driver circuit 200 illustrated in FIG. 2, the V-Sync signal is also provided to the microprocessor 108, for example by way of a general purpose input/output port (not shown) of the microprocessor 108, so that the microprocessor 108 is able to monitor the V-Sync signal.

For the illustrated embodiment, the microprocessor 108 is preferably the main processor of the device in which the display and control/driver circuit are provided. However, it is within the contemplation of the present invention for the device to comprise a further processor (not shown) for performing tasks other than controlling the display and display control/driver circuit. Where this is the case, the V-Sync signal may alternatively be monitored by the further processor of the device.

When the microprocessor 108 determines an opportunity to reduce or halt the refresh rate, based on the type of image to be displayed on the LCD panel 110, the microprocessor 108 interrupts, say, a clock signal (not shown) provided to the control/driver circuit 200 to halt the refresh operation.

The clock signal for the driver/control circuit 200 illustrated is provided to the LCD controller 140, which controls the timing and synchronisation of the various elements of the control/driver circuit 200 during a refresh operation. The effect of halting the clock signal provided thereto is that the control/driver circuit 200, with the exception of the microprocessor 108, will in essence be 'frozen'.

The halting of the clock signal is preferably achieved by the microprocessor 108, or by a further processor of the device, by way of clock management functionality, which may be an integral part of the microprocessor 108, or further processor of the device.

Alternatively, as described with regard to the enhanced embodiment of the present invention in FIG. 5, the clock signal control may be provided by a separate clock management unit 570 (of FIG. 5). In this regard, the clock management unit 570 controls clock signals provided to various components of the device in which the display 110 and control/driver circuit 200 are provided. Where the clock management unit 570 halts the clock signal for the control/driver circuit 200, this is preferably performed under instruction from the microprocessor 108, as described later.

Based on the type of image being displayed, the microprocessor determines when to resume the clock signal to the control/driver circuit 200, to resume the refresh operation. The period of time for which the clock signal is interrupted is selected such that an image being

displayed by the display remains substantially unaffected to the human eye.

In this way, the normal refresh rate of the display 110, as controlled by the control/driver circuit 200, can be such that the display is refreshed sufficiently frequently for moving pictures and the like, such as video clips, to be adequately displayed without a user of the device experiencing flickering etc. When a static image is displayed, which does not require such a high refresh rate as moving pictures etc, the refresh rate can be reduced by periodically halting the refresh operation as described above.

Preferably, when reducing the refresh rate in this way, the clock signal is halted once each refresh cycle, i.e. once for each complete display refresh. This can most easily be achieved by monitoring the V-Sync signal, as described above. It can be seen in FIG. 4 that the V-Sync signal is, for the illustrated embodiment, set 'high' during the refresh cycle (V-Sync duty cycle). At the end of the refresh cycle the V-Sync signal goes 'low' for a short duration 422 before again going high to signify the start of the next refresh cycle.

In the preferred embodiment of the present invention, the microprocessor 108 monitors the V-Sync signal. When a low signal is detected, signifying the short period between refresh cycles, the microprocessor 108 halts, or causes to halt, the clock signal to the control/driver circuit 200 for a required period of time. The effect of this is to extend the period between refresh cycles, effectively reducing the number of refresh cycles per second, and so

reducing the refresh rate. Thus, the refresh rate can be variably reduced as required by varying the period of time for which the clock signal to the control/driver circuit 200 is halted.

In this way, the problem of providing an unnecessarily high refresh rate, which results in an unnecessarily high power consumption by the display and the display control/driver circuit, can be alleviated, with the microprocessor 108 controlling the refresh rate depending on the type of image etc being displayed.

According to an enhanced embodiment of the present invention there is provided a display device, for example a mobile communications device, comprising a display and a display control/driver circuit, and in which the above described method of the present invention is implemented.

FIG. 5 illustrates an example of part of a processor system 500 that handles the provision of clock signals to a processor (CPU), for example the microprocessor 108 of FIG. 2, and peripheral components of the microprocessor 108 within the processor system 500, such as a traffic controller (TC) 520, display driver circuit (LCD), for example the control/driver circuit illustrated in FIG. 2 200, external memory interface (EMIF) 540 etc.

For the illustrated embodiment, the display driver 200 is a liquid crystal display driver, which is used to drive a liquid crystal display (not shown) such as a thin film transistor (TFT) display, with which the processor system 500 is used. However, it will be appreciated that a driver for any other type of display, with which the

processor system 500 is used, may be substituted for the liquid crystal display driver without affecting the scope of the present invention.

As can be seen, an oscillator 550 provides a clock signal to the processor system 500. This clock signal is used as an origin for further clock signals within the processor system 500. It will therefore be referred hereinafter as the seed clock signal. For the illustrated embodiment the seed clock signal has a frequency of 12MHz.

The processor system 500 comprises a Digital Phased Locked Loop (DPLL) 560, which has as an input the 12MHz seed clock signal from the oscillator 550. The DPLL 560 uses the seed clock signal to generate as an output a reference clock signal (RF_CLK), by multiplying and/or dividing the seed clock signal.

The processor system 500 further comprises a clock management unit 570 for providing clock management functionality of the device, which has as an input the reference clock signal generated by the DPLL 560. The clock management unit 570 multiplies and/or divides the reference clock signal from the DPLL 560 to provide individual clock signals for the microprocessor 108 and its peripheral components. Thus, in the illustrated embodiment, the clock management unit provides a CPU_CLK clock signal to the microprocessor 108, a TC_CLK clock signal to the traffic controller 520, an LCD_CLK clock signal to the display driver 200 and an EMIF_CLK clock signal to the external memory interface 540, along with any further clock signals required within the processor system 500.

The clock rates provided to each of the microprocessor 108 and peripheral components 520, 200, 540 are dependent jointly on the generation of the reference clock signal REF_CLK by the DPLL 560, and individually on the generation of the specific clock signals CPU_CLK, TC_CLK, LCD_CLK and EMIF_CLK by the clock management unit 570.

The DPLL 560 and clock management unit 570 are each configurable by the microprocessor 108, such that the microprocessor 108 is able to adjust the clock signals provided by them. In this way, the microprocessor 108 is able to alter the clock signals provided to itself and to the peripheral components, both universally through reconfiguration of the DPLL 560 and/or individually through reconfiguration of the clock management unit 570.

According to the present invention, the display control/driver 200 controls a refresh operation of the display (not shown) of the device.

In accordance with a timing signal of the refresh operation of the display, a clock signal provided to the control/driver circuit is interrupted, for example by the clock management unit 570, to halt the refresh operation. This is preferably initiated by the microprocessor 108, which monitors the timing signal, and when required instructs the clock management unit 570 to halt the clock signal to the display control/driver circuit 200.

After a period of time, which is preferably determined by the microprocessor 108 depending on the image being displayed on the display, the clock signal to the

control/driver circuit is resumed. For example, the resumption of the clock signal to the control/driver circuit is made in response to a signal from the microprocessor 108 to the clock management unit 570, to resume the refresh operation. The period of time for which the clock signal is interrupted is selected such that an image being displayed by the display remains substantially unaffected to the human eye.

Referring now to FIG. 6, a flowchart of the preferred process of adapting a refresh rate of a display is illustrated, in accordance with an preferred embodiment of the present invention. The process includes the step of a processor receiving an image to be displayed, in step 610. The processor then determines the type of image to be displayed, by any known mechanism, as shown in step 620. The processor (or clock management function) then varies or halts one or more clock signals provided to any circuit or device in the display refresh (control and/or driver) circuitry, for a period of time, to vary the refresh rate of the image being displayed.

It will be understood that the image or video communication device and method of display refresh control described above provides at least some of the following advantages:

(i) The refresh rate is varied or halted in response to the type of images being displayed to keep the power consumption of the display device to a minimum without noticeable flickering of the display device to the display viewer/user.

(ii) Power consumption of a display device is dynamically optimised whilst maintaining a quality of viewed image or video.

All other features and implementations herein described and/or illustrated in the drawings are considered solely as preferred additions and/or alternatives, and are not limiting on the scope of the present invention.

Whilst the specific and preferred implementations of the embodiments of the present invention are described above, it is clear that one skilled in the art could readily apply variations and modifications of such inventive concepts.

Thus, a portable communication device having a display and a method of reducing the refresh rate of a display, in particular when displaying a static image, have been described that substantially alleviate the problems of known display technology.

Claims

1. A method (600) of refreshing an image on a display, the method comprising the step of:

receiving an image to be displayed at a display (610);

the method characterised by the steps of:

processing the received image to determine a type of image to be displayed (620); and

varying or halting a rate at which the displayed image is refreshed based on the type of image (630).

2. The method (600) of refreshing an image on a display according to Claim 1, wherein the step of varying or halting (630) is further characterised by the step of varying or halting a clock signal provided to circuitry involved in a display refresh operation.

3. The method (600) of refreshing an image on a display according to Claim 1 or Claim 2, wherein the step of varying or halting a refresh rate is further characterised by the step of varying or halting a clock signal for a time period dependent upon the type of image being displayed.

4. The method (600) of refreshing an image on a display according to Claim 2, wherein the step of varying or halting the clock signal is based on varying or halting at least one of the following timing parameters: a vertical synchronisation (420), a horizontal synchronisation (430), data (440), pixel rate (450).

5. An image or video communication device (100), adapted to perform the steps of method Claim 1.

6. The image or video communication device (100) according to Claim 5, wherein the image or video communication device (100) is one of:

a cellular phone, a portable or mobile radio, a personal digital assistant, a laptop computer, a wirelessly networked PC.

7. A display driver (111) for controlling a refresh rate of a display device (110) adapted to perform any of the steps of Claim 1.

8. A video or image display device (100), the video or image display device (100) comprising:

a display (110) for displaying an image;

display refresh circuitry (200), operably coupled to the display (110), to refresh an image on the display (110); and

a processor (108), operably coupled to the display (110) and display refresh circuitry (200), for processing a received image to determine an image type to be displayed;

wherein the video or image display device (100) is characterised in that the processor (108) varies or halts a clock signal provided to the display refresh circuitry dependent upon the image being displayed.

9. The video or image display device (100) according to claim 8, further characterised by:

a clock management function (570), operably coupled to and under control of the processor (108), wherein the clock management function (570) varies or halts a clock signal provided to the display refresh

circuitry (200) in response to a control signal from the processor (108) based on the image being displayed.

10. The video or image display device (100) according to claim 8 or Claim 9, wherein the processor (108) determines a time to vary or halt the clock signals to the display refresh circuitry (200) based on a timing signal of at least one of the following timing parameters relating to the display (110): a vertical synchronisation (420), a horizontal synchronisation (430), data (440), pixel rate (450).

11. The video or image display device (100) according to Claim 8 or Claim 9, wherein the processor (108) determines a time period for varying or halting the clock signal dependent upon the type of image being displayed.

12. A display driver (111) adapted to control a refresh rate of a display device (110) according to Claim 8.

FIG. 1

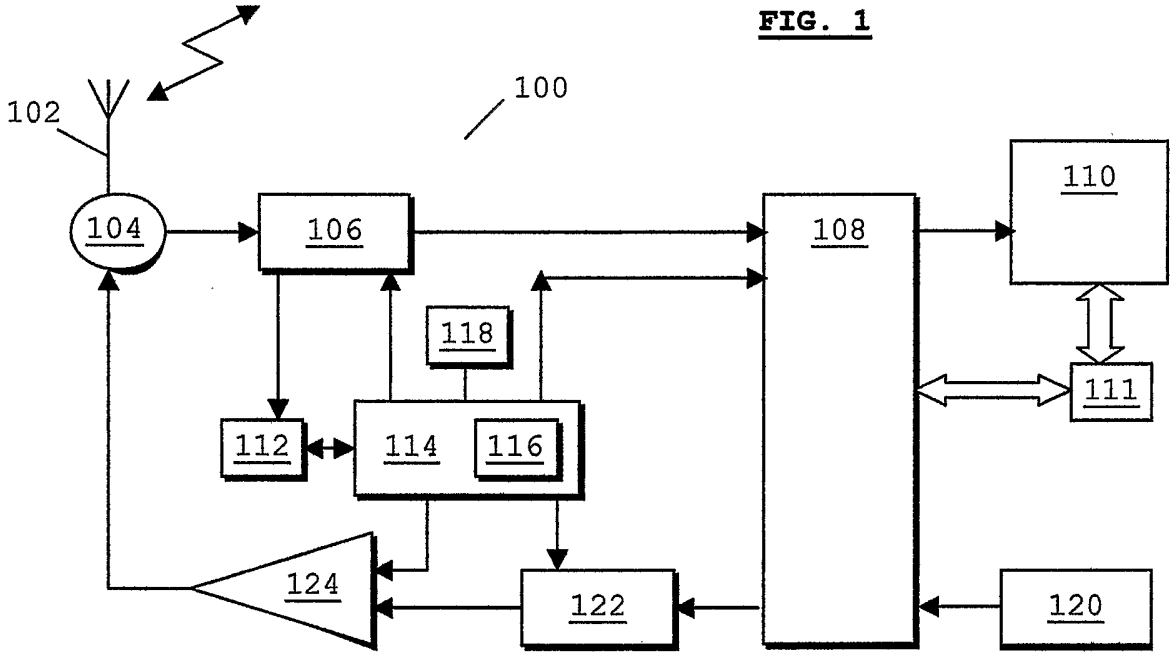


FIG. 2

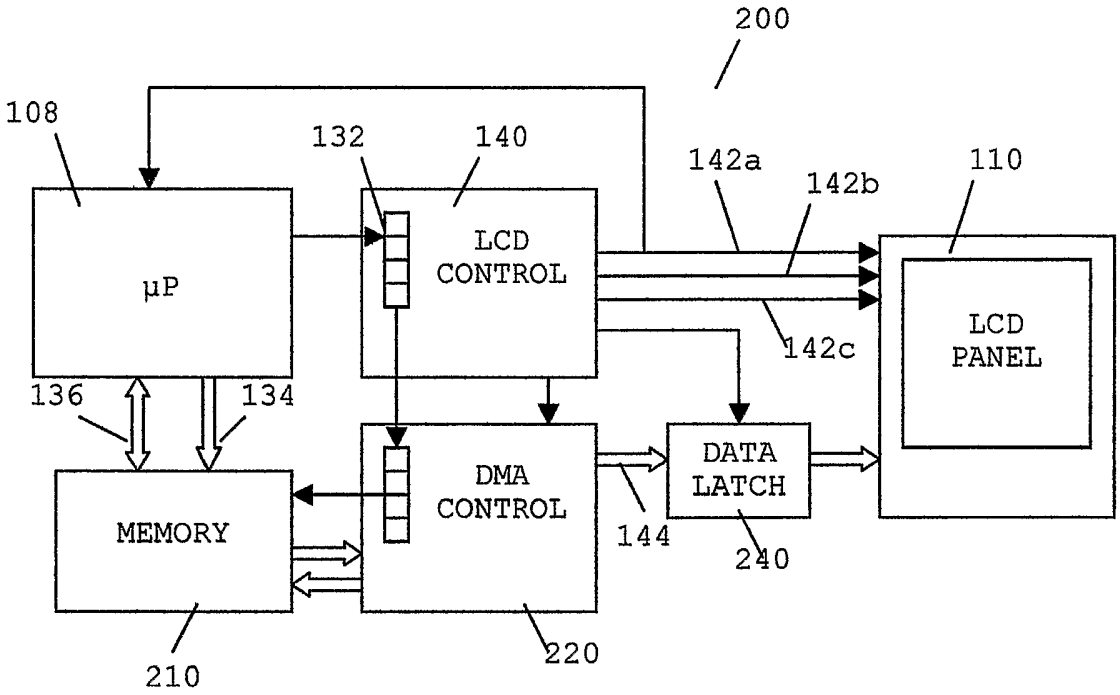

200
108
132
140
142a
142b
110
µP
LCD CONTROL
LCD PANEL
142c
136
134
DMA CONTROL
DATA LATCH
MEMORY
144
240
210
220

FIG. 3

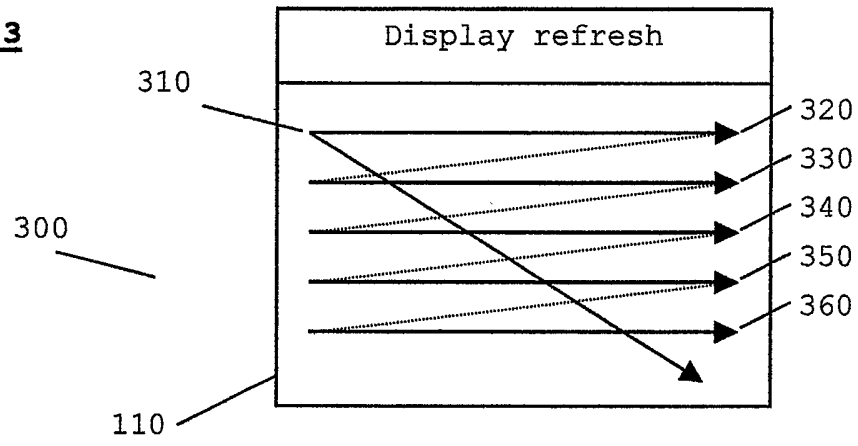

Display refresh
310
320
330
340
350
360
300
110

FIG. 4

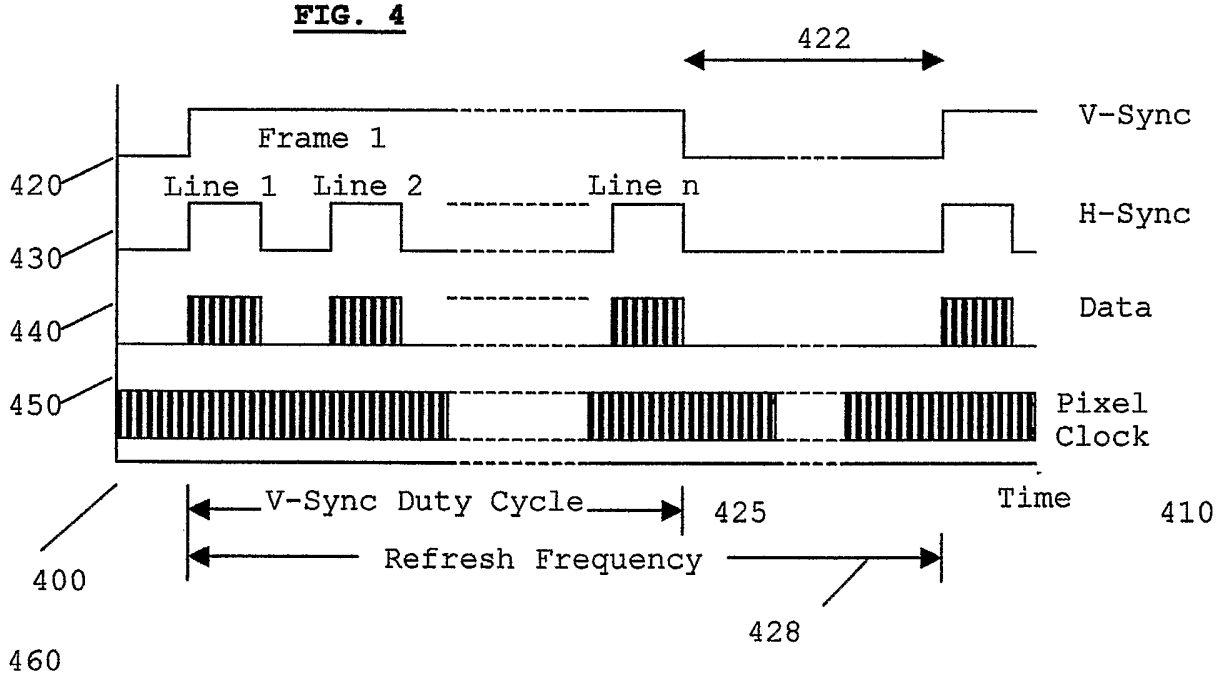

422
V-Sync
Frame 1
420
Line 1
Line 2
Line n
H-Sync
430
Data
440
450
Pixel Clock
V-Sync Duty Cycle
425
Time
410
400
Refresh Frequency
428
460

FIG. 5

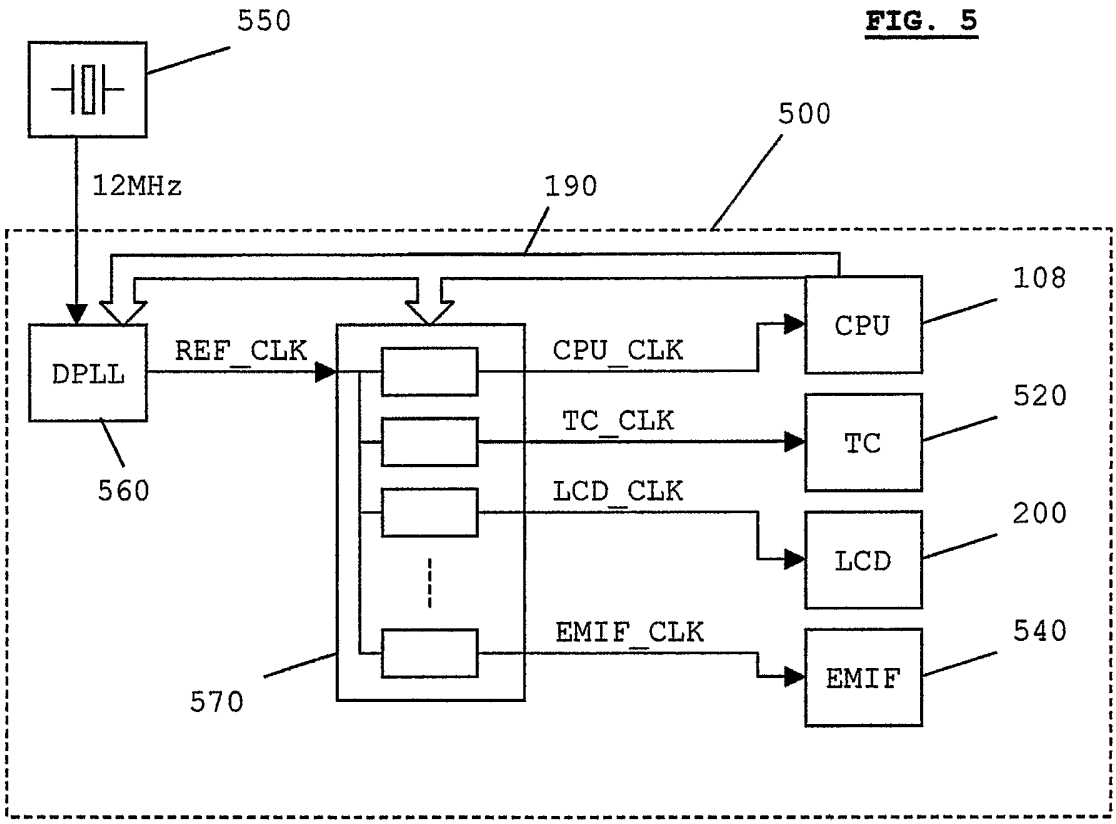
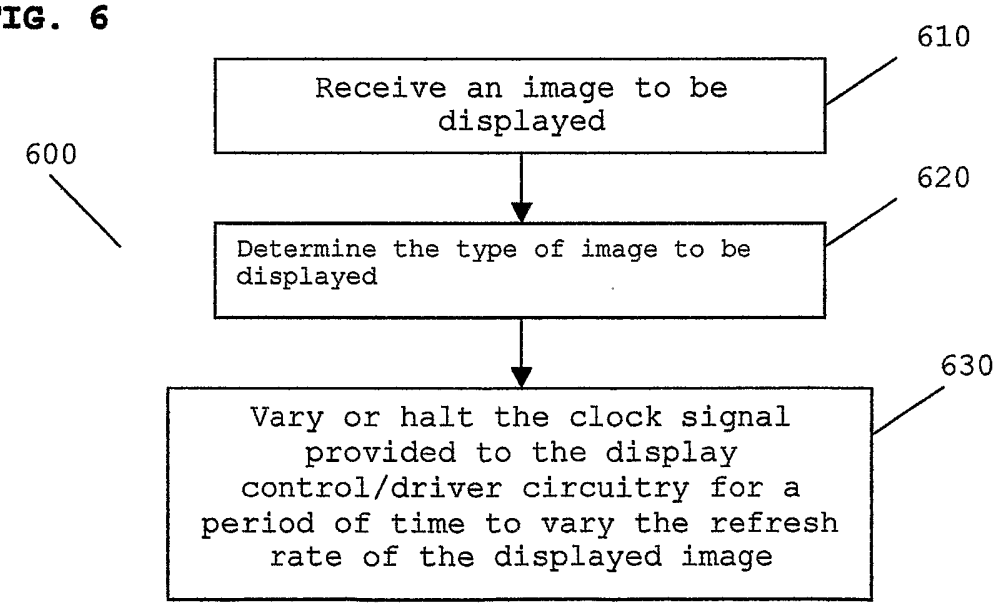

550
500
12MHz
190
108
CPU
DPLL
REF_CLK
CPU_CLK
520
TC_CLK
TC
560
LCD_CLK
200
LCD
EMIF_CLK
540
EMIF
570

FIG. 6


610
Receive an image to be displayed
600
620
Determine the type of image to be displayed
630
Vary or halt the clock signal provided to the display control/driver circuitry for a period of time to vary the refresh rate of the displayed image

INTERNATIONAL SEARCH REPORT

Inte nal Application No
PCT/GB 03/02294

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36 G09G5/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 170 968 A (TOKYO SHIBAURA ELECTRIC CO) 9 January 2002 (2002-01-09) paragraph '0012! paragraph '0021! - paragraph '0022! paragraph '0029! paragraph '0033! paragraph '0045! - paragraph '0048! paragraph '0053! - paragraph '0062! figures 3,11-14	1-12
X	EP 0 655 725 A (ROHM CO LTD) 31 May 1995 (1995-05-31)	1,5,7,8, 12
A	column 3, line 50 -column 4, line 15 claim 1 figure 2	2-4,6, 9-11

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 September 2003	10/10/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Farricella, L

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A	EP 1 184 836 A (SHARP KK) 6 March 2002 (2002-03-06) abstract	1,7,8
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Int[illegible]al Application No
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