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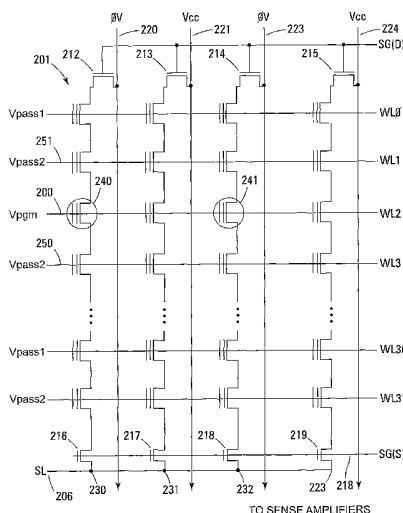
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(54) Title: MINIMIZING ADJACENT WORDLINE DISTURB IN A MEMORY DEVICE



(57) Abstract: A selected wordline that is coupled to cells for programming is biased with a programming voltage. The unselected wordlines that are adjacent to the selected wordline are biased at a first predetermined voltage. The remaining wordlines are biased at a second predetermined voltage that is greater than the first predetermined voltage. The first predetermined voltage is selected by determining what unselected, adjacent wordline bias voltage produces a minimized V_{pass} disturb in response to the selected wordline programming voltage.

MINIMIZING ADJACENT WORDLINE DISTURB IN A MEMORY DEVICE

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to memory devices and in particular the
5 present invention relates to programming of non-volatile memory devices.

BACKGROUND OF THE INVENTION

Memory devices are typically provided as internal, semiconductor, integrated
circuits in computers or other electronic devices. There are many different types of memory
10 including random-access memory (RAM), read only memory (ROM), dynamic random
access memory (DRAM), synchronous dynamic random access memory (SDRAM), and flash
memory.

Flash memory devices have developed into a popular source of non-volatile
memory for a wide range of electronic applications. Flash memory devices typically use a
15 one-transistor memory cell that allows for high memory densities, high reliability, and low
power consumption. Common uses for flash memory include personal computers, personal
digital assistants (PDAs), digital cameras, and cellular telephones. Program code and system
data such as a basic input/output system (BIOS) are typically stored in flash memory devices
for use in personal computer systems.

20 Two common types of flash memory array architectures are the "NAND" and
"NOR" architectures. These architectures are named for the resemblance that the basic
memory cell configuration of each architecture has to a basic NAND or NOR gate circuits,
respectively.

In the NOR array architecture, the floating gate memory cells of the memory array
25 are arranged in a matrix. The gates of each floating gate memory cell of the array matrix are
connected by rows to word select lines (wordlines) and their drains are connected to column
bitlines. The source of each floating gate memory cell is typically connected to a common
source line. The NOR architecture floating gate memory array is accessed by a row decoder
activating a row of floating gate memory cells by selecting the wordline connected to their
30 gates. The row of selected memory cells then place their stored data values on the column
bitlines by flowing a differing current if in a programmed state or not programmed state from
the connected source line to the connected column bitlines.

A NAND array architecture also arranges its array of floating gate memory cells in a matrix such that the gates of each floating gate memory cell of the array are connected by rows to wordlines. Each memory cell, however, is not directly connected to a source line and a column bit line. The memory cells of the array are instead arranged together in strings, typically of 8, 16, 32, or more each, where the memory cells in the string are connected together in series, source to drain, between a common sourceline and a column bitline. The NAND architecture floating gate memory array is then accessed by a row decoder activating a row of floating gate memory cells by selecting the word select line connected to their gates. In addition, the wordlines connected to the gates of the unselected memory cells of each string are also driven. However, the unselected memory cells of each string are typically driven by a higher gate voltage so as to operate them as pass transistors and allowing them to pass current in a manner that is unrestricted by their stored data values. Current then flows from the sourceline to the column bitline through each floating gate memory cell of the series connected string, restricted only by the memory cells of each string that are selected to be read. This places the current encoded stored data values of the row of selected memory cells on the column bitlines.

Figure 1 illustrates a column of a typical prior art NAND flash memory device. The selected wordline for the flash memory cells being programmed is typically biased at a voltage that is greater than 16V. The illustrated wordline 100 of the cell to be programmed is biased at 19V. The unselected wordlines for the remaining cells are typically biased at approximately 10V. As NAND flash memory is scaled, parasitic capacitance coupling between the selected wordline and adjacent floating gates (FG) and control gates (CG) becomes problematic. Because of the parasitic coupling, the adjacent cells are more prone to V_{pass} disturb than the other cells that also share the common bitline with the cells being programmed.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a way to minimize programming induced V_{pass} and adjacent wordline stress between a selected wordline and adjacent unselected wordlines.

SUMMARY

The above-mentioned problems with adjacent wordline disturb in a memory device and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

5 The embodiments of the present invention encompass a method for minimizing adjacent wordline disturb during programming of an array of memory cells. The memory array is arranged in rows and columns wherein each row is coupled by a wordline and each column is coupled by a bitline.

 The method comprises biasing a selected wordline with a programming voltage.
10 The selected wordline is coupled to the memory cell or cells to be programmed. The unselected wordlines that are adjacent to the selected wordline are biased at a first predetermined voltage. The remaining wordlines are biased at a second predetermined voltage that is greater than the first predetermined voltage.

 Further embodiments of the invention include methods and apparatus of varying
15 scope.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a typical prior art NAND architecture memory array with wordline biasing.

20 Figure 2 shows a diagram of one embodiment for a flash memory array of the present invention with wordline biasing.

 Figure 3 shows a flowchart of one embodiment of a method of the present invention for programming memory cells in a flash memory array.

 Figure 4 shows a block diagram for one embodiment of an electronic system of
25 the present invention.

DETAILED DESCRIPTION

 In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof and in which is shown, by way of illustration,
30 specific embodiments in which the invention may be practiced. In the drawings, like

numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following
5 detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

Figure 2 illustrates a diagram of one embodiment for a flash memory array of the present invention with wordline biasing levels. The memory array of Figure 2, for purposes of clarity, does not show all of the elements typically required in a memory array. For
10 example, only four bitlines are shown 220 – 224 when the number of bitlines required actually depends upon the memory density.

The array is comprised of an array of floating gate cells 201 arranged in series strings 230 – 233. Each of the floating gate cells 101 are coupled drain to source in each series chain 230 – 233. A word line (WL0 – WL31) that spans across multiple series strings
15 230 – 233 is coupled to the control gates of every floating gate cell in a row in order to control their operation. The bitlines 220 – 224 are eventually coupled to sense amplifiers (not shown) that detect the state of each cell.

In operation, the wordlines (WL0 – WL31) select the individual floating gate memory cells in the series chain 230 – 233 to be written to or read from and operate the
20 remaining floating gate memory cells in each series string 230 – 233 in a pass through mode. Each series string 230 – 233 of floating gate memory cells is coupled to a source line 206 by a source select gate 216 – 219 and to an individual bitline 220 – 224 by a drain select gate 212 – 215. The source select gates 216 – 219 are controlled by a source select gate control line SG(S) 218 coupled to their control gates. The drain select gates 212 – 215 are controlled
25 by a drain select gate control line SG(D) 214.

In the embodiment illustrated in Figure 2, one wordline is selected for programming of certain cells in the row. In this embodiment, two cells 240 and 241 are to be programmed so that their bitlines 220 and 223 are at ground potential (0V). The remaining unselected bitlines 221 and 224 are biased at V_{cc} .

30 The wordline 200 for the selected row is biased at a V_{pgm} voltage. In one embodiment, this voltage is greater than 16V. In another embodiment, the V_{pgm} voltage is in a

range of 15V – 21V. Alternate embodiments may use other programming voltages or voltage ranges. For example, the V_{pgm} voltage could go lower or higher depending on the tunnel oxide thickness, the oxide-nitride-oxide thickness, the physical dimensions of the cell (for direct gate coupling), and the pitch of the array (for parasitic coupling).

5 Unselected wordlines that are not adjacent to the selected wordline 200 are biased at a V_{pass1} voltage. This voltage might range from 8 to 11V. In one embodiment, $V_{\text{pass1}} = 10\text{V}$. Alternate embodiments may use other wordline voltages to bias non-adjacent, unselected wordlines during a program operation.

10 In order to reduce the problems with V_{pass} disturb and adjacent wordline stress in adjacent rows and cells, the wordlines for the unselected rows 250 and 251 adjacent to the selected row are biased at a different voltage (V_{pass2}) than the remaining unselected wordlines. In one embodiment, V_{pass2} is less than V_{pass1} . In another embodiment, V_{pass2} is 9V when V_{pass1} is 10V.

15 In one embodiment, V_{pgm} on the selected wordline is incrementally increased for every programming pulse during a programming operation. In such an embodiment, a starting voltage is chosen as is a step voltage by which the starting voltage is increased every programming pulse, up to a maximum number of pulses. In such an embodiment, V_{pass2} on the adjacent, unselected wordlines can either be held constant or incrementally decreased with the V_{pgm} increases. If V_{pass2} is held constant, a desired voltage that results in minimal
20 adjacent wordline disturb over the range of V_{pgm} voltages can be found empirically.

 If V_{pass2} is decreased as V_{pgm} is increased, V_{pass2} can be ramped downward using various methods. In one embodiment, V_{pass2} is stepped down incrementally as some fraction of the step up voltage used for V_{pgm} . For example, if V_{pgm} starts at 16.4V and the step voltage is +0.6V, V_{pass2} might start at 9.6V with a step voltage of -0.2V (i.e., 1/3 of the V_{pgm} step).
25 Therefore, V_{pgm} pulses would be 16.4V, 17.0V, 17.6V, and 18.2V. V_{pass2} would therefore be 9.6V, 9.4V, 9.2V, and 9.0V respectively.

 In another embodiment, V_{pass2} may be a set fraction of V_{pgm} so that as V_{pgm} ramps up, V_{pass2} remains a preset percentage of V_{pgm} . For example, V_{pass2} may be $0.47V_{\text{pgm}}$. Alternate embodiments may use other percentages of V_{pgm} .

$V_{\text{pass}2}$ can be determined empirically by testing a flash memory device during manufacture to determine what $V_{\text{pass}2}$ produces the least amount of V_{pass} disturb in cells in the unselected, adjacent rows. This voltage can then be used for other flash memory devices.

5 In yet another embodiment, to take into account differences in flash memory dies, a number of voltage trims (e.g., 10V, 9V, 8V, 7V, 6V) can be built into the memory device. Each individual memory device can then be tested at different $V_{\text{pass}2}$ voltages to determine which voltage option provides the least amount of program disturb. The selected $V_{\text{pass}2}$ is then used in that particular die.

10 In still another embodiment, $V_{\text{pass}2}$ may be different depending on the distance of the adjacent, unselected wordline from array ground or the select gate so that each adjacent, unselected wordline has a different wordline bias voltage. In other words, the adjacent, unselected wordline closest to the source line of the array may have a different $V_{\text{pass}2}$ voltage than the adjacent, unselected wordline closest to the drain line of the array.

15 Figure 3 illustrates a flowchart of one embodiment of a method of the present invention for programming memory cells in a flash memory array. An appropriate $V_{\text{pass}2}$ voltage is determined at some point as described previously 301. The selected wordline of the row in which the desired cells are to be programmed is biased with a programming pulse having an amplitude of V_{pgm} 302.

20 The adjacent, unselected wordlines are biased with the appropriate $V_{\text{pass}2}$ 305 in order to reduce or eliminate V_{pass} stress and adjacent wordline stress. The selected bitlines coupled to the cells to be programmed are biased at ground level 307.

25 Figure 4 illustrates a functional block diagram of a memory device 400 that can incorporate the flash memory cells of the present invention. The memory device 400 is coupled to a processor 410. The processor 410 may be a microprocessor or some other type of controlling circuitry. The memory device 400 and the processor 410 form part of an electronic system 420. The memory device 400 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

30 The memory device includes an array of flash memory cells 430. The memory array 430 is arranged in banks of rows and columns. The control gates of each row of memory cells is coupled with a wordline while the drain and source connections of the

memory cells are coupled to bitlines. As is well known in the art, the connection of the cells to the bitlines depends on whether the array is a NAND architecture or a NOR architecture.

An address buffer circuit 440 is provided to latch address signals provided on address input connections A0 – Ax 442. Address signals are received and decoded by a row decoder 444 and a column decoder 446 to access the memory array 430. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 430. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

The memory device 400 reads data in the memory array 430 by sensing voltage or current changes in the memory array columns using sense amplifier/buffer circuitry 450. The sense amplifier/buffer circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array 430. Data input and output buffer circuitry 460 is included for bi-directional data communication over a plurality of data connections 462 with the controller 410. Write circuitry 455 is provided to write data to the memory array.

Control circuitry 470 decodes signals provided on control connections 472 from the processor 410. These signals are used to control the operations on the memory array 430, including data read, data write, and erase operations. The control circuitry 470 may be a state machine, a sequencer, or some other type of controller. The control circuitry 470 of the present invention, in one embodiment, is responsible for executing the method of the present invention for controlling the values of the programming voltage, the voltages on the adjacent, unselected wordlines, and the voltages on the non-adjacent, unselected wordlines.

The flash memory device illustrated in Figure 4 has been simplified to facilitate a basic understanding of the features of the memory and is for purposes of illustration only. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art. Alternate embodiments may include the flash memory cell of the present invention in other types of electronic systems.

CONCLUSION

In summary, the embodiments of the present invention provide a way to reduce or eliminate the Vpass disturb on the closest, adjacent cells that are not being programmed. This

can be accomplished by reducing the unselected wordline voltage for wordlines adjacent to the selected wordline.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to
5 achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

What is claimed is:

1. A method for minimizing adjacent wordline disturb while programming at least one cell in an array of memory cells that are arranged in rows and columns, each row coupled by a wordline and each column coupled by a bitline, the method comprising:
biasing a selected wordline with a programming voltage, the selected wordline coupled to the at least one memory cell; and
biasing unselected wordlines adjacent to the selected wordline at a first predetermined voltage and remaining wordlines at a second predetermined voltage that is greater than the first predetermined voltage.
2. The method of claim 1 and further including:
biasing, at ground potential, bitlines that are coupled to the at least one memory cell to be programmed; and
biasing, at a third predetermined voltage, bitlines that are not coupled to the at least one memory cell to be programmed.
3. The method of claim 2 wherein the third predetermined voltage is V_{cc} .
4. The method of claim 1 wherein the programming voltage is 19V.
5. The method of claim 1 wherein the programming voltage is in a range of 15V – 21V.
6. The method of claim 1 wherein the first predetermined voltage is 9V and the second predetermined voltage is 10V.
7. The method of claim 1 wherein the programming voltage is increased over a time period by a predetermined step voltage and the first predetermined voltage is decreased over the time period by a predetermined fraction of the predetermined step voltage.
8. The method of claim 1 wherein the array of memory cells is an array of flash memory cells.

9. The method of claim 8 wherein the array of flash memory cells is arranged in a NAND architecture.
10. A method for minimizing adjacent wordline disturb while programming at least one memory cell in a NAND array of memory cells arranged in rows and columns, each row coupled by a wordline and each column coupled by a bitline, the method comprising:
 - biasing a selected wordline with a programming voltage, the selected wordline coupled to at least one memory cell to be programmed;
 - biasing, at a first predetermined voltage, unselected wordlines adjacent to the selected wordline; and
 - biasing, at a second predetermined voltage, unselected wordlines that are not adjacent to the selected wordline, wherein the second predetermined voltage is greater than the first predetermined voltage.
11. The method of claim 10 wherein the programming voltage is ramped up over a period of time and the first predetermined voltage is ramped down over the period of time.
12. The method of claim 11 wherein the first predetermined voltage is a predetermined fraction of an amount that the programming voltage is ramped up.
13. The method of claim 10 wherein biasing the selected wordline with a programming voltage includes coupling a plurality of programming pulses to the selected wordline such that each pulse has an amplitude that is incrementally greater than an amplitude of a previous pulse.
14. The method of claim 10 wherein the first predetermined voltage is one volt less than the second predetermined voltage.
15. A method for minimizing adjacent wordline disturb while programming at least one memory cell in a NAND array of memory cells arranged in rows and columns, each

row coupled by a wordline and each column coupled by a bitline, the method comprising:

biasing a selected wordline with a programming voltage, the selected wordline coupled to at least one memory cell to be programmed;

biasing, at a first predetermined voltage, unselected wordlines adjacent to the selected wordline;

biasing, at a second predetermined voltage, unselected wordlines that are not adjacent to the selected wordline, wherein the second predetermined voltage is greater than the first predetermined voltage; and

biasing, at ground potential, bitlines coupled to the at least one memory cell.

16. The method of claim 15 and further including biasing, at V_{cc} , bitlines not coupled to the at least one memory cell.

17. A flash memory device comprising:
a memory cell array arranged in rows and columns, each row of cells coupled by a wordline and each column of cells coupled by a bitline; and
control circuitry for controlling biasing of the wordlines during a program operation wherein the control circuitry is adapted to set a program voltage on a selected wordline and is adapted to set a predetermined voltage on unselected wordlines that are adjacent to the selected wordline, the predetermined voltage being less than a voltage that biases unselected wordlines that are not adjacent to the selected wordline.

18. The device of claim 17 wherein the memory array is a NAND memory cell array.

19. The device of claim 17 wherein the control circuitry is a state machine.

20. The device of claim 17 wherein each unselected, adjacent wordline is biased by a different predetermined voltage than the other unselected, adjacent wordline.

21. The device of claim 17 wherein the control circuitry is further adapted to adjust the program voltage and the predetermined voltage over a period of time.

22. The device of claim 21 wherein the control circuitry is adapted to increase the program voltage over the period of time and decrease the predetermined voltage over the period of time.
23. The device of claim 21 wherein the predetermined voltage is a substantially constant percentage of the program voltage over the period of time.
24. An electronic system comprising:
a processor for generating memory control signals; and
a flash memory device coupled to the processor, the device comprising:
a memory cell array arranged in rows and columns, each row of cells coupled by a wordline and each column of cells coupled by a bitline; and
control circuitry for controlling biasing of the wordlines during a program operation wherein the control circuitry is adapted to set a program voltage on a selected wordline and is adapted to set a predetermined voltage on unselected wordlines that are adjacent to the selected wordline, the predetermined voltage being less than a voltage that biases unselected wordlines that are not adjacent to the selected wordline.
25. The system of claim 24 wherein the control circuitry is further adapted to control biasing of the bitlines such that bitlines coupled to cells to be programmed are biased with 0V.
26. The system of claim 25 wherein the control circuitry is further adapted to control biasing of the bitlines such that bitlines not coupled to the cells to be programmed are biased with V_{cc} .
27. A method for minimizing adjacent wordline disturb in a memory device having a plurality of wordlines each coupling a row of memory cells, the method comprising:
biasing a selected wordline with a programming voltage;

determining a level of V_{pass} disturb on adjacent wordlines to the selected wordline;
and

adjusting biasing of the adjacent wordlines such that the level of V_{pass} disturb in the adjacent wordlines is substantially minimized.

28. The method of claim 27 wherein adjusting biasing starts at a first predetermined voltage that is less than a second predetermined voltage used to bias remaining wordlines.
29. The method of claim 27 wherein the biasing of the adjacent wordlines changes over time in response to the biasing of the selected wordline.

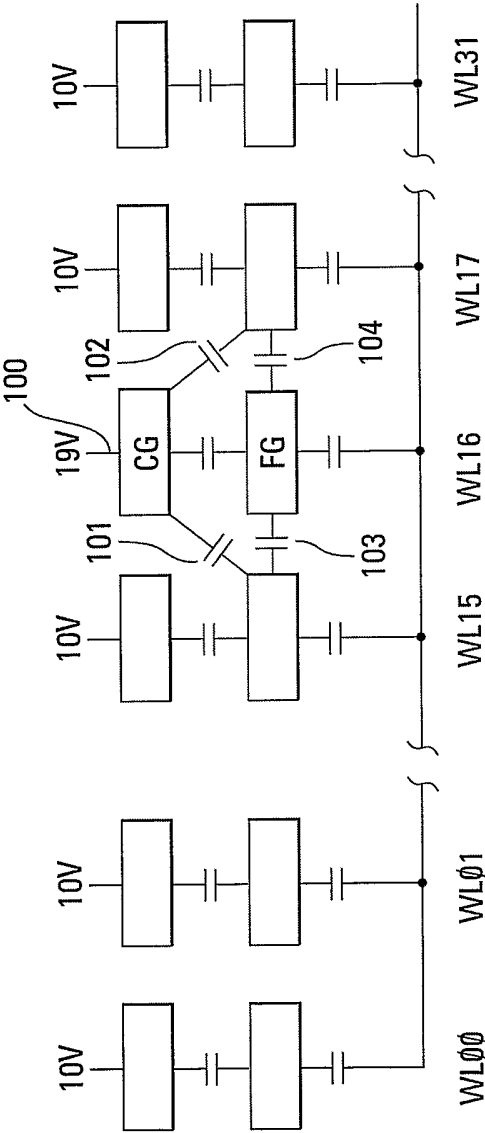
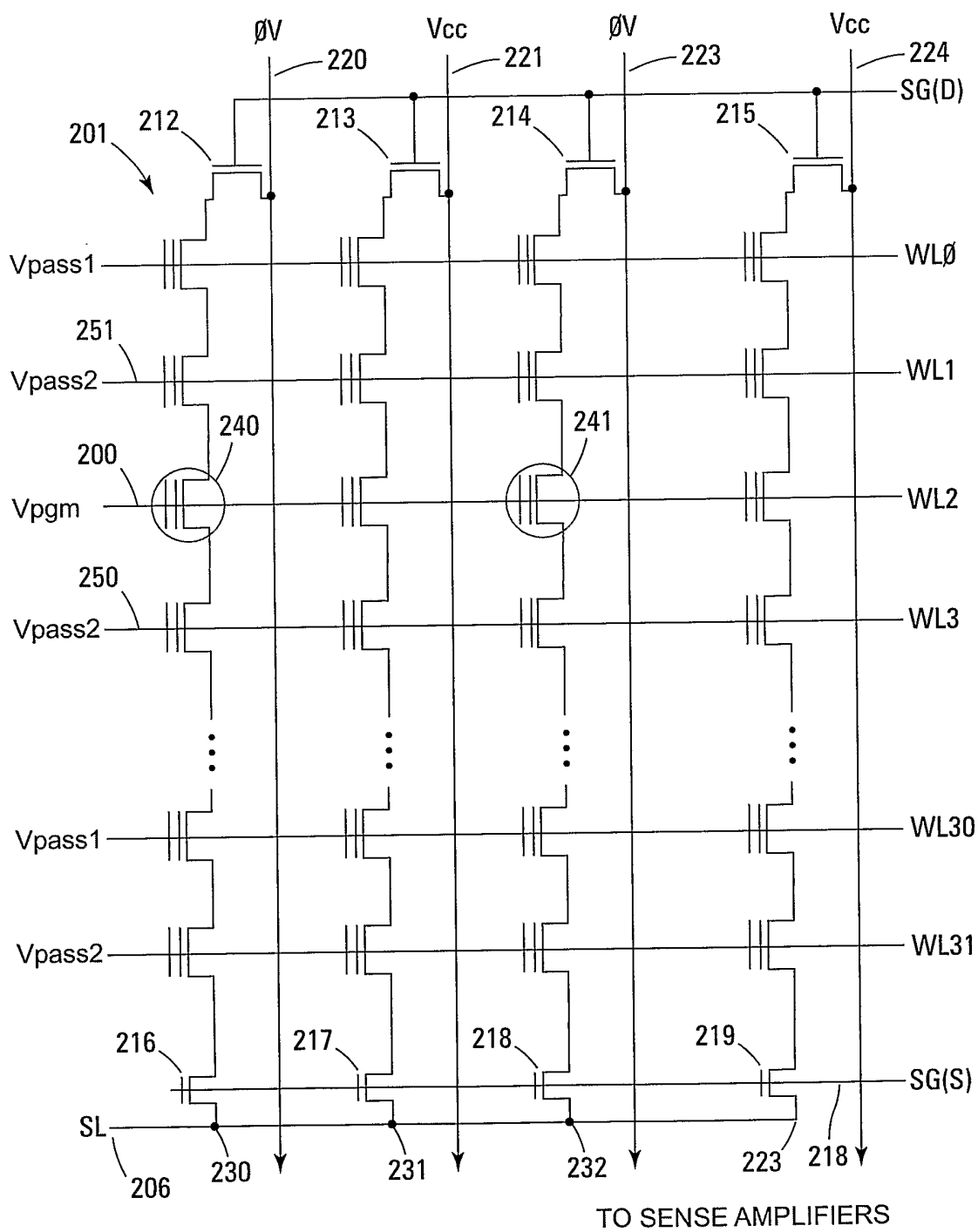
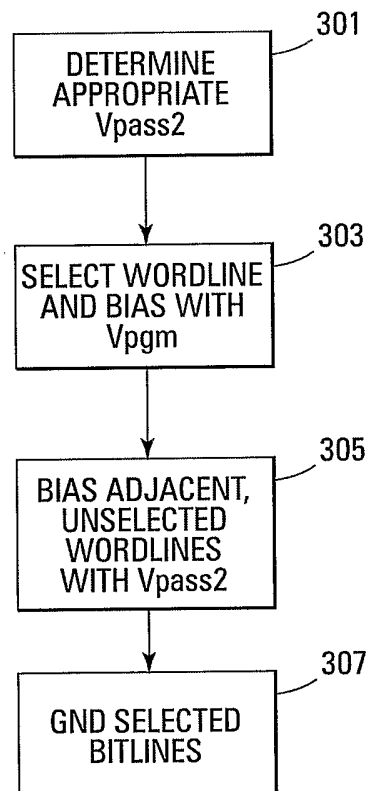


Fig. 1
Prior Art

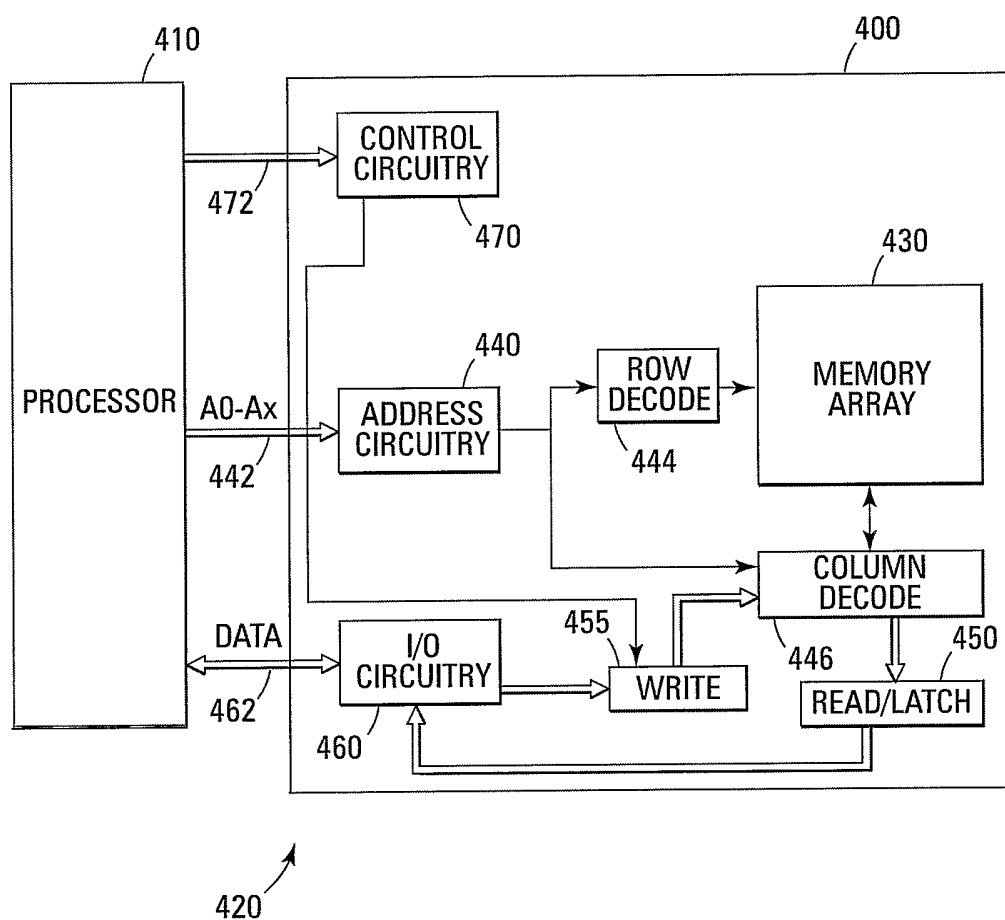
2/4

*Fig. 2*

3/4

*Fig. 3*

4/4

*Fig. 4*

INTERNATIONAL SEARCH REPORT

US2005/022469

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C16/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 107 658 A (ITOH ET AL) 22 August 2000 (2000-08-22)	1-3, 7-12, 15-18, 20-26
Y	column 2, line 11 - column 17, line 5; figures 13,14,20,23	4-6,13, 14,19 28,29
Y	----- -/--	

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

* Special categories of cited documents:

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Name and mailing address of the ISA

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INTERNATIONAL SEARCH REPORT

US2005/022469

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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