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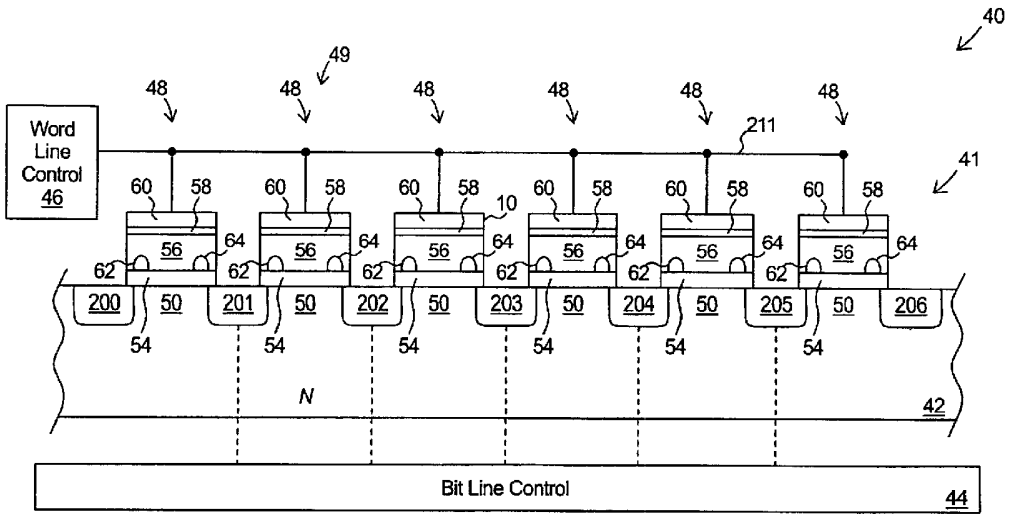
(54) Title: IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL



(57) Abstract: A method of detecting a charge stored on a charge storage region (62) of a first dual bit dielectric memory cell (49) within an array (40) of dual bit dielectric memory cells (48) comprises coupling a first bit line (201) that forms a source junction with a channel region (50) of the first memory cell (49) to ground (68). A high voltage is applied to a gate (60) of the first memory cell (49) and to a second bit line (202) that is the next bit line to the right of the first bit line (201) and separated from the first bit line (201) only by the channel region (50). A third bit line (203), that is the next bit line to the right of the second bit line (202), is isolated such that its potential is effected only by its junctions with the a second channel region (50) and a third channel region (50) on opposing sides of the third bit line (203). A high voltage is applied to a pre-charge bit line that is to the right of the third bit line (203) and current flow is detected at the second bit line (202) to determine the programmed status of a source bit (62) of the first memory cell (49).

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IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL

Technical Field

The present invention relates generally to flash memory cell devices and more specifically, to improvements in pre-charge reading methods for reading a charge previously stored in a dual bit dielectric memory cell dielectric memory cell structure.

Background of the Invention

Conventional floating gate flash memory types of EEPROMs (electrically erasable programmable read only memory), utilize a memory cell characterized by a vertical stack of a tunnel oxide (SiO_2), a polysilicon floating gate over the tunnel oxide, an interlayer dielectric over the floating gate (typically an oxide, nitride, oxide stack), and a control gate over the interlayer dielectric positioned over a crystalline silicon substrate. Within the substrate are a channel region positioned below the vertical stack and source and drain diffusions on opposing sides of the channel region.

The floating gate flash memory cell is programmed by inducing hot electron injection from the channel region to the floating gate to create a non volatile negative charge on the floating gate. Hot electron injection can be achieved by applying a drain to source bias along with a high control gate positive voltage. The gate voltage inverts the channel while the drain to source bias accelerates electrons towards the drain. The accelerated electrons gain 5.0 to 6.0eV of kinetic energy which is more than sufficient to cross the 3.2eV Si-SiO_2 energy barrier between the channel region and the tunnel oxide. While the electrons are accelerated towards the drain, those electrons which collide with the crystalline lattice are re-directed towards the Si-SiO_2 interface under the influence of the control gate electrical field and gain sufficient energy to cross the barrier.

Once programmed, the negative charge on the floating gate disburses across the semi conductive gate and has the effect of increasing the threshold voltage of the FET characterized by the source region, drain region, channel region, and control gate. During a "read" of the memory cell, the programmed state (e.g. negative charge stored on the gate), or the non-programmed state (e.g. neutral charge stored on the gate) of the memory cell can be detected by detecting the magnitude of the current flowing between the source and drain at a predetermined control gate voltage. More recently dielectric memory cell structures have been developed. A conventional array of dielectric memory cells 10a - 10f is shown in cross section in Figure 1. Each dielectric memory cell is characterized by a vertical stack of an insulating tunnel layer 18, a charge trapping dielectric layer 22, an insulating top oxide layer 24, and a polysilicon control gate 20 positioned on top of a crystalline silicon substrate 15. Each polysilicon control gate 20 may be a portion of a polysilicon word line extending over all cells 10a-10f such that all of the control gates 20a - 20g are electrically coupled.

Within the substrate 15 is a channel region 12 associated with each memory cell 10 that is positioned below the vertical stack. One of a plurality of bit line diffusions 26a - 26g separate each channel region 12 from an adjacent channel region 12. The bit line diffusions 26 form the source region and drain region of each cell 10. This particular structure of a silicon channel region 22, tunnel oxide 12, nitride 14, top oxide 16, and polysilicon control gate 18 is often referred to as a SONOS device.

Similar to the floating gate device, the SONOS memory cell 10 is programmed by inducing hot electron injection from the channel region 12 to the nitride layer 22 to create a non volatile negative charge within charge traps existing in the nitride layer 22. Again, hot electron injection can be achieved by applying a drain-to-source

bias along with a high positive voltage on the control gate 20. The high voltage on the control gate 20 inverts the channel region 12 while the drain-to-source bias accelerates electrons towards the drain region. The accelerated electrons gain 5.0 to 6.0 eV of kinetic energy which is more than sufficient to cross the 3.2 eV Si-SiO_2 energy barrier between the channel region 12 and the tunnel oxide 18. While the electrons are accelerated towards the drain region, those electrons which collide with the crystalline lattice are re-directed towards the Si-SiO_2 interface under the influence of the control gate electrical field and have sufficient energy to cross the barrier. Because the nitride layer stores the injected electrons within traps and is otherwise a dielectric, the trapped electrons remain localized within a drain charge storage region that is close to the drain region. For example, a charge can be stored in a drain bit charge storage region 16b of memory cell 10b. The bit line 26b operates as the source region and bit line 26c operates as the drain region. A high voltage may be applied to the channel region 20b and the drain region 26c while the source region 26b is grounded.

Similarly, a source-to-drain bias may be applied along with a high positive voltage on the control gate to inject hot electrons into a source charge storage region that is close to the source region. For example, grounding the drain region 26c in the presence of a high voltage on the gate 20b and the source region 26b may be used to inject electrons into the source bit charge storage region 14b.

As such, the SONOS device can be used to store two bits of data, one in each of the source charge storage region 14 (referred to as the source bit) and the charge storage region 16 (referred to as the drain bit).

Due to the fact that the charge stored in the storage region 14 only increases the threshold voltage in the portion of the channel region 12 beneath the storage region 14 and the charge stored in the storage region 16 only increases he threshold voltage in the portion of the channel region 16 beneath the storage region 16, each of the source bit and the drain bit can be read independently by detecting channel inversion in the region of the channel region 12 between each of the storage region 14 and the storage region 16. To "read" the drain bit, the drain region is grounded while a voltage is applied to the source region and a slightly higher voltage is applied to the gate 20. As such, the portion of the channel region 12 near the source/channel junction will not invert (because the gate 20 voltage with respect to the source region voltage is insufficient to invert the channel) and current flow at the drain/channel junction can be used to detect the change in threshold voltage caused by the programmed state of the drain bit.

Similarly, to "read" the source bit, the source region is grounded while a voltage is applied to the drain region and a slightly higher voltage is applied to the gate 20. As such, the portion of the channel region 12 near the drain/channel junction will not invert and current flow at the source/channel junction can be used to detect the change in threshold voltage caused by the programmed state of the source bit.

In a typical flash memory array, the structure wherein each of multiple cells shares a common word line with adjacent cells creates a problem in reading each cell. For example, when reading bit 14b, the bit line 26b is grounded while a voltage is applied to bit line 26c and to the gate 20b. Current flow at the bit line 26c (representing electrons pulled from the grounded bit line 26b through the channel region 12b) is used to detect threshold voltage of the cell 10b to determine the programmed state of the source bit 14b.

A problem is that because the gate 20b is coupled by the same wordline as gates 20c - 20f, the gate 20c is also biased high. As such, a current may also flow into the bit line 26c through the cell 20c thereby causing a false read of the bit 14b. To prevent such a current flow, a pre-charge bias is typically applied to the bit line 26d. However, even a small difference in voltage between the bit line 26c and the bit line 26d can cause a

current flow and a false read.

What is needed is an improved method for reading a dual bit dielectric memory cell that does not suffer the disadvantages of the known methodologies.

Summary of the Invention

A first aspect of the present invention is to provide a method of detecting a charge stored on a source charge storage region of a first dual bit dielectric memory cell within an array of dual bit dielectric memory cells. The method comprises grounding a first bit line that forms a source junction with a channel region of the first memory cell. The channel region is to the right of first bit line. A high voltage is applied to a second bit line that forms a drain junction with the channel region and is positioned to the right of the channel region and separated from the first bit line only by the channel region. A high voltage is applied to a gate of the first memory cell. A third bit line, that is the next bit line to the right of the second bit line, is isolated such that its potential is effected only by its junctions with the a second channel region and a third channel region on opposing sides of the third bit line. A high voltage is applied to a pre-charge bit line that is to the right of the third bit line and current flow is detected at the second bit line.

In a first embodiment, the pre-charge bit line may be a fourth bit line that is the next bit line to the right of the third bit line and separated from the third bit line only by the third channel region.

The method may also comprise applying a high voltage to a second pre-charge bit line, the second pre-charge bit line being a fifth bit line that is the next bit line to the right of the fourth bit line and separated from the fourth bit line only by the fourth channel region.

In a second embodiment, the pre-charge bit line may be a fifth bit line. The method may comprise isolating a fourth bit line, that is the next bit line to the right of the third bit line, such that its potential is effected only by its junctions with the third channel region and a fourth channel region on opposing sides of the fourth bit line. The fifth bit line may be the next bit line to the right of the fourth bit line and separated from the fourth bit line only by the fourth channel region.

In this embodiment, the method may further comprise applying a high voltage to a second pre-charge bit line, the second pre-charge bit line being a sixth bit line that is the next bit line to the right of the fifth bit line.

A second aspect of the present invention is also to provide a method of detecting a charge stored in a charge storage region adjacent to a first bit line within an array of dual bit dielectric memory cells. The method comprises applying a positive voltage bias to a second bit line with respect to the first bit line. The second bit line is separated from the first bit line only by a first channel region that is positioned beneath the charge storage region. A positive voltage bias is applied to a word line with respect to the first bit line. The word line is positioned over the first channel region. A neutral voltage bias is applied to a pre-charge bit line with respect to the second bit line. The pre-charge bit line may separated from the second bit line by: i) a second channel region that is adjacent to the second bit line; ii) a third bit line that is adjacent to the second channel region; and iii) a third channel region that is adjacent to the third bit line. The third bit line may be isolated such that its potential is affected only by its junctions with each of the second channel region and the third channel region. Current flow is detected at the second bit line to determine the programmed state of the charge storage region.

The method may further comprise applying a neutral voltage bias to a second pre-charge bit line with respect to the second bit line. The second pre-charge bit line may be separated from the second bit line by: i) the second channel region that is adjacent to the second bit line; ii) the third bit line that is adjacent to the second

channel region; iii) the third channel region that is adjacent to the third bit line; iv) the pre-charge bit line; and v) a fourth channel region that is adjacent to the pre-charge bit line.

In an alternative embodiment of the second aspect of the present invention, the pre-charge bit line may be separated from the second bit line by: i) a second channel region that is adjacent to the second bit line; ii) a third bit line that is adjacent to the second channel region; iii) a third channel region that is adjacent to the third bit line; iv) a fourth bit line that is adjacent to the third channel region; and v) a fourth channel region that is adjacent to the fourth bit line. In such embodiment, the method may further comprise isolating the fourth bit line such that its potential is effected only by its junctions with each of the third channel region and the fourth channel region.

The alternative embodiment method may further comprise applying a neutral voltage bias to a second pre-charge bit line with respect to the second bit line. The second pre-charge bit line may be separated from the second bit line by: i) the second channel region that is adjacent to the second bit line; ii) the third bit line that is adjacent to the second channel region; iii) the third channel region that is adjacent to the third bit line; iv) the fourth bit line that is adjacent to the third channel region; v) the fourth channel region that is adjacent to the fourth bit line; vi) the pre-charge bit line; and vii) a fifth channel region that is adjacent to the pre-charge bit line.

A third aspect of the present invention is to provide an array of dual bit dielectric memory cells. The array comprises a first bit line and a second bit line, positioned to the right of the first bit line, each of a first conductivity semiconductor. A first channel region of an opposite conductivity semiconductor is positioned between the first bit line and the second bit line - and forms a junction with each of the first bit line and the second bit line. A charge storage layer is positioned above the first channel region and separated from the first channel region by a first insulating barrier. A gate is positioned over the charge storage layer and separated from the charge storage layer by a second insulating barrier. A second channel region of the first conductivity semiconductor is positioned to the right of the second bit line and forms a junction with the second bit line, a third bit line of the first conductivity semiconductor is positioned to the right of the second channel region and forms a junction with the second channel region, a third channel region of the opposite conductivity semiconductor is positioned to the right of the third bit line and forms a junction with the third bit line, and a pre-charge bit line of the first conductivity semiconductor is positioned to the right of the third channel region. A word line control circuit operates to couple a high voltage to the gate and a bit line control circuit operates to: i) coupling the first bit line to ground; ii) couple a high voltage to the second bit line; iii) isolating the third bit line such that its potential is effected only by its junctions with the second channel region and the third channel region; and iv) couple a high voltage to the pre-charge bit line. A current sensor circuit detects state of a charge stored in the charge storage layer by detecting current flow at the second bit line.

In a first embodiment of the third aspect of the present invention, the pre-charge bit line may be a fourth bit line that forms a junction with the third channel region and is separated from the third bit line only by the third channel region. Consistent with the first embodiment, the array may further comprise: i) a fourth channel region of the opposite conductivity semiconductor and positioned to the right of the fourth bit line and forming a junction with the fourth bit line; and ii) a second pre-charge bit line of the first conductivity semiconductor, the second pre-charge bit line being a fifth bit line that is to the right of the fourth channel region and forms a junction with the fourth channel region. The bit line control circuit may further provide for applying a high voltage to the second pre-charge bit line.

In a second embodiment of the third aspect of the present invention, the array may further comprise: i) a fourth bit line of the first conductivity semiconductor and positioned to the right of the third channel region and forms a junction with the third channel region; and ii) a fourth channel region of the opposite conductivity semiconductor and positioned to the right of the fourth bit line and forms a junction with the fourth bit line. The pre-charge bit line is a fifth bit line that is the right the forth bit line and separated from the fourth bit line only by the fourth channel region. And, the bit line control circuit may further provides for isolating the fourth bit line such that its potential is effected only by its junctions with the third channel region and the fourth channel region.

Further yet, the array may comprise: i) a fifth channel region of the opposite conductivity semiconductor and positioned to the right of the fifth bit line and forms a junction with the fifth bit line; and ii) a second pre-charge bit line of the first conductivity semiconductor and being a sixth bit line that is positioned to the right of the fifth channel region and forms a junction with the fifth channel region. The bit line control circuit may further provide for applying a high voltage to the second pre-charge bit line.

In a third embodiment of the fifth aspect of the present invention, a voltage control circuit may provide for: i) applying a positive voltage bias to the second bit line with respect to the first bit line; ii) applying a positive voltage bias to the word line with respect to the first bit line; iii) applying a neutral voltage bias to the pre-charge bit line with respect to the second bit line; and iv) isolating the third bit line such that its potential is effected only by its junctions with each of the second channel region and the third channel region.

For a better understanding of the present invention, together with other and further aspects thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, and its scope will be pointed out in the appended clams.

Brief Description of the Drawings

Figure 1 is a schematic, cross sectional view of a dielectric memory cell array known in the prior art;

Figure 2 is a schematic, block diagram view of a dielectric memory cell array in accordance with one embodiment of the present invention;

Figure 3 is a schematic, cross sectional view of the dielectric memory cell array of Figure 2;

Figure 4a is a state machine diagram representing exemplary operation of an array control circuit; and

Figure 4b is a table representing exemplary operating embodiments of an array control circuit in accordance with this invention.

Description of the Preferred Embodiments

The present invention will now be described in detail with reference to the drawings. In the drawings, like reference numerals are used to refer to like elements throughout. Further, the diagrams are not drawn to scale and the dimensions of some features are intentionally drawn larger than scale for purposes of showing clarity.

Figure 2 shows an exemplary embodiment of a dual bit dielectric memory cell array 40 in block diagram form. The array 40 comprises a plurality of dual bit dielectric memory cells 48, an array control circuit 62, and a current sense circuit 66 fabricated on a crystalline semiconductor substrate. The array of dual bit dielectric memory cells 48 is arranged in a matrix format with horizontal rows of polysilicon word lines 210-213 and vertical columns of alternating bit line diffusions 200-205 and channel regions 50 within the substrate 42. Each cell 48 within a column shares the same channel region 50 and the two bit lines adjacent to the channel

region with other cells 48 in the column. Each cell 48 within a row shares the same word line 72 with other cells 48 in the row.

Reference is not made to the cross section diagram of a row of dual bit dielectric memory cells which share a common word line 211 as shown in Figure 3 in conjunction with the Figure 2. It should be appreciated that the polysilicon word line 211 is structure to form a control gate 60 over each cell 48 in the row. The bit line diffusions 200 - 206 are of opposite semi conductive conductivity as the channel regions 50 such that the bit line diffusions 200 - 206 form a source region and a drain region for each cell in the column. In the exemplary n-mos device, the channel region 50 is an n-type semiconductor such as crystalline silicon lightly implanted with an electron donor impurity such arsenic and the bit line diffusion 200 - 206 is a p-type semiconductor such as crystalline silicon implanted with a hole donor impurity such as boron.

Above the channel region 50 is a first insulating barrier or tunnel layer 54 which may comprise silicon dioxide. The thickness of the tunnel layer 54 may be within a range of about 50 to about 150 angstroms. An embodiment with a more narrow bracket includes a tunnel layer 54 thickness within a range of about 60 to about 90 angstroms and even narrower yet, a tunnel layer 54 with a thickness of about 70 to about 80 angstroms.

Above the tunnel layer is a charge trapping layer 56 that includes both a source charge trapping region or source bit 62 and a drain charge trapping region or drain bit 64 each for storing a neutral charge representing an un-programmed state or a negative charge representing a programmed state. The charge trapping layer 56 may comprise a nitride compound with suitable charge trapping properties and may have a thickness on the order of 20 to 100 angstroms. In the exemplary embodiment, the nitride compound may be selected from the group consisting of Si_2N_4, Si_3N_4 and SiO_xN_4.

Above the charge trapping layer 56 is a top dielectric layer 58. The top dielectric layer 58 may be silicon dioxide or may be a material with a dielectric constant greater than the dielectric constant than silicon dioxide (e.g. a high K material). In a preferred embodiment, the high K material may be selected from the group of materials consisting of Al_2O_3, $HfSi_xO_y$, HfO_2, ZrO_2, and $ZrXi_xO_y$ and other materials with similarly high dielectric constants. If the top dielectric layer 58 is silicon dioxide, the layer 58 may have a thickness on the order of 60 to 100 angstroms. Alternatively, if the top dielectric layer 58 is a high K material, its electrical thickness may be on the order of 60 to 100 angstroms while its physical thickness may be within a range of about 70 to 130 angstroms. An embodiment with a more narrow bracket includes a top dielectric layer 58 with a thickness within a range of about 80 to about 120 angstroms and even narrower yet, a top dielectric layer 58 with a thickness of about 90 to about 100 angstroms.

Above the top dielectric layer 58 is the word-line 211 forming the gate 60 over each cell 48 within a row. In the exemplary embodiment, the gate 60 may comprises polysilicon with a thickness on the order of 4,000 angstroms. The word-line 211 is coupled to the word line control circuit 46.

The array control circuit comprises a word line control circuit 46, a bit line control circuit 44, a voltage divider circuit 64, a coupling to an operating power source (Vcc) 70 and a coupling to a ground 68. In operation, the array control circuit 62 operates to selectively couple each word line 210-213 and each bit line 200-205 to a voltage provided by the voltage divider 64 or to ground (or to isolate a word line 210-213 or bit line 200-205 from all voltage sources and ground such that is potential is effected only by electrical interaction with other structure of the array 40). The coupling is in such a manner that each source charge trapping region

62 and each drain charge trapping region 64 within the array 40 can be erased, selectively programmed, and selectively read. The array control circuit 62 also operates to couple a selected bit line (for example bit line 202) to the current sensor 66 such that a current on the selected bit line 202 may be measured to indicate the programmed state of a selected source charge trapping region 62 or drain charge trapping region 64 of a cell 48 within a column of cells in which such selected bit line 202 is either a source or a drain.

The current sensor 66 may utilize known circuits for sensing current on the selected bit line 202 that is coupled to the current sensor 66 by the bit line control circuit 44. The current sensed represents the programmed state of a selected one of a source charge trapping region 62 or a drain charge trapping region 64 when applicable potentials are coupled to applicable word lines and bit lines by the array control circuit 62 for reading the selected charge trapping region as described in more detail herein.

Array Control Circuit

Turning briefly to Figure 4a in conjunction with Figure 2 and Figure 3, the array control circuit 62 operates in three states, a program state 76 where in charge is selectively stored into the source charge trapping region 62 or the drain charge trapping region 64 of a selected one of the memory cells 48 (e.g. selected memory cell 49), a read state 78 wherein a stored charge is detected from the source charge trapping region 62 or the drain charge trapping region 62 of a selected one of the memory cells 48 to reproduce data originally stored in such charge trapping region, and an erase state 78 wherein charge stored in charge trapping regions 62 and 64 of one or more memory cells 48 is removed prior to reprogramming in the program state 76.

When in the program state 76, the source charge trapping region 62 is programmed by injecting electrons into the source charge trapping region 62 using a hot electron injection technique. More specifically, the array control circuit 62 couples bit lines 200 - 206 and word lines 210 - 213 to various potentials (e.g provided by the voltage divider 64 and ground 68) to apply a high source-to-drain bias while applying a high voltage to the control gate 60. For example, referring to selected cell 49, this may be accomplished by the bit line control circuit 44 coupling the bit line 202, which represents the drain region of selected cell 49, to ground 68 and coupling the bit line 201, which represents the source region of selected cell 49, to a voltage source from the voltage divider 64 of approximately 5 volts. Simultaneously, word line control circuit 46 couples the word line 211, representing the control gate 60 of the selected cell 49, to a voltage source from the voltage divider 64 of approximately 10 volts. The voltage on the control gate 60 inverts the channel region 50 of the selected cell 49 while the high source-to-drain bias draws and accelerates electrons from the drain region bit line 202 into the channel region 50 towards the source region bit line 201.

The 4.5eV to 5eV kinetic energy gain of the electrons is more than sufficient to surmount the 3.1eV to 3.5eV energy barrier at channel region 50/tunnel layer 54 interface and, while the electrons are accelerated towards source region 201, the field caused by the high voltage on control gate 60 redirects the electrons towards the source charge trapping region 62. Those electrons that cross the interface into the source charge trapping region 62 remain trapped within the charge trapping layer 56 for later reading.

Similarly, the drain charge trapping region 64 is programmed by injecting electrons into the drain charge trapping region 64 using a hot electron injection technique. More specifically, the array control circuit 62 couples bit lines 200 - 206 and word lines 210 - 213 to various potentials (e.g provided by the voltage divider 64 and ground 68) to apply a high drain-to-source bias while applying a high voltage to the control gate 60. For example, again referring to selected cell 49, this may be accomplished by the bit line control circuit 44 coupling

the bit line 201, which represents the source region of the selected cell 49, to ground 68 and the bit line control circuit 44 coupling the bit line 202, which represents the drain region of the selected cell 49, to a voltage source from the voltage divider 64 of approximately 5 volts. Simultaneously, the word line control circuit 46 couples the word line 211, representing the control gate 60 of the selected cell 49, to a voltage source form the voltage divider 64 of approximately 10 volts. The voltage on the control gate 60 inverts the channel region 50 while the high drain-to-source bias draws and accelerates electrons from the source region bit line 201 into the channel region 50 towards the drain region bit line 202.

Again, the 4.5eV to 5eV kinetic energy gain of the electrons is more than sufficient to surmount the 3.1eV to 3.5eV energy barrier at the channel region 52/tunnel layer 54 interface and, while the electrons are accelerated towards drain region 52, the field caused by the high voltage on control gate 60 redirects the electrons towards the drain charge trapping region 64.

When in the erase state 74, the array control circuit may couple applicable bit lines 200-206 and word lines 210-213 to applicable potentials such that the source charge trapping region 62 and the drain charge trapping region 64 of multiple cells 48 are erased using either a hot hole injection technique or by tunneling the electrons from the charge trapping layer 56 to the gate 60. Both techniques are known in the art.

When in the read state 78, the presence of trapped electrons (e.g a negative charge representing a programmed state) in a selected source charge trapping region 62 or drain charge trapping region 64 are detected. It is recognized that the presence of trapped electrons within a source charge trapping region 62 or a drain charge trapping region 64 effect depletion within the channel region 50 below such charge trapping regions. As such, the presence of trapped electrons in either the source charge trapping region 62 or the drain charge trapping region 64 effect the threshold voltage of a field effect transistor (FET) characterized by the control gate 60, a bit line diffusion 200 - 206 that functions as a source region, and a bit line diffusion 200 - 206 that functions as a drain region. Therefore, each bit of the dual bit memory cell 48 may be "read", or more specifically, the presence of electrons stored within each of the source charge trapping region 62 and the drain charge trapping region 64 may be detected by operation of the FET.

In particular, the presence of electrons stored within a source charge trapping region 62 of the selected cell 49 may be detected by applying a positive voltage to the control gate 60 and a lesser positive voltage to the bit line 202 that functions as the drain region while the bit line 201 that functions as the source region is coupled to ground 68. The current flow is then measured at the bit line 202 that functions as the drain region. Assuming proper voltages and thresholds for measurement (and assuming no current leakage from adjacent memory cells 48 within the same row as the selected cell 49 and assuming no current leakage form memory cells 48 within the same column as the selected cell 49, if there are electrons trapped within the source charge trapping region 62, no current (or at least no current above a threshold) will be measured at the bit line 202 comprising the drain region. Otherwise, if the source charge trapping region 62 is charge neutral (e.g., no trapped electrons) then there will be a measurable current flow into bit line functioning as the drain region. Similarly, the presence of electrons stored within the drain charge trapping region 64 may be detected by the same method, and merely reversing the bit line 202 functioning as the source region and the bit line functioning as the drain region.

Recognizing that current leakage from adjacent memory cells 48 in the same row as the selected cell 49 may affect accurate reading. The table of Figure 4b represents four exemplary embodiments 80, 82, 84, and 86 of operation of the array control circuit 62 for reading the source charge trapping region 62 in the presence of

possible current leakage from adjacent cells 48. The same embodiments may be utilized for reading a drain charge trapping region 64 by reversing the potential applied to each of the bit lines representing the source region and the drain region in accordance with the teachings above.

Referring to the table of Figure 4b in conjunction with Figure 3, exemplary embodiment 80 comprises the word line control circuit 46 coupling the word line 211 associated with the selected cell 49 to be read to a gate voltage source on the order of 10 volts from the voltage divider 64 while coupling adjacent word lines 210 and 212 to ground 68. The bit line control circuit 44 couples the bit line 201 that comprises the source region of the selected cell 4 to be read to ground 68. The bit line control circuit 44 further couples the bit line 202 that comprises the drain region of the selected cell 49 to be read to a high voltage source form the voltage divider 64 that is a positive voltage greater than ground and less than or equal to the gate voltage (e.g. the drain bit line 202 has a neutral bias to the voltage of gate 60 and a positive bias to the source bit line 201 while the gate 60 has a positive bias to the source bit line 201). For example, if the source bit 62 of the selected cell 49 is to be read, the bit line control circuit couples the bit line 201 to ground 68 and bit line 202 to the high voltage.

The bit line control circuit 44 isolates the next bit line to the right of the drain bit line (e.g bit-line 203) in the example of reading the source bit 62 of the selected cell 49 such that its potential may float while being effected only by its junctions with each of the channel regions 50 on opposing sides of the bit line 203.

The bit line control circuit couples the next bit line to the right of bit line 203 (e.g. bit line 204), to the high voltage source such that it is neutral biased to the voltage on the control gate 60 and positive biased with respect to the source bit line 201. Because 204 is coupled to the high voltage source, it may be referred to as a pre-charged bit line.

The exemplary embodiment 82 comprises the word line control circuit 46 coupling the word line 211 associated with the selected cell 49 to be read to the gate voltage from the voltage divider 64 while coupling adjacent word lines 210 and 212 to ground 68. The bit line control circuit 44 couples the bit line 201 that comprises the source region of the selected cell 49 to ground 68 and couples the bit line 202 that comprises the drain region of the selected cell 49 to the high voltage source from the voltage divider 64.

The bit line control circuit 44 isolates the next bit line to the right of the drain bit line 202 (e.g. isolates the bit line 203) such that its potential may float while being effected only by its junctions with each of the channel regions 50 on opposing sides of the bit line 203.

The bit line control circuit 44 couples the next two bit lines (e.g. 204 and 205) to the right of floating bit line 203 to the high voltage source such that both of these pre-charged bit lines are neutral biased with respect to the voltage of the control gate 60 and positive biased with respect to the voltage of the source bit line 201.

The exemplary embodiment 84 comprises the word line control circuit 46 coupling the word line 211 associated with the selected cell 49 to be read to the gate voltage from the voltage divider 64 while coupling adjacent word lines 210 and 212 to ground 68. The bit line control circuit 44 couples the bit line 201 that comprises the source region of the selected cell 49 to ground 68 and couples the bit line 202 that comprises the drain region of the selected cell 49 to the high voltage source form the voltage divider 64.

The bit line control circuit 44 isolates the next two bit lines to the right of the drain bit line (e.g. isolates the bit lines 203 and 204) such that the potential of each may float while being effected only by its junctions with each of the channel regions 50 on opposing sides.

The bit line control circuit couples the next bit line (e.g. 205) to the right of the two floating bit lines

203 and 204 to the high voltage source such that this pre-charged bit line is neutral bias with respect to the voltage of the control gate 60 and biased high with respect to the voltage of the source bit line 201.

The exemplary embodiment 86 comprises the word line control circuit 46 coupling the word line 211 associated with the selected cell 49 to be read to the gate voltage source from the voltage divider 64 while coupling adjacent word lines 210 and 212 to ground. The bit line control circuit 44 couples the bit line 201 that comprises the source region of the selected cell 49 to ground and couples the bit line 202 that comprises the drain region of the selected cell 49 to the high voltage source form the voltage divider 64.

The bit line control circuit 44 isolates the next two bit lines to the right of the drain bit line (e.g. isolates the bit lines 203 and 204) such that the potential of each may float while being effected only by its junctions with each of the channel regions 50 on opposing sides.

The bit line control circuit couples the next two bit lines (e.g. 205 and 206) to the right of floating bit lines 203 and 204 to the high voltage source such that both of these pre-charged bit lines are neutral bias with respect to the voltage of the control gate 60 and biased high with respect to the voltage of the source bit line 201.

In summary, the method for reading data from a dual bit dielectric memory cell of this invention provides for more accurate reading in view of potential current leakage from adjacent cells. Although this invention has been shown and described with respect to certain preferred embodiments, it is obvious that equivalents and modifications will occur to others skilled in the art upon the reading and understanding of the specification. For example, Although the cells of the array are shown as a substantially planar structure formed on the silicon substrate, it should be appreciated that the teachings of this invention may be applied to both planar, fin formed, and other dielectric memory cell structures which may be formed on suitable semiconductor substrates which include, for example, bulk silicon semiconductor substrates, silicon-on-insulator (SOI) semiconductor substrates, silicon-on-sapphire (SOS) semiconductor substrates, and semiconductor substrates formed of other materials known in the art. The present invention includes all such equivalents and modifications, and is limited only by the scope of the following claims.

CLAIMS

What is claimed is:

1. A method of detecting a charge stored on a source charge storage region 62 of a first dual bit dielectric memory cell 49 within an array 40 of dual bit dielectric memory cells 48, the method comprising:

grounding a first bit line 201 that forms a source junction with a channel region 50 of the first memory cell 49, the channel region 50 being to the right of the first bit line 201;

applying a high voltage to a gate 60 of the first memory cell 49;

applying a high voltage to a second bit line 202 that forms a drain junction with the channel region 50, the second bit line 202 positioned to the right of the first bit line 201 and to the right of the channel region 50;

isolating a third bit line 203 such that its potential is effected only by its junctions with the a second channel region 50 and a third channel region 50;

the third bit line 203 being to the right of the second bit line 202 and separated from the second bit line 202 only by the second channel region 50 that is positioned there between;

the third channel region 50 being positioned to the right of the third bit line 203;

applying a high voltage to a pre-charge bit line, the pre-charge bit line being to the right of the third bit line 203; and

detecting current flow at the second bit line 202.

2. The method of claim 1, wherein the pre-charge bit line is a fourth bit line 204 that is the next bit line to the right of the third bit line 203 and separated from the third bit line 203 only by the third channel region 50 that is positioned there between.

3. The method of claim 2, further comprising applying a high voltage to a second pre-charge bit line, the second pre-charge bit line being a fifth bit line 205 that is the next bit line to the right of the fourth bit line 204 and separated from the fourth bit line 204 only by a fourth channel region 50 positioned there between.

4. The method of claim 1, further comprising

isolating a fourth bit line 204, that is the next bit line to the right of the third bit line 203, such that its potential is effected only by its junctions with the third channel region 50 and a fourth channel region 50 on opposing sides of the fourth bit line 204; and

wherein the pre-charge bit line is a fifth bit line 204 that is the next bit line to the right of the fourth bit line 204 and separated from the fourth bit line 204 only by the fourth channel region 50 positioned there between.

5. The method of claim 4, further comprising a high voltage to a second pre-charge bit line, the second pre-charge bit line being a sixth bit line 206 that is the next bit line to the right of the fifth bit line 205 and separated from the fifth bit line 205 only by a fifth channel region 50 positioned there between.

6. An array 40 of dual bit dielectric memory cells 48, the array 40 comprising:

a first bit line 201 of a first conductivity semiconductor;

a first channel region 50 of an opposite conductivity semiconductor forming a junction with the first bit line 201;

a charge storage layer 56 positioned above the first channel region 50 and separated from the first channel region 50 by a first insulating barrier 54;

a word line 211 forming a gate 60 positioned over the charge storage layer 56 and separated from the charge storage layer 56 by a second insulating barrier 58;

a second bit line 202 of the first conductivity semiconductor positioned to the right of the channel region 50 and forming a junction with the channel region 50;

a second channel region 50 of the first conductivity semiconductor and positioned to the right of the second bit line 202 and forming a junction with the second bit line 202;

a third bit line 203 of the first conductivity semiconductor and positioned to the right of the second channel region 50 and forming a junction with the second channel region 50;

a third channel region 50 of the opposite conductivity semiconductor and positioned to the right of the third bit line 203 and forming a junction with the third bit line 203;

a pre-charge bit line of the first conductivity semiconductor and positioned to the right of the third channel region 203;

a word line control circuit 46 for applying a high voltage to the gate 60;

a bit line control circuit 44 for:

coupling the first bit line 201 to ground 68;

applying a high voltage to the second bit line 202;

isolating the third bit line 203 such that its potential is effected only by its junctions with the second channel region 50 and the third channel region 50;

applying a high voltage to the pre-charge bit line; and

a current sensor circuit 66 for detecting the state of a charge stored in the charge storage layer 56 by detecting current flow at the second bit line 202.

7. The array 40 of memory cells 48 of claim 6, wherein the pre-charge bit line is a fourth bit line 204 that forms a junction with the third channel region 50 and is separated from the third bit line 203 only by the third channel region 50.

8. The array 40f memory cells 48 of claim 7, further comprising:

a fourth channel region 50 of the opposite conductivity semiconductor and positioned to the right of the fourth bit line 204 and forming a junction with the fourth bit line 204;

a second pre-charge bit line of the first conductivity semiconductor, the second pre-charge bit line being a fifth bit line 305 that is to the right of the fourth channel region 50 and forms a junction with the fourth channel region 50; and wherein

the bit line control circuit 44 further provides for applying a high voltage to the second pre-charge bit line.

9. The array 40 of memory cells 48 of claim 6:

further comprising:

a fourth bit line 204 of the first conductivity semiconductor and positioned to the right of the third channel region 50 and forming a junction with the third channel region 50;

a fourth channel region 50 of the opposite conductivity semiconductor and positioned to the right of the fourth bit line 204 and forming a junction with the fourth bit line 204;

wherein:

the pre-charge bit line is a fifth bit line 205 that is the right the forth bit line 204 and separated from the fourth bit line 204 only by the fourth channel region 50;

the bit line control circuit further provides for isolating the fourth bit line 204 such that its potential is effected only by its junctions with the third channel region 50 and the fourth channel region 50.

10. The array 40 of memory cells 48 of claim 9, further comprising:

a fifth channel region 50 of the opposite conductivity semiconductor and positioned to the right of the fifth bit line 205 and forming a junction with the fifth bit line 205;

a second pre-charge bit line of the first conductivity semiconductor and being a sixth bit line 206 that is positioned to the right of the fifth channel region 50 and forming a junction with the fifth channel region 50; and

wherein

the bit line control circuit further provides for applying a high voltage to the second pre-charge bit line.

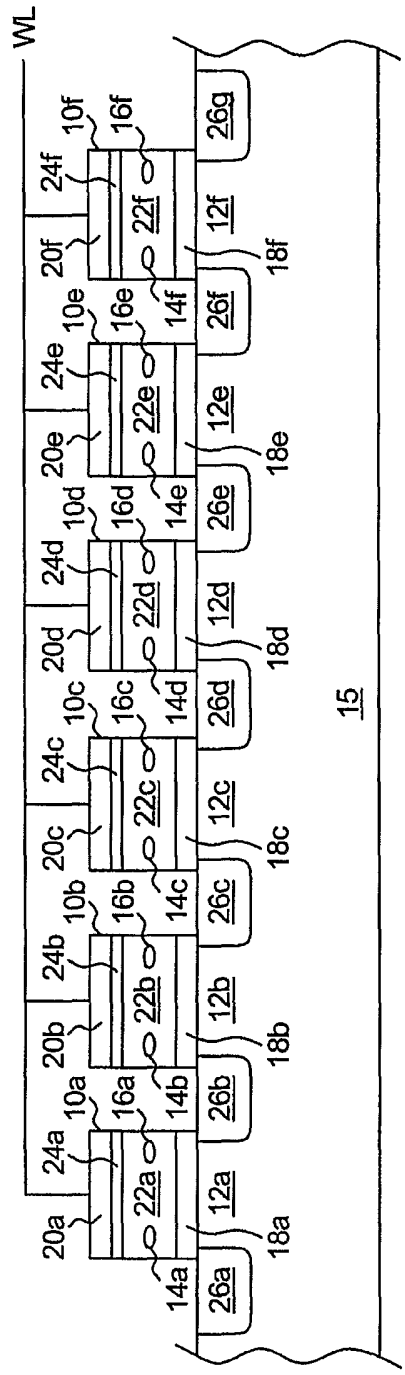
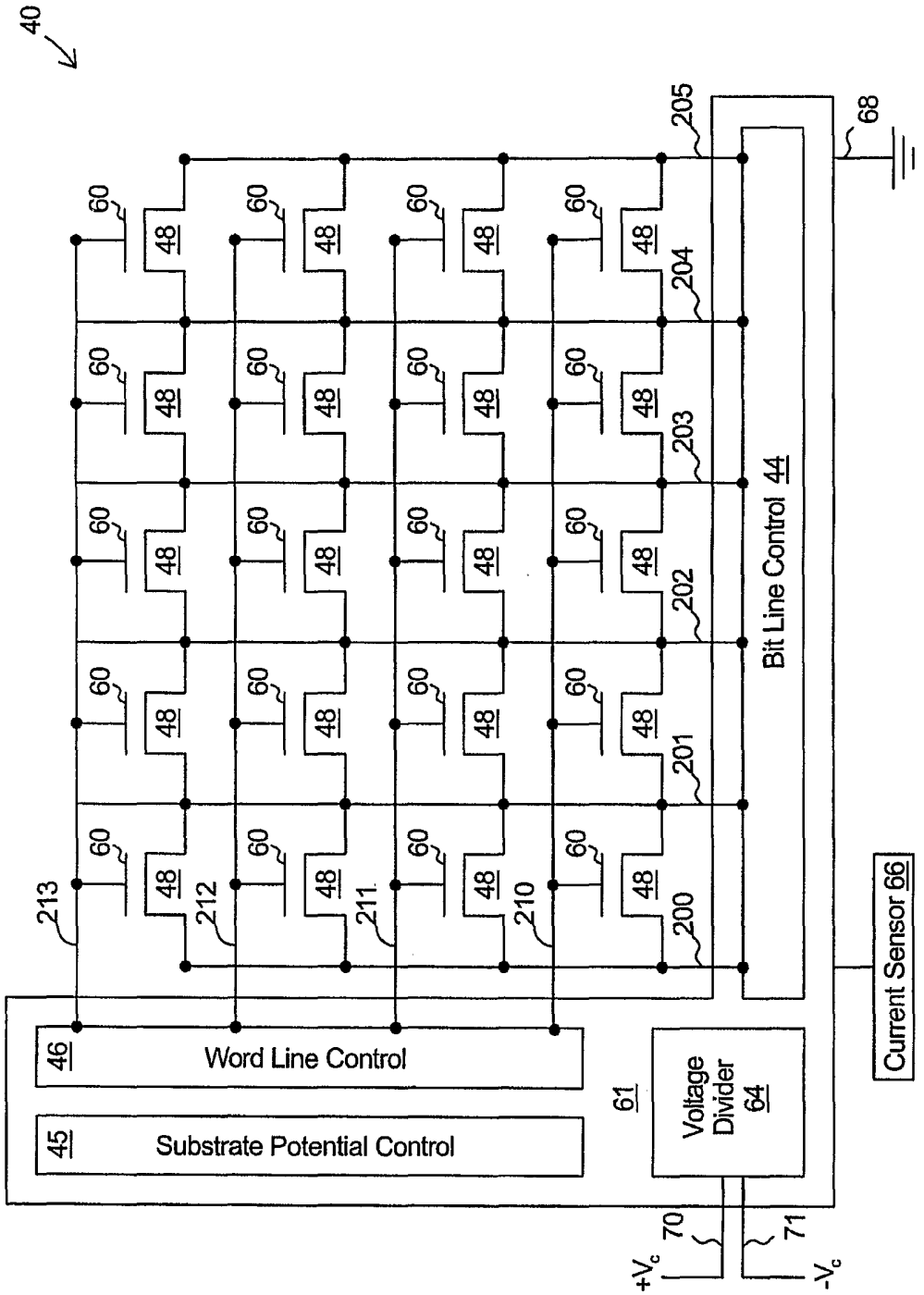


Figure 1
(Prior Art)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205
68
60
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204
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202
201
200
213
212
211
210
Bit Line Control 44
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Word Line Control
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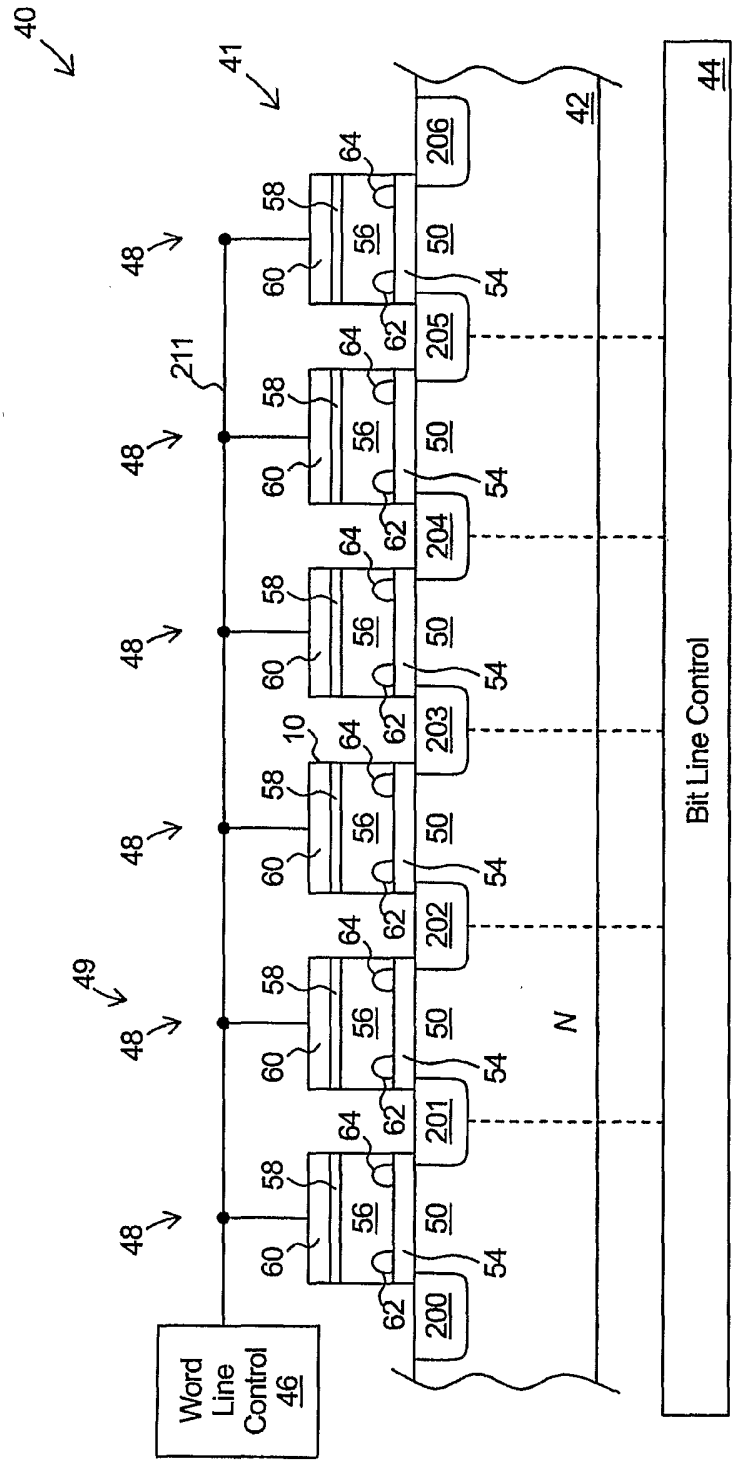
Substrate Potential Control
61
Voltage Divider 64
Current Sensor 66
70
71
+Vc
-Vc

Figure 2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41
42
44
Word Line Control 46
Bit Line Control
N
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201
202
203
204
205
206
211
10
48
49
50
54
56
58
60
62
64

Figure 3

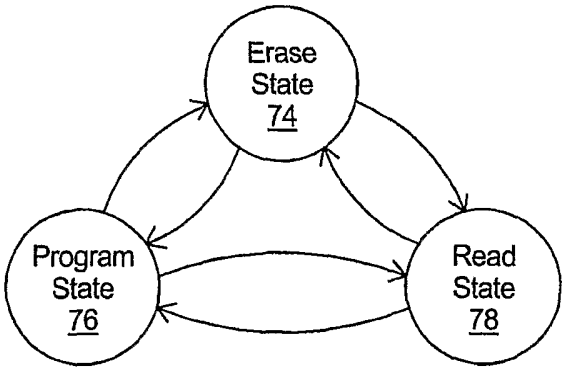

Figure 4

	Programming Voltage	Read Voltage
Selected Word Line 211	Programming Voltage 220	Read Voltage 94
Unselected Word Line 210, 212	Negative Bias Voltage 221	Read Bias Voltage 96

Figure 5

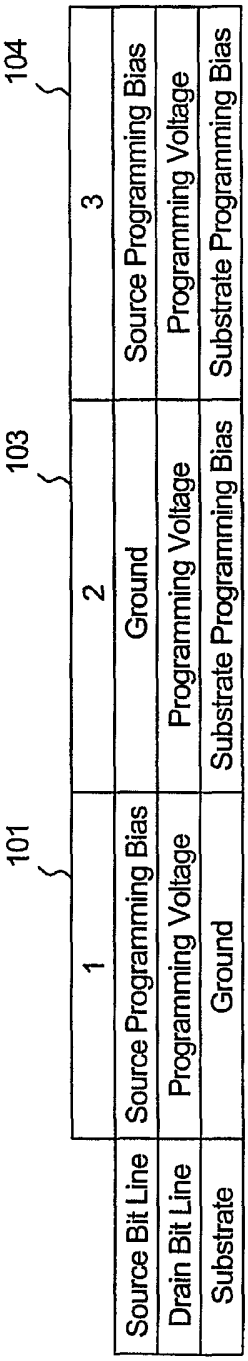

Figure 6

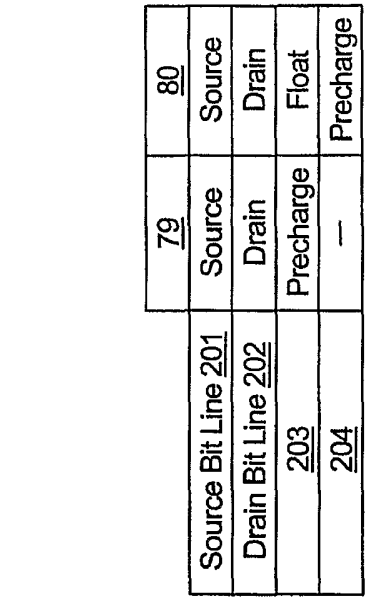

Figure 8

Figure 7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/23087

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C7/12 G11C16/24 G11C16/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 448 518 A (JINBO TOSHIKATSU) 5 September 1995 (1995-09-05) column 3, line 44 -column 6, line 38; figures 3,4	1-10
Y	US 2001/046150 A1 (EITAN BOAZ ET AL) 29 November 2001 (2001-11-29) paragraph '0102! - paragraph '0107!; figure 10	1-10
Y	US 2002/034101 A1 (SEMI ATSUSHI) 21 March 2002 (2002-03-21) paragraph '0020! - paragraph '0037! paragraph '0047! - paragraph '0080!; figures 1,6	1-10

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 October 2003	10/11/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ramcke, T

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/23087

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

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