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(54) Title: ADAPTIVE RECONSTRUCTION OF INFORMATION SIGNALS IN A PLURAL CHANNEL SYSTEM

(57) Abstract

Apparatus for processing information signals in a plurality of information channels comprises a comparator (634-648) for comparing samples of a first information signal in a first channel (Y) with a plurality of selected combinations of the samples of the first signal (Y). A selecting means (650) selects from among the plurality of selected combinations that combination which is the best match with the samples being compared. A generating means (706-772) generates new samples within at least a second of the plurality of information channels (I) by use of the signal (I) in the second channel and the best match combination.

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ADAPTIVE RECONSTRUCTION OF INFORMATION
SIGNALS IN A PLURAL CHANNEL SYSTEM

5   The present invention relates to transmission
systems, and more particularly, to plural channel color
television systems with different channel bandwidths.
         A first aspect of the present invention relates
to reducing the required system data rate without
10 sacrificing picture quality.
         U.S. Patent Application number 132,137, filed
March 20, 1980, entitled "DATA RATE REDUCTION FOR DIGITAL
VIDEO SIGNALS BY SUBSAMPLING AND ADAPTIVE RECONSTRUCTION",
describes a method of data rate reduction for digital video
15 systems by deleting, i.e., not transmitting, every other
picture sample, and transmitting in place of the deleted
samples, a set of "steering" or control bits which enable
the deleted samples to be reconstructed from the nondeleted
(transmitted) samples. In particular, the steering or
20 control bits contain information as to which of the average
of pairs of undeleted samples surrounding the deleted sample
is a closest match to the deleted sample. Thus, at the
receiver the average of the pair that is a closest match to
the deleted sample is substituted for the deleted sample.
25 The present invention contemplates a video signal including
a plurality of component signals, such as red, blue and
green color components of a television signal. Although a
system according to the aforementioned application, when
used with a plural channel system having multiple signal
30 components, will have a lower data rate than a conventional
system, distinct sets of steering bits would be required
for each channel in order to reconstruct the deleted samples
of each channel.
         It is therefore desirable to reduce still further
35 the required data rate and amount of hardware needed.
         A second aspect of the present invention relates
to a television system which has a wide bandwidth luminance
channel and narrow-bandwidth chroma channels. For example,
in a proposed television system, the luminance channel is
40 sampled at four times the chroma subcarrier frequency, while

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two chroma channels are sampled at only twice said frequency
to conserve bandwidth. This system is known as the 4:2:2

5 system. In accordance with the Sampling Theorem (developed
by Nyquist) a bandwidth limited analog signal can be
completely characterized by sampling (or modulating) at a
rate (commonly called the Nyquist rate) which is at least
twice the highest frequency component of the analog signal.

10 Sampling at less than the Nyquist rate results in alias
signals (beats) occurring in the recovered sampled signal.
In the 4:2:2 system the color signal resolution is limited
to one half the luminance signal resolution (by bandwidth
limiting) to avoid aliasing in the narrow-bandwidth color

15 channels.

        It is therefore desirable in accordance with this
second aspect of the invention to have a system where all
channels have a more nearly equal resolution without
increasing the bandwidth of the channel through which

20 they pass.

        In accordance with the principles of the present
invention a method and apparatus for processing information
signals in a plurality of information channels, comprises
comparing samples of information signals in at least one of

25 the channels with a plurality of selected combinations of
the samples within the channel; selecting from among the
plurality of selected combinations that combination which
is the best match with the samples being compared; and
generating new samples within at least one other of the

30 information channels by use of the signal in that one
other channel and the best match combination.

        IN THE DRAWINGS:

        FIGURE 1 shows a diagram useful in explaining
three sampled line-scan rasters which all have distinct

35 sets of steering bits;

        FIGURE 2 is a block diagram of a transmitter in
accordance with the first aspect of the present invention;

        FIGURE 3 shows portions of sampled rasters of
three channels, wherein the transmitted steering bits of

40 only a single channel are located in place of the

undisplayed deleted samples;

FIGURE 4 is a block diagram of a receiver in
5 accordance with the first aspect of the present invention;

FIGURE 5 is a block diagram of a transmission
system including a receiver as in FIGURE 4 together with
an alternate embodiment of a transmitter;

FIGURE 6 illustrates a block diagram of an encoder
10 for encoding samples of a video signal and control signals
in accordance with an embodiment of the first aspect of the
invention;

FIGURE 7 illustrates a block diagram of a decoder
for decoding information encoded by the apparatus of
15 FIGURE 6;

FIGURE 8 shows a block diagram of a minimum-error
logic circuit used in FIGURE 6;

FIGURES 9, 10, 11 and 12 illustrate block diagrams
of filters used in FIGURES 6 and 7;
20 FIGURE 13 shows a block diagram of a digital delay
line used in FIGURES 6, 7, 9, 10, 11 and 12.

FIGURE 14 shows a block diagram of a majority logic
circuit used in FIGURE 2; and

FIGURE 15 shows a block diagram of a steering
25 bit generator that is used in place of the majority logic
circuit used in FIGURE 2.

FIGURE 16 shows an encoder in accordance with
the second aspect of the invention;

FIGURE 17 shows sample patterns on a scanning
30 raster; and

FIGURE 18 shows a decoder in accordance with the
second aspect of the invention.

Referring to the drawing, FIGURE 1 shows portions
of sampled line scanned rasters 10, 12 and 14 respectively
35 and associated signals representative of the red, green
and blue color components of a scene. The symbols R, G,
and B, indicate red, green and blue picture samples of
the rasters 10, 12 and 14 that will be transmitted. These
transmitted samples occur at a 7.16 MHz rate in a preferred
40 embodiment, which is twice the NTSC color subcarrier

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frequency. Thus, a sample occurs every 140 nanoseconds.
The letter S with appropriate subscript represents steering
5   bits that would be transmitted in place of deleted samples
of picture elements if the system of the prior U.S.
application is used for each channel. The steering bits
also occur at a 7.16 MHz rate. It will be noted that every
other sample of the video signal originally sampled at 14.32
10 MHz rate has been deleted in each raster and that the
position of the deleted samples in the raster alternates
in a position from horizontal line to horizontal line.
Therefore, the position of the steering bits also alternates
from line to line. This alternation enables the steering
15 bits to contain information as to which of the surrounding
four pairs of transmitted·samples is the closest or best
match to a particular deleted sample.

Additionally, this best match information indicates
a raster direction that has the least amount of change
20 (least resolution). In FIGURE 1, for the particular
deleted sample designated 114 in the green field, the
average of the vertically adjacent samples 116 and 118,
the average of the horizontally adjacent samples 120 and 122,
the average of the left diagonal samples 128 and 130, or the
25 average of the right diagonal samples 126 and 124, are
compared with sample 114, and the results of the comparisons
are evaluated by a logic circuit to determine which average
of the surrounding samples to be transmitted is the best
approximation to sample 114, which is not to be transmitted.
30 In place of deleted sample 114, a set of steering bits is
added to the bits carrying information as to the amplitude
of previous transmitted sample 120. Since in the above
example there are four choices, the steering word can
comprise as few as two bits, and since they are replacing
35 a deleted sample of eight bits, there is a net reduction
in the amount of information being transmitted (see the
prior application for a more detailed explanation). The
same concept is used for the red and blue fields to
generate steering bits, for a total of three sets of
40 steering bits.

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    The first aspect of the present invention uses
a single set of steering bits to control the steering in
5 all three channels. This is possible because the three
channels of components of a television signal, e.g., R, G,
B, or Y, I, Q, are normally highly redundant when
representing a typical scene, and therefore one set of
steering bits will suffice to indicate the direction of
10 resolution in all three. That is, all three channels will
not ordinarily have edges in different directions at the
same time. Thus, the edges will normally occur in the
same direction.

    FIGURE 2 shows a block diagram of a transmitter
15 for carrying out this concept. Red, green and blue color
representative digital component signals of a single
television raster scan signal are received at input
terminals 16, 18 and 20 respectively. They are applied
to encoders 22R, 22G, and 22B respectively. Outputs 24R,
20 24G, and 24B supply eight parallel digital bits representing
every other sample of the respective input signals to switch
contacts 28R, 28G, and 28B respectively for a time period
until the next sample is present at outputs 24R, 24G, and
24B. For example, if the signals at inputs 16, 18 and 20
25 occur at 70 nanosecond intervals, the signals at outputs
24R, 26G, and 24B, are each simultaneously present for
140 nanoseconds. Outputs 26R, 26G, and 26B each provide
two steering bits in place of the samples that are not
present at outputs 24R, 26G, and 24B respectively. The
30 steering bits are applied to a majority logic circuit 30.
Majority logic circuit 30 is a means of deciding, based
on majority voting of the three sets of steering bits,
which of the three sets of steering bits will best
represent all three channels during reconstruction at the
35 receiver. Thus, if any two or more sets of steering bits
are the same, one of these sets will be transmitted as
the majority steering bits called "Sm" at output 31 and
are present for 140 nanoseconds. Otherwise, the bits
from a single component signal will be selected. Since
40 green is the largest component of a luminance signal, it

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is preferable to select its steering bits for transmission.
Alternately, steering bits may be chosen from the
5 component signal having the largest amplitude. The
selected steering bits are applied to two-bit input contact
28S of switch 32. Rate control circuit 34 sequentially
moves switch 32 among the contacts 28 so that at one-bit
output 36 of the transmitted samples from each of the
10 color component channels are serially supplied along with
the single set of steering bits from majority logic circuit
30. Since there are a total of 26 (3 channels x 8 bits +
1 channel x 2 bits) contacts 28, switch 32 must cycle at a
rate 26 times that of the data rate of the signals at
15 outputs 24R, 24G, 24B of the encoders 22R, 22G, and 22B.
With this system, the samples and data can be represented
as shown in FIGURE 3 where the number of steering bits is
reduced to 1/3 of that needed for fully independent
steering of each channel as shown in FIGURE 1.
20   The picture is reconstructed exactly as in the
independent channel case of the prior U.S. patent
application except that the majority steering bits are
used to steer all three channels as is shown in the
receiver of FIGURE 4. The transmitted data is received at
25 terminal 38 and applied to a serial-to-parallel converter
40 which simultaneously applies the red transmitted
samples to input 42R of red decoder 44R, the green
transmitted samples to input 42G of green decoder 44G,
and the blue transmitted samples to input 42B of blue
30 decoder 44B. Further, the majority steering bits are
simultaneously applied in parallel to inputs 46R, 46G, and
46B of the decoders 44R, 44G, and 44B respectively.
Decoder 44R provides at output terminal 48R, the
reconstructed digital red signal; the decoder 44G

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supplies at output terminal 48G, the reconstructed digital
green signal; and the decoder 44B applies an output
5   terminal 48B, the reconstructed digital blue signal, all
of the reconstruction having been done using majority
steering bits.

The same concept of using a single set of
steering bits may also be used in a luminance (Y) and two
10   color component (I,Q; R-Y, B-Y) system with one slight
difference. The Y channel will have a higher data rate
and consequently a higher bandwidth than either the I or
Q channels. Hence, since the luminance channel Y will have
more resolution than the color channels I and Q, the
15   direction of reconstruction indicated for this channel
will be adequate for the lower bandwidth channels.
Therefore, steering bits derived only from the Y channel
are used to reconstruct the luminance as well as the color
component channels. As shown in FIGURE 5, Y, I and Q
20   digital signals are received at input terminals 50, 52 and
54. In a particular embodiment, the Y signal comprises
samples occurring at four times the color subcarrier
frequency, while the I and Q signals comprise samples
occurring at only twice the subcarrier frequency. The
25   signals are applied to encoders 56Y, 56I and 56Q. Samples
occurring at two times the subcarrier frequency are provided
by the encoders at output 58Y and at the subcarrier
frequency at outputs 58I and 58Q. Encoder 56Y also provides
steering bits at output 60. These steering bits occur at
30   twice the subcarrier rate. All of these signals are
applied to a parallel-to-series converter 62 where they are
sequentially sent as serial data over a transmission path
64 to a serial-to-parallel converter 66. Serial-to-parallel
converter 66 simultaneously provides steering bits from
35   the Y signal to decoders 68Y, 68I and 68Q. It also provides
the Y signal to decoder 68Y, the I signal to decoder 68I,
and the Q signal to decoder 68Q. The decoder 68Y
provides a reconstructed digital Y signal occurring at
four times the subcarrier frequency at output terminal 70Y,
40   the decoder 68I provides a reconstructed digital I signal

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which occurs at two times the subcarrier frequency at
output terminal 70I, and the decoder 68Q provides a
5   reconstructed digital Q signal at output terminal 70Q which
occurs at two times the subcarrier frequency.

FIGURE 6 illustrates an encoder for use in
FIGURES 2 and 5. An input 632 receives the digital
video signal having samples occurring, in a particular
10   embodiment, at 14.32 MHz with 8 bits per sample. The
8 bits of each sample are applied to a delay line 641 and
to filters 634, 636, 638 and 640. These filters are used
to provide the average of the surrounding samples. By
"average" is meant adding together the signal values
15   represented by each of the two 8-bit samples and then
dividing the resulting sum by two. As can be determined
by inspection of FIGURE 1, sample points 128 and 130 are
spaced in time by two horizontal lines and four signal
sampling intervals. In the NTSC system, this corresponds to
20   approximately 127 microseconds plus 280 nanoseconds.

FIGURE 9 illustrates the details of filter 634 which
comprises a digital delay line 900 having a delay of
127 microseconds plus 280 nanoseconds coupled between input
terminals 632 and an input terminal of a digital adder 902.
25   Undelayed signals from terminal 632 also are coupled to a
second input terminal of adder 902. The digital sum of
these signals, corresponding to the video signals at
sample points 128 and 130, is obtained at the output
terminal of adder 902 and coupled to an input terminal of
30   a digital divider 904. Divider 904 divides this summed
signal by two to provide at its output terminal an 8-bit
parallel signal representing the average signal of sample
points 128 and 130. This averaged signal is coupled to an
input terminal of a comparator 642 in FIGURE 6. Delay line
35   641 also comprises an 8-bit digital delay line and has a
delay of about 63.5 microseconds plus 140 nanoseconds.
This time is equal to one-half of the total delay of delay
line 900 of filter 634, and delays the video at sample
point 114 of FIGURE 1 that is not to be transmitted so it

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will be in time coincidence with the averaged signal from
filter 634 so the two signals can be compared by comparator
5   642. Filter 636 supplies the average of points 120 and 122
(a "horizontal" average). It comprises an 8-bit wide
digital delay line 1002 in FIGURE 10 having a delay of
about 140 nanoseconds. The input (undelayed) and output
(delayed) signals of this delay line are averaged by adder
10   1004 and divider 1006. An additional equalizing delay of
one line plus 70 nanoseconds to compensate for the delay
line 641 is provided by delay line 1000 within filter 636.
The output signal of filter 636 from divider 1006 is
supplied to a comparator 644 in FIGURE 6. Filter 638
15   supplies the average of diagonal points 124 and 126 (a
"second diagonal" average). It comprises an 8-bit digital
delay line 1102 in FIGURE 11 having a delay of two
horizontal lines minus 280 nanoseconds. The delayed and
undelayed signals are averaged by adder 1104 and divider
20   1106, while the digital signal from input 632 is first
delay equalized by a 280 nanosecond delay line 1100. The
output signal from divider 1106 is applied to a comparator
646 in FIGURE 6. Lastly, filter 640 supplies the average
of points 116 and 118 (a "vertical" average). It comprises
25   an 8-bit digital delay line 1202 in FIGURE 12 having a
delay of two horizontal lines. The delayed and undelayed
signals are averaged by adder 1204 and divider 1206, while
the digital signal from input 632 is first delay equalized
by a 140 nanosecond delay line 1200. The output signal
30   from divider 1206 is applied to a comparator 648 in
FIGURE 6.
              FIGURE 13 shows an 8-bit wide delay line for use
in the filters 634, 636, 638 and 640 and delay 641. It
comprises eight shift registers 1302, 1304, 1306, 1308,
35   1310, 1312, 1314 and 1316, each of which receives one bit
of the 8-bits simultaneously present at input 1300. The
bits are shifted within the registers under the control of
a clock signal from clock 1338 coupled to shift inputs
1318, 1320, 1322, 1324, 1326, 1328, 1330, and 1334. The

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number of stages of the shift registers are chosen to
achieve the desired delay. The outputs of the shift
5 registers are coupled to 8-bit parallel output 1336.
Comparators 642, 644, 646 and 648 each comprise an 8-bit
subtractor that also receives the original 8-bit samples
through delay line 641 in addition to the outputs of
filters 634, 636, 638 and 640 respectively. The respective
10 two signals in each comparator are subtracted and then the
absolute value is taken of the resulting difference. The
comparators apply absolute value signals to a minimum
error logic circuit 650.

As shown in FIGURE 8, minimum error logic
15 circuit 650 comprises 6 magnitude comparators 882, 884, 886,
888, 890 and 892, each of which receives two 8-bit numbers
from different pairs of the output signals of comparators
642, 644, 646 and 648 and supplies at its respective
output a one-bit logic level indication to indicate which
20 of the two respective input numbers is smaller. It should
be noted that there àre only six possible combinations of
four numbers taken in pairs, thus giving rise to the six
magnitude comparators. It is only necessary to look at
three of the magnitude comparator outputs to determine if
25 a specific magnitude comparator input is the lowest. Thus
NOR gates 894, 896, and 898 are used to detect if the
output signal from comparators 642, 644, and 646
respectively are the lowest. If none are the lowest, the
output signal from 648 is assumed to be the lowest which
30 will be true, or none will be lowest, i.e., they are all
equal, in which latter case the output signal from any
comparator will do. The output signals from gates 894,
896, and 898 are coded by OR gates 800 and 802 into the
2-bit control signal on bus 604 in accordance with the
35 following truth table:

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Line No.	Lowest Signal			
	642	644	646	648
604a	1	0	1	0
604b	0	1	1	0

The output of minimum error logic circuit 650 comprises two
bits in accordance with the above table which indicate which
of the pairs of samples of adjacent points is the closest
match, i.e., represents which direction has the least
change of the video signal around the sample point 114.
This two-bit signal makes up the control signal indicating
which of the transmitted video sample signals most closely
represents the untransmitted video signal so that complete
video information can be obtained upon decoding. The
two central bits are applied to a switch 652 in FIGURE 6,
which is a two-bit switch operated in synchronization with
an 8-bit switch 654 in FIGURE 6 at a 7.16 MHz switching
rate. This switching rate, since it is 14.32 MHz divided
by 2, causes switch 654 to pass or transmit only every
other 8-bit sample. The 2 control bits from logic circuit
650, that indicate which of the adjacent samples are to be
used in reconstructing the untransmitted points, are passed
by switch 652, and together with the 8 bits simultaneously
passed by switch 654 representing a transmitted point,
form a 10-bit parallel word at 10-bit parallel output 655.
          FIGURE 7 shows a decoder for use in the present
invention. The 10-bit parallel signal is received at
input 760. The 8 bits representing a sample of a picture
point are applied by 8-bit bus 761 to filters 762, 764,
766 and 768, the internal construction of which is the
same as filters 634, 636, 638 and 640 respectively. The
same 8 bits are also applied to contact 769a of 8-bit
switch 770 through delay line 706 that has the same delay
as delay line 641 and which compensates for the delay
through filters 762, 764, 766, and 768. The two control

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bits are brought out on 2-bit bus 771 and applied to·
control decoder 772 for control of switches 774, 776,
778, and 780. This decoder comprises a one-of-four
decoder, such as integrated circuit No. SN 74S139,
manufactured by Texas Instruments, that takes the two
control bits and gives a 4-bit parallel output, only one
of which will be high. The 4 parallel bits are applied
to the switches 774, 776, 778 and 780 respectively. Since
only one of the outputs of control decoder 772 will be
high, only one of the switches 774, 776, 778 and 780 will
be closed at any one time at a 7.16 MHz rate. This
applies the signal from that one of the filters 762, 764,
766, and 768 which is the closest match for a missing
sample to contact 769b of switch 770. Switch 770 is
switched at a 14.32 MHz rate between its two inputs 769a
and 769b, and thus alternately supplies a sample point
of the original picture and a reconstructed 8-bit signal
to its output 769c and to decoder output 782. Since
each of the signals occurs at a 7.16 MHz rate, the
resulting signal from output 769c of switch 770 is at
14.32 MHz.

FIGURE 14 shows a block diagram of a majority
logic circuit 30 used in FIGURE 2. In general, it is
desired to use the following rules in order to select the
steering bits. If the red, blue and green sets of
steering bits are all the same, then any one of the sets
can be used, and in this embodiment the red set is used.
If red and green or blue and green are the same, then the
green set is used. If red and blue are the same, then
either red or blue can be used, and in this embodiment
red is used. If all steering bits are different, the
green set is used.

As shown in FIGURE 14, red, blue and green
steering bits (S_R, S_B, and S_G) are received on two-bit
lines 1401, 1403 and 1405 respectively from encoder
outputs 26R, 26B, 26G respectively. The first pair of
corresponding bits of the red and blue steering bits

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are applied to respective inputs of exclusive-NOR gate
1407. Gate 1407 supplies a high signal to one input of
5   AND gate 1409, if both of its inputs are the same. The
remaining second pair of corresponding bits of the red and
blue sets of steering bits are applied to respective inputs
of exclusive-NOR gate 1411. Gate 1411 supplies a high
signal to the other input of AND gate 1409, if both of its
10 inputs are high. Gate 1409 supplies a high signal if
both its inputs are high, i.e., there is a match between
both corresponding pairs of the red and blue steering
bits. The high signal from gate 1409 controls two-bit
switch 1413 so its wiper arm is contacting contact 1415
15 (the position not shown in FIGURE 14) to supply to input 28S
of FIGURE 2 the red steering bits for use as majority
steering bits. If there is no match for either of the
corresponding pairs, then the output signals from either
or both of gates 1407 and 1411 is low and hence the
20 output signal from gate 1409 is also low. Switch 1413
then is in the position shown in FIGURE 14, i.e.,
contacting contact 1417, and the green steering bits are
supplied as the majority steering bits. Thus, the rules
described above are carried out.

25   FIGURE 15 shows a block diagram of a circuit
used instead of majority logic circuit 30 of FIGURE 2.
The circuit of FIGURE 15 provides steering bits from
whichever of signals R, G or B has the greatest
amplitude. Input terminals 1502, 1504, 1506 are coupled
30 to input terminals 16, 18, and 20 respectively and
respectively receive the red, green, and blue digital
signals, and respectively apply said signals to eight-bit
digital delay lines 1508, 1510 and 1512, which delay
lines have the same delay as is inherent in encoders 22R,
35 22G, 22B. The red and green delayed signals are then
applied to magnitude comparator 1514. The delayed green
signal is also applied to magnitude comparator 1518, while
the delayed blue signal is applied to magnitude comparators
1516 and 1518. Magnitude comparator 1516 supplies a zero

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signal to AND gates 1520 and 1522 if the red signal is
less than the blue signal. Similarly, comparator 1518
supplies a zero signal to gate 1522 if the green signal is
less than the blue signal.

The output signals from gates 1520 and 1522 are
called "01" and "02" respectively and are determined in
accordance with the following truth table.

Video Signal Condition	Output Of			01	02
	1514	1516	1518		
R < G < B	0	0	0	1	0
R < B < G	0	0	1	0	0
B < R < G	0	1	1	0	0
G < R < B	1	0	0	1	0
G < B < R	1	1	0	0	1
B < G < R	1	1	1	0	1

The output signals 01 and 02 are present on
two-bit bus 1524, and are used to control switch 1526,
which switch has input terminals 1528, 1530 and 1532 that
receive green, red, and blue steering bits from outputs
26G, 26R, and 26B respectively. An output terminal 1534
supplies to terminal 28S steering bits in accordance with
output signals 01 and 02 (as indicated next to terminals
1528, 1530, and 1532), which in turn is in accordance with
the R, G or B signal having the largest amplitude.

FIGURE 16 shows another embodiment of an encoder
in accordance with the second aspect of the invention. Y,
I and Q analog signals are applied to LPFs (low pass filters)
1601, 1603, and 1605 respectively. The output signals from
the LPFs 1601, 1603 and 1605 are applied to ADCs (analog to
digital converters) 1607, 1609, and 1611, respectively.
A clock signal at about four times the color subcarrier
frequency (4xSC) is generated by generator 1613 and applied
as a sampling signal to ADC 1607 and to divide-by-two
frequency divider 1615. The twice subcarrier frequency
(2xSC) from divider 1615 is applied as a sampling signal

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to ADCs 1609 and 1611. The 8-bit output signals from the
ADCs comprise digital samples of the analog input signals.
5 The position of the Y signal samples on a scanning raster
is shown in FIGURE 17(a). The exact value of the frequency
of the clock signal from generator 1613 is chosen to have
an odd number of samples in each scanning line. This
choice causes the 2xSC samples of both the I and Q signals
10 to be alternate-line offset with respect to signals of the
same type, as shown in FIGURE 17(b). Other ways of
achieving sample offset are known. For example, if an
even number of samples in each scanning line is used,
then the divided 2xSC clock signal can be "paled", which is
15 a shifting of the phase of the clock signal by 180 degrees
from line to line.

In FIGURE 16 all of the LPFs have a bandwidth
cut-off frequency slightly less than 2xSC. However, since
the sampling signals to ADC 1609 and 1611 are 2xSC the
20 Nyquist bandwidth limit for the I and Q channels should be
about 1xSC. Therefore, aliasing will occur in these
channels which will be apparent upon decoding. Thus, the
I and Q channel bandwidth allows passage of signals which
will be sampled at rates at which aliasing will occur.
25 However, due to the phase offset depicted in FIGURE 17(b),
the aliasing will usually occur in a raster direction other
than the direction of the high frequency (highest
resolution) information. Thus, it is usually possible to
remove the aliasing by filtering in the direction of the
30 alias.

FIGURE 18 shows a decoder circuit for
accomplishing this. The 8-bit 4xSC rate Y signal from
FIGURE 16 is applied to a circuit almost identical to
FIGURE 6 and to DAC (digital to analog converter) 1802 that
35 provides the analog Y output signal. As in FIGURE 6,
equalizing delay line 641, filters 634, 636 and 640,
comparators 642, 644, 646 and 648 and minimum error logic
650 all serve to detect in which direction the Y signal has
the least resolution (least amount of change) and to
40 provide a 2-bit output signal from logic 650 that conveys

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this information. This information will be accurate since
the sampling rate for the Y signal satisfies the Nyquist
5   criterion, and therefore there is no aliasing in the Y
channel.

The 8-bit 2xSC rate I and Q signals are
respectively applied to circuits that are essentially
the same as the decoder of FIGURE 7, except that there is
10 now a common control decoder 772. The filters 762, 764,
766 and 768 provide I or Q signals averaged in four
directions, and control decoder 772 sets switches 1804 and
1806 to provide an output signal averaged in the direction
of least resolution as determined from the Y signal. The
15 signal samples from switches 1804 and 1806 are interpolated
between the signal samples from delay lines 706. This
filtering removes aliasing in that direction. For example,
if the scene is of a picket fence having vertically aligned
pickets, there is horizontal information and the aliases in
20 the I and Q signals are in the vertical direction. The
alias free Y signal indicates that the direction of least
resolution is vertical, and this is the direction in which
the filtering is done, i.e. selected as output signals by
switches 1804 and 1806. Switches 770 are switched at 2xSC
25 and alternately provide the delay-equalized 2xSC signals
from delay lines 706, and the 2xSC now alias-free signals
from switches 1804 and 1806. Thus high definition 4xSC
rate signals are applied to DACs 1808 and 1810 in channels
having a bandwidth equal to the sampling rate, without the
30 adverse effect of alias. Therefore analog Y, I and Q
signals are available at the outputs of DACs 1802, 1808
and 1810 respectively. Instead of I and Q signals, other
color difference signals, such as B-Y and R-Y, could have
been used.

35   It will be appreciated that other embodiments
are possible within the spirit and scope of the first
aspect of the invention. For example, transmission path
64 can include a video recorder/reproducer. Further, the
steering or control signal or bits can be transmitted in
40 parallel with the transmitted samples for greater speed.

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Similarly, other embodiments are possible within
the spirit and scope of the second aspect of the invention.
5 For example, the samples could be analog samples, or the
invention can be applied to a system where the Y signal
is not sampled and the I and Q signals amplitude modulate
a color subcarrier.

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CLAIMS:

5   1.   A method for removing aliases from at
least a first component signal of a video signal using
one alias free component of said video signal, said method
comprising determining from said alias free component
the direction of least resolution, and averaging said

10   alias containing component in said direction.

           2.   A method as claimed in Claim 1, further
comprising a second alias containing component signal,
and wherein said alias containing component signals

15   comprise color difference signals and said alias free
signal comprises a luminance signal.

20   3.   A method as claimed in Claim 1, wherein
said determining step comprises averaging said alias
free signal in a plurality of directions, forming the
absolute values of the differences between said
averages and a reference signal, and selecting the
minimum absolute value.

25

           4.   A method as claimed in Claim 1, wherein
said averaging step comprises forming averages of said
alias containing component in a plurality of directions,
and selecting the average in the direction of least

30   resolution.

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5.   A method of encoding at least two signal
components of a video signal, comprising periodically
5   sampling at least a first signal component, said
first signal component having frequency
components that can exceed one half the sampling
frequency, and sampling a second signal component at
a frequency at least about twice the maximum of its
10   highest frequency and about twice the sampling frequency
of said first component signal.

6.   A method as claimed in Claim 5, further
comprising periodically sampling a third signal component
15   of said video signal with offset samples, said third
signal component having frequency components that
can exceed one half the sampling frequency, said first
and third signal components comprising color difference
signals, said second signal component comprising a
20   luminance signal.

7.   An apparatus for removing aliases from
at least a first component signal of a video signal
using one alias free component of said video signal, said
25   apparatus comprising determining means for determining·
from said alias free component the direction of least
resolution, and averaging means for averaging said alias
containing component in said direction.

30   8.   An apparatus as claimed in Claim 7, said
apparatus further comprising a second alias containing
component signal,·and wherein said alias containing
component signals comprise color difference signals and
said alias free signal comprises a luminance signal.

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9. A method as claimed in Claim 7, wherein
said determining means comprises filter means averaging
5   said alias free signal in a plurality of directions,
comparator means for forming the absolute values of
the differences between said averages and a reference
signal, and minimum error logic means for selecting
the minimum absolute value.
10

10. An apparatus as claimed in Claim 7,
wherein said averaging means comprises filter means
for forming averages of said alias containing component
in a plurality of directions, and control decoder means
15   for selecting the average in the direction least
resolution.

11. An apparatus for encoding at least two
signal components of a video signal, comprising means
20   for periodically sampling at least a first signal component
with offset samples, said first signal component having
frequency components that can exceed one half the sampling
frequency, and means for sampling a second signal component
at a frequency at least about twice the maximum of
25   its highest frequency and about twice the sampling
frequency of said first component signal.

12. An apparatus as claimed in Claim 11, further
comprising means for periodically sampling a third signal
30   component of said video signal with offset samples,
said third signal component having frequency components
that can exceed one half the sampling frequency, said
first and third signal components comprising color
difference signals, said second signal component
35   comprising a luminance signal.

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13. A method of transmitting information signals
present in a plurality of information channels, each
signal comprising first and second time portions, said
method comprising transmitting said first portions,
generating control signals from the information of at
least one channel adapted to control the reconstruction
of a plurality of said second portions from the transmitted
first portions, and transmitting said control signals.

14. A method as claimed in claim 13, wherein said
transmitted control signal always is from the same channel.

15. A method as claimed in claim 13, wherein said
channels are at least three in number.

16. A method as claimed in claim 15, wherein said
generating step comprises generating control signals in all
channels, and further comprising determining which of said
control signals are transmitted by majority voting.

17. A method as claimed in claim 15, wherein said
generating step comprises generating control signals in all
three channels and further comprising determining which
of said control signals are transmitted in accordance
with which information signal has the greatest amplitude.

18. A method as claimed in claim 15, wherein said
three channels comprise red, green and blue color
television signals respectively.

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19. A method as claimed in claim 15, wherein said three channels comprise luminance and in-phase and quadrature color television signals respectively.

20. A method as claimed in claim 13, wherein said control signal represents the closest match of the untransmitted second portions of selected combinations of said first portions.

21. An apparatus for transmitting information signals present in a plurality of information channels, each signal comprising first and second time portions, said apparatus comprising means for transmitting said first portions, means for generating a control signal for at least one channel adapted to control the reconstruction of said second portions from the transmitted first portions, and means for transmitting a control signal from only one channel at a time.

22. An apparatus as claimed in claim 21, wherein said transmitted control signal always is from the same channel.

23. An apparatus as claimed in claim 21, wherein said channels are at least three in number.

24. An apparatus as claimed in claim 23, wherein said generating means generates control signals in all channels and further comprising majority logic means for determining which of said control signals are transmitted.

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25.   An apparatus as claimed in claim 23,wherein
said three channels comprise red, green and blue color
5   representative television signals respectively.

26.   An apparatus as claimed in claim 23, wherein
said three channels comprise luminance and in-phase and
10   quadrature color television signals respectively.

27.   An apparatus as claimed in claim 21, wherein
said control signal represents the closest match of the
15   untransmitted second portions of selected combinations of
said first portions.

28.   An apparatus as claimed in claim 23, wherein
20   said generating means comprises means for generating
control signals in all three channels and further
comprising means for determining which of said control
signals are transmitted in accordance with which
information signal has the greatest amplitude.
25

29.   A television sampled transmission channel
adapted for carrying information relating to a plurality
of components of a television signal, comprising:
30   first sampling means for sampling a first
component of said television signal to form samples of a
first component; ·
          second sampling means for sampling a second
component of said television signal to form samples of a
35   second component;
          first transmitting means coupled to first sampling
means for transmitting through said channel a portion of
said samples of said first component;

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Claim 29 (continued):

second transmitting means coupled to said second
5 sampling means for transmitting through said channel a
portion of said samples of said second component;
first and second averaging means coupled to said
first and second transmitting means, respectively, for
generating a plurality of averages of said portions of said
10 first and second components;
control signal generating means coupled to said
transmitting means and to said averaging means for
generating control signals indicative of which of said
averages most closely approximates those portions of said
15 samples which are transmitted, and for transmitting said
control signal; and
decoding means coupled to said first and second
transmitting means and to said control signal generating
means and responsive to one of said control signals for
20 generating for each of said components a regenerated
average signal and for combining said regenerated average
signals with said samples of said first and second
components for reconstituting said components.

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30. A method for processing information signals in a plurality of information channels, comprising:

5   comparing samples of said information signals in at least one of said channels with a plurality of selected combinations of said samples within said channel;

selecting from among the plurality of selected combinations those combinations which are the best match 10 with the samples being compared; and

generating new samples within at least one other of said plurality of information channels by use of the signal in said one other channel and said best match combination.

15

31. Apparatus for processing information signals in a plurality of information channels, comprising:

means for comparing samples of said information 20 signals in at least one of said channels with a plurality of selected combinations of said samples within said channel;

means for selecting from among the plurality of selected combinations those combinations which are the best 25 match with the samples being compared; and

means for generating new samples within at least one other of said plurality of information channels by use of the signal in said one other channel and said best match combination.

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R = RED SAMPLES
S_R = RED STEERING BITS

G = GREEN SAMPLES
S_G = GREEN STEERING BITS

B = BLUE SAMPLES
S_B = BLUE STEERING BITS

Fig. 1 — AN ADAPTIVE COMPONENT SYSTEM

R = RED SAMPLES

G = GREEN SAMPLES
S_M = MAJORITY STEERING BITS

B = BLUE SAMPLES
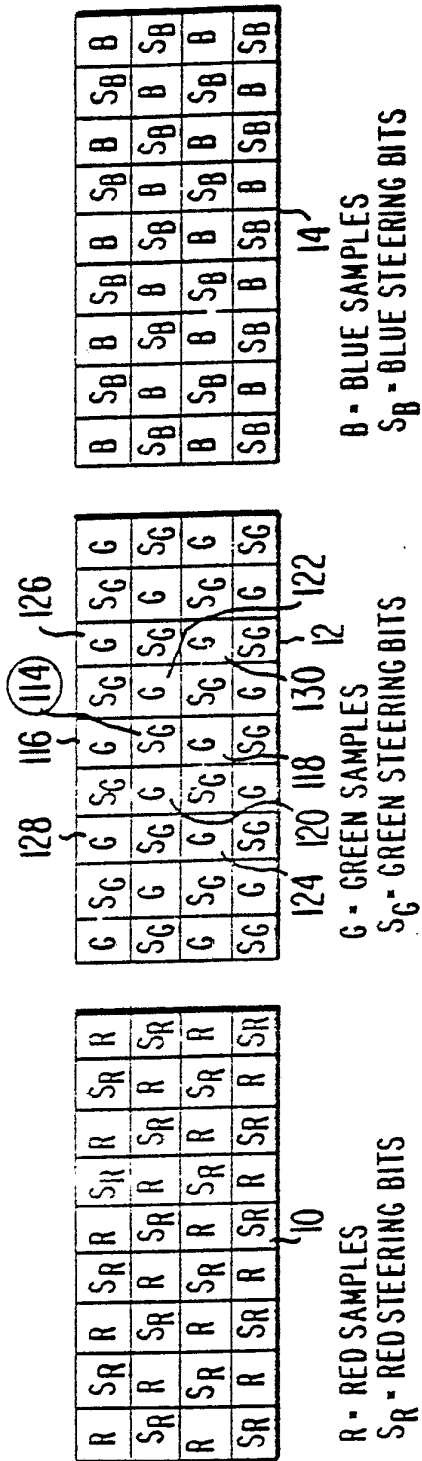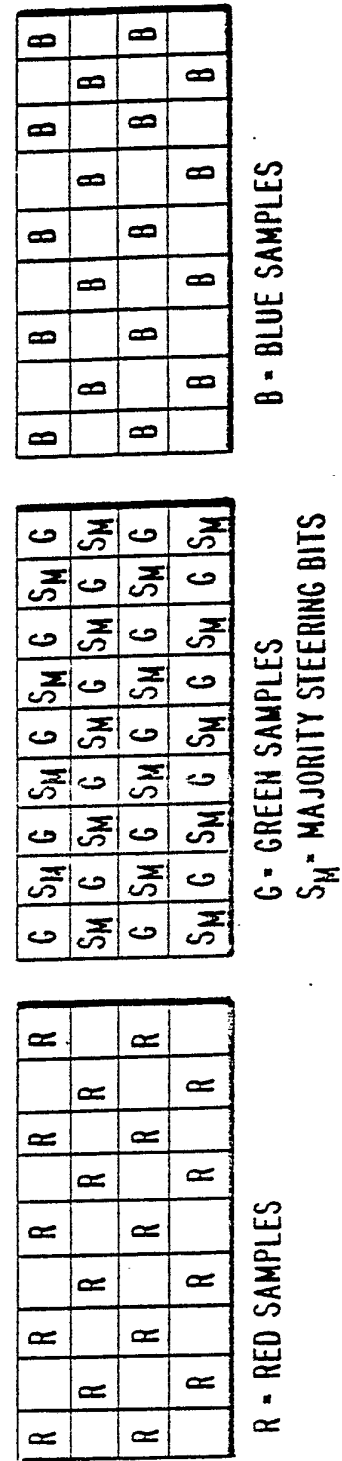
*Fig. 3* — DATA REQUIRED WITH A SINGLE SET OF STEERING BITS

−2−
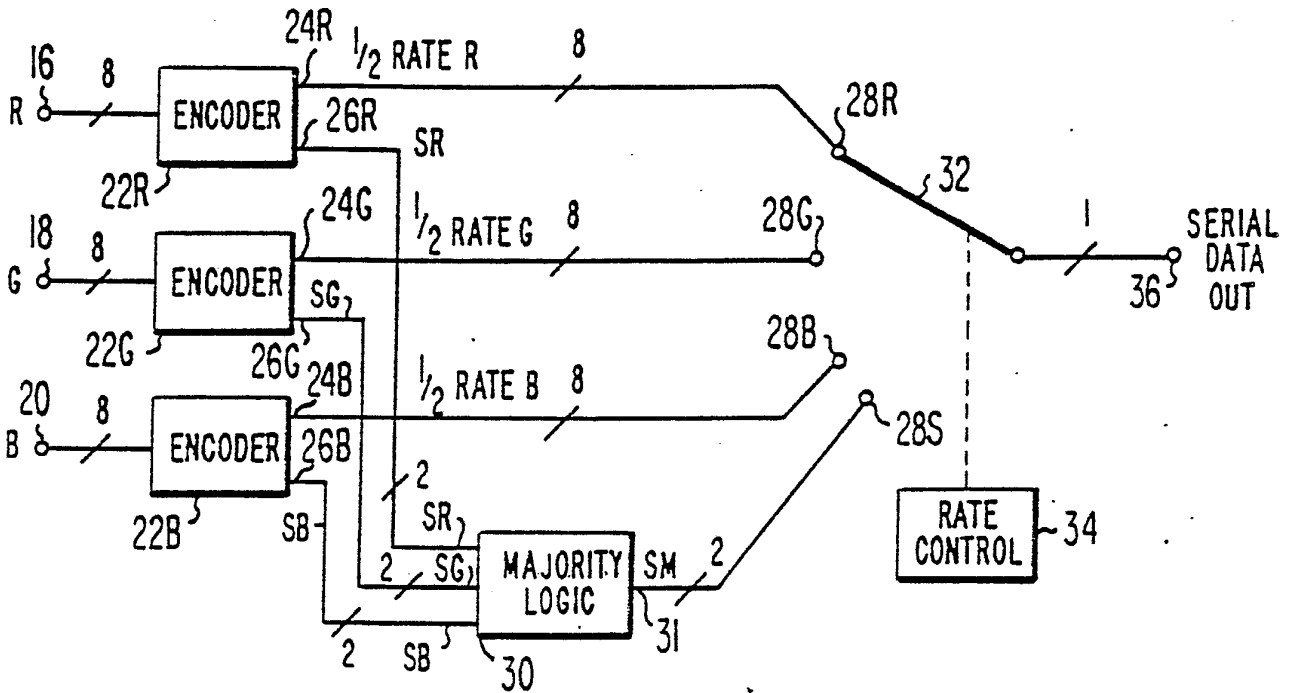
Fig. 2 − AN ADAPTIVE COMPONENT SYSTEM WITH A SINGLE SET OF STEERING BITS
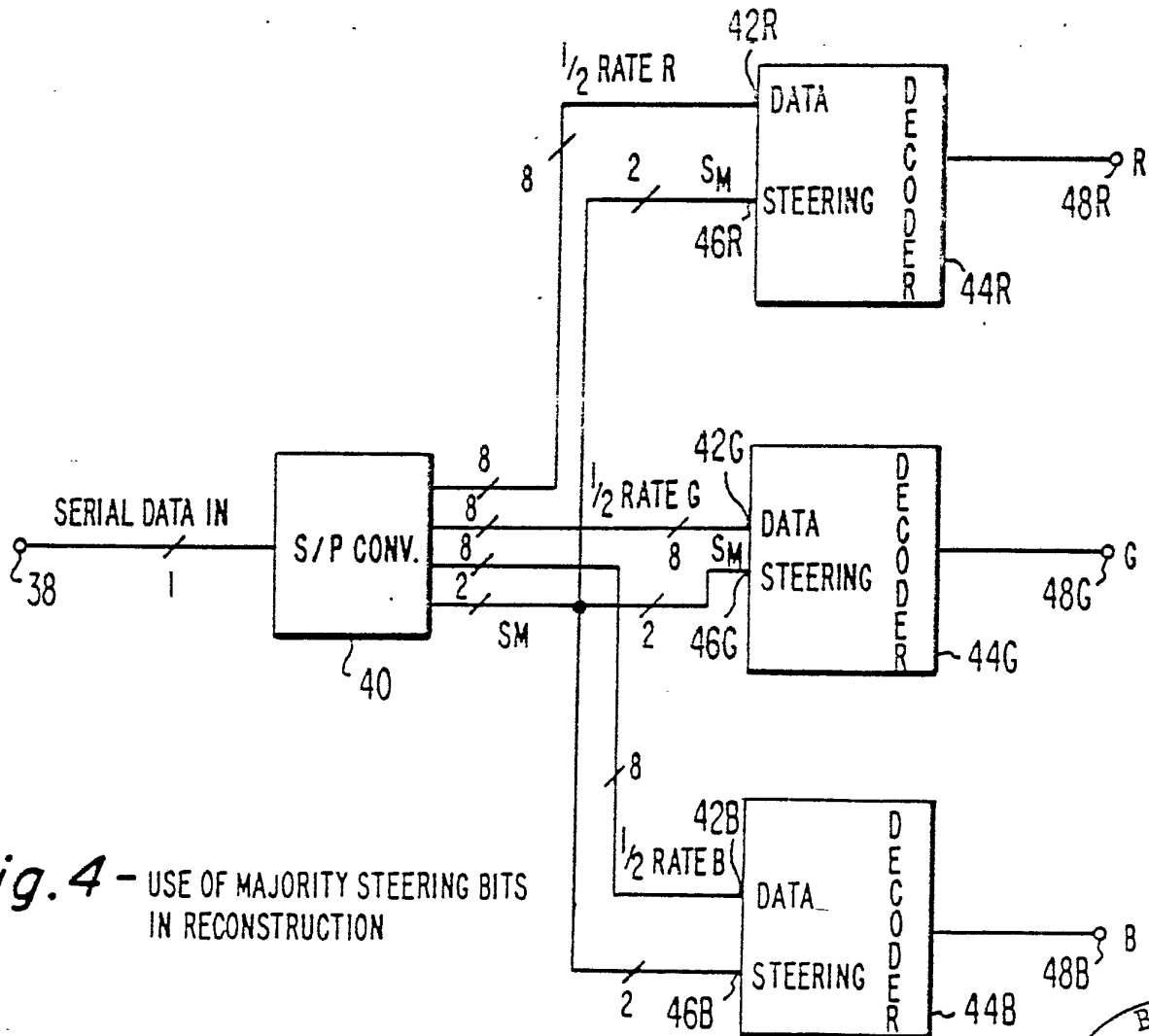
Fig. 4 − USE OF MAJORITY STEERING BITS IN RECONSTRUCTION

−3−
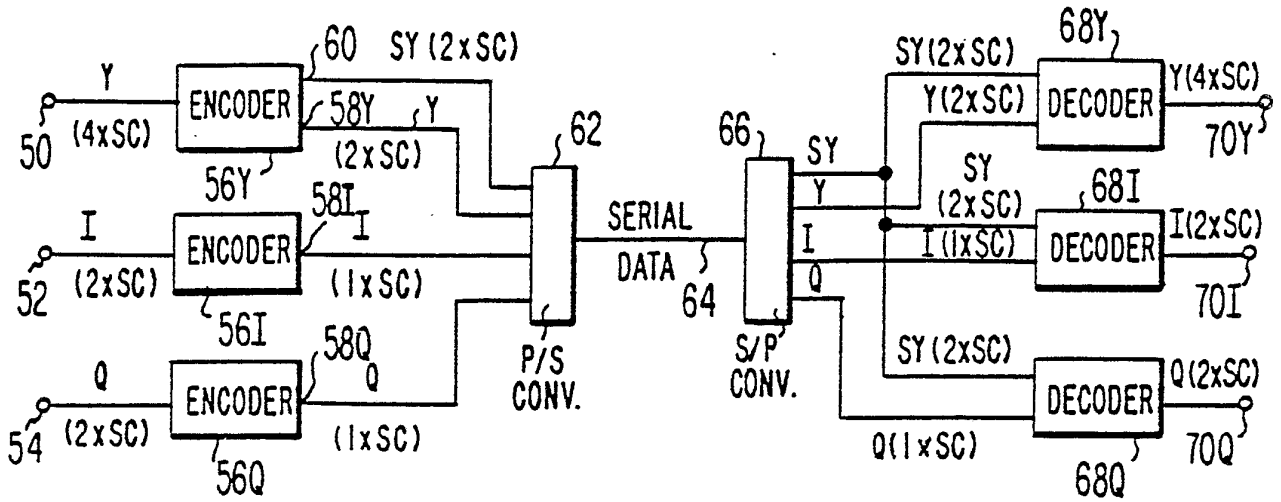
Fig.5 − USE OF LUMINANCE STEERING BITS IN AN ADAPTIVE COMPONENT SYSTEM

ENCODER

Fig.6

−4−

DECODER
Fig. 7

-5-

Fig.8

−6−

$$127 \mu S + 280ns$$

Fig.9

$$63.5 \mu s + 70ns$$ 140ns

Fig.10

280ns $$127 \mu s - 280ns$$

Fig.11

140ns $$127 \mu s$$

Fig.12

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Fig. 13

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Fig. 14

Fig. 15

−9−

Y ──→ │ FILTER │ ────────────────→ │ ADC │ ──→ 8
        1601   1607

I ──→ │ FILTER │ ────────────────→ │ ADC │ ──→ 8
        1603   1609

Q ──→ │ FILTER │ ────────────────→ │ ADC │ ──→ 8
        1605   1611

│ CLOCK │ ──→ │ ÷2 │ ──→
   1613   1615

Fig. 16

○ ○ ○ ○ ○ LINE 1   ○   ○   ○ LINE 1
○ ○ ○ ○ ○ LINE 2   ○   ○   ○ LINE 2
○ ○ ○ ○ ○ LINE 3   ○   ○   ○ LINE 3
○ ○ ○ ○ ○ LINE 4   ○   ○   ○ LINE 4

        Y   I/Q

Fig. 17a   ## Fig. 17b

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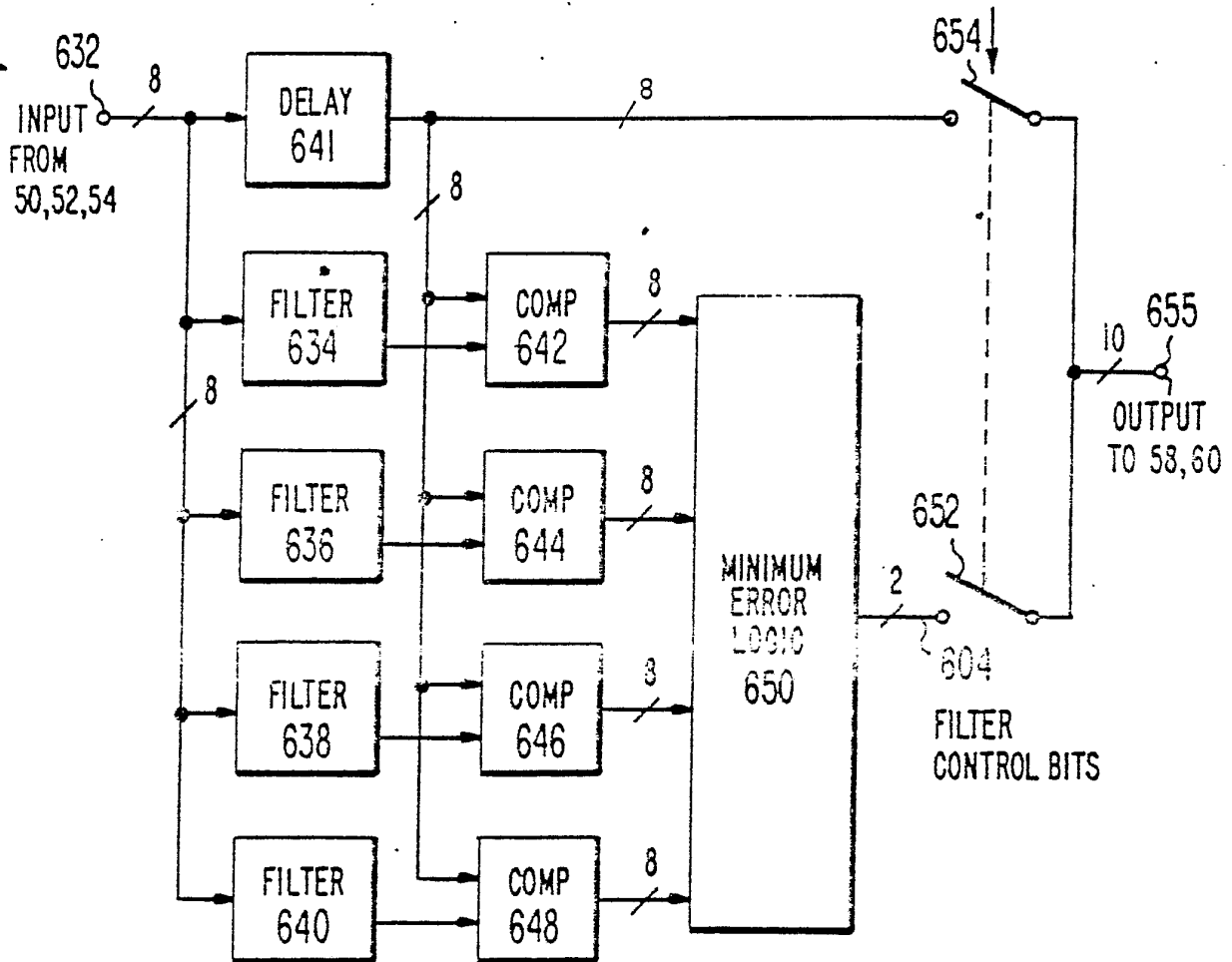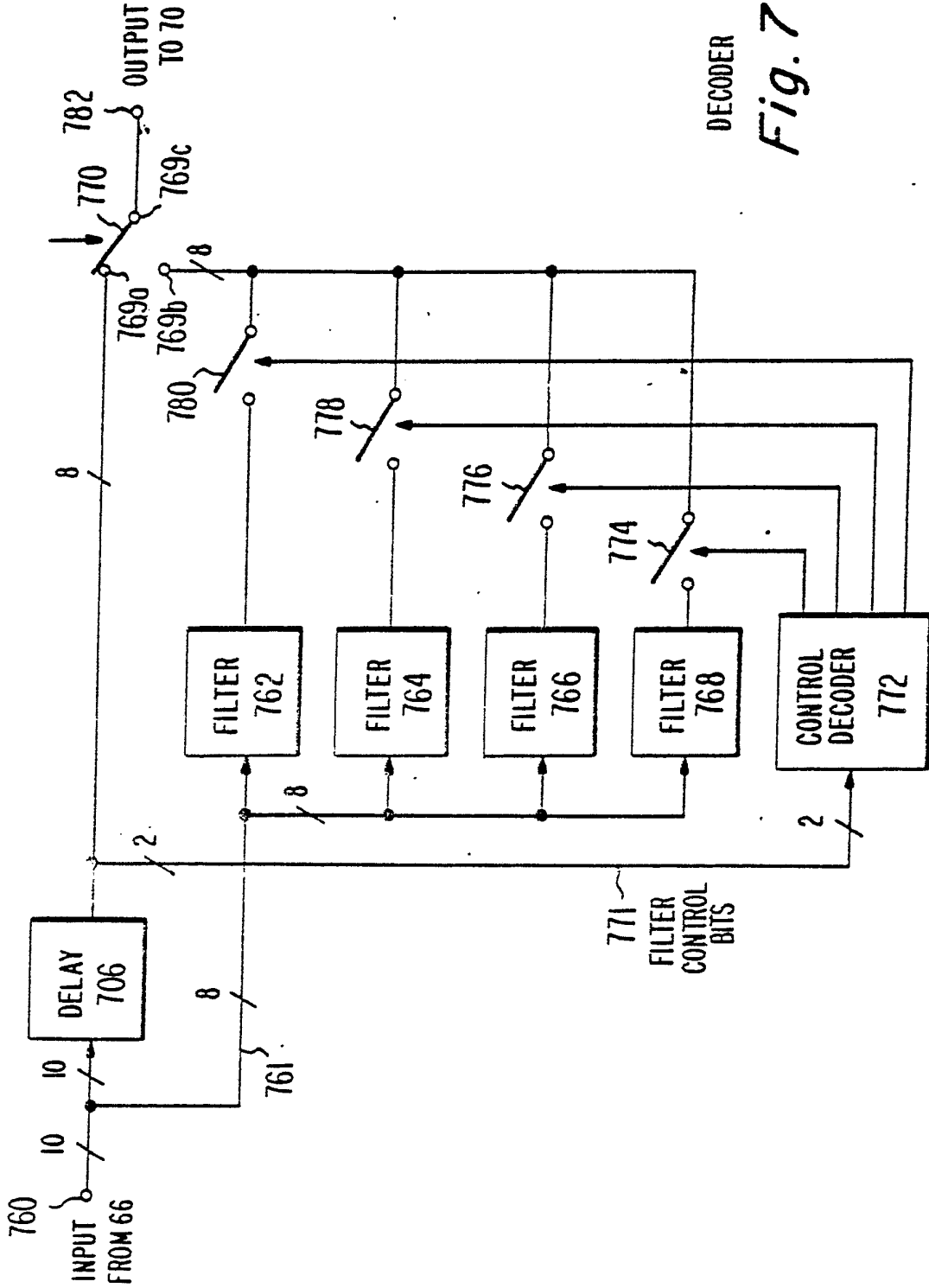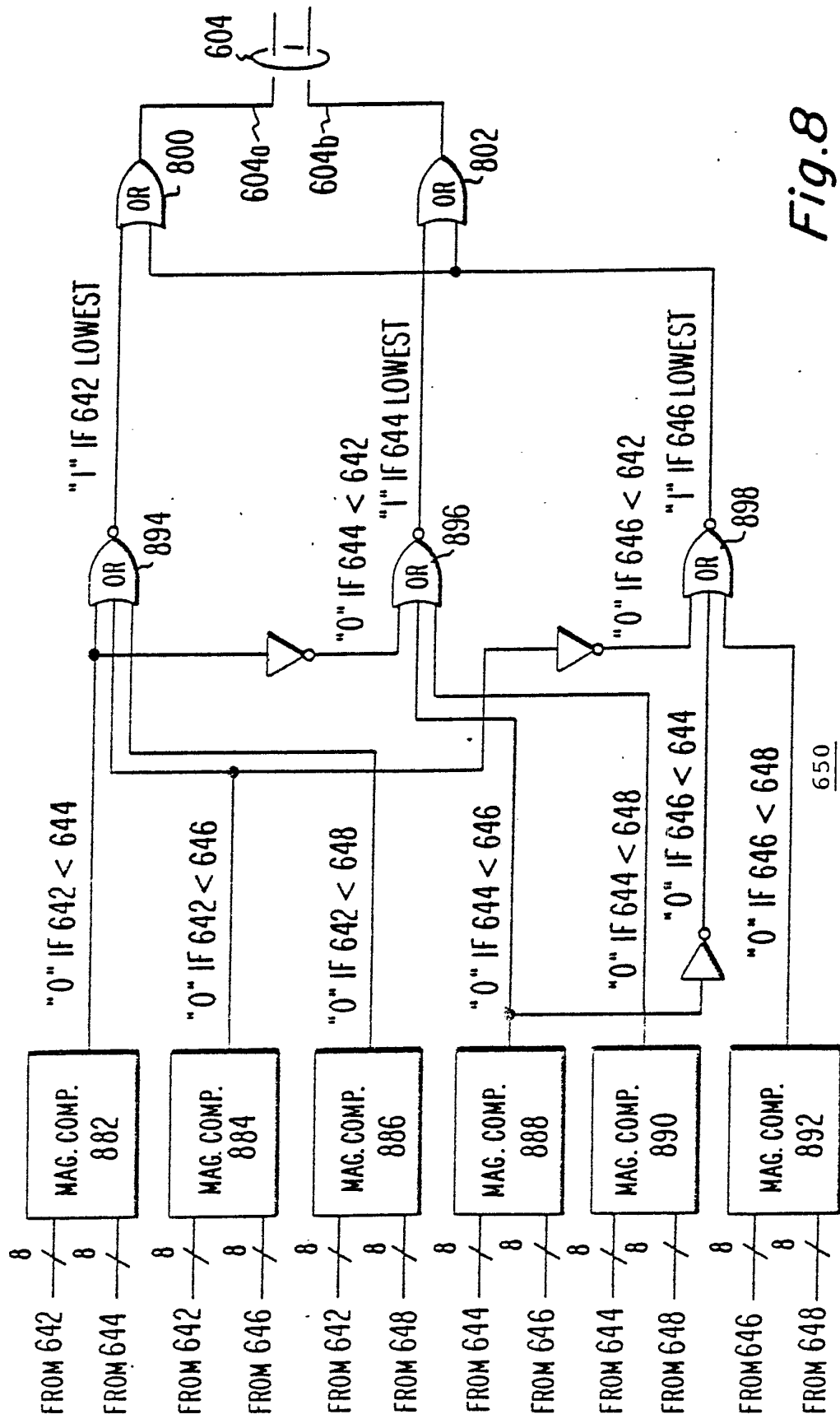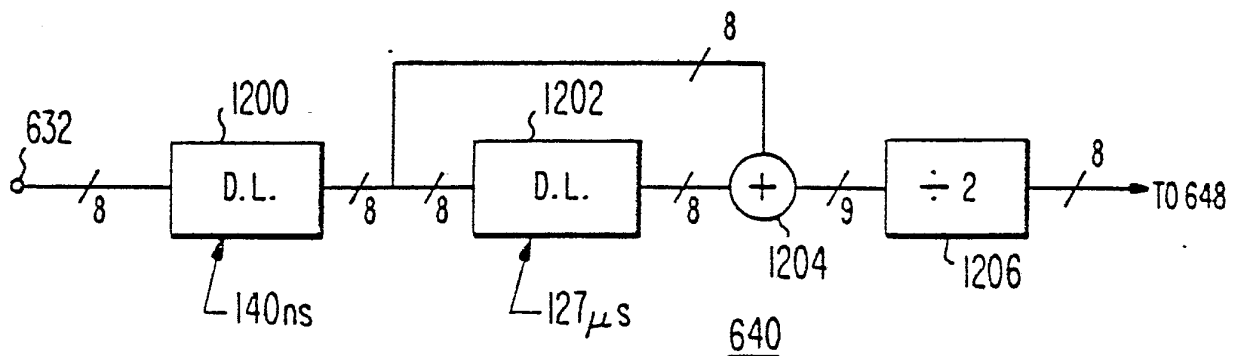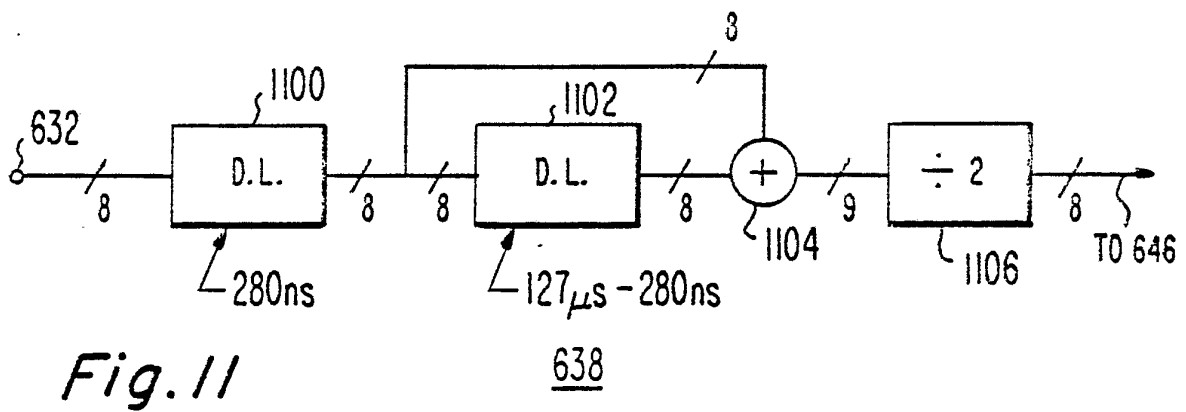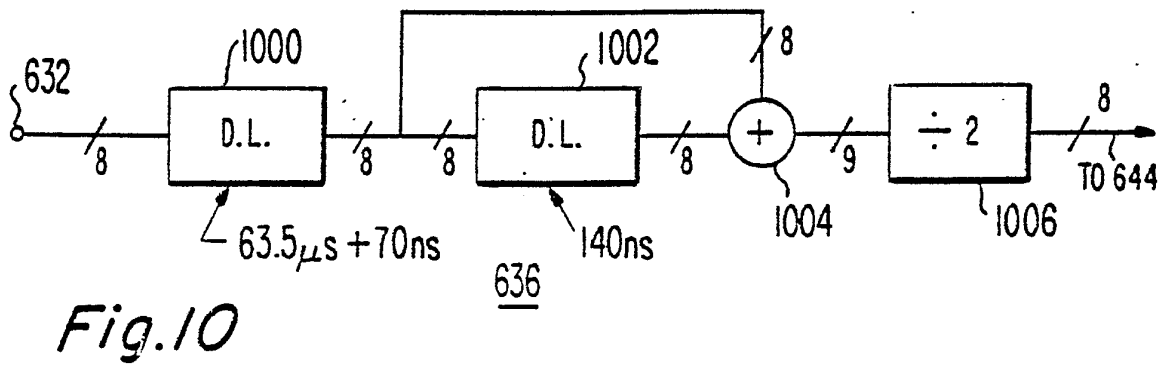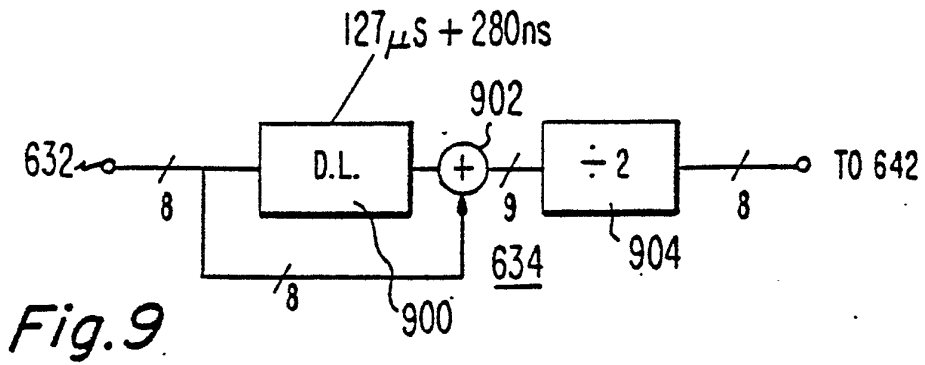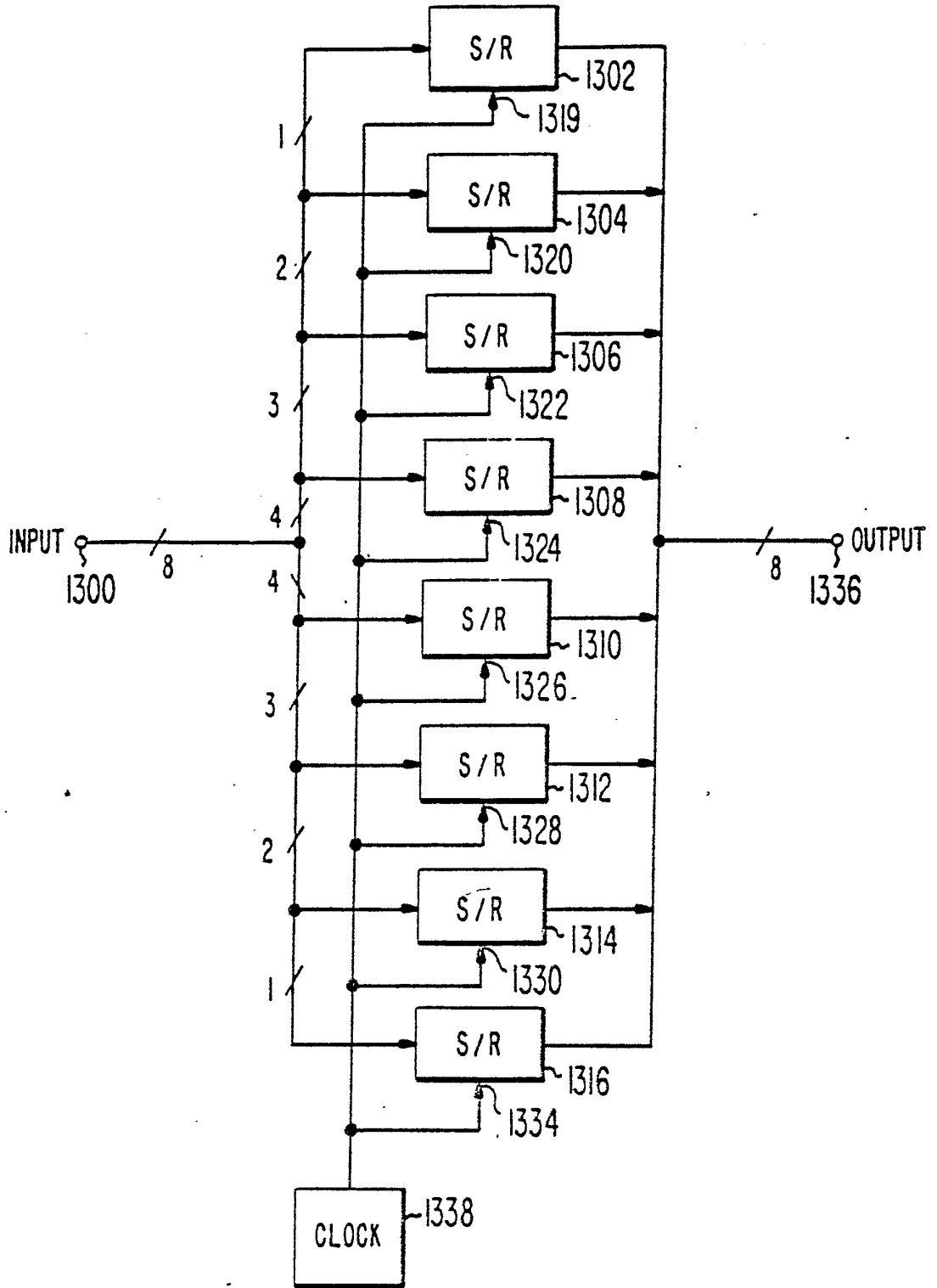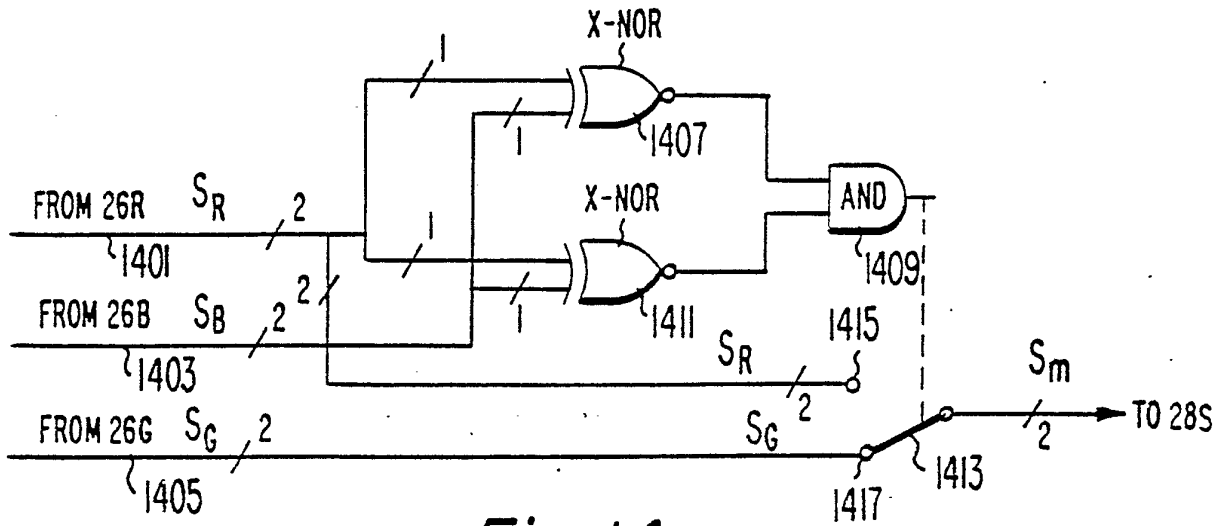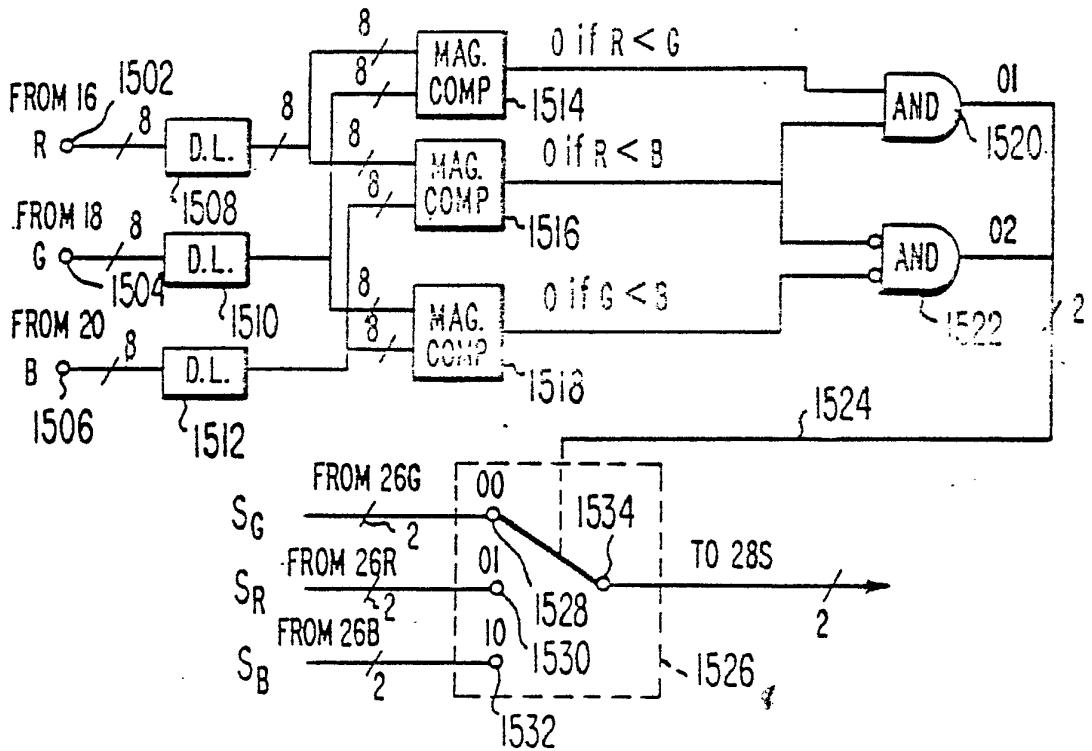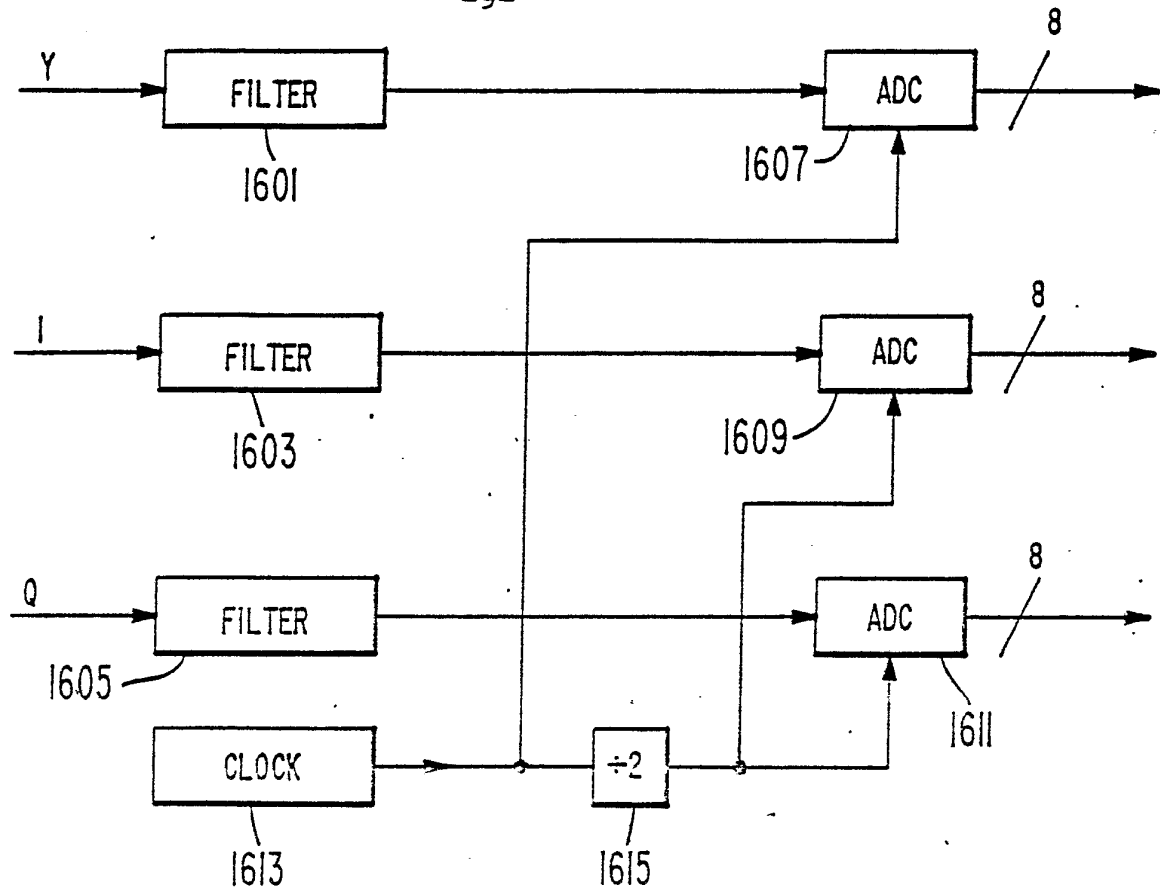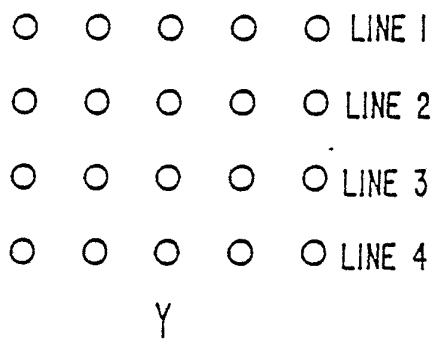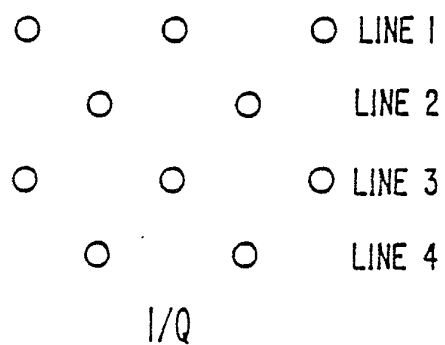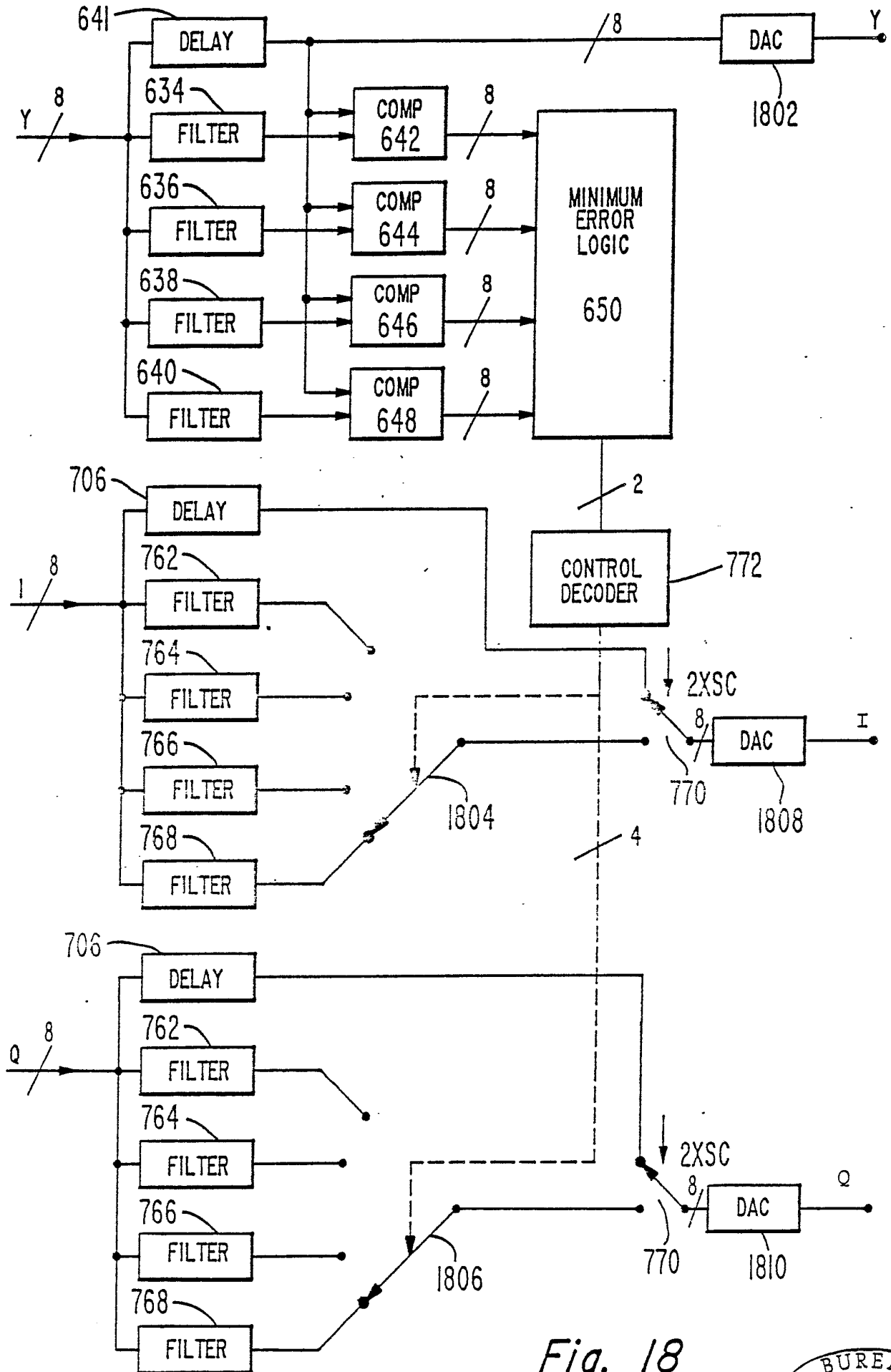
Fig. 18

INTERNATIONAL SEARCH REPORT

International Application No PCT/US81/00968

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.3 H04N 9/32
U.S. CL. 358/13

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	358/13, 133, 138 370/77, 109

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [*]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 3,462,547 Published 19 August 1969 Marcovski	1-29
A	US, A, 4,204,227 Published 20 May 1980 Gurley	2,6,8,12,18, 19,25,26
P	US, A, 4,217,609 Published 12 August 1980 Hatori et al	1-29
P	US, A, 4,227,204 Published 7 October 1980 Rossi	1-29

* Special categories of cited documents: [15]

"A" document defining the general state of the art

"E" earlier document but published on or after the international filing date

"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited-to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
16 November 1981	25 NOV 1981

International Searching Authority [1]	Signature of Authorized Officer [10]
ISA/US	Richard Murray