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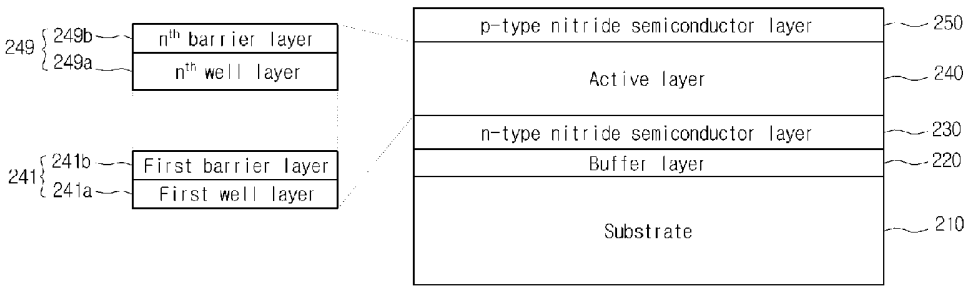
(54) **Title:** NITRIDE SEMICONDUCTOR LIGHT EMITTING DEVICE AND FABRICATING METHOD THEREOF



(57) **Abstract:** A nitride semiconductor light emitting device including: a first nitride semiconductor layer; an active layer formed on the first nitride semiconductor layer and including at least one barrier layer grown under hydrogen atmosphere of a high temperature; and a second nitride semi conductor layer formed on the active layer, and a method of fabricating the same are provided. According to the light emitting device and method of fabricating the same, the light power of the light emitting device is increased and the operation reliability is enhanced.

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Description

NITRIDE SEMICONDUCTOR LIGHT EMITTING DEVICE AND FABRICATING METHOD THEREOF

Technical Field

[1] The present invention relates to a nitride semiconductor light emitting device and fabrication method thereof, and more particularly, to a nitride semiconductor light emitting device and fabrication method thereof that can enhance the light power and reliability of the light emitting device.

Background Art

[2] In general, nitride semiconductors are in the limelight as a material for blue light emitting diodes, blue laser diodes or the like.

[3] Fig. 1 is a sectional view of a general nitride semiconductor light emitting device.

[4] Referring to Fig. 1, the general nitride semiconductor light emitting device includes a sapphire substrate 110, a buffer layer 120 formed on the sapphire substrate 110, an n-type nitride semiconductor layer 130 formed on the buffer layer 120, an active layer 140 formed on the n-type nitride semiconductor layer 130, and a p-type nitride semiconductor layer 150 formed on the active layer 140.

[5] The n- and p-type nitride semiconductor layers 130 and 150 are formed by doping a variety of dopants into a gallium nitride (GaN). Representative example of n-type dopants includes silicon (Si), and representative example of p-type dopants includes magnesium (Mg).

[6] The active layer is a layer through which light emits. As a representative growth method of the active layer, and is generally made in an InxGa1-xN($0 \leq x \leq 1$) single well structure or multi-well structure in which Indium (In) and gallium (Ga) are contained in predetermined ratios. The active layer of InxGa1-xN($0 \leq x \leq 1$) is generally grown under an environment of nitrogen atmosphere and at a temperature of less than 900 ℃.

[7] In detail, a general growth method below 900 ℃ is performed in a nitrogen(N2) atmosphere for a proper composition ratio of In and Ga. However, in the thin film growth of InxGa1-xN($0 \leq x \leq 1$), as the In introduction amount into GaN increases or the Ga introduction amount into InN increases, a serious phase dissociation phenomenon occurs, which is problematic. To solve such a phase dissociation phenomenon, if the growth temperature is increased, In phase dissociation phenomenon increases, which makes it difficult to obtain a good quality thin layer.

[8] Meanwhile, when the active layer is grown in a relatively low temperature, In segregation occurs from thin InGaN layer, which deteriorates the layer quality, and many crystal defects also occur at an interface between InxGa1-xN($0 \leq x \leq 1$) and GaN

due to a lattice difference therebetween. Also, the In phase dissociation phenomenon increases, which makes it difficult to obtain a good quality layer, and also the occurring crystal defects are combined with crystal defects of a lower structure to decrease the light emitting efficiency and the device reliability.

[9] Finally, in the related art growth method, in the case of the materials, such as InGaN/GaN, a strong piezo electric field is generated inside the active layer because of a stress due to a large lattice mismatch, and electron-hole wave functions are separated, resulting in a deterioration in the light emitting efficiency.

Disclosure of Invention

Technical Problem

[10] The present invention is to provide a nitride semiconductor light emitting device that can enhance the crystallinity of $In_xGa_{1-x}N(0\leq x\leq 1)$ constituting an active layer by decreasing crystal defects due to a large lattice mismatch between $In_xGa_{1-x}N(0\leq x\leq 1)$ and $In_yGa_{1-y}N(0\leq y\leq 1)$ of a nitride semiconductor.

[11] Also, the present invention is to provide a nitride semiconductor light emitting device having a low driving voltage and a high light emitting efficiency in which the light emitting efficiency is increased due toa thin active layer having $In_xGa_{1-x}N(0\leq x\leq 1)$ of In composition and a fabrication method thereof.

[12] Also, the present invention is to provide a nitride semiconductor light emitting device having an enhanced light power and reliability and a fabrication method thereof.

Technical Solution

[13] There is provided a nitride semiconductor light emitting device including: a first nitride semiconductor layer; an active layer formed on the first nitride semiconductor layer and including at least one barrier layer grown under hydrogen atmosphere of a high temperature; and a second nitride semiconductor layer formed on the active layer.

[14] Also, there is provided a nitride semiconductor light emitting device including: a buffer layer; a first nitride semiconductor layer formed on the buffer layer; an active layer formed on the first nitride semiconductor layer and including at least a pair of a well layer and a barrier layer having an IN(indium) composition ratio of less than 10 %; and a second nitride semiconductor layer formed on the active layer.

[15] Also, there is provided a method of fabricating a nitride semiconductor light emitting device, the method including: forming a first nitride semiconductor laeyr; forming an active layer on the first nitride semiconductor layer, the forming of the active layer including forming a well layer and a barrier layer grown under a hydrogen atmosphere at a high temperature; and forming a second nitride semiconductor layer on the active layer.

Advantageous Effects

[16] According to the nitride semiconductor light emitting device of the present invention, a barrier layer grown in a hydrogen atmosphere at a high temperature decreases crystal defects due to a large lattice mismatch between a well layer and the barrier layer constituting the active layer and enhances the crystallinity of the active layer.

[17] Also, the light emitting device with a high light power and an increased reliability can be obtained.

Brief Description of the Drawings

[18] The spirit of the present invention will be understood from the accompanying drawings. In the drawings:

[19] Fig. 1 is a sectional view of a general nitride semiconductor light emitting device;

[20] Fig. 2 a sectional view of a nitride semiconductor light emitting device according to a first embodiment of the present invention;

[21] Fig. 3 a sectional view of a nitride semiconductor light emitting device according to a second embodiment of the present invention; and

[22] Fig. 4 a sectional view of a nitride semiconductor light emitting device according to a third embodiment of the present invention.

Best Mode for Carrying Out the Invention

[23] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to accompanying drawings.

[24] <First embodiment>

[25] Fig. 2 a sectional view of a nitride semiconductor light emitting device according to a first embodiment of the present invention.

[26] Referring to Fig. 2, the nitride semiconductor light emitting device according to the present invention includes a buffer layer 220 formed on a substrate 210, an n-type nitride semiconductor layer 230 formed on the buffer layer 220, an active layer 240 formed on the n-type nitride semiconductor layer 230, the active layer 240 including well layers 241a, 249a and barrier layers 241b, 249b, and a p-type nitride semiconductor layer 250 formed on the active layer 240.

[27] In detail, the active layer 240 is formed between the n-type nitride semiconductor layer 230 and the p-type nitride semiconductor layer 250. In particular, the active layer 240 is characterized by including the barrier layers 241b, 249b grown in a high temperature hydrogen atmosphere so as to reduce crystal defects.

[28] Also, the active layer 240 may have a single quantum well structure consisting of a first well layer 241a and a first barrier layer 241b, or a multi-quantum well structure consisting of a plurality of well layers 241a, 249a and a plurality of barrier layers 241b,

249b alternatively formed. Preferably, the plurality of well layers 241a, 249a and the plurality of barrier layers 241b, 249b are arranged to include 4 to 10 pairs of periodically repeated well layers and barrier layer, each pair consisting of one well layer and one barrier layer.

[29] Also, it is preferable that each of the well layers 241a, 249a should have a composition of $In_xGa_{1-x}N(0\leq x\leq 1)$ of which In composition ratio is 10 - 20 % and each of the barrier layers 241b, 249b should have a composition of $In_YGa_{1-Y}N(0\leq y\leq 1)$ of which In composition ratio is below 10 %.

[30] Hereinafter, a method of fabricating a nitride semiconductor light emitting device according to an embodiment of the present invention will be described.

[31] First, a buffer layer 220 is formed on a substrate 210. The substrate 210 may be a sapphire substrate, a silicon substrate or a silicon carbide (SiC) substrate, which are widely used in the nitride semiconductor light emitting devices.

[32] Next, an n-type nitride semiconductor layer 230 serving as a first nitride semiconductor layer is formed on the buffer layer 220. After the n-type nitride semiconductor layer 230 is formed, a process step of forming an active layer 240 is performed.

[33] Describing the process step of forming the active layer 240 in more detail, a well layer 241a having a composition of $In_xGa_{1-x}N(0\leq x\leq 1)$ is formed on the n-type nitride semiconductor layer 230. Preferably, the well layer 241a is formed with a composition of $In_xGa_{1-x}N(0\leq x\leq 1)$ of which In composition ratio is 10 % to 20 %. After the well layer 241a is formed, a barrier layer 241b having a composition of $In_YGa_{1-Y}N(0\leq y\leq 1)$ is formed on the well layer 241a. Preferably, the barrier layer 241b is formed with a composition of $In_YGa_{1-Y}N(0\leq y\leq 1)$ of which In composition ratio is below 10 %.

[34] Herein, the barrier layer 241b is formed at a thickness range of 30 - 200Åin a high temperature hydrogen atmosphere. If the barrier layer 241b is formed so thin, the crystal defects-removing effects, such as defects, inclusion or the like generated in a boundary between $In_xGa_{1-x}N(0\leq x\leq 1)$ and $In_YGa_{1-Y}N(0\leq y\leq 1)$ constituting the well layers and the barrier layers, are decreased, so that the device performance enhancement effect is reduced. Accordingly, it is preferable that the barrier layer 241b be 30 Å or more thick. Further, if the barrier layer 241b is formed so thick, the resistance, which is happening during fabrication of device, is increased, so that the electrical characteristics and the light emitting efficiency of the device are lowered. Accordingly, it is preferable that the barrier layer 241b be 200 Å or less thick. Resultantly, it is preferable that the barrier layer 241b be formed at a thickness range of 30 - 200 Å.

[35] In addition, when the barrier layer 241b is formed in the hydrogen atmosphere above 900 ℃ according to the present invention, it shows remarkably decreased crystal defects, compared with the related art barrier layer of $In_YGa_{1-Y}N(0\leq y\leq 1)$ having a

multi-well structure formed in a temperature below 900℃. However, if the growth temperature of the barrier layer 241b exceeds 1,040 ℃, the crystal defects increase. To this end, it is preferable that the the temperature range for the formation of the barrier layer 241b be in a range of 900 - 1,040 ℃.

[36] By the above process steps, the active layer 240 is formed with a single quantum well structure consisting of a single well layer 241a and a single barrier layer 241b or a multi-quantum well structure consisting of a plurality of well layers and barrier layers alternatively arranged.

[37] After the active layer 240 is formed, a p-type nitride semiconductor layer 250 serving as a second nitride semiconductor layer is formed on the active layer 240.

[38] The barrier layer suppresses crystal defects existing in the lower structure of the substrate 210, the buffer layer 220 and the n-type nitride semiconductor layer 230 and dislocations such as defects or inclusions occurring in a boundary between InxGa1-x N($0 \leq x \leq 1$) and InYGa1-YN($0 \leq y \leq 1$) from being propagated, thereby enhancing the device reliability. Hence, the light power of the light emitting device is improved and the device reliability is increased.

[39] <Second embodiment>

[40] Hereinafter, a nitride semiconductor light emitting device and fabrication method thereof according to a second embodiment of the present invention will be described.

[41] Fig. 3 a sectional view of a nitride semiconductor light emitting device according to a second embodiment of the present invention.

[42] Referring to Fig. 3, the nitride semiconductor light emitting device according to the present invention includes a buffer layer 320 formed on a substrate 310, an n-type nitride semiconductor layer 330 formed on the buffer layer 320, an active layer 340 formed on the n-type nitride semiconductor layer 330, the active layer 340 including at least barrier layers 341b, 349b, and a p-type nitride semiconductor layer 350 formed on the active layer 340.

[43] The active layer 340 is formed between the n-type nitride semiconductor layer 330 and the p-type nitride semiconductor layer 350. The active layer 340 includes the barrier layers 341b, 349b grown in a high temperature nitrogen atmosphere so as to decrease crystal defects. One period of the active layer 340 includes a first well layer 341a formed on the n-type nitride semiconductor layer 330, a first barrier layer 341b grown on the first well layer 341a in a high temperature hydrogen atmosphere, and a seed layer 341c formed on the first barrier layer 341b.

[44] In detail, the active layer 340 includes a plurality of well layers 341a, 349a, a plurality of barrier layers 341b, 349b and a plurality of seed layers 341c, 349c alternatively arranged. Preferably, the plurality of well layers 341a, 349a, the plurality of barrier layers 341b, 349b and the plurality of seed layers 341c, 349c, one period

consisting of one well layer, one barrier layer and one seed layer, are formed in four or ten periods.

[45] The seed layers 341c, 348c are grown with a composition of InzGa1-zN(0 〈 z 〈 1) or a single layer of InN. The seed layers serve as a seed while the well layers are formed directly on the seed layers such that In is sufficiently introduced into the well layers.

[46] The nitride semiconductor light emitting device thus formed according to the second embodiment of the present invention is characterized by including forming the seed layers prior to forming the well layers such that the characteristics of the well layers are improved and In is sufficiently supplied into the well layers.

[47] Hereinafter, a method of fabricating the nitride semiconductor light emitting device according to the second embodiment of the present invention will be described in detail.

[48] First, a buffer layer 320 is formed on a substrate 310. Next, an n-type nitride semiconductor layer 330 serving as a first nitride semiconductor layer is formed on the buffer layer 320. After the n-type nitride semiconductor layer 330 is formed, a process step of forming an active layer 340 is performed.

[49] To form the active layer 340, a well layer 341a having a composition of InxGa1-x N(0≤x≤1) is formed on the n-type nitride semiconductor layer 330. After the well layer 341a is formed, a barrier layer 341b is formed on the well layer 341a. Since the process steps from the forming of the n-type nitride semiconductor layer 330 to the forming of the barrier layer 341b are the same as those in the first embodiment, their detailed description will be omitted.

[50] After the barrier layer 341b is formed, a seed layer 341c is formed with a composition of InzGa1-zN(0 〈 z 〈 1) or in a single layer of InN. The seed layer 341c serves as a seed while a well layer 342a is formed with a composition of InxGa1-x N(0≤x≤1) such that In is sufficiently supplied into the well layer 342a with a composition of InxGa1-xN(0≤x≤1). Accordingly, a carrier localization caused by a phase dissociation of the inside of the well layer or a non-uniform In composition becomes adjustable. Meanwhile, a composition ratio of In in the seed layer 341c with a composition of InzGa1-zN is preferably above 10 % to an overall composition.

[51] In a general case, the well layer with a composition of InxGa1-xN(0≤x≤1) has a composition ratio containing 15% In. In order to increase the In composition ratio of the well layer 342a in the nitride semiconductor light emitting device according to the present invention, the In composition ratio in InzGa1-zN(0 〈 z 〈 1) constituting the seed layer 341c is made above 10 %. By doing so, In introduction effect into the well layer increases, so that the well layer 342a can be formed with a composition ratio containing 15 % or more In.

[52] The seed layer 341c of a single layer of InzGa1-zN(0 〈 z 〈 1) or InN is preferably grown at a thickness below 20 Å. This is because if the seed layer 341c is thicker than the well layer 342a, In isolation phenomenon may occurs at a boundary between the seed layer 341c and the well layer 342a, which results in the deterioration in the layer quality or in the light emitting characteristic.

[53] After the seed layer 341c is grown, a heat treatment of the seed layer 341c may be added. Example of the heat treatment includes a process step of thermally annealing the seed layer 341c at the same temperature as the growth temperature of the seed layer 341c or a process step of elevating the growth temperature while the well layer 342b is grown. The above heat treatment promotes In introduced into the seed layer 341c to form a lattice bond with Nitrogen(N) and also helps Ga and In to bond with each other while the well layer 342a is formed.

[54] After the seed layer 341c is formed, well layer 342a is formed with a composition of InxGa1-xN(0≤x≤1). While the well layer 342a is formed with the composition of In xGa1-xN(0≤x≤1), a sufficient amount of In is introduced into the well layer 342a from the seed layer 341c formed in the previous process step. Accordingly, a high temperature growth of active layer can be induced to obtain thin active layer having the high quality composition of InxGa1-xN(0≤x≤1).

[55] Resultantly, a nitride semiconductor light emitting device having a high light emitting efficiency can be obtained due to the carrier localization effect of the high quality thin InGaN layer having the high In composition ratio.

[56] Through the above process steps, a single quantum well structure consisting of the well layer 341a/barrier layer 341b/seed layer 341c can be obtained or a multi-quantum well structure further including a plurality of well layers/barrier layers/seed layers additively grown on the seed layer 341c of the single quantum well structure can be obtained.

[57] In forming the final quantum well structure of the active layer 349, the well layer 349a and the barrier layer 349b are formed, but the seed layer is omitted, which is because an additional well layer does not exist on the seed layer if formed, and the barrier layer 349b directly contacts the p-type nitride semiconductor layer 350 to obtain a normal operation environment of light emitting device due to the formation of a contact layer.

[58] Subsequently, a p-type nitride semiconductor layer serving as a second nitride semiconductor layer 350 is formed on the active layer 340.

[59] Elements, which are not particularly described in the above description for the second embodiment, can be referred from the description of the first embodiment.

[60] The characteristics of the nitride semiconductor light emitting device according to the second embodiment will now be described.

[61] The barrier layers 341b, 349b in the active layer 340 are grown in the high temperature hydrogen atmosphere to reduce the crystal defects. Accordingly, the crystal defects of the lower structure including the substrate 310, the buffer layer 320 and the n-type nitride semiconductor layer 330, and the dislocations, such as the defects or inclusions, occurring at the boundary between InxGa1-xN($0 \leq x \leq 1$) and InY Ga1-YN($0 \leq y \leq 1$), can be prevented from being propagated, thereby enhancing the device reliability.

[62] Also, while the nitride semiconductor light emitting device according to the present invention is fabricated, the seed layers 341c, 348c help In to be sufficiently introduced into the well layers 342a, 349a having the composition of InxGa1-xN($0 \leq x \leq 1$) during the growth of the well layers342a, 349a. The above behavior of the seed layers 341c, 348c induces a natural rise of the growth temperature being caused by the high In composition ratio such that a thin InGaN layer grown at a high temperature can be obtained, thereby enhancing the light emitting efficiency due to the carrier localization effect.

[63] Recent research results show that an energy band gap of InN is a very small value of 0.7 eV (corresponds to a wavelength of 1,771 nanometers), which means that the energy gap of InxGa1-xN($0 \leq x \leq 1$) includes infrared ray region to ultra violet ray region. Accordingly, it is possible to fabricate an LCD emitting lights at all wavelengths.

[64] However, according to the nitride semiconductor light emitting device and fabrication method thereof provided in the first and second embodiments, since the first well layers 241a, 341a are grown directly on the n-type nitride semiconductor layers 230, 330, respectively, the lattice structure defects of the first well layers 241a, 341a may not be sufficiently reduced.

[65] <Third embodiment>

[66] The third embodiment of the present invention is provided to solve the above drawback, and provides a fabrication method with a structure that can cope with the lattice structure defects of the first well layers 241a, 341a first grown.

[67] Fig. 4 a sectional view of a nitride semiconductor light emitting device according to a third embodiment of the present invention.

[68] Referring to Fig. 4, to solve lattice structure defects of a first well layer 441a, an additional barrier layer 439 is further formed between the first well layer 441a and an n-type nitride semiconductor layer 430, which is to remove the crystal defects of the first well layer 441a and at the same time to stably operate the light emitting device. The additional barrier layer 439 is grown in a high temperature hydrogen atmospher.

[69] The process step of forming the additional barrier layer 439 is performed between the process step of forming the aforementioned n-type nitride semiconductor layer 430

and the process step of forming the first well layer 441a.

[70] Through the method of fabricating the nitride semiconductor light emitting device according to the third embodiment of the present invention, the crystal defects existing of the lower structure including a substrate 410, a buffer layer 420 and the n-type nitride semiconductor layer 430 can be prevented from being propagated to the first well layer 441a. Also, dislocations such as defects or inclusions occurring at a boundary between the well layer having the composition of $In_xGa_{1-x}N(0\leq x\leq 1)$ and the barrier layer having the composition of $In_yGa_{1-y}N(0\leq y\leq 1)$ can be efficiently prevented from being propagated, thereby minimizing the crystal defects of the active layer.

Industrial Applicability

[71] According to the nitride semiconductor light emitting device of the present invention, the barrier layer grown in a high temperature hydrogen atmosphere decreases crystal defects due to a large lattice mismatch between the well layer having the composition of $In_xGa_{1-x}N(0\leq x\leq 1)$ and the barrier layer having the composition of $In_yGa_{1-y}N(0\leq y\leq 1)$ and enhances the crystallinity of the active layer having the composition of $In_xGa_{1-x}N(0\leq x\leq 1)$.

[72] Also, the seed layer having the composition of $In_zGa_{1-z}N(0\leq z\leq 1)$ of which In content is high can increase the light emitting efficiency and allow light having a wide wavelength band to be obtained.

[73] In addition, a nitride semiconductor light emitting device with an improved light power and reliability can be obtained.

Claims

[1] A nitride semiconductor light emitting device comprising:
a first nitride semiconductor layer;
an active layer formed on the first nitride semiconductor layer and including at least one barrier layer grown under hydrogen atmosphere of a high temperature; and
a second nitride semiconductor layer formed on the active layer.

[2] The nitride semiconductor light emitting device of claim 1, wherein the active layer is a single quantum well structure including a well layer and the barrier layer, or a multi-quantum well structure in which the well layer and the barrier layer are in plurality and the plurality of well layers and the plurality of barrier layers are alternatively stacked.

[3] The nitride semiconductor light emitting device of claim 2, wherein a barrier layer formed under a hydrogen atmosphere of a high temperature is interposed between the first nitride semiconductor layer and the active layer.

[4] The nitride semiconductor light emitting device of claim 1, wherein the active layer comprises a well layer formed beneath the barrier layer and a plurality of seed layers for In supply on the barrier layer.

[5] A nitride semiconductor light emitting device comprising:
a buffer layer;
a first nitride semiconductor layer formed on the buffer layer;
an active layer formed on the first nitride semiconductor layer and including at least a pair of a well layer and a barrier layer having an IN(indium) composition ratio of less than 10 %; and
a second nitride semiconductor layer formed on the active layer.

[6] The nitride semiconductor light emitting device of claim 5, wherein the active layer comprises 4 to 10 pairs of periodically repeated well layers and barrier layer, each pair consisting of one well layer and one barrier layer.

[7] The nitride semiconductor light emitting device of claim 5, wherein the well layers and the barrier layers are formed in a plurality of pairs, and a seed layer containing In is interposed between the respective pairs of well layers and barrier layers.

[8] The nitride semiconductor light emitting device of claim 7, wherein the seed layer is a single layer of InzGa1-zN(0 〈 z 〈 1) or InN.

[9] The nitride semiconductor light emitting device of claim 7, wherein the seed layer has an In composition ratio of more than 10 %.

[10] The nitride semiconductor light emitting device of claim 7, wherein the seed

layer is 20 Å or less thick.

[11] The nitride semiconductor light emitting device of claim 5, wherein the well layer has a composition of $In_xGa_{1-x}N(0\leq x\leq 1)$ of which In composition ratio is 10 - 20 %.

[12] The nitride semiconductor light emitting device of claim 5, wherein the barrier layer has a composition of $In_yGa_{1-y}N(0\leq y\leq 1)$ and is grown under a hydrogen atmosphere at a temperature of more than 900℃.

[13] The nitride semiconductor light emitting device of claim 5, wherein the barrier layer is 30 - 200 Å thick.

[14] The nitride semiconductor light emitting device of claim 5, wherein the barrier layer has a growth temperature of 900 - 1040 ℃.

[15] The nitride semiconductor light emitting device of claim 5, wherein a barrier layer having a composition of $In_yGa_{1-y}N(0\leq y\leq 1)$ is grown ahead of the well layer on the first nitride semiconductor layer.

[16] A method of fabricating a nitride semiconductor light emitting device, the method comprising:
forming a first nitride semiconductor layer;
forming an active layer on the first nitride semiconductor layer, the forming of the active layer including forming a well layer and a barrier layer grown under a hydrogen atmosphere at a high temperature; and
forming a second nitride semiconductor layer on the active layer.

[17] The method of claim 16, wherein the barrier layer has a growth temperature of 900 - 1040 ℃.

[18] The method of claim 16, wherein the barrier layer is 30 - 200 Å thick.

[19] The method of claim 16, directly after the barrier layer is grown, forming a seed layer.

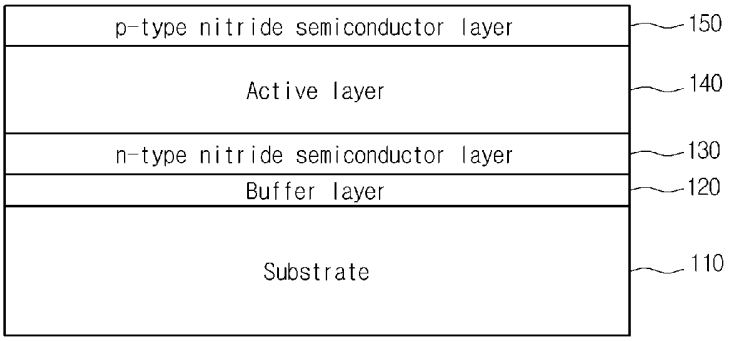
[20] The method of claim 19, wherein the seed layer is formed at a thickness of less than 20 Å with an In content of more than 10 %.

[21] The method of claim 19, after forming the seed layer, thermally annealing the seed layer.

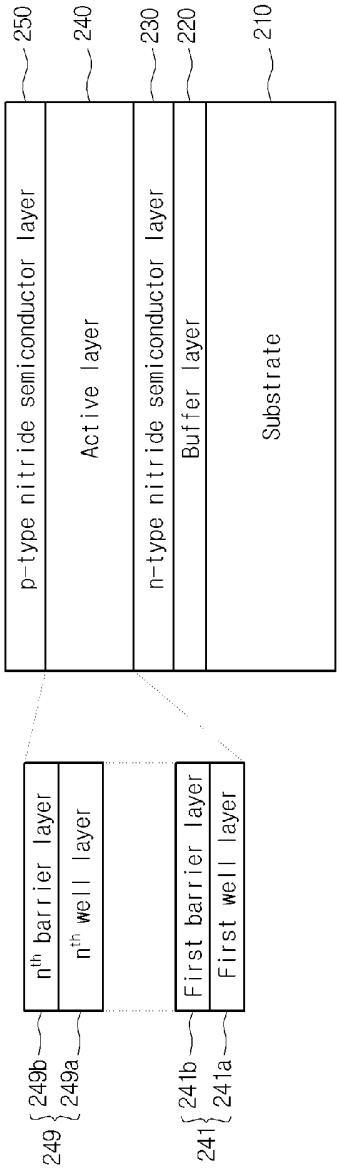
[22] The method of claim 16, directly after forming the first nitride semiconductor layer, forming the barrier layer under a hydrogen atmosphere at a high temperature.

[23] The method of claim 16, wherein a buffer layer is grown below the first nitride semiconductor layer and a substrate is grown below the buffer layer.

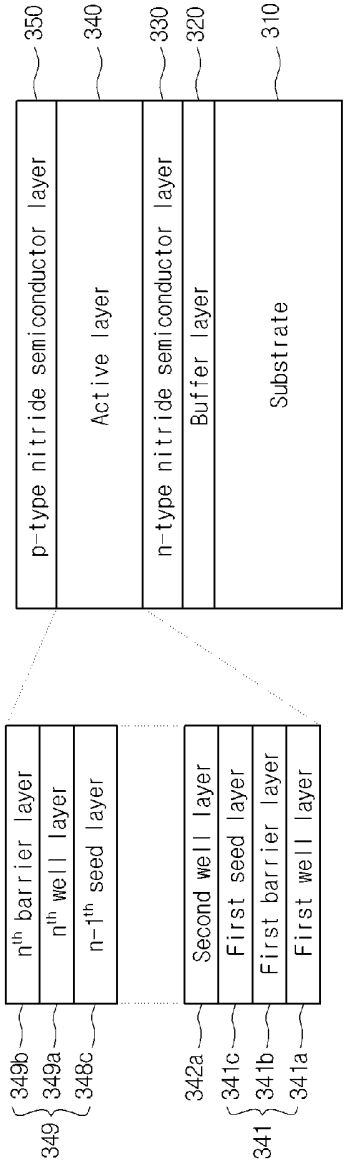
[Fig. 1]


p-type nitride semiconductor layer
150
Active layer
140
n-type nitride semiconductor layer
130
Buffer layer
120
Substrate
110

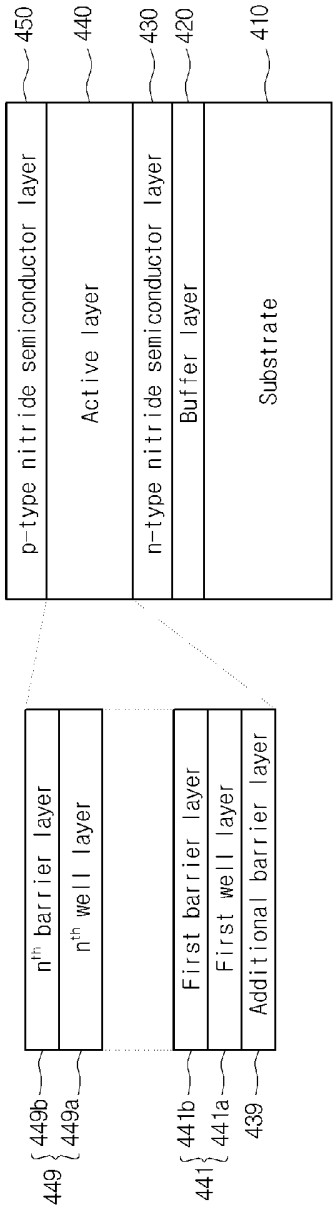
[Fig. 2]


250
240
230
220
210
p-type nitride semiconductor layer
Active layer
n-type nitride semiconductor layer
Buffer layer
Substrate
nth barrier layer
nth well layer
First barrier layer
First well layer
249b
249a
249
241b
241a
241

[Fig. 3]


350
340
330
320
310
p-type nitride semiconductor layer
Active layer
n-type nitride semiconductor layer
Buffer layer
Substrate
nth barrier layer
nth well layer
n-1th seed layer
Second well layer
First seed layer
First barrier layer
First well layer
349b
349a
348c
342a
341c
341b
341a
349
341

[Fig. 4]


450
440
430
420
410
p-type nitride semiconductor layer
Active layer
n-type nitride semiconductor layer
Buffer layer
Substrate
nth barrier layer
nth well layer
First barrier layer
First well layer
Additional barrier layer
449b
449a
449
441b
441a
441
439

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/003702

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/00(2006.01)i, H01S 5/30(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 H01L H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Patents and applications for inventions since 1975
Korean Utility models and applictions for Utility models since 1975
Japanese Utility models and application for Utility models since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)

e-KIPASS : "quantum", "well", "barrier", "hydrogen"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP 11-74622 A (TOSHIBA CORP.) 16 MARCH 1999 see the abstract, [0022]~[0052], figures 1~4	5-6, 11, 13, 15 1-4, 16-23, 7-10, 12,14
X A	JP 2000-174366 A (MITSUBISHI CABLE IND. LTD.) 23 JUNE 2000 see the abstract, [0039], figure 1	5-6, 11, 13, 15 1-4, 16-23, 7-10, 12,14
X A	JP 2002-158374 A (TOYODA GOSEI CO., LTD.) 31 MAY 2002 see the abstract, claims 1-9, [0019]~[0058]	5-6, 11, 13-15 1-4, 16-23, 7-10, 12
A	KR 2004-0041732 A (OPTRONIX INCORPERATION) 5 JUNE 2004 see the abstract, figure 3	1-23

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 FEBRUARY 2006 (09.02.2006)	**10 FEBRUARY 2006 (10.02.2006)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer KIM, Dong Yup Telephone No. 82-42-481-5749

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/003702

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 2003-0083820 A (LG ELECTRONICS INC.) 1 NOVEMBER 2003 see the whole text, figure 3e	1-23
A	JP 11-26812 A (TOYODA GOSEI CO., LTD.) 29 JANUARY 1999 see the abstract, figures 1-2	1-23
A	JP 2000-286202 A (TOYODA GOSEI CO., LTD.) 13 OCTOBER 2000 see the abstract, claims 1-14, whole text	1-23
A	JP 2001-0048266 A (KWANGJU INSTITUTE OF SCIENCE AND TECHNOLOGY) 15 JUNE 2001 see the abstract, embodiments 1~6	1-23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/003702

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Claimed invention (i) : Clims 1-4, 16-23 are directed to a nitride semiconductor LED containing the barrier layers formed in hydrogen atmosphere at high temperature

Claimed invention (ii) : Claims 5-15 are directed to a nitride semiconductor LED including the InGaN barrier layer in which the Indium content is less than 10%.

Hence, the application contains separate groups of inventions.

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2005/003702

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 11-74622 A	16.03.1999	JP 3311275 B	05.08.2002
JP 2000-174366 A	23.06.2000	NONE	
JP 2002-158374 A	31.05.2002	JP 10135514 A	22.05.1998
		JP 3304787 B	22.07.2002
		KR 19980024551 A	06.07.1998
		KR 10050458145 B	23.02.2005
		TW 575971 B	11.02.2004
		US 06040588 A	21.03.2000
		US 06326236 BA	04.12.2001
		US 06420733 BB	16.07.2002
		US 06541293 BB	01.04.2003
		US 06821800 BB	23.11.2004
		US 20010048112 A1	06.12.2001
		US 20020146854 A1	10.10.2002
		US 20030124789 A1	03.07.2003
KR 2004-0041732 A	05.06.2004	NONE	
KR 2003-0083820 A	01.11.2003	NONE	
JP 11-26812 A	29.01.1999	NONE	
JP 2000-286202 A	13.10.2000	CN 1225032 C	26.10.2005
		CN 1270420 A	18.10.2000
		EP 1041609 A1	04.10.2000
		JP 3440873 B	25.08.2003
		KR 20020038073 Y	23.12.2002
		TW 447149 B	21.07.2001
		US 20040115917A1	17.06.2004
		US 6713789 BA	30.03.2004
		US 6939733 BB	06.09.2005
JP 2001-0048266 A	15.06.2001	KR 100342013 B	27.06.2002