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(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

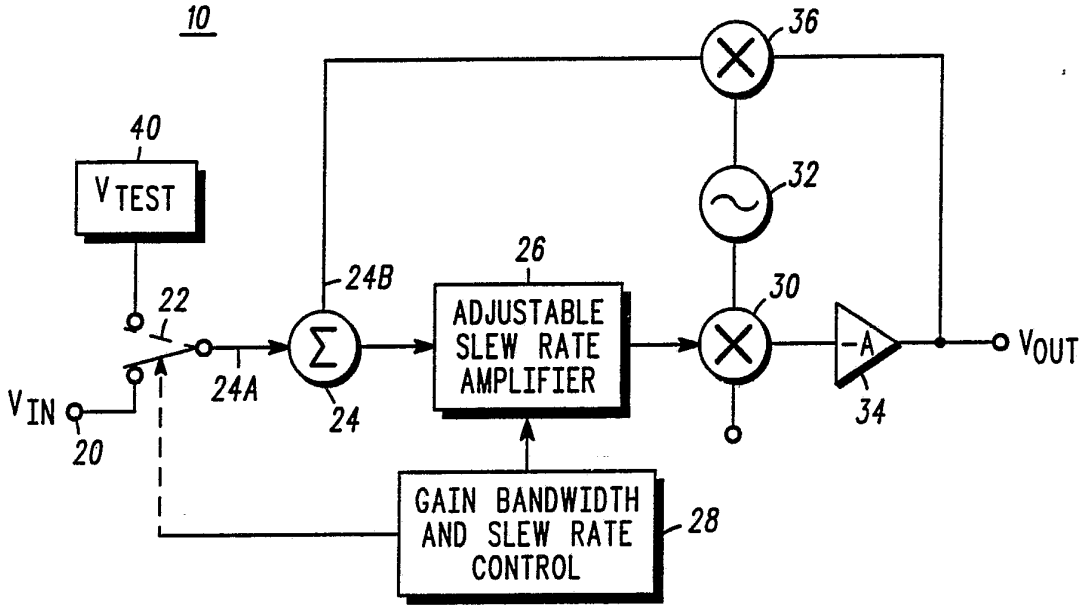
(72) Inventor: GAILUS, Paul, H. ; 550 Grego Court, Prospect Heights, IL 60070 (US).

(74) Agents: PARMELEE, Steven, G. et al.; Motorola, Inc., Intellectual Property Department, 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

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(54) Title: CONTROLLED SLEW RATE AMPLIFIER



(57) Abstract

An adjustable slew rate amplifier (26) in the input stage of an amplifier circuit (10) helps reduce off-channel frequency splatter. In instances where test sequences are input to an amplifier circuit that are used to measure maximum permissible input levels to the amplifier (34), inclusion of a low slew rate amplifier in the input loop further prevents the production of off-channel frequency splatter caused even by the input test sequence. The adjustable slew rate amplifier (26) is run at full slew rate, providing full-bandwidth amplification, during periods of normal circuit operation.

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CONTROLLED SLEW RATE AMPLIFIER

Technical Field

This invention relates generally to linear amplifier circuits. In particular, this invention relates to negative feedback linear amplifier circuits that adjust input signal levels to maximize output power and efficiency while preventing output signal distortion caused by over driving the amplifier stage.

Background of the Invention

Electronic amplifier circuits are well known in the art. These devices employ various techniques to improve their linearity. There is often a need to maximize output power and efficiency of a linear amplifier circuit by providing sufficient input drive signal levels. However, with any given amplifier there is a drive level beyond which linearity is severely degraded. When overdriven by an input signal most amplifier circuits will inherently generate undesired signals as either adjacent channel frequency splatter or other unwanted signals.

Electronic amplifier circuits that run in Class B or AB are desirable because of their relatively high efficiency and are somewhat linear but require negative

feedback to obtain the improved linearity demanded by many applications. Reducing output signal distortion or frequency splatter in a class B or class AB amplifier might permit use of these amplifiers in communications applications requiring relatively distortion-free amplification. Negative feedback reduces distortion as long as the amplifier is not overdriven. Since negative feedback actually increases distortion and unwanted signals when the amplifier is overdriven, it is important to prevent an amplifier from being overdriven.

In many communications applications, adjacent channel frequency splatter caused by an overdriven final amplifier stage in a radio transmitter causes undesirable interference with adjacent channel users. In such applications, which may be typically employed in digital or analog communications systems using signals with a time-varying amplitude, a test signal might be used to determine the maximum allowable input level to the final amplifier stage in order to prevent the final amplifier from being overdriven. In instances where an input test sequence is used to determine the maximum input level to an amplifier, even the input test sequence may cause undesirable adjacent frequency splatter at the instant that the amplifier's maximum drive level has been reached.

As an input signal to an amplifier increases in amplitude, an ideal output amplifier circuit would track changes in the input level and amplify the input level producing a substantially exact copy of the input signal. Practical limitations of an electronic amplifier limit the ability of a circuit to infinitely follow input signal levels. As an input signal level increases to the point

where the output amplifier stage can no longer amplify it accurately, the output stage will begin to saturate and, if the amplifier's output signal is fed back to the input in a negative feedback loop, an algebraic addition of the amplifier's input signal with its feedback error signal, can produce substantial distortion in the signal input to the amplifier stage.

In some communications applications, it may be desirable to limit the amount of frequency splatter caused by overdriving an amplifier, even during intervals when the maximum input level for the amplifier is being determined by a test sequence. An amplifier circuit that includes the ability to limit adjacent frequency splatter even when a maximum drive level is being measured by a test sequence would be an improvement over the prior art.

Summary of the Invention

There is provided herein an amplifier circuit that reduces off-channel frequency splatter caused by excessive input signal levels, including off-channel splatter caused by input test signals used to established maximum input signal levels. The amplifier circuit in the preferred embodiment is comprised of an inverting amplifier stage, a feedback circuit that samples the output of the amplifier and couples a portion of the output signal back to the amplifiers input, and an adjustable slew rate amplifier coupled between the amplifier stage input and the input signal source, the slew rate of which is reduced during periods when input level test sequences are input to the amplifier circuit.

(The test sequences are typically slow rise-time signals or voltage ramps used to establish a maximum input level.)

The adjustable slew rate amplifier has its slew rate limited, or controlled, during periods when a test signal is being input to the amplifier stage to determine the maximum input signal level which the amplifier stage can accept without clipping. The adjustable slew rate amplifier reduces off-channel splatter from the amplifier caused by its being overdriven by the test sequences by virtue of its ability to suppress signals being input to the amplifier that exceed the amplifiers ability to follow the rise time of the signals.

At least two different slew rates are established under the control of an external circuit. In an operational mode the slew rate amplifier has a maximum slew rate that is capable of accurately tracking the rise time of input signal levels experienced under normal operating conditions. In its limited slew rate mode, entered when input test signals that have typically slow rise times are being input to the amplifier, the reduced slew rate of the amplifier is sufficient to follow the input test signal but is suppresses undesirable emission from the amplifier when overdrive occurs.

Brief Description of the Drawings

FIG. 1 shows a block diagram of an amplifier circuit providing reduced off-channel frequency splatter;

FIG. 2 shows a block diagram of an amplifier providing reduced off-channel frequency splatter for use with quadrature amplitude signals; and

FIG. 3 shows a schematic diagram of an adjustable slew rate amplifier contemplated in FIG. 1 and FIG. 2.

Detailed Description of the Preferred Embodiment

FIG. 1 shows a simplified block diagram of an amplifier circuit (10) that provides reduced off-frequency splatter that may be caused by clip detection sequences input to an amplifier to determine its maximum allowable drive level. In the amplifier circuit (10) shown in FIG. 1, an input signal (20) from an external source, such as an audio modulator or other source is coupled to a first input (24A) of a summing network (24) through a selection switch (22) The output of the summer (24) is coupled to an adjustable slew rate amplifier (26) which, in its normal operational mode, has a maximum slew rate sufficient to accommodate the rise time of the signals from the signal source (20).

As seen in FIG. 1, the output of the adjustable slew rate amplifier (26) is coupled to a first multiplier, (also known as a mixer and which in FIG. 1 is a two-input mixer) circuit (30), the other input of which is coupled to the output of a local oscillator (32) (not shown). The multiplier circuit (30) mixes or heterodynes the output of the adjustable slew rate amplifier to a frequency equal to the sum (or difference depending upon the desired product frequency) of the local oscillator frequency and the frequency of the output of the adjustable slew rate amplifier (26).

The output of the multiplier circuit (30) is amplified by an inverting amplifier stage (34) to produce an output voltage V_{out}. The output signal of the

inverting amplifier stage (34) might be coupled to an antenna, for example; it might also be coupled to subsequent signal processing stages as required by the particular application considered for the amplifier circuit (10).

In the amplifier circuit shown in FIG. 1, the output of the inverting amplifier stage (34) is coupled to a second multiplier, stage (36) (also known as a mixer) the other input of which receives the local oscillator signal (32). The second multiplier stage (36) heterodynes the output of the inverting amplifier stage (34) by the same local oscillator signal from the local oscillator (32) to produce the baseband signal input to the adjustable slew rate amplifier (26) from the summing node (24). The output of the second multiplier stage (36) is coupled to the second input (24B) of the summing network (24).

(The embodiment shown contemplates being used in a radio. Alternate embodiments of the invention might not use the single frequency conversion shown in FIG. 1 but might use multiple conversion. Still other embodiments of the invention might not use any frequency conversion in the amplifier circuit shown and perform essentially all functions at a single frequency, baseband for example.)

The summing network (24) produces at an output, a signal that is substantially the algebraic sum of the first input (24A) and the second input (24B). Since the final amplifier stage (34) is an inverting amplifier, the algebraic addition of the signal at input (24A) and the addition of the signal (24B) produces as a net result, a subtraction of these two signals. The output from the

summer (24) can be thought of as an error signal which is amplified by the adjustable slew rate amplifier (26). If the input signal to the adjustable slew rate amplifier (26) has a slew rate or rise time that exceeds the ability of the adjustable slew rate amplifier to follow it, the adjustable slew rate amplifier will limit the slew rate time of the signal input to the first multiplier (30), to the maximum slew rate capability of the slew rate amplifier.

The maximum slew rate of the adjustable slew rate amplifier (26) is substantially reduced under the control of the gain bandwidth and slew rate control circuit (28) during times when a test signal from a test signal source (40) is switched into the summing network (24) by means of the source selector switch (22). The test signal is used to establish the maximum input level that the amplifier circuit (10) can accept at the first input (24A) of the summing network (24).

The maximum input signal level that the amplifier circuit (10) can accurately reproduce can be determined by putting a slow rise time signal from the test signal source (40) that increases slowly to a point at which the output from the inverting amplifier stage (34) begins to saturate or clip. When this maximum input signal level is reached, its determination can thereafter be used to limit input signal excursion from the signal source (20) to eliminate distortion or splatter caused by overdriving the amplifier stage (34).

During the time that the test signal from the test signal source (40) is being input to the summing network (24) adjacent or off-channel frequency splatter caused by clipping of the amplifier can be avoided by reducing

the slew rate of the adjustable slew rate amplifier (26). Adding the adjustable slew rate amplifier and reducing its slew rate during instances when the input drive level are being measured virtually precludes the generation of any off-channel frequency splatter, even during input test sequences to the amplifier, which can cause clipping. In this manner very clear signal sources can be maintained in communication systems that require minimal adjacent channel interference.

FIG. 2 shows a block diagram of another application of the preferred embodiment of the amplifier circuit that reduces off-channel frequency splatter, including off-channel frequency splatter caused by clip detection sequences. In this figure the amplifier circuit, a so-called quadrature amplifier, amplifies an in-phase component designated as I-channel as well as a quadrature component designated as Q-channel. (The I and Q signal components are baseband signals, which are used to scale the magnitudes of local oscillator signals that are ninety degrees apart from each other. The I and Q signals as well as the phase or frequency of the local oscillator can be used to carry information.)

In this figure, a digital signal processor controls digital to analog convertors 50I and 50Q, respectively, that generate the input information signals for a communications device such as a radio transmitter. The output of the digital to analog convertors 50I and 50Q are both low-pass-filtered in I channel and Q channel low pass filters 42I and 42Q. The output of the low pass filters for the I channels and Q channels are both input to I channel and Q channel summing circuits 24I and 24Q respectively. The output of these summing

circuits are coupled to I channel and Q channel adjustable slew rate amplifier circuits (26I and 26Q) . Both of these adjustable slew rate amplifiers (26I and 26Q) are controlled by a gain bandwidth slew rate control circuit (28) not shown in Fig. 2. (The slew rate control circuit (28) might include a microprocessor or other circuitry capable of determining when the slew rate of the adjustable slew rate amplifiers is to be reduced.)

As shown in FIG. 1, the output of these adjustable slew rate amplifiers (26I and 26Q) are both coupled into multiplier circuits (30I and 30Q). These two multiplier circuits both obtain their heterodyning frequencies from a local oscillator (32) (not shown in Fig. 2) the quadrature or Q component of which is generated by phase shifting the local oscillator signal by ninety degrees in a phase shifting network (33).

The output of both the I channel and Q channel multiplier circuits (30I and 30Q) are summed in a summing network (35) the output of which is amplified by the final amplifier stage (34), similar to the implementation shown in FIG. 1.

In FIG. 2 the output of the final amplifier stage (34) is sampled and returned to two multiplier circuits (36I and 36Q) which restore the output of the final amplifier stage (34) to baseband frequencies by multiplying the amplifier output signals by a second local oscillator signal 32P that has been phase shifted from the local oscillator signal 32 for loop stability (one copy of signal 32P is also phase shifted by 90 degrees to return the Q channel component back to baseband). The negative feedback loop of the quadrature

amplifier is completed by connecting the fedback signals from the multipliers (36I and 36Q) to the second inputs of the I channel and Q channel first summers (24I and 24Q).

In communications applications that require multi-level QAM or quadrature amplitude modulation signals, or other variable amplitude signals, such as single sideband, the amplifier circuit shown in FIG. 2 can reduce off-channel frequency splatter even caused by clip detection sequences as described above. When a clip detection sequence is input at summing networks 24I and 24Q, which test sequence is typically comprised of a slow rise time ramp voltage, the slew rate of the adjustable amplifiers (26I and 26Q) is reduced to suppress the generation of harmonics or spurious signals caused by a test sequence that rises beyond the point at which the final amplifier stage (34) can accurately amplify it.

An adjustable slew rate amplifier used in FIGs. 1 and 2 is shown in FIG. 3. The adjustable slew rate amplifier (26) may be considered as a voltage to current convertor or a transconductance amplifier, the output of which is shunted by an RC network.

Slew rate adjustment is achieved by means of adjusting the tail current I through the constant current source transistor Q_5. Q_1 and Q_2 form a differential pair. Q_3 and Q_4 form a current mirror to provide an active load for the collectors of Q1 and Q2. If the collector current through Q_5 is established to be relatively large, both Q_1 and Q_2 may conduct fairly heavily through Q_3, Q_4, respectively. (RE1 and RE2 may be selected to limit the

amount of collector current and increase the output impedance of the active load.)

When the collector current (I) through Q_5 is relatively large the voltage swing on the inverting and non-inverting terminals V_{IN-} and V_{IN+} may swing relatively freely with the resultant output current at the collectors of Q_4 and Q_2 swinging between -I and +I where I is the value of current through Q_5. As the rate of change of output voltage across the capacitor is equal to 1/C times the current through the capacitor, a relatively large collector current through Q_5 will permit the output voltage across the capacitor C_0 to change very quickly.

If the collector current I through Q_5 is made relatively small, the maximum rate of change of the output voltage, also known as the slew rate, will also be small, regardless of the input signal excursion across the bases of Q_1 and Q_2.

It should be seen that an adjustable slew rate amplifier has been shown which when incorporated into a signal loop of an amplifier stage can be used to reduce adjacent channel frequency splatter when the maximum input level signals that the amplifier can amplify is being measured during test signals. In this fashion, even test sequence frequency splatter can be reduced further improving or reducing off-channel interference in radio communication systems that require precise splatter control.

Although an inverting amplifier is shown in Fig.1, alternate embodiments might include using a non-inverting gain stage for the amplifier (34). Using a non-inverting amplifier would thereafter require using some other signal inversion means, such as an inverting

voltage amplifier or inverting operational amplifier, between the output of the amplifier (34) and the second input (24B) of the summer (24) so as to produce a difference signal output from the summer (24). Furthermore, the amplifier (34) need not provide voltage amplification but might provide current gain if an appropriate output load is selected. Alternate embodiments might also contemplate using a voltage or current follower as the final amplifier (34) so long as a negative feedback signal is provided to the summer circuits (24, or 24I and 24Q).

What is claimed is:

1. In an amplifier circuit (10) providing signals at a circuit output node that are amplified versions signals at a circuit input node, the amplifier circuit having at least one internal signal amplifier stage (34) with an input and an output, providing signals at its output that are inverted versions of signals at its input, a method of limiting spurious signals from the output of the amplifier circuit (34) caused by overdriving the internal signal amplifier stage during the input of predetermined rise time clip detection input signal test sequences that are input to the amplifier circuit, said method comprised of the steps of:

sampling the output signal from the amplifier circuit to provide a feedback signal;

adding the feedback signal to the predetermined rise time clip detection input signal test sequences to produce an error signal;

testing the error signal to identify internal signal amplifier stage output signal clipping; and

amplifying the error signal in an adjustable slew rate amplifier, having at least first and second slew rates determined by a control signal to the adjustable slew rate amplifier, to produce an input signal for the one internal signal amplifier stage so as to limit undesirable signal components from the output of the amplifier during input of the predetermined rise time clip detection input signal test sequences.

2. An amplifier circuit that reduces off-channel frequency splatter caused by excessive input signal levels, by establishing input signal levels at which clipping might occur using predetermined rise-time test signals comprised of:

an inverting amplifier means (34), having an input and an output, for providing output signals at the output that are at least inverted versions of signals at the input;

sampling means (36), having an input and an output, the input coupled to the output of the amplifier means (34), for providing a feedback signal at the output that is a portion of the output signals of the amplifier means (34);

summing means (24), having at least first and second inputs (24A and 24B), and an output, for providing a signal at the output that is substantially an algebraic summation of signals at the first and second inputs, said first input of the summing means (24B) being coupled to the output of the sampling means (36), said second input (24A) being coupled to a signal source (20) to be amplified by the amplifier circuit (34);

adjustable slew rate amplifier means (26) having an input and an output, for providing at least first and second amplifier slew rates during predetermined intervals in response to a slew rate control signal, said input coupled to the output of

the summing means (24), said output coupled to the input of the amplifier means; and

slew rate control means (28), coupled to the adjustable slew rate amplifier means (26) for providing a control signal to the adjustable slew rate amplifiers (26).

3. The amplifier circuit of claim 2 where said inverting amplifier (34) is a voltage amplifier.

4. The amplifier circuit of claim 2 where said sampling means (36) is a feedback circuit.

5. The amplifier circuit of claim 2 where said sampling means (36) includes a two-input signal mixer (36), mixing signals output from the inverting amplifier with a local oscillator signal (32).

6. The amplifier circuit of claim 2 where said adjustable slew rate amplifier means (26) includes a transconductance amplifier.

7. The amplifier circuit of claim 2 where said slew rate control means (26) is a microprocessor.

8. An amplifier circuit providing reduced off-channel frequency splatter caused by clip detection test sequences comprised of:

an amplifier (34), having an input and an output, providing output signals at the output that are versions of signals at the input;

sampling means (36), having an input and an output, the input coupled to the output of the amplifier (34), for providing a feedback signal that is a fractional portion of the output signals of the amplifier (34);

summing means (24), having at least first and second inputs (24A and 24B), and an output, for providing a signal at the output that is substantially an algebraic summation of signals at the first and second inputs (24A and 24B), said first input of the summing means (24B) being coupled to the output of the sampling means (36), said second input (24A) being coupled to a signal source (20) to be amplified by the amplifier (34);

inverter means, having an input and an output, for providing signals at the output that are inverted versions of signals at the input, said inverter means being operationally coupled between the output of the sampling means and the first input of the summing means;

adjustable slew rate amplifier means (26) having an input and an output, for providing at least first and second amplifier slew rates during predetermined intervals in response to a slew rate control signal, said input coupled to the output of the summing means (24), said output coupled to the input of the amplifier; and

slew rate control means (28), coupled to the adjustable slew rate amplifier means for providing a control signal to the adjustable slew rate amplifier means (26).

9. The amplifier circuit of claim 10 where said slew rate control means (28) is a microprocessor.

10. A phase quadrature amplifier circuit for amplifying signals with in-phase (I) and quadrature (Q) components and that reduces off-channel frequency splatter caused by excessive I and Q input signal levels, by establishing I and Q input signal levels at which clipping might occur using predetermined rise-time test signals comprised of:

an inverting amplifier means (34), having an input and an output, for providing output signals at the output that are at least inverted versions of signals at the input;

channel sampling means (36I, 36Q, 32P, 37) having an input and at least an I-channel output and a Q-channel output, the input coupled to the output of the amplifier means (34), for providing I and Q feedback signals at the I and Q outputs that are proportional to the output signals of the amplifier means (34);

I-signal summing circuit (24I), having at least a first and a second input (Vii and Vfi) and an output (Vei), providing a signal at the output that is substantially an algebraic summation of signals at the first and second inputs, said first input (Vfi) of the I-signal summing circuit being coupled to the I output of the channel sampling means (36I, 36Q, 32P, 37), said second input (Vii) being coupled to an I-channel signal source (50I, 42I) to be amplified by the amplifier circuit;

Q-signal summing circuit (24Q), having at least a first and second input (Viq and Vpq), and an output (Veq), providing a signal at the output (Veq)that is substantially an algebraic summation of signals at the first and second inputs, said first input (Vfq) of the Q-signal summing circuit being coupled to the Q output of the channel sampling means, said second input (Viq) being coupled to a Q-channel signal source (50Q and 42Q) to be amplified by the amplifier circuit;

I-channel adjustable slew rate amplifier means (26I) having an input and an output, for providing at least first and second amplifier slew rates during predetermined intervals in response to a slew rate control signal (28), said input coupled to the output of the I-signal summing circuit, said output coupled to the input of the amplifier means (34);

Q-channel adjustable slew rate amplifier means (26Q) having an input and an output, for providing at least first and second amplifier slew rates during predetermined intervals in response to a slew rate control signal (28), said input coupled to the output of the Q-signal summing circuit, said output coupled to the input of the amplifier means; and

slew rate control means (28), coupled to the I-channel and Q-channel adjustable slew rate

amplifier means for providing a control signal to the adjustable slew rate amplifiers.

FIG.1

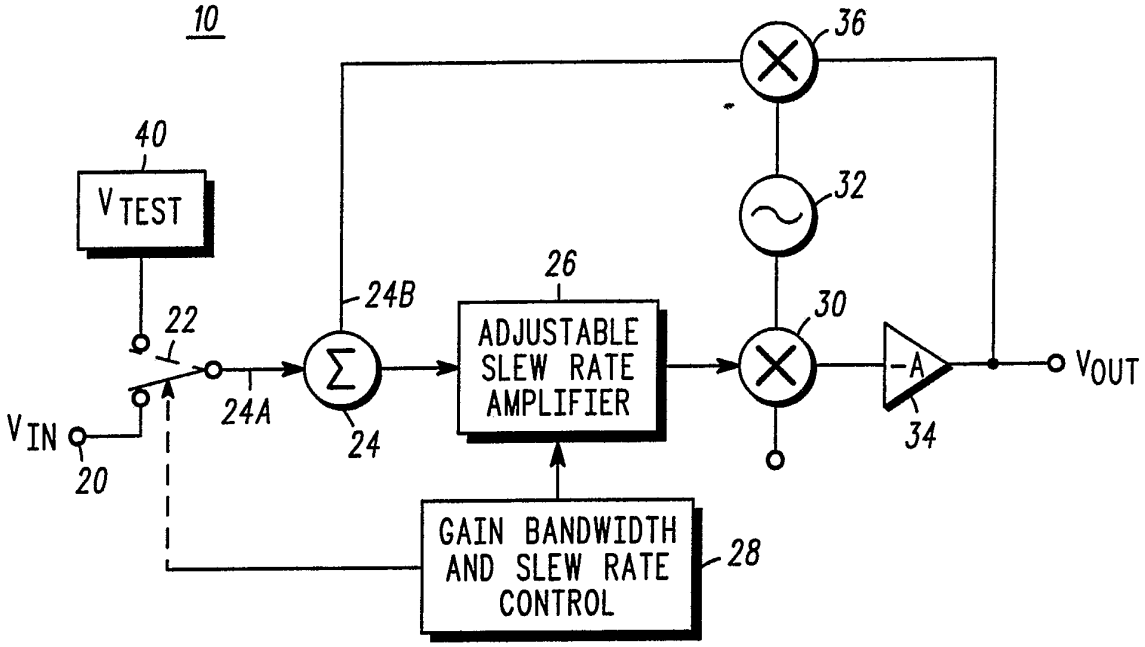
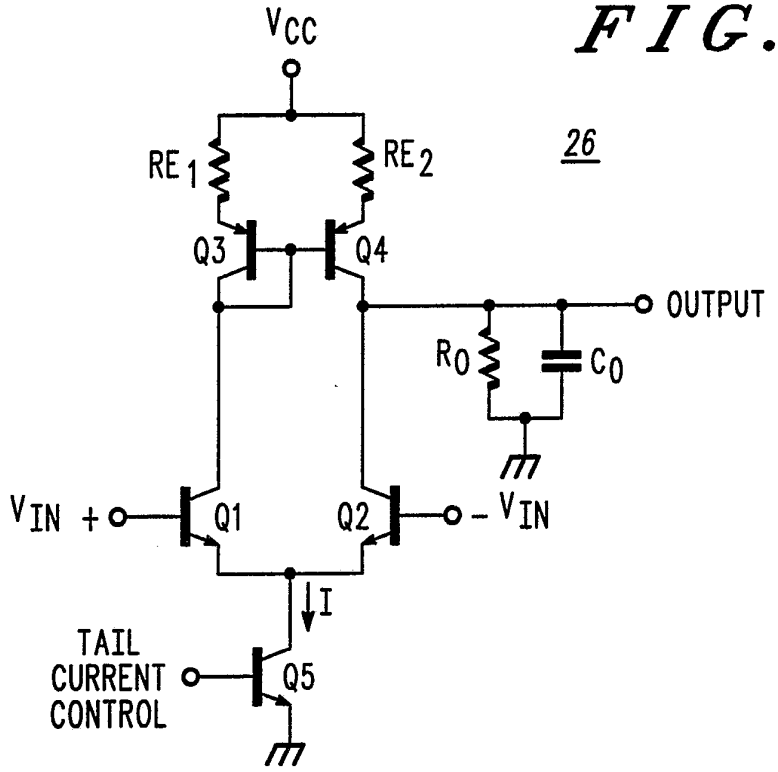

10
36
40
V TEST
32
26
24B
22
30
ADJUSTABLE SLEW RATE AMPLIFIER
-A
V OUT
24A
24
34
V IN
20
GAIN BANDWIDTH AND SLEW RATE CONTROL
28

FIG.3


V CC
RE 1
RE 2
26
Q3
Q4
OUTPUT
R O
C O
V IN +
Q1
Q2
- V IN
I
TAIL CURRENT CONTROL
Q5

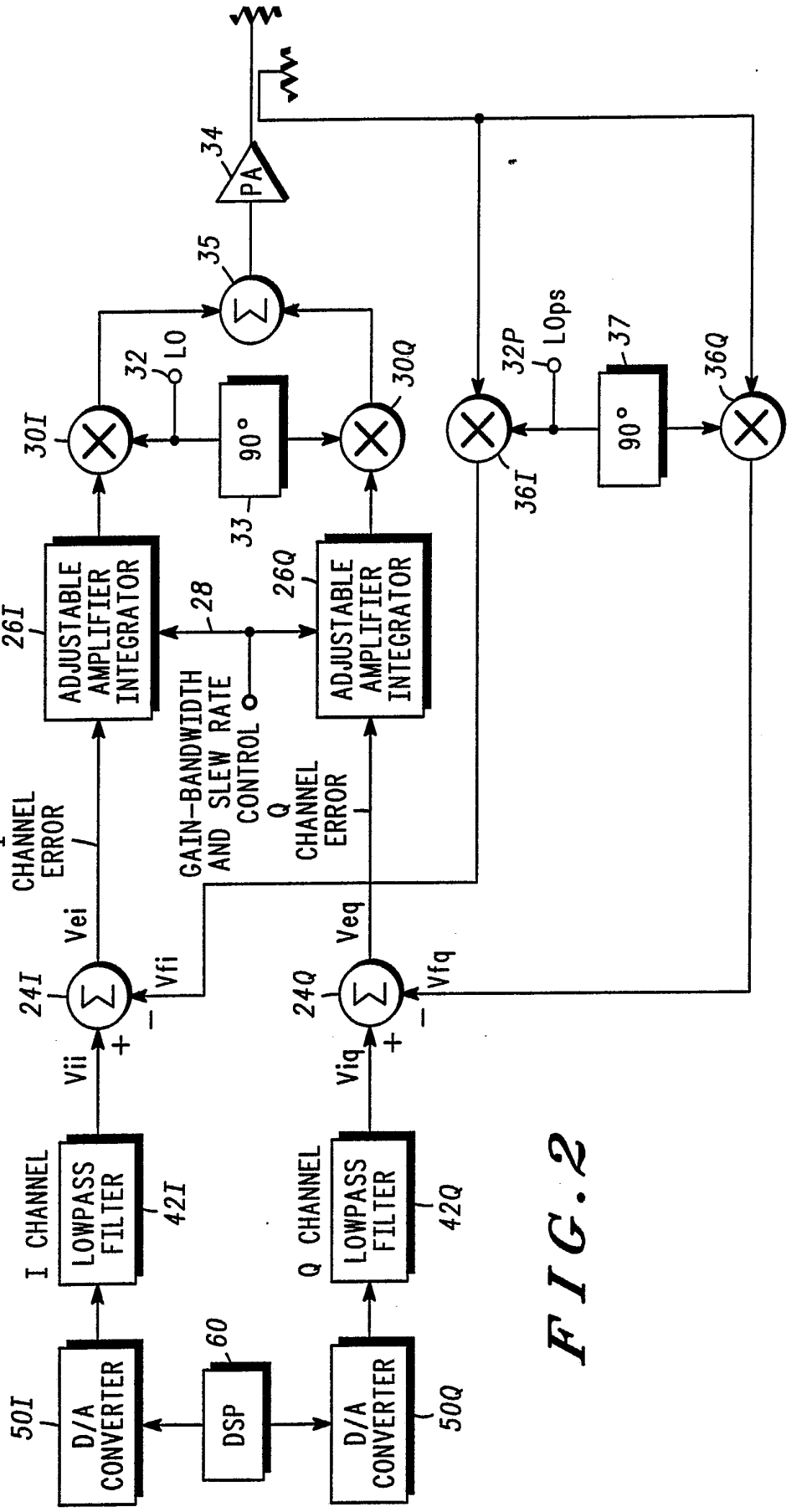

D/A CONVERTER
50I
DSP
60
D/A CONVERTER
50Q
I CHANNEL LOWPASS FILTER
42I
Q CHANNEL LOWPASS FILTER
42Q
Vii
Viq
24I
24Q
Vei
Veq
Vfi
Vfq
I CHANNEL ERROR
Q CHANNEL ERROR
GAIN-BANDWIDTH AND SLEW RATE CONTROL
28
ADJUSTABLE AMPLIFIER INTEGRATOR
26I
ADJUSTABLE AMPLIFIER INTEGRATOR
26Q
30I
30Q
32
LO
90°
33
35
PA
34
32P
LOps
36I
90°
37
36Q

FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/06454

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.(5): H03G 3/30

U.S. CL.: 330/2

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	307/540,542,546; 330/2, 129,149,278; 332/103, 105; 375/39

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	US, A, 4,318,053 (SONDERMEYER) 02 March 1982. See the entire document.	1-9
A	US, A, 4,048,573 (EVANS et al) 13 September 1977. See the entire document.	1-9
A	US, A, 4,926,443 (REICH) 15 May 1990. See Fig. 3 and col. 5, line 38 to col. 5, line 38 to col. 6, line 35.	10

* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
16 December 1991	16 JAN 1992
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ISA/US	NGUYEN NGOC-HO INTERNATIONAL DIVISION For Steven J. Mottola Ngoc Nguyen

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