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(71) Applicant (for all designated States except US): **SEA-GATE TECHNOLOGY LLC** [US/US]; 7801 Computer Avenue S, Bloomington, Minnesota 55435 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ROELOFS, Andreas** [DE/US]; 7017 Boyd Avenue, Eden Prairie, Minnesota 55346 (US). **SIEGERT, Markus** [DE/US]; 4333 Colfax Avenue South, Minneapolis, Minnesota 55409 (US). **VENUGOPALAN, Vaithyanathan** [IN/US]; 9851 Harrison Road, Apt. 308, Bloomington, Minnesota 55437 (US). **WEI, Tian** [CN/US]; 4101 West 98th Street, #202, Bloomington, Minnesota 55437 (US). **YONGCHUL, Ahn** [KR/US]; 1685 Oakbrooke Way, Eagan, Minnesota 55122 (US). **MURALIKRISHNAN, Balakrishnan** [IN/US]; 13159 Spencer Sweet Pea Lane, Eden Prairie, Min-

[Continued on next page]

(54) Title: PCMO NON-VOLATILE RESISTIVE MEMORY WITH IMPROVED SWITCHING

(57) Abstract: A resistive sense memory cell includes a layer of crystalline praseodymium calcium manganese oxide and a layer of amorphous praseodymium calcium manganese oxide disposed on the layer of crystalline praseodymium calcium manganese oxide forming a resistive sense memory stack. A first and second electrode are separated by the resistive sense memory stack. The resistive sense memory cell can further include an oxygen diffusion barrier layer separating the layer of crystalline praseodymium calcium manganese oxide from the layer of amorphous praseodymium calcium manganese oxide a layer. Methods include depositing an amorphous praseodymium calcium manganese oxide disposed on the layer of crystalline praseodymium calcium manganese oxide forming a resistive sense memory stack.

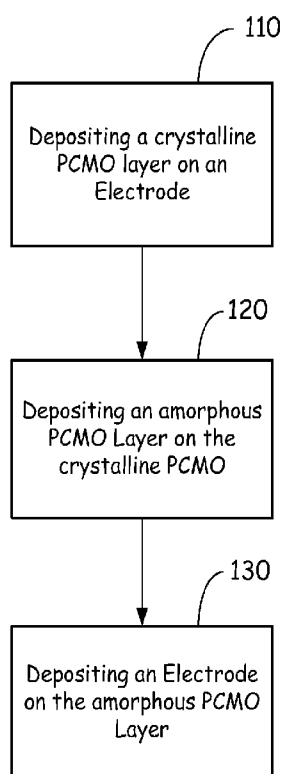


FIG. 5



nesota 55347 (US). **OLLE, Heinonen** [US/US]; 15824  
Park Terrace Drive, Eden Prairie, Minnesota 55346 (US).

(74) **Agent: BUENZOW, Jennifer**; Seagate Technology LLC,  
7801 Computer Avenue S, Bloomington, Minnesota  
55435 (US).

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DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,  
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KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD,  
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EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,  
LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK,  
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GW, ML, MR, NE, SN, TD, TG).

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**PCMO NON-VOLATILE RESISTIVE MEMORY WITH IMPROVED SWITCHING****BACKGROUND**

- [01] Fast growth of the pervasive computing and handheld/communication industry has generated exploding demand for high capacity non-volatile solid-state data storage devices. Current technology like flash memory, that utilizes a floating gate from which electrons tunnel, has several drawbacks such as slow access speed, limited endurance, and the integration difficulty. Flash memory (NAND or NOR) also faces significant scaling problems.
- [02] Resistive sense memories are promising candidates for future non-volatile and universal memory by storing data bits as either a high or low resistance state. One such memory, resistive RAM (RRAM) has a variable resistance layer that can switch between a high resistance state and a low resistance state (for example by the presence or absence of a conductive filament or interface effect variation) by application of a current or voltage.
- [03] However, many yield-limiting factors must be overcome before resistive sense memory enters the production stage, including better switching current characteristics.

**BRIEF SUMMARY**

- [04] The present disclosure relates to non-volatile resistive sense memory that includes a dual layer of calcium-doped praseodymium manganite or praseodymium calcium manganese oxide, hereafter referred to as PCMO. In particular the present disclosure relates to resistive memory cells that include a layer of crystalline PCMO and a layer of amorphous PCMO disposed on the layer of crystalline PCMO forming a resistive sense memory stack. In some embodiments the resistive sense memory stack includes an oxygen diffusion barrier layer separating the layer of crystalline PCMO from the layer of amorphous PCMO a layer.
- [05] In one illustrative embodiment, a resistive sense memory cell includes a layer of crystalline PCMO and a layer of amorphous PCMO disposed on the layer of crystalline PCMO forming a resistive sense memory stack. A first and second electrode are separated by the resistive

sense memory stack. The resistive sense memory cell can further include an oxygen diffusion barrier layer separating the layer of crystalline PCMO from the layer of amorphous PCMO.

[06] These and various other features and advantages will be apparent from a reading of the following detailed description.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[07] The disclosure may be more completely understood in consideration of the following detailed description of various embodiments of the disclosure in connection with the accompanying drawings, in which:

[08] **FIG. 1** is a schematic side view diagram of an illustrative nonvolatile resistive sense memory cell;

[09] **FIG. 2** is a schematic side view diagram of another illustrative nonvolatile resistive sense memory cell;

[10] **FIG. 3** is a schematic diagram of an illustrative nonvolatile resistive sense memory cell including a semiconductor transistor;

[11] **FIG. 4** is a schematic diagram of an illustrative nonvolatile resistive sense memory array;

[12] **FIG. 5** is a flow diagram of an illustrative method of forming a nonvolatile resistive sense memory cell;

[13] **FIGs. 6A-6C** are schematic cross-section views of a nonvolatile resistive sense memory cell at various stages of manufacture.

[14] **FIG. 7** is a flow diagram of another illustrative method of forming a nonvolatile resistive sense memory cell; and

[15] **FIGs. 8A-8D** are schematic cross-section views of another nonvolatile resistive sense memory cell at various stages of manufacture.

- [16] The figures are not necessarily to scale. Like numbers used in the figures refer to like components. However, it will be understood that the use of a number to refer to a component in a given figure is not intended to limit the component in another figure labeled with the same number.

#### DETAILED DESCRIPTION

- [17] In the following description, reference is made to the accompanying set of drawings that form a part hereof and in which are shown by way of illustration several specific embodiments. It is to be understood that other embodiments are contemplated and may be made without departing from the scope or spirit of the present disclosure. The following detailed description, therefore, is not to be taken in a limiting sense.
- [18] Unless otherwise indicated, all numbers expressing feature sizes, amounts, and physical properties used in the specification and claims are to be understood as being modified in all instances by the term “about.” Accordingly, unless indicated to the contrary, the numerical parameters set forth in the foregoing specification and attached claims are approximations that can vary depending upon the desired properties sought to be obtained by those skilled in the art utilizing the teachings disclosed herein.
- [19] As used in this specification and the appended claims, the singular forms “a”, “an”, and “the” encompass embodiments having plural referents, unless the content clearly dictates otherwise. As used in this specification and the appended claims, the term “or” is generally employed in its sense including “and/or” unless the content clearly dictates otherwise.
- [20] Spatially related terms, including but not limited to, “lower”, “upper”, “beneath”, “below”, “above”, and “on top”, if used herein, are utilized for ease of description to describe spatial relationships of an element(s) to another. Such spatially related terms encompass different orientations of the device in use or operation in addition to the particular orientations depicted in the figures and described herein. For example, if a cell depicted in the figures is turned over or flipped over, portions previously described as below or beneath other elements would then be above those other elements.

- [21] As used herein, when an element, component or layer for example is described as being “on” “connected to”, “coupled with” or “in contact with” another element, component or layer, it can be directly on, directly connected to, directly coupled with, in direct contact with, or intervening elements, components or layers may be on, connected, coupled or in contact with the particular element, component or layer, for example. When an element, component or layer for example is referred to as begin “directly on”, “directly connected to”, “directly coupled with”, or “directly in contact with” another element, there are no intervening elements, components or layers for example.
- [22] The present disclosure relates to non-volatile resistive sense memory that includes a dual layer of calcium-doped praseodymium manganite or praseodymium calcium manganese oxide or PCMO (e.g.,  $\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$ ). In particular the present disclosure relates to resistive memory cells that include a layer of crystalline PCMO and a layer of amorphous PCMO disposed on the layer of crystalline PCMO forming a resistive sense memory stack. In some embodiments the resistive sense memory stack includes an oxygen diffusion barrier layer separating the layer of crystalline PCMO from the layer of amorphous PCMO. These devices have been shown to switch at lower voltages (on the order of one volt) or currents and provide more symmetric switching characteristics than other single layer PCMO devices. In addition, inclusion of the oxygen diffusion barrier layer has been shown to improve the data state retention of the memory cell. While the present disclosure is not so limited, an appreciation of various aspects of the disclosure will be gained through a discussion of the examples provided below.
- [23] **FIG.1** is a schematic side view diagram of an illustrative nonvolatile resistive sense memory cell **10**. The resistive sense memory cell **10** includes a layer of crystalline PCMO **16**, a layer of amorphous PCMO **15** disposed on the layer of crystalline PCMO **16** forming a resistive sense memory stack **18**. A first electrode **12** and a second electrode **14** are separated by the resistive sense memory stack **18**.
- [24] The term PCMO refers to  $\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$  (wherein X is in a range from 0.2 to 0.6 in some embodiments). This material deposited between noble metal or oxide electrodes is a

promising candidate for resistive sense memory material. This material provides interface effect RRAM as opposed to filament-formation RRAM. Interface effect RRAM materials are complex metal oxides that contain two or more materials and no initial forming is required of these materials, as opposed to filament-formation RRAM. Applying a current through the material in one direction places the material in a high resistance state. Applying a current through the material in an opposing direction places the material in a low resistance state. However, this material appears to suffer from a number of drawbacks. This material requires a relatively high switching voltage, in a range from 3 to 5 volts and secondly, this material appears to possess asymmetric switching where the switching voltage in one direction is 50% larger than the opposing direction switching voltage. In addition, this material appears to exhibit low data state retention duration. The resistive sense memory cell constructions described herein appear to overcome these deficiencies.

- [25] When the PCMO material is deposited at a temperature greater than 400 degrees centigrade, the PCMO material forms a crystal structure. The crystal structure improves the electrical conductivity of the PCMO material. When the PCMO material is deposited at a temperature less than 400 degrees centigrade or less than 375 degrees centigrade or less than 350 degrees centigrade, the PCMO material is amorphous. Amorphous PCMO material is a better electrical insulator than crystalline PCMO material.
- [26] The crystalline PCMO material acts as an oxide conductor that additionally functions as the oxygen supply for the amorphous PCMO material. The amorphous PCMO material forms a tunnel barrier where the tunnel barrier height or thickness is controlled by the oxygen concentration of the amorphous PCMO material. In many embodiments the amorphous PCMO has a thickness in a range from 1 to 10 nanometers or from 1 to 7 nanometers or from 1 to 5 nanometers and the crystalline PCMO material has a thickness in a range from 10 to 100 nanometers or from 10 to 75 nanometers or from 20 to 50 nanometers. Oxygen ion migration between the PCMO layers allows the memory cell to switch between the high and low resistance data state.

- [27] The electrodes **12**, **14** can be formed of any useful inert and conducting material. In many embodiments, the electrodes **12**, **14** are formed of a noble metal or an inert metal such as, tungsten (W), nickel (Ni), molybdenum (Mo), platinum (Pt), gold (Au), palladium (Pd), and rhodium (Rh) for example. The first electrode **12** can be, but need not be formed on a substrate. The substrate, if utilized, can include silicon, a mixture of silicon and germanium, and other similar materials. **FIG. 1** and **FIG. 2** do not depict an optional substrate.
- [28] **FIG.2** is a schematic side view diagram of another illustrative nonvolatile resistive sense memory cell **10**. The resistive sense memory cell or non-volatile memory cell **10** includes a layer of crystalline PCMO **16**, a layer of amorphous PCMO **15**, and an oxygen diffusion barrier layer **17** separating the layer of crystalline PCMO **16** from the layer of amorphous PCMO **15**, forming a resistive sense memory stack **18**. A first electrode **12** and a second electrode **14** are separated by the resistive sense memory stack **18**.
- [29] The oxygen diffusion barrier layer **17** enhances the thermal stability of the memory cell. The oxygen diffusion barrier layer **17** can be formed of any useful material that allows oxygen ions to move through it in the presence of an electrical bias, but inhibits oxygen or oxygen ion transport through it in the absence of an electrical bias. Examples of useful oxygen diffusion barrier layer **17** materials include metals or conductive oxides. Metallic oxygen diffusion barrier layer material includes platinum, for example. Conductive oxide oxygen diffusion barrier layer material includes IrO, RuO, SrRuO<sub>3</sub>, lanthanum calcium manganese oxide (i.e., LCMO), and the like, for example. The oxygen diffusion barrier layer **17** can have any useful thickness. In many embodiments, the oxygen diffusion barrier layer **17** has a thickness in a range from 1 to 10 nanometers, or from 2 to 10 nanometers.
- [30] When a voltage potential is applied across the resistive sense memory stack **18** in a first direction, oxygen ions are driven from the layer of crystalline PCMO **16** to the layer of amorphous PCMO **15** through the oxygen diffusion barrier layer **17**. This process is field driven. The diffusion thorough the oxygen diffusion barrier layer **17** is driven by the concentration gradient of oxygen ions between the adjacent surfaces of the crystalline PCMO **16** and the layer of amorphous PCMO **15**. When the voltage is removed the oxygen now in



the layer of amorphous PCMO **15** is not driven through the oxygen diffusion barrier layer **17** and no oxygen gradient will be present. This reduces the oxygen diffusion through the oxygen diffusion barrier layer **17** and enhances the memory retention of the nonvolatile resistive sense memory cell **10**.

- [31] **FIG. 3** is a schematic diagram of an illustrative nonvolatile resistive sense memory cell **20** including a semiconductor transistor **22**. Memory cell or unit **20** includes a resistive sense memory cell **10**, as described herein, electrically coupled to semiconductor transistor **22** via an electrically conducting element **24**. Transistor **22** includes a semiconductor substrate **21** having doped regions (e.g., illustrated as n-doped regions) and a channel region (e.g., illustrated as a p-doped channel region) between the doped regions. Transistor **22** includes a gate **26** that is electrically coupled to a word line **WL** to allow selection and current to flow from a bit line **BL** to memory cell **10**. An array of resistive sense memory units **20** can be formed on a semiconductor substrate utilizing semiconductor fabrication techniques.
- [32] **FIG. 4** is a schematic diagram of an illustrative nonvolatile resistive sense array **30**. Memory array **30** includes a plurality of word lines **WL** and a plurality of bit lines **BL** forming a cross-point array. At each cross-point a resistive sense memory cell **10**, as described herein, is electrically coupled to word line **WL** and bit line **BL**. A select device (not shown) can be at each cross-point or at each word line **WL** and bit line **BL**.
- [33] **FIG. 5** is a flow diagram of an illustrative method of forming a nonvolatile resistive sense memory cell. **FIG.s 6A-6C** are schematic cross-section views of a nonvolatile resistive sense memory cell at various stages of manufacture.
- [34] At **FIG. 6A** a layer of crystalline PCMO **16** is deposited on a first electrode **12** at block **110** of **FIG. 5**. The layer of crystalline PCMO **16** is deposited at a temperature sufficient to form a crystal structure in the PCMO layer **16**. In many embodiments the deposition temperature is greater than 400 degrees centigrade. Both the layer of crystalline PCMO **16** and the first electrode **12** can be formed by physical vapor deposition, chemical vapor deposition, electrochemical deposition, molecular beam epitaxy and atomic layer deposition. While not

illustrated, the first electrode **12** can be deposited on a substrate. The substrate includes, but is not limited to silicon, a mixture of silicon and germanium, and other similar material.

- [35] At **FIG. 6B** a layer of amorphous PCMO **15** is deposited on the layer of crystalline PCMO **16** at block **120** of **FIG. 5**. The layer of amorphous PCMO **15** is deposited at a temperature sufficient to form an amorphous or non-crystalline PCMO layer **15**. In many embodiments the deposition temperature is less than 400 degrees centigrade, or less than 375 degrees centigrade, or less than 350 degrees centigrade.
- [36] At **FIG. 6C** a second electrode **14** is deposited on the layer of amorphous PCMO **15** at block **130** of **FIG. 5**. The second electrode **14** can be formed using the deposition methods described above. Additional metal contact layer(s) can be formed on the second electrode **14**.
- [37] **FIG. 7** is a flow diagram of another illustrative method of forming a nonvolatile resistive sense memory cell. **FIG.s 8A-8D** are schematic cross-section views of another nonvolatile resistive sense memory cell at various stages of manufacture.
- [38] At **FIG. 8A** a layer of crystalline PCMO **16** is deposited on a first electrode **12** at block **210** of **FIG. 7**. The layer of crystalline PCMO **16** is deposited at a temperature sufficient to form a crystal structure in the PCMO layer **16**, as described above. While not illustrated, the first electrode **12** can be deposited on a substrate. The substrate includes, but is not limited to silicon, a mixture of silicon and germanium, and other similar material.
- [39] At **FIG. 8B** an oxygen diffusion barrier layer **17** is deposited on the layer of crystalline PCMO **16** at block **220** of **FIG. 7**. The oxygen diffusion barrier layer **17** can be formed using the deposition methods described above.
- [40] At **FIG. 8C** a layer of amorphous PCMO **15** is deposited on the oxygen diffusion barrier layer **17** at block **230** of **FIG. 7**. The layer of amorphous PCMO **15** is deposited at a temperature sufficient to form an amorphous or non-crystalline PCMO layer **15**, as described above.

- [41] At FIG. 8D a second electrode 14 is deposited on the layer of amorphous PCMO 15 at block 240 of FIG. 7. The second electrode 14 can be formed using deposition methods described above. Additional metal contact layer(s) can be formed on the second electrode 14.
- [42] Thus, embodiments of the NON-VOLATILE RESISTIVE SENSE MEMORY WITH IMPROVED SWITCHING are disclosed. The implementations described above and other implementations are within the scope of the following claims. One skilled in the art will appreciate that the present disclosure can be practiced with embodiments other than those disclosed. The disclosed embodiments are presented for purposes of illustration and not limitation, and the present invention is limited only by the claims that follow.

What is claimed is:

1. A resistive sense memory cell comprising:  
a layer of crystalline praseodymium calcium manganese oxide;  
a layer of amorphous praseodymium calcium manganese oxide disposed on the layer of crystalline praseodymium calcium manganese oxide forming a resistive sense memory stack; and  
a first and second electrode separated by the resistive sense memory stack.
2. A resistive sense memory cell according to claim 1 wherein the layer of crystalline praseodymium calcium manganese oxide has a thickness in a range from 10 to 75 nanometers and the layer of amorphous praseodymium calcium manganese oxide has a thickness in a range from 1 to 7 nanometers.
3. A resistive sense memory cell according to claim 1 wherein the first and second electrodes are formed of noble metals.
4. A resistive sense memory cell according to claim 1 further comprising an oxygen diffusion barrier layer separating the layer of crystalline praseodymium calcium manganese oxide from the layer of amorphous praseodymium calcium manganese oxide.
5. A resistive sense memory cell according to claim 4 wherein the oxygen diffusion barrier layer is a metallic oxygen diffusion barrier layer.
6. A resistive sense memory cell according to claim 5 wherein the oxygen diffusion barrier layer has a thickness in a range from 1 to 10 nanometers.
7. A resistive sense memory cell according to claim 5 wherein the oxygen diffusion barrier layer is a platinum layer.

8. A resistive sense memory cell according to claim 1 wherein the praseodymium calcium manganese oxide comprises  $\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein X is in a range from 0.2 to 0.6.
9. A resistive sense memory cell according to claim 4 wherein the oxygen diffusion barrier layer is a conductive oxide oxygen diffusion barrier layer.
10. A non-volatile memory cell comprising:
  - a layer of crystalline praseodymium calcium manganese oxide;
  - a layer of amorphous praseodymium calcium manganese oxide;
  - an oxygen diffusion barrier layer separating the crystalline praseodymium calcium manganese oxide layer from the amorphous praseodymium calcium manganese oxide layer, forming a resistive sense memory stack, wherein the oxygen diffusion barrier layer allows oxygen ions to move through it with an electrical bias, but inhibits oxygen or oxygen ion transport through it in absence of an electrical bias; and
  - a first and second electrode separated by the resistive sense memory stack.
11. A non-volatile memory cell according to claim 10 wherein the layer of crystalline praseodymium calcium manganese oxide has a thickness in a range from 10 to 75 nanometers and the layer of amorphous praseodymium calcium manganese oxide has a thickness in a range from 1 to 7 nanometers.
12. A non-volatile memory cell according to claim 11 wherein the oxygen diffusion barrier layer has a thickness in a range from 1 to 10 nanometers.
13. A non-volatile memory cell according to claim 10 wherein the first and second electrodes are formed of tungsten, nickel, molybdenum, platinum, gold, palladium, rhodium, and alloys, mixtures or combinations thereof.

14. A non-volatile memory cell according to claim 10 wherein the oxygen diffusion barrier layer is a metallic oxygen diffusion barrier layer comprising platinum.
15. A non-volatile memory cell according to claim 10 wherein the praseodymium calcium manganese oxide comprises  $\text{Pr}_{1-X}\text{Ca}_X\text{MnO}_3$ , wherein X is in a range from 0.2 to 0.6.
16. A non-volatile memory cell according to claim 10 wherein the oxygen diffusion barrier layer is a conductive oxide oxygen diffusion barrier layer comprising  $\text{IrO}$ ,  $\text{RuO}$ ,  $\text{SrRuO}_3$ , lanthanum calcium manganese oxide, or combinations thereof.
17. A method comprising:  
depositing a layer of crystalline praseodymium calcium manganese oxide on a first electrode;  
depositing a layer of amorphous praseodymium calcium manganese oxide on the layer of crystalline praseodymium calcium manganese oxide; and  
depositing a second electrode on the layer of amorphous praseodymium calcium manganese oxide, forming a resistive sense memory cell.
18. A method according to claim 17 wherein the crystalline praseodymium calcium manganese oxide is deposited at a temperature of at least 400 degrees centigrade.
19. A method according to claim 17 wherein the amorphous praseodymium calcium manganese oxide is deposited at a temperature of less than 400 degrees centigrade.
20. A method according to claim 17 further comprising depositing an oxygen diffusion barrier layer between the layer of crystalline praseodymium calcium manganese oxide and the layer of amorphous praseodymium calcium manganese oxide.

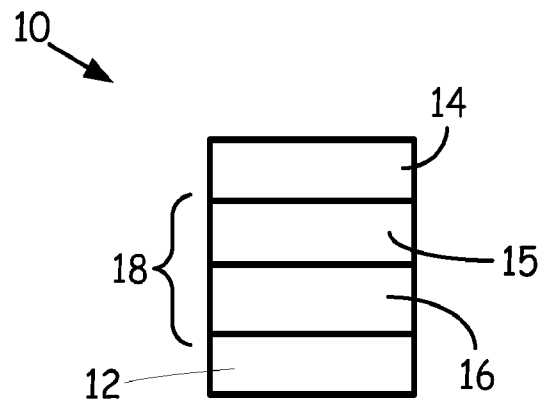


FIG. 1

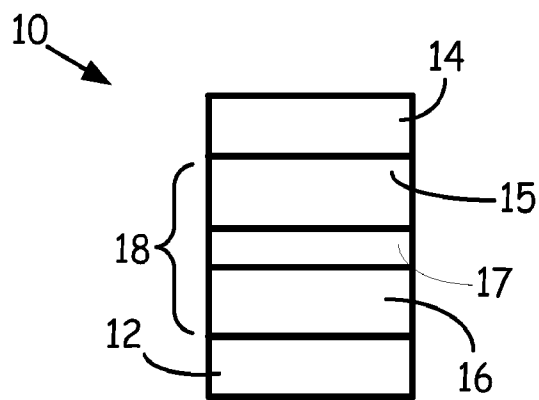


FIG. 2

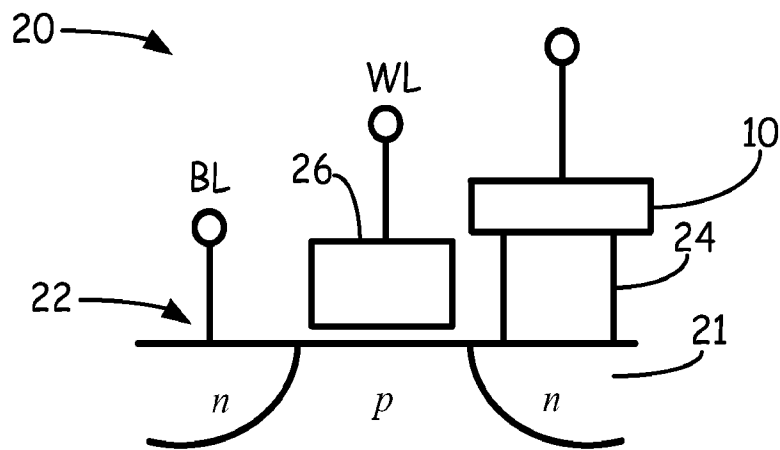


FIG. 3

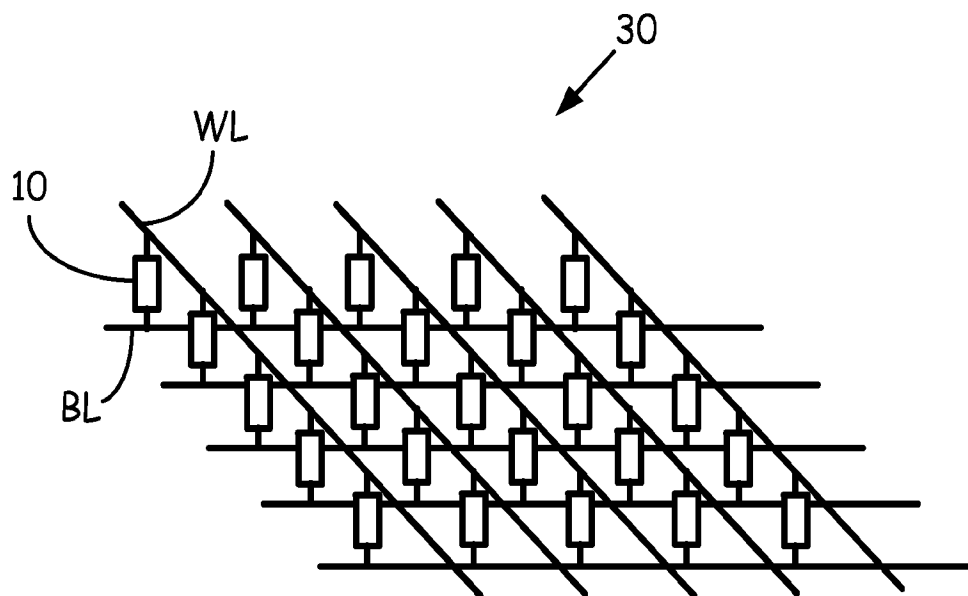


FIG. 4



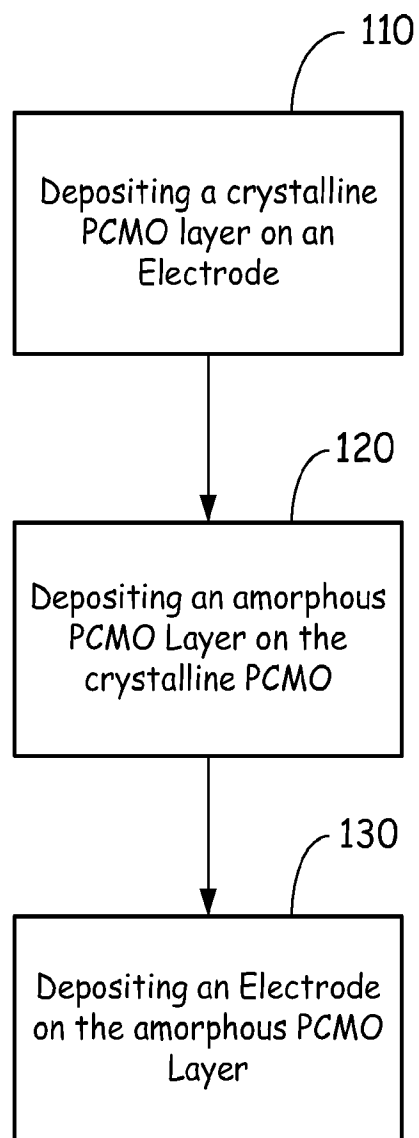


FIG. 5

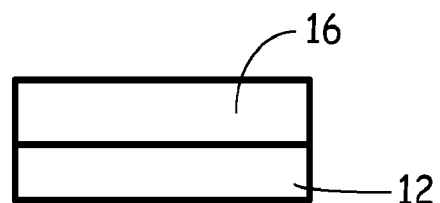


FIG. 6A

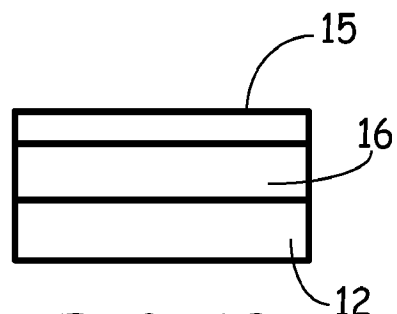


FIG. 6B

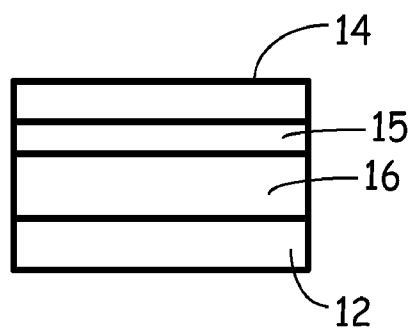


FIG. 6C

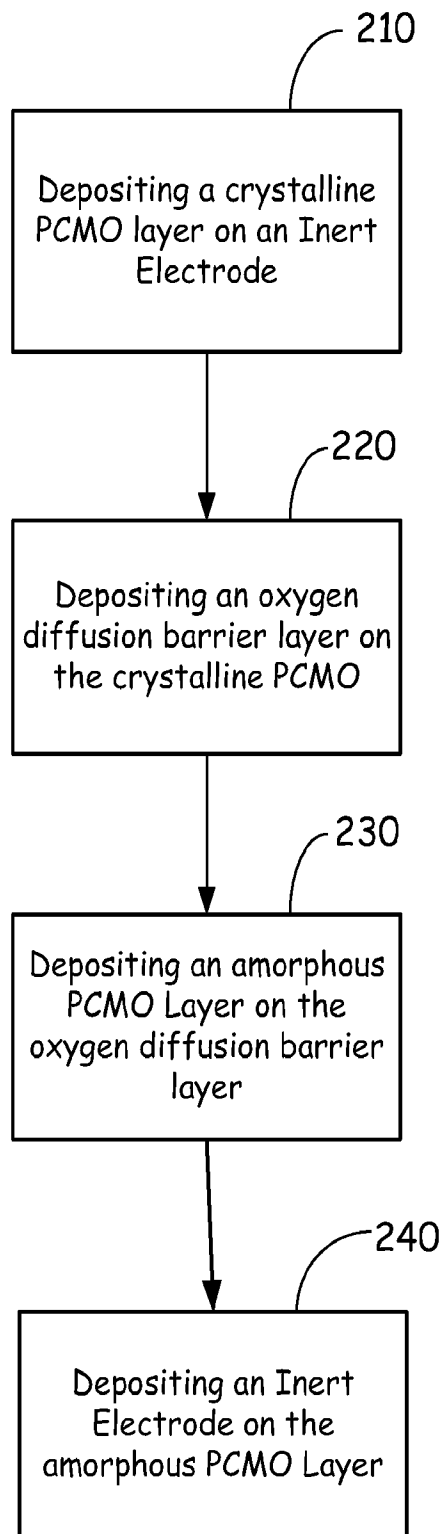


FIG. 7

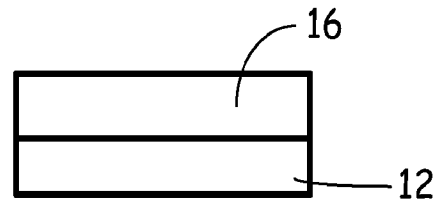


FIG. 8A

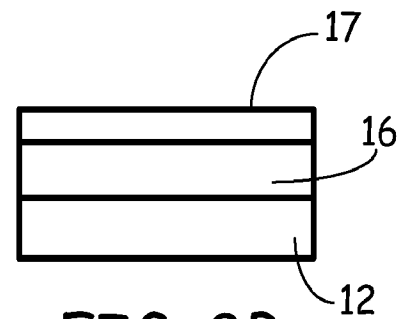


FIG. 8B

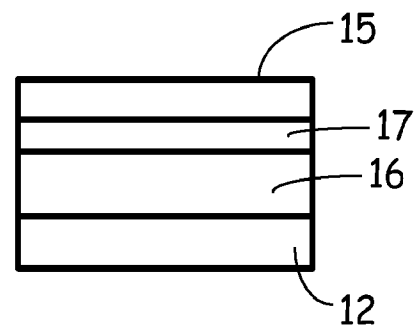


FIG. 8C

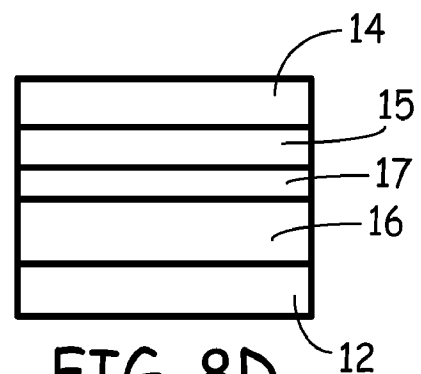


FIG. 8D

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2010/041545

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> INV. G11C13/00      H01L27/10      H01L27/24      H01L45/00 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) G11C H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/235247 A1 (HSU SHENG TENG [US] ET AL) 25 November 2004 (2004-11-25)	1,3,17-19
Y	paragraphs [0025], [3135] - [0037]; figures 4A-B	8,18,19
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X	US 2005/239262 A1 (ZHUANG WEI-WEI [US] ET AL ZHUANG WEI-WEI [US] ET AL) 27 October 2005 (2005-10-27)	1,3,17
Y	paragraphs [0023] - [0024], [0026], [0045]; figure 1B	8,18,19
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X	WO 2005/117021 A1 (UNITY SEMICONDUCTOR CORP [US]; CHEVALLIER CHRISTOPHE J [US]; KINNEY WA) 8 December 2005 (2005-12-08)	1-3,8,17
Y	paragraphs [0158] - [0175], [ 182]	18,19
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<div style="display: flex; justify-content: space-between;"> <span><input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C.</span> <span><input checked="" type="checkbox"/> See patent family annex.</span> </div>		
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Date of the actual completion of the international search	Date of mailing of the international search report	
29 September 2010	07/10/2010	
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