



## COMPLIANT PRINTED CIRCUIT WAFER PROBE DIAGNOSTIC TOOL

### Field of the Invention

**[0001]** The present disclosure relates to a compliant printed circuit that forms the basis of a diagnostic tool for testing wafer-level integrated circuit (IC) devices.

### Background of the Invention

**[0002]** There are many applications where a wafer probe is used to connect an IC device to a printed circuit board (PCB) so that the electrical connection is made in a separable manner. As illustrated in Figure 1, a wafer probe 20 in a test system 22 may have a plurality of probe members 24 that connect terminals 26 (or contact pads) on an IC device 28 to corresponding terminals 30 (or contact pads) on a PCB 32. The probe members 24 are held against the terminals 26 on the IC device 28 by applying a load 34 (or force) that maintains intimate contact and reliable connection during testing. No permanent connection is required such that the IC device 28 can be removed or replaced without a need to reflow solder connections.

**[0003]** The probe members 24 in the wafer probe 20 have at least two interface points for every probe member 24, a first interface 36 with the IC device 28 and a second interface 38 with the PCB 32. When the wafer probe is used 20 to connect to the IC device 28, there may be an assumption that the connection point for each terminal 26 is reliable. In the event the system is powered and the function of the IC device 28 is not as expected, any one of many connection points at the interfaces 36, 38 may be a cause of an error.

**[0004]** If the IC device 28 is removed and replaced and the issue is resolved, then a conclusion can be drawn that all of the other components in the test system 22 are connected and functioning properly. In the event the error is not resolved or another issue is introduced, the user must systematically sort through the various components and connections within the test system 22 to resolve the issue. In many cases, the wafer probe 20 may be a source of error due to the number of connections at the interfaces 36, 38 and the potential for at least one of those connections to be improperly positioned. A typical method to identify and resolve a wafer probe connection error is to replace the wafer probe 20 with another new wafer probe, or place the wafer probe 20 on an interface known to function properly to attempt to determine if the wafer probe 20 is the source of the error. If the new

wafer probe functions properly, then the initial wafer probe 20 can be deemed the source of the error. If the new wafer probe does function properly, then the issue is not resolved because the issue may be common or related to how the wafer probe 20 interfaces to the IC device 28 or to the PCB 32. This systematic troubleshooting process can be extremely time consuming and can cause major delays, and can impact the ability to continue testing IC devices.

**[0005]** There are several limitations to traditional methods of identifying and resolving wafer probe connection problems. The common method of replacing the wafer probe 20 with another is typically the first avenue, and requires that additional wafer probes 20 are available. Also, a successful result depends entirely on whether the issue is isolated to the initial wafer probe 20. This method can identify if there is an anomaly with the initial wafer probe 20 such as a damaged contact or poor connection. In the event the new wafer probe 20 does not produce desired results, further investigation is required. There may be a problem that is common to the wafer probes generally, and additional investigation is needed to determine if the source of the error remains with the wafer probe 20 or if the issue is elsewhere.

**[0006]** Another method of identifying and resolving wafer probe 20 connection errors may involve creating an external validation vehicle such as a PCB that mimics the system board. This method can be more determinant than an "in the system" approach such as replacing the wafer probe. The wafer probe interfaces 36, 38 can be isolated and if there is an issue with the group of contacts or with specific contacts the issue can be readily identified. A limitation of this method, however, can include that it requires that these external tools be created ahead of time so they are available if and when they are needed, which would result in additional effort and expense that is wasted if the wafer probe performs as expected.

**[0007]** Establishing these tools ahead of time can provide confidence that the wafer probe is functioning properly and, in the end, reduce effort because the user can trust that the wafer probe is working. However, there is some risk that the external tools may not match the actual system circuit board precisely in form and/or function, and that issues that are not present on the external tools may be present on the system PCB. Another limitation is that it can be difficult to mimic the terminal pattern of the IC device being tested due to the fine feature size and pitch. Still another limitation with this method may be the adverse consequences of failing to produce these external tools ahead of time, since the lead time to design and

produce these tools can be long. Still another limitation is that an external circuit board or test system may not precisely match the make-up of the actual system, and/or utilize an exact IC device. Typically, a surrogate IC device is used to simulate the actual IC device and a surrogate PCB is used to simulate the system PCB. The surrogate IC device and surrogate PCB may manifest issues different from or not present in the actual IC device and surrogate PCB. Similarly, the surrogates may not manifest issues present in the actual IC device and PCB. Accordingly, problems may go undetected.

**[0008]** In the event these methods do not identify the problem, the actual IC device can be soldered to the site intended for the wafer probe so that the wafer probe can be eliminated from the equation. However, this method defeats the advantages of using a wafer probe, including eliminating the desired separability.

#### Brief Summary of the Invention

**[0009]** The present application relates to a compliant printed circuit that forms the basis of a diagnostic tool for testing wafer-level IC devices. The compliant printed circuit can operate as an electrical interconnect between a wafer probe and wafer-level IC devices. A variety of passive and active electrical devices are incorporated into the present diagnostic tool to provide testing capabilities independent of, and/or supplementary to, conventional testing stations.

**[0010]** The present invention leverages the capabilities of printed electronics to provide a diagnostic tool that can validate wafer probe function external to the system and while the wafer probe is installed in the system. The present invention provides an electrical interconnect that will enable next generation electrical performance. Some of the embodiments include a high performance interconnect architecture on the interconnect.

**[0011]** Printing processes permit compliant printed circuits and electrical devices of diagnostic tools to be produced by a direct writing method based upon images, without the need for artwork, lengthy lead-times for circuit design and production, and subtractive circuit techniques. The present diagnostic tools can be simple or complex, and can be produced in minutes. The diagnostic tools can also be adapted as needed to accommodate additional diagnostic functions or tests. The additive nature of many printing processes, such as for example the inkjet printing process, can also provide an excellent avenue to directly print many electrical functions such as passive components, transistors, display function or adaptive intelligence.

Revisions can be accomplished in moments by altering the image files and reprinting the diagnostic tool. By contrast, revisions to the tools formed using traditional methods, may take weeks.

**[0012]** A diagnostic tool according to the present disclosure can be as simple as a daisy chain to verify continuity, or as complex as functional testing directly on the compliant printed circuit. Positioning functional testing on the present diagnostic tool dramatically increases the value to the user, without the need to connect to external systems or testing analyzers. The diagnostic tools can be printed with simple low-cost or low-speed circuitry, or the circuitry can be printed with high frequency capability in the event an external measurement tool is connected.

**[0013]** The cost to produce a diagnostic tool in accordance with the present invention is a fraction of the cost of a conventional tool. A tool produced with conventional methods might cost \$10,000 to \$20,000 to design and produce, typically with a 4-6 week lead-time. A diagnostic tool according to the present disclosure can be produced in minutes for a fraction of the cost. The ability to modify the design or correct errors which would cause the \$20,000 investment to be wasted, and reprint easily at little additional cost, offers tremendous improvements over conventional methods. Image libraries and design rules can be created to semi-automate the design process and dramatically reduce engineering time with tremendous flexibility to make changes substantially on the fly during the testing process.

**[0014]** The use of additive printing processes can permit the material set in a given layer to vary. Traditional PCB and circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

**[0015]** The compliant printed circuit can be processed to add functions and electrical enhancements not found in traditional printed circuits. A diagnostic tool according to the present disclosure can be configured with conductive traces that

reduce or redistribute the terminal pitch, without the addition of an interposer or daughter substrate. Grounding schemes, shielding, electrical devices, and power planes can be added to the present diagnostic tools, reducing the number of connections to the PCB and relieving routing constraints while increasing performance.

**[0016]** The resulting circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to recesses in a previously deposited layer. The use of additive printing processes permit conductive material, non-conductive material, and semi-conductive material to be deposited and positioned on a single layer.

**[0017]** In one embodiment, pre-formed conductive trace materials are located in the recesses. The recesses can be plated to form conductive traces with substantially rectangular cross-sectional shapes. In another embodiment, a conductive foil is pressed into at least a portion of the recesses. The conductive foil is sheared along edges of the recesses. The excess conductive foil not located in the recesses is removed and the recesses are plated to form conductive traces with substantially rectangular cross-sectional shapes.

**[0018]** One embodiment of the present disclosure can be directed to a diagnostic tool for wafer-level IC devices that are coupled to testing electronics by a wafer probe. A first diagnostic tool can include a first compliant printed circuit having a plurality of contact pads configured to form an electrical interconnect at a first interface between distal ends of probe members in the wafer probe and contact pads on one or more wafer-level IC devices. A plurality of printed conductive traces can electrically couple a plurality of the contact pads on the first compliant printed circuit. A plurality of electrical devices can be printed on the first compliant printed circuit at a position away from the first interface. The electrical devices can be coupled to the conductive traces and can be adapted to provide one or more of continuity testing at the first interface or functionality testing of the wafer-level IC devices.

**[0019]** The electrical devices printed on the first compliant printed circuit can be a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae. The first compliant printed circuit can optionally include one or more printed layers, such as for example a dielectric layer, a ground plane, or a power plane.

**[0020]** A second diagnostic tool can be provided with IC testing devices and configured to form an electrical interconnect with proximal ends of the probe members in the wafer probe at a second interface. The IC testing devices can be dedicated integrated circuits, printed circuit boards including or connected to testing logic, a test station, and the like. The second diagnostic tool can be programmed to provide one or more of continuity testing at the second interface, testing of the first diagnostic tool, or functional testing of the wafer-level IC device. The first and second diagnostic tools can be used separately or together.

**[0021]** Another embodiment is directed to a diagnostic tool that can include a dedicated IC testing device and can be configured to form an electrical interconnect at a first interface with proximal ends of probe members in a wafer probe. A first compliant printed circuit with a plurality of contact pads is electrically coupled to the contact pads on the dedicated IC testing device. A plurality of printed conductive traces can be coupled to a plurality of contact pads on the first compliant printed circuit. A plurality of electrical devices is printed on the first compliant printed circuit at a position away from the first interface. The electrical devices are coupled to the conductive traces and are programmed to provide one or more of continuity testing at the first interface, continuity testing at a second interface between distal ends of the probe members in the wafer probe and the wafer-level IC device, or functionality testing of the wafer-level IC device.

**[0022]** Another embodiment is directed to a method of making a first diagnostic tool for testing wafer-level IC devices coupled to testing electronics by a wafer probe. The method comprising the steps of printing a plurality of contact pads on a first compliant printed circuit. The contact pads are configured to form an electrical interconnect at a first interface between distal ends of probe members in the wafer probe and contact pads on the wafer-level IC device. A plurality of the conductive traces is electrically coupled to a plurality of the contact pads on the first compliant printed circuit. A plurality of electrical devices is printed on the first compliant printed circuit at a position away from the first interface so that the electrical devices are electrically coupled to the conductive traces. The first compliant printed circuit is positioned to form an electrical interconnect at the first interface. One or more of continuity at the first interface or functionality of one or more wafer-level IC devices is evaluated.

### Brief Description of the Several Views of the Drawing

**[0023]** Figure 1 is a cross-sectional view of a prior art wafer probe used to test IC devices.

**[0024]** Figure 2 is a schematic illustration of a test system with a diagnostic tool electrically coupling a wafer-level IC device to a testing system in accordance with an embodiment of the present disclosure.

**[0025]** Figure 3 is a schematic illustration of test system with an alternate diagnostic tool mated with a dedicated IC testing device in accordance with an embodiment of the present disclosure.

**[0026]** Figure 4 is a schematic illustration of a test system with an alternate diagnostic tool merged with a dedicated IC testing device in accordance with an embodiment of the present disclosure.

**[0027]** Figure 5 is a schematic illustration of a test system with a diagnostic tool substituted for the wafer-level IC device in accordance with an embodiment of the present disclosure.

**[0028]** Figure 6 is a schematic illustration of a test system with first and second diagnostic tools in accordance with an embodiment of the present disclosure.

**[0029]** Figure 7 is a schematic illustration of a test system with first and second diagnostic tools adapted to engage with land grid array (LGA) devices in accordance with an embodiment of the present disclosure.

### Detailed Description of the Invention

**[0030]** Figure 2 is a schematic illustration of diagnostic tool 50 electrically coupled at an interface 52 of a wafer probe 54 and a wafer-level IC device 56 in accordance with an embodiment of the present disclosure. A compliant printed circuit 58 of the diagnostic tool 50 is positioned to function as an electrical interconnect between probe members 60 on the wafer probe 54 and contact pads 62 on the wafer-level IC device 56.

**[0031]** The wafer probe 54 permits testing an interface 74 between an IC testing device 72 and proximal ends 76 of the probe members 60 of the wafer probe 54. And the IC testing device 72 can be engaged or disengaged with the probe members 60 of the wafer probe 54 without reflowing solder. In the illustrated embodiment, the IC testing device 72 is a printed circuit board, either including, or connected to, testing electronics. In another embodiment, the IC testing device 72 can be one or more dedicated integrated circuits programmed to perform testing functions.

**[0032]** The compliant printed circuit 58 can operate with fine contact-to-contact spacing (or “pitch”) on the order of less than 1.0 millimeter pitch, and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. The compliant printed circuit 58 can be a flexible polymeric sheet 64 having a plurality of conductive traces 66 arranged in an array to electrically couple with distal ends 68 of probe members 60 and contact pads 62 on the wafer-level IC device 56. Force F1 is preferably applied to the wafer probe 54 to compressively couple distal ends 68 with the contact pads 62 through the compliant printed circuit 58. The traces 66 electrically couple the probe members 60 and contact pads 62 with electrical devices 70A, 70B, 70C (collectively “70”) positioned at distal end of the diagnostic tool 50 away from the first interface. The electrical devices 70 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like.

**[0033]** In the configuration of Figure 2, the diagnostic tool 50 can evaluate the operation of the wafer-level IC device 56, the interface 52 of the wafer probe 54 and the wafer-level IC device 56, the wafer probe 54, the interface 74 between IC testing device 72 and the proximal ends 76 of probe members 60, and/or the IC testing device 72. For example, LCD 70A can display a pin-map of the probe members 60, LED’s 70B can indicate open/short, and integrated circuit 70C can provide specific diagnostic functionality to make the diagnostic tool 50 more than a basic open or short testing tool. In one embodiment, the IC testing device 72 is a dedicated electrical device designed to validate operation of the test system 90. Once operation of the test system 90 is verified, the wafer probe 54 is ready to test production IC devices. The production IC devices are positioned in the test system in place of the IC testing device 72.

**[0034]** The flexible polymeric sheet 64 optionally includes contact members 80 arranged in an array along a surface 82 of the compliant printed circuit 58 that correspond with the contact pads 62 on the wafer-level IC device 56. The contact members 80 can optionally have a pitch that is different than pitch of the distal ends 68 of the probe members 60. In an alternate embodiment, a variety of other circuit members can be substituted for the wafer-level IC device 56, such as for example

another flexible circuit, a packaged or unpackaged bare die silicon device, an integrated circuit device, an organic or inorganic substrate, or a rigid circuit.

**[0035]** The flexible polymeric sheet 64 is optionally singulated around the contact members 80. Singulation is a complete or partial separation of the terminal 80 from the sheet 64 that does not disrupt the electrical integrity of the conductive trace 66. The singulation can be a slit surrounding a portion of the contact member 80. The slit can be located adjacent to the perimeter of the contact member 80 or offset therefrom. Singulation of the compliant printed circuit 58 can control the amount of force transferred to the wafer-level IC device 56, and the range of motion singulation of the CPC 58 also assist with creating a more evenly distributed force vs. deflection profile across the array.

**[0036]** The singulations can be formed at the time of manufacture of the polymeric sheet 64 or can be subsequently patterned by mechanical methods such as stamping or cutting, chemical methods such as photolithography, electrical methods such as excess current to break a connection, a laser, or a variety of other techniques. In one embodiment, a laser system, such as an Excimer laser, a CO<sub>2</sub> laser, or a YAG laser, creates the singulation. A singulated structure is advantageous in several ways, because the force of movement is greatly reduced where the compliant printed circuit 58 is no longer a continuous membrane, but a series of flaps or bond sites with a living hinge and bonded contact.

**[0037]** The IC testing device 72 has a plurality of contact pads 73. Force F1 preferably compressively couples the contact pads 73 with the proximal ends 76 of the probe members 60. The force F1 can be provided by a variety of mechanisms, such as disclosed in U.S. Pat. Nos. 7,101,210 (Lin et al.); 6,971,902 (Taylor et al.); 6,758,691 (McHugh et al.); 6,461,183 (Ohkita et al.); and 5,161,983 (Ohno et al.), which are hereby incorporated by reference. The proximal ends 76 of the probe members 60 can be configured to electrically couple with a variety of types of contact pads 73 on the IC testing device 72.

**[0038]** The compliant printed circuit 58 and the electrical devices 70 are preferably manufactured using printing technology, such as for example, inkjet printing, screen printing, printing through a stencil, flexo-gravure printing, and offset printing, rather than traditional PCB fabrication techniques. Various methods of printing the compliant printed circuit and the electrical devices are disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson);

6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are incorporated herein by reference. For example, conductive inks containing metal particles are printed onto the compliant printed circuit 58 and subsequently sintered.

**[0039]** A printing process can preferably be used to fabricate various functional structures, such as conductive paths and electrical devices without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

**[0040]** Recesses may be formed in layers of the compliant printed circuit 58 to permit control of the location, cross section, material content, and aspect ratio of the contact members 80 and the conductive traces 66 in the compliant printed circuit 66. Maintaining the conductive traces with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the recesses to control the aspect ratio of the conductive traces 66 results in a more rectangular or square cross-section of the conductive traces, with the corresponding improvement in signal integrity.

**[0041]** U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated herein by reference, teach using inkjet printing to make various electrical devices, such as resistors, capacitors, diodes, inductors (or elements which can be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical

elements, transistors (including, light emitting, light sensing or solar cell elements, field effect transistors, top gate structures), and the like.

**[0042]** U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference, teach using aerosol printing to create various electrical devices and features.

**[0043]** Printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semiconductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

**[0044]** A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or teflon.

**[0045]** The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

**[0046]** The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from Dupont located in Wilmington, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

**[0047]** Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also

include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

**[0048]** Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinylidenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic/organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicyclobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

**[0049]** Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, *Adv. Mater.*, 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, *Appl. Phys. Lett.* 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181 (Bridenbaugh et al.), which is incorporated herein by reference.

**[0050]** A protective layer can optionally be printed onto the electrical devices and features. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

**[0051]** Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having

properties similar to those described above can be used in accordance with the present invention.

**[0052]** An inkjet print head, or other print head, preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

**[0053]** Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

**[0054]** The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electropneumatic, electrostatic, rapid ink heating, magnetohydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

**[0055]** While inkjet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: premetered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; aerosol printing processes; and other similar techniques.

**[0056]** The additive nature of inkjet printing of electrical devices and features provides an excellent means to print the desired functions directly on the compliant printed circuit 58, rather than mounting the electrical devices discretely. For example, the electrical devices 70 can be a capacitor, a resistor, a battery, a filter, a signal or power altering and enhancing device, a memory device, an embedded integrated circuit, and a RF antenna. The electrical devices 70 can be printed on either surface of the polymeric sheet 64. Inkjet printing can also be used to form

additional layers on the flexible polymeric sheet 64, such as for example dielectric layers covering the conductive traces 66, power planes, ground planes, and the like.

**[0057]** Positioning such electrical devices 70 on the compliant printed circuit 58 in close proximity to the IC testing device 72 can improve performance of the diagnostic tool 50. The present diagnostic tool 50 can permit integrated circuit manufacturers to reduce the pitch of the probe members 60 on the wafer-level IC device 56, and perform any required signal routing in the compliant printed circuit 58, rather than in the IC testing device 72 or by adding daughter boards to the system. IC manufacturers also are limited by the wafer probe 54, and the configuration of the probe members 60 therein, when designing the configuration of contact pads 62 on the wafer-level IC device 56. Performing routing (of a connection between the probe members 60 and contact pads 62) in the compliant printed circuit 58 can permit quick and inexpensive changes.

**[0058]** In another embodiment, the conductive traces 66 of the compliant printed circuit 50 are formed by transferring pre-patterned or pre-etched thin conductive foil circuit traces to recesses in a layer of the compliant printed circuit 50. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses not occupied by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses.

**[0059]** In another embodiment, a thin conductive foil is pressed into the recesses, and the edges of the recesses act to cut or shear the conductive foil. The process positions a portion of the conductive foil in the recesses, but leaves the negative pattern of the conductive foil not wanted outside and above the recesses for easy removal. Again, the foil in the recesses is preferably post plated to add material to increase the thickness of the conductive traces and to fill any voids left between the conductive foil and the recesses.

**[0060]** Figure 3 is a schematic illustration of an alternate diagnostic tool 100 mated with IC testing device 102, according to one embodiment of the present disclosure. The IC testing device 102 is preferably a dedicated IC adapted to test a wafer-level IC device 120. Conductive traces 104 on the compliant printed circuit 106 are electrically coupled with contact pads 108 on the IC testing device 102,

either by soldering on in a solderless manner. The illustrated IC testing device 102 is a land grid array (LGA) device, but any other IC package configuration can be used with the diagnostic tool 100 of Figure 3.

**[0061]** The compliant printed circuit 106 can be configured to simulate the system in which the wafer-level IC device 120 will be used, with desired functions, such as for example open/close shorting, daisy chain, or a diagnostic IC built into the electrical devices 112A, 112B, 112C (collectively "112") of the diagnostic tool 100. An electrical connection 134 can be optionally provided between the diagnostic tool 100 and the wafer-level IC device 120.

**[0062]** In the configuration of Figure 3, a test system 132 can evaluate the operation of the wafer-level IC device 120, an interface 122 of a wafer probe 110 and the wafer-level IC device 120, the wafer probe 110, and the interface 124 between IC testing device 102 and the proximal ends 126 of probe members 128. Again, the compliant printed circuit 106 and the electrical devices 112 are preferably manufactured using inkjet printing technology, aerosol printing technology, or other maskless deposition techniques, as previously described, rather than traditional PCB fabrication techniques.

**[0063]** Figure 4 is a schematic illustration of an alternate diagnostic tool 150 substantially as shown in Figure 3 with a compliant printed circuit 156 merged with an IC package 152 in accordance with an embodiment of the present disclosure. The conductive traces 154 on the compliant printed circuit 156 can be electrically coupled with an IC testing device 160, such as for example by wire bonding 162. The compliant printed circuit 156 is preferably attached or bonded to the IC package 152. As used herein, "bond" or "bonding" refers to, for example, adhesive bonding, solvent bonding, ultrasonic welding, thermal bonding, or any other techniques suitable for attaching adjacent layers.

**[0064]** Figure 5 is a schematic illustration of a diagnostic (test) system 200 with a diagnostic tool 202 substituted for the wafer in accordance with an embodiment of the present disclosure. Conductive traces 204 on a compliant printed circuit 206 electrically couple probe members 208 on a wafer probe 210 with electrical devices 212A, 212B, 212C (collectively "212"). The electrical devices 212 are also on the CPC 206, positioned away from an interface 218 of the wafer probe 210 and the CPC 206.

**[0065]** An IC testing device 214 couples with the wafer probe 210 as discussed above with reference to Fig. 2. In the configuration of Figure 5, the diagnostic tool 202 can evaluate an interface 218 of the wafer probe 210 and the CPC 206, the wafer probe 210, an interface 220 between IC testing device 214 and proximal ends 222 of probe members 208 of the wafer probe 210, and/or the IC testing device 214. Again, the compliant printed circuit 206 and the electrical devices 212 are preferably manufactured using Inkjet printing technology as previously described, rather than traditional PCB fabrication techniques.

**[0066]** Figure 6 is a schematic illustration of a diagnostic (test) system 250 with a first diagnostic tool 256 and a second diagnostic tool 252 in accordance with an embodiment of the present disclosure. The second diagnostic tool 252 can be merged with a dedicated IC testing device 254 and used in conjunction with the first diagnostic tool 256. The first diagnostic tool 256 functions as an interconnect a between wafer probe 258 and a wafer-level IC device 260. The second diagnostic tool 252 may comprise a compliant printed circuit 275 positioned to function as an electrical interconnect with proximal ends 264 of probe member 266. The compliant printed circuit 275 can be a flexible polymeric sheet 276 having a plurality of contact pads 282 constructed and arranged to form an electrical interconnect with proximal ends 264 of probe members 266 in the wafer probe 258 at a second interface 262.

**[0067]** In the diagnostic system of Figure 6, the second diagnostic tool 252 can evaluate the interface 262 between the dedicated IC testing device 254 and the proximal ends 264 of the probe members 266 in the wafer probe 258, while the first diagnostic tool 256 can evaluate the wafer probe 258, an interface 268 of a wafer-level IC device 260 and the wafer probe 258, and the wafer-level IC device 260. An electrical connection 270 can permit electrical devices 272A, 272B, 272C (collectively "272") on the second diagnostic tool 252 to interact with electrical devices 274A, 274B, 274C (collectively "274") on the first diagnostic tool 256 to provide additional functionality and cross-checking of the various diagnostic tests.

**[0068]** The electrical devices 272, 274 can be a variety of passive and active devices, such as for example, a power plane, a ground plane, a capacitor, a resistor, a battery, a filter, a signal or power altering and enhancing device, a memory device, an embedded integrated circuit, or a RF antennae. The electrical devices 272, 274 can be printed on either surface of the polymeric sheets 276, 278 using a printing technology as previously described. The test system 250 of Figure 6 can eliminate

the need for a separate test station 280 or can supplement the functionality of the test station 280.

**[0069]** Figure 7 is a schematic illustration of a diagnostic (test) system 300 including a first diagnostic tool 312 and a second diagnostic tool 302. The second diagnostic tool 302 can have a dedicated IC testing device 310 merged with a compliant printed circuit 306. The first diagnostic tool 312 can function as an interconnect between a wafer probe 314 and wafer-level IC device 316. A compliant printed circuit 318 of the first diagnostic tool 312 can include printed contact members 320 configured to electrically couple with contact pads 322 on the wafer-level IC device 316.

**[0070]** In the configuration of Figure 7, the second diagnostic tool 302 can evaluate the interface 330 of the IC testing device 310 and the wafer probe 314 and test the functionality of the wafer-level IC device 316. The first diagnostic tool 312 can evaluate the interface 334 between probe members 336 in the wafer probe 314 and the wafer-level IC device 316 and can also test the functionality of the wafer-level IC device 316. An electrical connection 340 can permit the electrical devices 342A, 342B, 342C (collectively "342") on the second diagnostic tool 302 to interact with electrical devices 344A, 344B, 344C (collectively "344") on the first diagnostic tool 312 to provide additional functionality and cross-checking of the various diagnostic tests.

**[0071]** Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the invention. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the invention.

**[0072]** Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the

practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

**[0073]** The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the embodiments of the present invention are not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

**[0074]** Other embodiments of the invention are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the invention, but as merely providing illustrations of some of the presently preferred embodiments of this invention. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the invention. Thus, it is intended that the scope of at least some of the present invention herein disclosed should not be limited by the particular disclosed embodiments described above.

**[0075]** Thus the scope of this invention should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be

encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A diagnostic tool for testing a wafer-level integrated circuit (IC) device coupled to testing electronics by a wafer probe, the diagnostic tool comprising:
  - a first compliant printed circuit comprising a plurality of contact pads configured to form an electrical interconnect at a first interface between distal ends of probe members in the wafer probe and contact pads on the wafer-level IC device;
  - a plurality of conductive traces printed on the first compliant printed circuit and electrically coupling to the plurality of contact pads; and
  - a plurality of electrical devices printed on the first compliant printed circuit at a position away from the first interface, the electrical devices coupled to the conductive traces and configured to provide one or more of continuity testing at the first interface or functionality testing of the wafer-level IC device.
2. The diagnostic tool of claim 1, wherein the conductive traces comprise substantially rectangular cross-sectional shapes.
3. The diagnostic tool of claim 1, wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer of the compliant printed circuit.
4. The diagnostic tool of claim 1, further comprising raised probe members printed on the compliant printed circuit in an array configured to electrically couple with the plurality of contact pads on the wafer-level IC device.
5. The diagnostic tool of claim 1, wherein the electrical devices comprise at least one of a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae.
6. The diagnostic tool of claim 1, wherein the first compliant printed circuit comprises one or more printed layers comprising one or more of a dielectric layer, a ground plane, or a power plane.
7. The diagnostic tool of claim 1, further comprising a second diagnostic tool coupled to an IC testing device and including a plurality of contact pads configured to form an electrical interconnect with proximal ends of the probe members in the wafer probe at a second interface.

8. The diagnostic tool of claim 7, wherein the IC testing device is programmed to provide one or more of continuity testing at the second interface, testing the first diagnostic tool, or testing the wafer-level IC device.

9. The diagnostic tool of claim 1, further comprising:

a dedicated IC testing device including a plurality of contact pads configured to form an electrical interconnect with proximal ends of the probe members in the wafer probe at a second interface;

a second compliant printed circuit electrically coupled to the dedicated IC device and having a plurality of printed conductive traces coupled to the plurality of contact pads on the dedicated IC testing device; and

a plurality of electrical devices printed on the second compliant printed circuit at a position away from the second interface, the electrical devices electrically coupled to the conductive traces on the second compliant printed circuit and configured to provide one or more of continuity testing at the second interface, functionality testing of the first diagnostic tool, or functionality testing of the wafer-level IC device.

10. The diagnostic tool of claim 9, wherein the second compliant printed circuit is electrically coupled with contact pads on the dedicated IC testing device using one or more of solder, wire bonding, and a compressive connection.

11. The diagnostic tool of claim 9, further comprising an electrical connection between the first diagnostic tool and the second diagnostic tool.

12. A diagnostic system for testing a wafer-level IC device coupled to testing electronics by a wafer probe, the diagnostic system comprising a first diagnostic tool comprising:

a dedicated IC testing device including a plurality of contact pads configured to form an electrical interconnect with proximal ends of probe members in the wafer probe at a first interface;

a first compliant printed circuit comprising a plurality of contact pads electrically coupled to the contact pads on the dedicated IC testing device and a plurality of printed conductive traces electrically coupled to the plurality of the contact pads of the first compliant printed circuit; and

a plurality of electrical devices printed on the first compliant printed circuit at a position away from the first interface, the electrical devices electrically coupled to the conductive traces and configured to provide one or more of continuity testing at the

first interface, continuity testing at a second interface between distal ends of the probe members in the wafer probe and the wafer-level IC device, or functionality testing of the wafer-level IC device.

13. The diagnostic system of claim 12, wherein the electrical devices comprise at least one of a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae.

14. The diagnostic system of claim 12, wherein the first compliant printed circuit comprises one or more printed layers comprising one or more of a dielectric layer, a ground plane, or a power plane.

15. The diagnostic system of claim 12, further comprising:

a second compliant printed circuit comprising a plurality of contact pads configured to form an electrical interconnect with distal ends of probe members in the wafer probe and contact pads on the wafer-level IC device at a second interface;

a plurality of printed conductive traces electrically coupled to the plurality of the contact pads on the second compliant printed circuit; and

a plurality of electrical devices printed on the second compliant printed circuit at a position away from the second interface, the electrical devices electrically coupled to the conductive traces on the second compliant printed circuit and adapted to provide one or more of continuity testing at the second interface or functionality testing of the wafer-level IC device.

16. The diagnostic system of claim 15, further comprising an electrical connection between the first diagnostic tool and the second diagnostic tool.

17. A method of making a first diagnostic tool for testing a wafer-level IC device coupled to testing electronics by a wafer probe, the method comprising the steps of:

printing a plurality of contact pads on a first compliant printed circuit, the contact pads configured to form an electrical interconnect at a first interface between distal ends of probe members in the wafer probe and contact pads on the wafer-level IC device;

printing a plurality of conductive traces electrically coupled to the plurality of contact pads on the first compliant printed circuit;

printing a plurality of electrical devices on the first compliant printed circuit at a position away from the first interface and in a manner such that the electrical devices are electrically coupled to the conductive traces;

positioning the first compliant printed circuit to form an electrical interconnect at the first interface; and

evaluating one or more of continuity at the first interface or functionality of one or more wafer-level IC devices.

18. The method of claim 17, wherein the conductive traces comprise substantially rectangular cross-sectional shapes.

19. The method of claim 17, further comprising printing a conductive material, a non-conductive material, and a semi-conductive material on a single layer of the compliant printed circuit.

20. The method of claim 17, further comprising printing one or more of a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae on the first compliant printed circuit.

21. The method of claim 17, further comprising printing one or more of a dielectric layer, a ground plane, or a power plane on the first compliant printed circuit.

22. The method of claim 17, further comprising a method of making a second diagnostic tool, the method comprising the steps of:

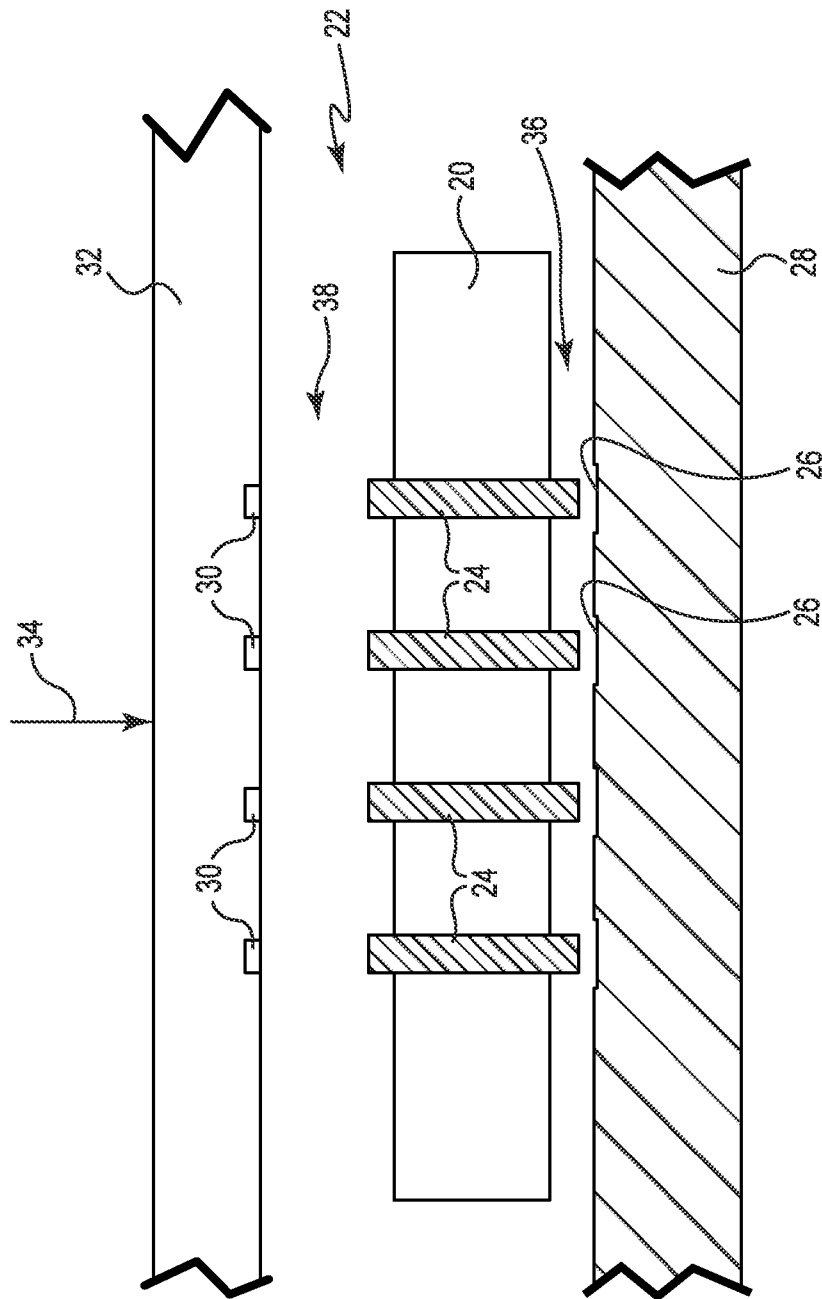
forming an electrical interconnect with proximal ends of the probe members and contact pads on a dedicated IC testing device at a second interface;

electrically coupling the dedicated IC testing device with a second compliant printed circuit;

printing a plurality of conductive traces to be electrically coupled to the dedicated IC device;

printing a plurality of electrical devices on the second compliant printed circuit at a position away from the second interface and such that the electrical devices are electrically coupled to the conductive traces on the second compliant printed circuit; and

evaluating one or more of continuity at the second interface, functionality of the first diagnostic tool, or functionality of the wafer-level IC device.



**Fig. 1**  
(Prior Art)



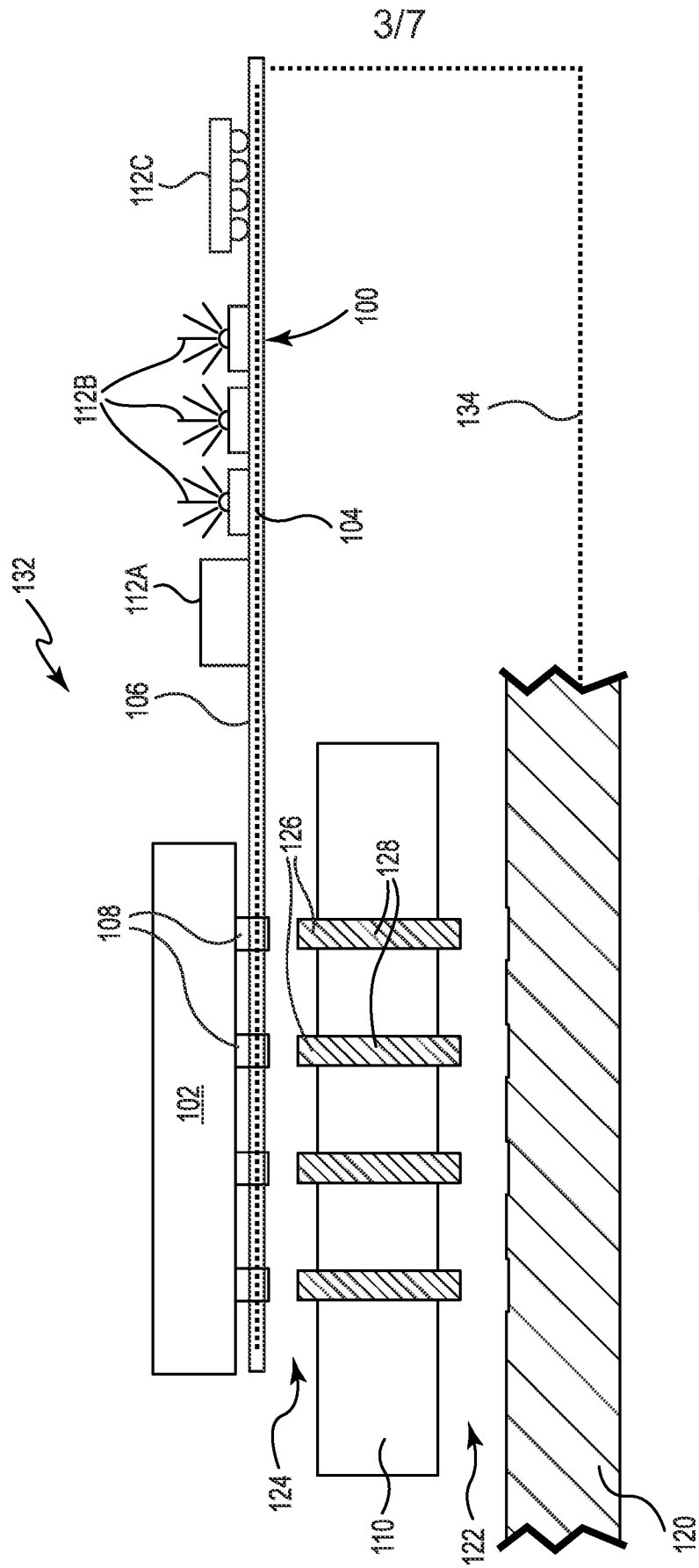


Fig. 3

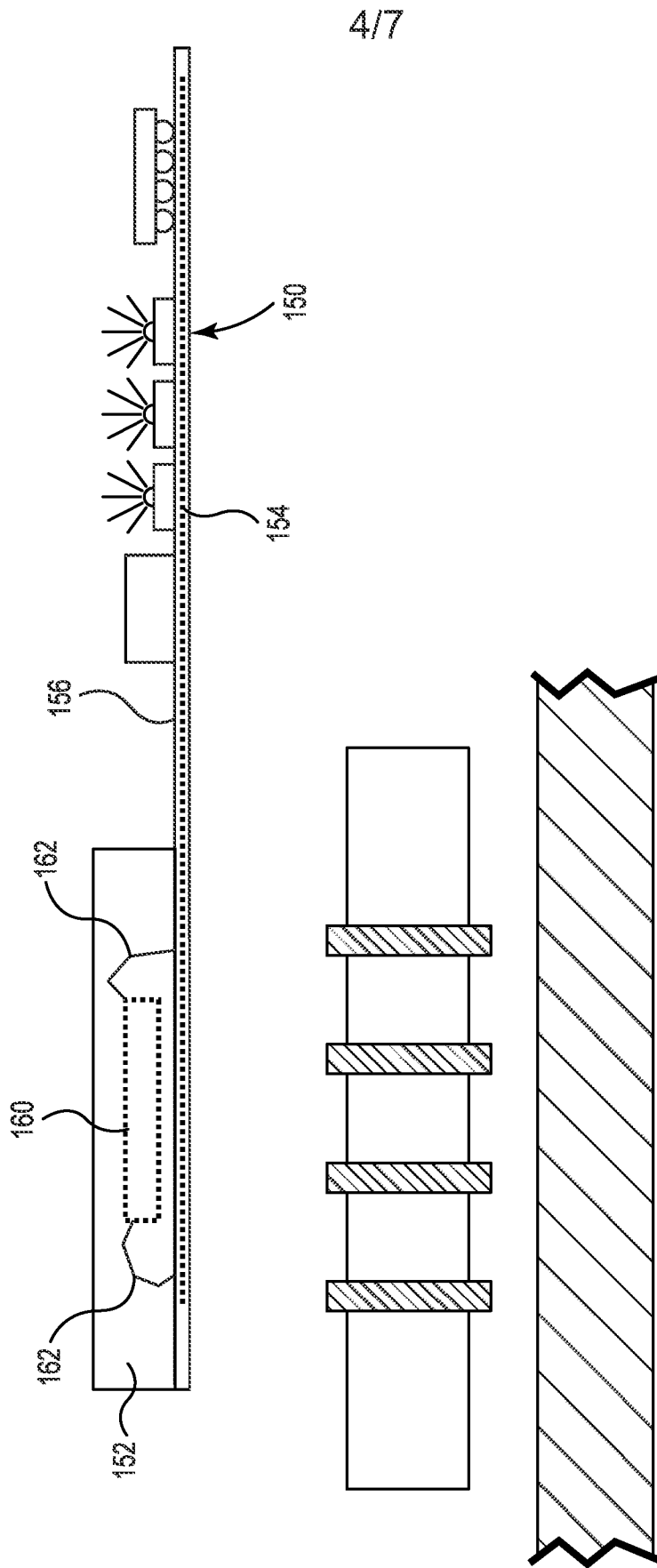


Fig. 4

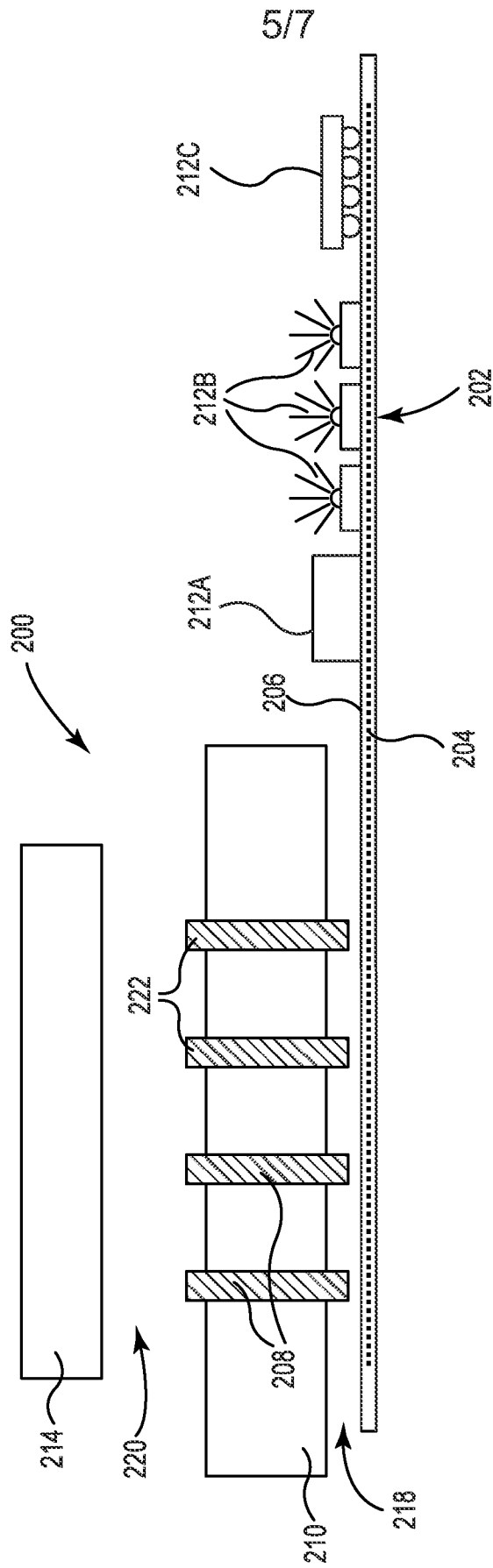


Fig. 5

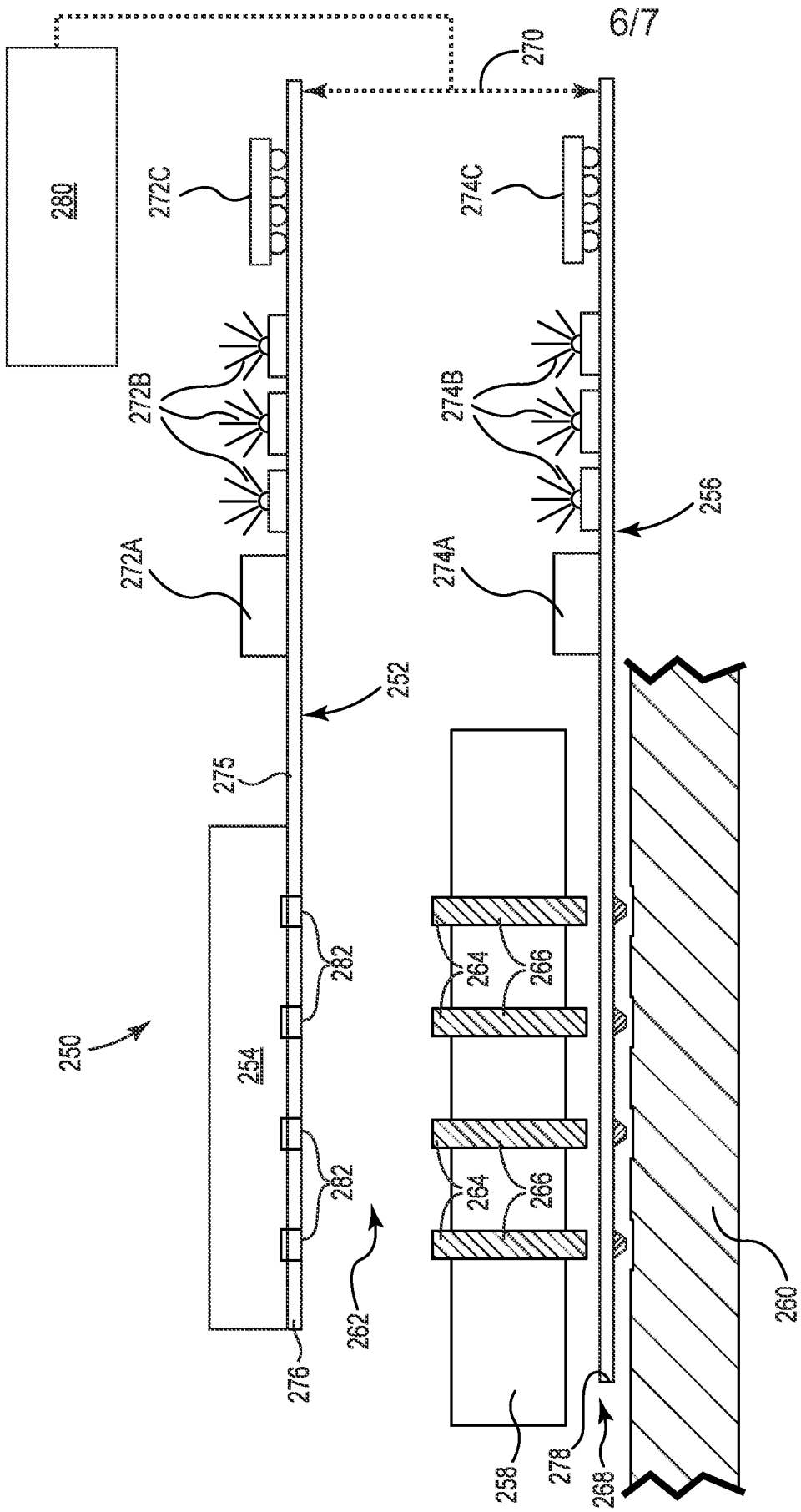


Fig. 6



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 10/36388

<p><b>A. CLASSIFICATION OF SUBJECT MATTER</b>                  IPC(8) - G01R 31/06 (2010.01)                  USPC - 438/17                  According to International Patent Classification (IPC) or to both national classification and IPC</p>														
<p><b>B. FIELDS SEARCHED</b></p> <p>Minimum documentation searched (classification system followed by classification symbols)                  USPC -- 438/17</p> <p>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched                  USPC: 438/612; 702/58</p> <p>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)                  PubWEST(PGPB, USPT, EPAB, JPAB):                  semiconductor, probe, diagnostic, test, conductive, metal, traces, wafer, IC, chip, contact pad, interconnect, foil, trace, trench, via, capacitor, memory, resistor</p>														
<p><b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b></p> <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>X ----- Y</td> <td>US 2008/0290885 A1 (Matsunami) 27 November 2008 (27.11.2008), entire document especially Abstract, paras [0030]-[0032], [0021], [0034], [0038], [0037], [0039], [0030]</td> <td>1, 3-17 and 19-22 ----- 2, 18</td> </tr> <tr> <td>Y</td> <td>US 5,378,981 A (Higgins, III), 03 January 1995 (03.01.1995), entire document especially Abstract, col 5, ln 35-41 and col 4, ln 1-5</td> <td>2, 18</td> </tr> <tr> <td>A</td> <td>US 2008/0265919 A1 (Izadian) 30 October 2008 (30.10.2008), entire document</td> <td>1-22</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	X ----- Y	US 2008/0290885 A1 (Matsunami) 27 November 2008 (27.11.2008), entire document especially Abstract, paras [0030]-[0032], [0021], [0034], [0038], [0037], [0039], [0030]	1, 3-17 and 19-22 ----- 2, 18	Y	US 5,378,981 A (Higgins, III), 03 January 1995 (03.01.1995), entire document especially Abstract, col 5, ln 35-41 and col 4, ln 1-5	2, 18	A	US 2008/0265919 A1 (Izadian) 30 October 2008 (30.10.2008), entire document	1-22
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<p><input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/></p>														
<p>* Special categories of cited documents:</p> <table border="0"> <tr> <td>"A" document defining the general state of the art which is not considered to be of particular relevance</td> <td>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>"E" earlier application or patent but published on or after the international filing date</td> <td>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>"O" document referring to an oral disclosure, use, exhibition or other means</td> <td>"&amp;" document member of the same patent family</td> </tr> <tr> <td>"P" document published prior to the international filing date but later than the priority date claimed</td> <td></td> </tr> </table>			"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family	"P" document published prior to the international filing date but later than the priority date claimed			
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"P" document published prior to the international filing date but later than the priority date claimed														
<p>Date of the actual completion of the international search                  26 July 2010 (26.07.2010)</p>		<p>Date of mailing of the international search report  <b>30 JUL 2010</b></p>												
<p>Name and mailing address of the ISA/US                  Mail Stop PCT, Attn: ISA/US, Commissioner for Patents                  P.O. Box 1450, Alexandria, Virginia 22313-1450                  Facsimile No. 571-273-3201</p>		<p>Authorized officer:                  Lee W. Young                  PCT Helpdesk: 571-272-4300                  PCT OSP: 571-272-7774</p>												