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(54) WIDE BANDGAP HEMTS WITH SOURCE CONNECTED FIELD PLATES

HEMTS MIT GROSSEM BANDABSTAND MIT SOURCE-VERBUNDENEN FELDPLATTEN

TRANSISTORS A HAUTE MOBILITE D'ELECTRONS A GRANDE LARGEUR DE BANDE INTERDITE COMPORTANT DES PLAQUES DE CHAMP RELIEES A LA SOURCE

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- **None**

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to high-electron mobility transistors and particularly to such transistors utilizing field plates.

Description of the Related Art

[0002] Improvements in the manufacturing of AlGaN/GaN semiconductor materials have helped advance the development of AlGaN/GaN transistors, such as high electron mobility transistors (HEMTs) for high frequency, high temperature and high power applications. AlGaN/GaN has large bandgaps, high peak and saturation electron velocity values [B. Gelmont, K. Kim and M. Shur, Monte Carlo Simulation of Electron Transport in Gallium Nitride, J.Appl.Phys. 74, (1993), pp. 1818-1821]. AlGaN/GaN HEMTs can also have 2DEG sheet densities in excess of $10^{13}cm^{-2}$ and relatively high electron mobility (up to 2019 cm^2/Vs) [R. Gaska, et al., Electron Transport in AlGaN-GaN Heterostructures Grown on 6H-SiC Substrates, Appl.Phys.Lett. 72, (1998), pp. 707-709]. These characteristics allow AlGaN/GaN HEMTs to provide very high voltage and high power operation at RF, microwave and millimeter wave frequencies.

[0003] AlGaN/GaN HEMTs have been grown on sapphire substrates and have shown a power density of 4.6 W/mm and a total power of 7.6 W [Y.F. Wu et al., GaN-Based FETs for Microwave Power Amplification, IEICE Trans. Electron. E-82-C, (1999). pp. 1895-1905]. More recently, AlGaN/GaN HEMTs grown on SiC have shown a power density of 9.8 W/mm at 8 GHz [Y.F. Wu, et al., Very-High Power Density AlGaN/GaN HEMTs, IEEE Trans.Electron.Dev. 48, (2001), pp. 586-590] and a total output power of 22.9 W at 9 GHz [M. Micovic, et al., AlGaN/GaN Heterojunction Field Effect Transistors Grown by Nitrogen Plasma Assisted Molecular Beam Epitaxy, IEEE Trans.Electron.Dev.48, (2001), pp. 591-596] .

[0004] U.S. Patent number 5,192,987 to Khan et al. discloses GaN/AlGaN based HEMTs grown on a buffer and a substrate. Other AlGaN/GaN HEMTs and field effect transistors (FETs) have been described by Gaska et al., High-Temperature Performance of AlGaN/GaN HFET's on SiC Substrates, IEEE Electron Device Letters, 18, (1997), pp. 492-494; and Ping et al., DC and Microwave Performance of High Current AlGaN Heterostructure Field Effect Transistors Grown on P-type SiC Substrates, IEEE Electron Devices Letters 19, (1998), pp. 54-56. Some of these devices have shown a gain-bandwidth product (f_T) as high as 67 gigahertz [K. Chu et al. WOCSEMMAD, Monterey, CA (February 1998)] and high power densities up to 2.84 W/mm at 10 GHz [G. Sullivan et al., High Power 10-GHz Operation of AlGaN HFET's in Insulating SiC, IEEE Electron Device Letters 19, (1998), pp. 198-200; and Wu et al., High Al-Content AlGaN/GaN MODFETs for Ultrahigh Performance, IEEE Electron Device Letters 19, (1998), pp. 50-53].

[0005] Electron trapping and the resulting difference between DC and RF characteristics have been a limiting factor in the performance of these devices. Silicon nitride (SiN) passivation has been successfully employed to alleviate this trapping problem resulting in high performance devices with power densities over 10W/mm at 10 Ghz. For example, U.S. Patent No. 6,586,781 discloses methods and structures for reducing the trapping effect in GaN-based transistors. However, due to the high electric fields existing in these structures, charge trapping is still an issue.

[0006] Field plates have been used to enhance the performance of GaN-based HEMTs at microwave frequencies [See S Kamalkar and U.K. Mishra, Very High Voltage AlGaN/GaN High Electron Mobility Transistors Using a Field Plate Deposited on a Stepped Insulator, Solid State Electronics 45, (2001), pp. 1645-1662]. These approaches, however, have involved a field plate connected to the gate of the transistor with the field plate on top of the drain side of the channel. This can result in a significant FP-to-drain capacitance and the field plate being connected to the gate adds additional gate-to-drain capacitance (Cgd) to the device. This can not only reduce gain, but can also cause instability due to poorer input-output isolation.

[0007] The publication of Saito W et al relates to design and demonstration of high breakdown voltage gain high electron mobility transistor (HEMT) using field plates structure for power electronics applications. The publication details are: Japanese journal of applied physics, 20040401 Japan Society of Applied Physics, JP - ISSN 0021-4922.

[0008] Published U.S. patent application no. 2002/1373118 discloses a field effect transistor structure that is formed with a body semiconductor layer having source , body, drift region and drain. An upper semiconductor layer is separated from the body by an oxide layer. The upper semiconductor layer is doped to have a gate region arranged over the body, a field plate region arranged over the drift region and at least one p-n junction forming at least one diode between the field plate region and the gate region. A source contact is connected to both the source and the field plate region. The connection between the source and the field plate does not run over the active area and at a vertical level higher than that of the field plate.

[0009] Published U.S. patent application no. 2003/222327 relates to a semiconductor device which includes a first-first conductivity type semiconductor layer having a cell region portion and a junction terminating region portion.

[0010] Published U.S. patent application no. 2002/005528 relates to a compound semiconductor device which includes a cap layer formed on a channel layer

and an insulating film formed on the cap layer, and a Γ-shaped gate electrode is provided in a gate recess opening, wherein an extension part of the Γ-shaped gate electrode extends over the insulating film toward a drain electrode, and the total thickness of the insulating film and the cap layer being is set such that the electric field formed right underneath the extension part of the gate electrode includes a component acting in a direction perpendicular to the substrate.

SUMMARY OF THE INVENTION

[0011] The present invention provides high electron-mobility transistors with a field plate connected to the source electrode, according to claim 1.

[0012] These and other further features and advantages of the invention would be apparent to those skilled in the art from the following detailed description, taking together with the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]

FIG. 1 is a plan view of one embodiment of a HEMT according to the present invention;
FIG. 2 is a sectional view of the HEMT in FIG. 1;
FIG. 3 is a plan view of another embodiment of a HEMT according to the present invention;
FIG. 4 is a sectional view of the HEMT in FIG. 3;
FIG. 5 is a table comparing the operating characteristics of a HEMT according to the present invention compared to a HEMT with no field plate and a HEMT with a gate connected field plate;
FIG. 6 is a chart showing the operating characteristics of a HEMT with a gate connected field plate;
FIG. 7 is a chart showing the operating characteristics of a HEMT with a source connected field plate;
FIG. 8 is a sectional view of a HEMT according to the present invention having a gamma shaped gate; and
FIG. 9 is a sectional view of a HEMT according to the present invention having a recessed gate.

DETAILED DESCRIPTION OF THE INVENTION

[0014] The field plate arrangements according to the present invention can be used with many different transistor structures, the invention, however, concerns a HEMT. Wide bandgap transistor structures generally include an active region, with metal source and drain electrodes formed in electrical contact with the active region, and a gate electrode formed between the source and drain electrodes for modulating electric fields within the active region. A spacer layer is formed above the active region. The spacer layer can comprise a dielectric layer, or a combination of multiple dielectric layers. A conductive field plate is formed above the spacer layer and extends a distance L_f from the edge of the gate electrode toward the drain electrode.

[0015] The field plate can be electrically connected to the source electrode. This field plate arrangement can reduce the peak electric field in the device, resulting in increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability. By having the field plate electrically connected to the source electrode, the reduced gain and instability resulting from gate connected field plates is reduced. When arranged according to the present invention, the shielding effect of a source-connected field plate can reduce C_{gd}, which enhances input-output isolation.

[0016] According to the present invention a high electron mobility transistor (HEMT) is used, which typically includes a buffer layer and a barrier layer on the buffer layer. A two dimensional electron gas (2DEG) layer/channel is formed at the junction between the buffer layer and the barrier layer. A gate electrode is formed on the barrier layer between source and drain electrodes.

[0017] According to the present invention, a spacer layer is formed on the barrier layer covering the barrier layer between the gate and drain electrode such that a field plate is formed on the spacer layer in electric isolation from the barrier layer. The spacer layer also covers the gate such that the field plate can overlap the gate while remaining in electrical isolation from the gate and the barrier layer. According to the invention the spacer layer covers the gate and the surface of the barrier layer between the gate and the source and drain electrodes. The spacer layer can comprise a dielectric layer, or a combination of multiple dielectric layers. Different dielectric materials can be used such as a SiN, SiO2, Si, Ge, MgOx, MgNx, ZnO, SiNx, SiOx, alloys or layer sequences thereof, or epitaxial materials as described below.

[0018] A conductive field plate is formed on the spacer layer and extends a distance L_f from the edge of the gate towards the drain electrode, with the field plate and gate electrode typically being formed during separate deposition steps. The field plate is also electrically connected to the source electrode.

[0019] It will be understood that when an element or layer is referred to as being "on", "connected to", "coupled to" or "in contact with" another element or layer, it can be directly on, connected or coupled to, or in contact with the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to", "directly coupled to" or "directly in contact with" another element or layer, there are no intervening elements or layers present. Likewise, when a first element or layer is referred to as being "in electrical contact with" or "electrically coupled to" a second element or layer, there is an electrical path that permits current flow between the first element or layer and the second element or layer. The electrical path may include capacitors, coupled inductors, and/or other elements that permit current flow even

without direct contact between conductive elements.

[0020] FIGs. 1 and 2 show one embodiment of a nitride based HEMT 10 according to the present invention which comprises a substrate 12 of silicon carbide, sapphire, spinet, ZnO, silicon, gallium nitride, aluminum nitride, or any other material capable of supporting growth of a Group-III nitride material. In some embodiments, the substrate 12 can comprise semi-insulating 4H-SiC commercially available from Cree, Inc. of Durham, NC.

[0021] A nucleation layer 14 can be formed on the substrate 12 to reduce the lattice mismatch between the substrate 12 and the next layer in the HEMT 10. The nucleation layer 14 should be approximately 1000 angstroms (Å) thick, although other thicknesses can be used. The nucleation layer 14 can comprise many different materials, with a suitable material being $Al_zGa_{1-z}N$ ($0<=z<=1$). The nucleation layer 14 can be formed on the substrate 12 using known semiconductor growth techniques such as Metal Oxide Chemical Vapor Deposition (MOCVD), Hydride Vapor Phase Epitaxy (HVPE), or Molecular Beam Epitaxy (MBE).

[0022] The formation of the nucleation layer 14 can depend on the material used for the substrate 12. For example, methods of forming a nucleation layer 14 on various substrates are taught in U.S. Patents 5,290,393 and 5,686,738. Methods of forming nucleation layers on silicon carbide substrates are disclosed in U.S. Patents 5,393,993, 5,523,589, and 5,739,554.

[0023] The HEMT 10 further comprises a high resistivity buffer layer 16 formed on the nucleation layer 14, with a suitable buffer layer 16 made of a Group III-nitride material such as $Al_{xG}a_yIn_{(1-x-y)}N$ ($0<=x<=1$, $0<=y<=1$, $x+y<=1$). In another embodiment according to the present invention the buffer layer 16 comprises a GaN layer that is approximately 2μm thick, with part of the layer doped with Fe.

[0024] A barrier layer 18 is formed on the buffer layer 16 such that the buffer layer 16 is sandwiched between the barrier layer 18 and the nucleation layer 14. Each of the buffer layer 16 and barrier layer 18 can comprise doped or undoped layers of Group III-nitride materials. The barrier layer 18 can comprise one or more layers of different materials such as InGaN, AlGaN, AlN, or combinations thereof. In one embodiment the barrier layer 18 comprises 0.8 nm of AlN and 22.5 nm of $Al_xGa_{1-x}N$ ($x\approx0.195$, as measured by photo luminescence). Exemplary structures are illustrated in U.S. Patent Nos. 6,316,793, 6,586,781, 6,548,333 and U.S. Published Patent Application Nos. 2002/0167023 and 2003/00020092. Other nitride based HEMT structures are illustrated in U.S. Patents 5,192,987 and 5,296,395. The buffer and barrier layers 16, 18 can be made using the same methods used to grow the nucleation layer 14. A two dimensional electron gas (2DEG) layer/channel 17 is formed at the heterointerface between the buffer and barrier layer 16, 18. Electric isolation between the devices is achieved with mesa etch or ion implementation outside the active area of the HEMT.

[0025] Metal source and drain electrodes 20, 22 are formed making ohmic contact through the barrier layer 18, and a gate 24 is formed on the barrier layer 18 between the source and drain electrodes 20, 22. Electric current can flow between the source and drain electrodes 20, 22 through a two-dimensional electron gas (2DEG) 17 induced at the heterointerface between the buffer layer 16 and the barrier layer 18 when the gate electrode 24 is biased at the appropriate level. The formation of source and drain ohmic contacts 20, 22 is described in detail in the patents and publications referenced above.

[0026] The source and drain electrodes 20, 22 can be made of different materials including but not limited to alloys of titanium, aluminum, gold or nickel. The gate 24 can also be made of different materials including but not limited to nickel, gold, platinum, titanium, chromium, alloys of titanium and tungsten, or platinum silicide. The gate 24 can have many different lengths, with a preferred gate length (L_g) being approximately 0.5 microns. As best shown in FIG. 1, the gate 24 is connected to and contacted at a gate electrode 28. As described below, in other transistor embodiments according to the present invention the gate 24 can be at least partially recessed in barrier layer 18.

[0027] A non-conducting spacer layer 26 is formed over the gate 24 and the surface of the barrier layer 18 between the gate 24 and the source and drain electrodes 20, 22. The spacer layer 26 can comprise a layer of non-conducting material such as a dielectric. Alternatively, it can comprise a number of different layers of dielectrics or a combination of dielectric layers. The spacer layer can be many different thicknesses, with a suitable range of thicknesses being approximately 0.05 to 2 microns.

[0028] Alternatively, and not falling under the scope of the claimed invention, the spacer layer 26 may be formed before device metallization, in which case the spacer layer 26 can comprise an epitaxial material such as a Group III nitride material having different Group III elements such as alloys of Al, Ga, or In, with a suitable spacer layer material being $Al_xGa_{1-x}N$ ($0\leq x\leq 1$). After epitaxial growth of the barrier layer 18, the spacer layer 26 can be grown using the same epitaxial growth method. The spacer layer 26 is then etched such that the gate 24, source electrode 20 and drain electrode 22 can be properly formed in contact with the buffer layer 18 and the 2DEG 17. A field plate can then be deposited on the spacer layer between the gate 24 and drain electrode 22. In those embodiments where the field plate overlaps the gate, an additional spacer layer of dielectric material should then be included at least partially over the gate to isolate the gate from the field plate.

[0029] A field plate 30 is formed on the spacer layer 26 between the gate 24 and the drain electrode 22, with the field plate 30 being in close proximity to the gate 24 but not overlapping it. A space between the gate 24 and field plate (L_{gf}) remains and should be wide enough to isolate from the field plate 30, while being small enough to maximize the field effect provided by the field plate 30.

If L_{gf} is too wide the field effect can be reduced. In one embodiment according to the present invention L_{gf} should be approximately 0.4 microns or less, although larger and smaller spaces can also be used.

[0030] The field plate 30 can extend different distances L_f from the edge of the gate 24, with a suitable range of distances for L_f being approximately 0.1 to 2 microns. The field plate 30 can comprise many different conductive materials with a suitable material being a metal, or combinations of metals, deposited using standard metallization methods. In one embodiment according to the present invention the field plate 30 comprises titanium/gold or nickel/gold.

[0031] The field plate 30 is electrically connected to the source electrode 20 and FIG. 1 shows two connection structures that can be used according to the present invention, although other connection structures can also be used. Conductive buses 32 can be formed on the spacer layer 26 to extend between the field plate 30 and the source electrode 20, which does not fall under the scope of the claimed invention, however. Different numbers of buses 32 can be used although the greater the number of buses the greater the unwanted capacitance that can be introduced by the buses and the busses 32 should cover less than all of the all of the topmost surface between gate 24 and source electrode 20. The buses should have a sufficient number so that current effectively spreads from the source electrode 20 into the field plate 30, while not covering too much of the HEMT's active region, with a suitable number of buses 32 being two.

[0032] According to the invention, the field plate 30 is electrically connected to the source electrode 20 through a conductive path 34 that does not run over the active regions of the HEMT 10, the field plate and the source electrode 20. As shown in FIG. 1, the field plate 30 extends beyond the width of the active area and the path 34 runs outside the active area of the HEMT at the side opposite the gate electrode 28. In alternative embodiments according to the present, invention, the conductive path could run outside the active area of the HEMT 10 on the side of the gate electrode 28, or the HEMT 10 could include two or more conductive paths running out the same or different sides of the HEMT 10.

[0033] After deposition of the field plate 30 and its connection to the source electrode 20, the active structure can be covered by a dielectric passivation layer (not shown), such as silicon nitride. Methods of forming the dielectric passivation layer are described in detail in the patents and publications referenced above.

[0034] FIGs. 3 and 4 show another embodiment of a HEMT 40 according to the present invention having many features that are similar to those in HEMT 10 of FIGs. 1 and 2. For the similar features the same reference numerals are used and the features are introduced without full description with the understanding that the description of the features above applies equally to the HEMT 40.

[0035] The HEMT 40 comprises a substrate 12, nucleation layer 14, buffer layer 16, 2DEG 17, barrier layer 18, source electrode 20, drain electrode 22, gate 24, spacer layer 26 and gate electrode 28. The HEMT 40 also comprises a field plate 42 that is formed on the spacer layer 26 primarily between the gate 24 and the drain electrode 22, but also overlapping a portion of the gate 24. For the HEMT 10 in FIGs. 1 and 2, L_{gf} is small, which can present some difficulties during fabrication. By having the field plate 42 overlap the gate 24 the HEMT 40 can be fabricated without having to meet the tolerances of L_{gf}. The overlapping section of the field plate 42, however, can introduce additional unwanted capacitance. In determining whether to use a field plate 30 or 42 the ease of manufacturing using field plate 42 must be balanced with the reduced capacitance provided by field plate 30.

[0036] The HEMT 40 also comprises either buses 44 or a conductive path 46 to electrically connect the field plate 42 to the source electrode 20, only the path 46 falling under the scope of the claimed invention. After deposition of the field plate 42 and its connection to the source electrode 20, the active structure can also be covered by a dielectric passivation layer (not shown), such as silicon nitride.

[0037] FIG. 5 shows a table 50 comparing the operating characteristics of GaN based HEMTs with no field plate to HEMTs having a field plate connected to the gate, and field plate connected to the source. The tests were conducted on HEMTs having a gate length (L_g) = 0.5 microns, field plate length (L_f) = 1.1 microns, and a device width (w) = 500 microns. HEMTs with source connected field plates exhibit improved maximum stable gain (MSG) and reduced reverse power transmission (S_{12}). Compared to the non field plate device, S_{12} of a HEMT with a gate connected field plate is increased by 71% at 4 GHz, while that of the device with a source connected field plate is actually reduced by 28%. The reduction in S_{12} for the latter in comparison with the non field plate device is attributed to the Faraday shielding effect by the grounded field plate. As a result, at 4 GHz the source connected field plate device exhibits a MSG 1.3 dB higher than the non field plate device and 5.2 dB higher than the gate connected field plate device. This advantage for source connected field plate devices was maintained at higher biases. Large signal performance was characterized by load-pull power measurement at 4 GHz. Both the gate connected field plate and source connected field plate devices outperformed the non field plate devices in both output power and power added efficiency (PAE) at 48V and above, while the source connected field plate devices consistently registered large signal gains 5-7 dB higher than that of the gate connected field plate devices.

[0038] FIG. 6 is a graph 60 showing the performance of a gate connected field plate device, and FIG. 7 is a graph 70 showing the performance of a source connected field plate device. Both field plate devices were able to operate at 118 V dc bias wherein tuning was optimized for the best combination of gain, PAE and output power at 3 dB compression (P_{3dB}). While both devices generate power densities of approximately 20 W/mm, the source

connected field plate device provides a 7 dB higher associated gain. With the achieved large-signal gain of 21 dB at 4 GHz and the estimated voltage swing of 224V, the voltage-frequency-gain product approaches 10 kV-GHz.

[0039] The source connected field plate arrangement according to the present invention can be used in many different HEMTs beyond those described above. For example, FIG. 8 shows another embodiment of a HEMT 80 according to the present invention that has many features similar to those in HEMTs 10 and 40, including a substrate 12, nucleation layer 14, buffer layer 16, 2DEG 17, barrier layer 18, source electrode 20, and drain electrode 22. HEMT 80, however, has a gamma (Γ) shaped gate 82 that is particularly adapted to high frequency operation. The gate length (L_g) is one of the important device dimensions in determining the speed of the device, and with higher frequency devices the gate length is shorter. Shorter gate length can lead to high resistance that can negatively impact high frequency operation. T-gates are commonly used in high frequency operation, but it can be difficult to achieve a well-coupled placement of a field plate with a T-gate.

[0040] The gamma gate 82 provides for low gate resistance and allows for controlled definition of the gate footprint. A spacer layer 84 is included that covers the gamma gate 82 and the surface of barrier layer 18 between the gamma gate 82 and the source and drain electrodes 20, 22. A space can remain between the horizontal portion of the gamma gate 82 and the top of the spacer layer 84. The HEMT 80 also includes a field plate 86 on the spacer layer 84 that overlaps that gamma gate 82, with the field plate 86 preferably deposited on the side of the gamma gate 82 not having a horizontal overhanging section. This arrangement allows for tight placement and effective coupling between the field plate 86 and the active layers below it. In other gamma gate embodiments the field plate can be similarly arranged to field plate 86, but instead of overlapping the gate, there can be a space between the edge of the gate and the field plate similar to space Lgf shown in FIG. 2.

[0041] The field plate 86 can be electrically connected to the source electrode 20 in many different ways. Because of the space between the lower surface of the horizontal section of the gate 82 and the spacer layer 84, it can be difficult to provide a conductive path directly between the field plate 86 and the source electrode 20. Instead, according to the invention a conductive path can be included between the field plate 86 and the source electrode 20 that runs outside the active area of the HEMT 80. Alternatively and not falling under the scope of the present invention, the gamma gate 82 can be completely covered by the spacer layer 84 with the space under the gate's horizontal section filled. Conductive paths can then run directly from the field plate 86 to the source electrode over the spacer layer 84. The active structure can then be covered by a dielectric passivation layer (not shown).

[0042] FIG. 9 shows still another HEMT 90 according to the present invention that can also be arranged with a source connected field plate. HEMT 90 also has many features similar to those in HEMTs 10 and 40 in FIGs. 1-4, including a substrate 12, nucleation layer 14, buffer layer 16, 2DEG 17, barrier layer 18, source electrode 20, and drain electrode 22. The gate 92, however, is recessed in the barrier layer 18, and is covered by a spacer layer 94. In other embodiments the bottom surface of the gate can be only partially recessed or different portions of the gate can be recessed to different depths in the barrier layer 18. A field plate 96 is arranged on the spacer layer 94 and is electrically connected to the source electrode 20 and the active structure can be covered by a dielectric passivation layer (not shown).

[0043] The embodiments above provide wide bandgap transistors, particularly HEMTs, with improved power at microwave and millimeter wave frequencies. The HEMTs exhibit simultaneous high gain, high power, and more stable operation due to higher input-output isolation. The structure could be extended to larger dimensions for high voltage applications at lower frequencies.

[0044] Although the present invention has been described in considerable detail with reference to certain preferred configurations thereof, other versions are possible. The field plate arrangement can be used in many different devices. The field plates can also have many different shapes and can be connected to the source electrode in many different ways. The scope of the invention, however, is only defined by the appended claims.

Claims

1. A high electron mobility transistor (HEMT) (10) comprising:

an active area comprising a plurality of active semiconductor layers (16,18) having a top surface, said plurality of active semiconductor layers (16, 18) on a substrate (12), wherein said plurality of active semiconductor layers comprises a buffer layer (16) and a barrier layer (18), and wherein said HEMT (10) is configured to induce a two dimensional electron gas (2DEG) (17) at a heterointerface between the buffer layer (16) and the barrier layer (18) of said HEMT;

source (20) and drain (22) electrodes on said active semiconductor layers and in electrical contact with said 2DEG;

a gate (24) between said source and drain electrodes and on said active semiconductor layers;

a spacer layer (26) covering said gate and all of said top surface of said active semiconductor layers between said gate and said source electrode, and between said gate and said drain electrode; and **characterised in that** the HEMT

further comprises
a field plate (30) on said spacer layer isolated from the active semiconductor layers and extending a distance (L_f) from said gate toward said drain electrode, said field plate comprising a portion extending beyond the width of said active area, said field plate electrically connected to said source electrode by a conductive path (34, 46), said conductive path connected to said field plate at said portion extending beyond the width of said active area, said conductive path running entirely outside of said active area, wherein said conductive path does not extend over said active area.

2. The HEMT of claim 1, further comprising a second conductive path, said second conductive path running outside of said active area at a same or different side of said active area as the first conductive path.

3. The HEMT of claim 1, wherein said spacer layer provides electrical isolation between said active semiconductor layers and said field plate.

4. The HEMT of claim 1, wherein said field plate at least partially overlaps said gate.

5. The HEMT of claim 1, wherein said spacer layer comprises a dielectric material, or multiple layers thereof.

6. The HEMT of claim 1, further comprising a nucleation layer (14) between said substrate and said buffer layer.

7. The HEMT of claim 1, wherein said field plate reduces the peak operating electric field in said HEMT.

Patentansprüche

1. Transistor (10) mit hoher Elektronenmobilität (HEMT), umfassend:

einen aktiven Bereich, umfassend eine Vielzahl von aktiven Halbleiterschichten (16, 18), welche eine obere Fläche aufweisen, wobei die Vielzahl von aktiven Halbleiterschichten (16, 18) auf einem Substrat (12), wobei die Vielzahl von aktiven Halbleiterschichten eine Pufferschicht (16) und eine Grenzschicht (18) umfasst, und
wobei der HEMT (10) dazu konfiguriert ist, ein zweidimensionales Elektronengas (2DEG) (17) an einer Heteroschnittstelle zwischen der Pufferschicht (16) und der Grenzschicht (18) des HEMT zu induzieren;
Source- (20) und Drain (22)-Elektroden auf den aktiven Halbleiterschichten, welche in elektrischem Kontakt mit dem 2DEG stehen;
ein Gate (24) zwischen den Source- und Drain-Elektroden und auf den aktiven Halbleiterschichten;
eine Abstandsschicht (26), welche das Gate und alle oberem Fläche der aktiven Halbleiterschichten zwischen dem Gate und der Source-Elektrode und zwischen dem Gate und der Drain-Elektrode bedeckt; und **dadurch gekennzeichnet, dass** der HEMT ferner Folgendes beinhaltet
eine Feldplatte (30) auf der Abstandsschicht, welche von den aktiven Halbleiterschichten isoliert ist und welche sich über eine Entfernung (L_f) von dem Gate in Richtung der Drain-Elektrode erstreckt, wobei die Feldplatte einen Teil umfasst, welcher sich über die Breite des aktiven Bereichs erstreckt, wobei die Feldplatte mit der Source-Elektrode durch eine Leiterbahn (34, 46) elektrisch verbunden ist, wobei die Leiterbahn mit der Feldplatte an dem Teil verbunden ist, welcher sich über die Breite des aktiven Bereichs erstreckt, wobei die Leiterbahn komplett außerhalb des aktiven Bereichs verläuft, wobei die Leiterbahn sich nicht über den aktiven Bereich erstreckt.

2. HEMT nach Anspruch 1, ferner umfassend eine zweite Leiterbahn, wobei die zweite Leiterbahn außerhalb des aktiven Bereichs an einer gleichen oder unterschiedlichen Seite des aktiven Bereichs als die erste Leiterbahn verläuft.

3. HEMT nach Anspruch 1, wobei die Abstandsschicht eine elektrische Isolation zwischen den aktiven Halbleiterschichten und der Feldplatte bereitstellt.

4. HEMT nach Anspruch 1, wobei die Feldplatte das Gate mindestens teilweise überlappt.

5. HEMT nach Anspruch 1, wobei die Abstandsschicht ein dielektrisches Material oder viele Schichten davon umfasst.

6. HEMT nach Anspruch 1, ferner umfassend eine Nukleierungsschicht (14) zwischen dem Substrat und der Pufferschicht.

7. HEMT nach Anspruch 1, wobei die Feldplatte das elektrische Spitzenbetriebsfeld im in dem HEMT reduziert.

Revendications

1. Transistor à haute mobilité d'électrons (HEMT) (10) comprenant :

une zone active comprenant une pluralité de

couches semi-conductrices actives (16, 18) ayant une surface supérieure, ladite pluralité de couches semi-conductrices actives (16, 18) étant sur un substrat (12), dans lequel ladite pluralité de couches semi-conductrices actives comprend une couche tampon (16) et une couche barrière (18), et

dans lequel ledit HEMT (10) est configuré pour induire un gaz électronique bidimensionnel (2DEG) (17) au niveau d'une hétéro-interface entre la couche tampon (16) et la couche barrière (18) dudit HEMT ;

des électrodes de source (20) et de drain (22) sur lesdites couches semi-conductrices actives et en contact électrique avec ledit 2DEG ;

une grille (24) entre lesdites électrodes de source et de drain et sur lesdites couches semi-conductrices actives ;

une couche d'espacement (26) recouvrant ladite grille et la totalité de ladite surface supérieure desdites couches semi-conductrices actives entre ladite grille et ladite électrode de source et entre ladite grille et ladite électrode de drain ; et **caractérisé en ce que** le HEMT comprend en outre

une plaque de champ (30) sur ladite couche d'espacement, isolée des couches semi-conductrices actives et s'étendant sur une distance (L_f) à partir de ladite grille vers ladite électrode de gain, ladite plaque de champ comprenant une partie s'étendant au-delà de la largeur de ladite zone active, ladite plaque de champ étant connectée électriquement à ladite électrode de source par un chemin conducteur (34, 46), ledit chemin conducteur étant connecté à ladite plaque de champ au niveau de ladite partie s'étendant au-delà de la largeur de ladite zone active, ledit chemin conducteur circulant totalement à l'extérieur de ladite zone active, dans lequel ledit chemin conducteur ne s'étend par sur ladite zone active.

2. HEMT selon la revendication 1, comprenant en outre un second chemin conducteur, ledit second chemin conducteur circulant à l'extérieur de ladite zone active sur un côté identique ou différent de ladite zone active par rapport au premier chemin conducteur.

3. HEMT selon la revendication 1, dans lequel ladite couche d'espacement fournit une isolation électrique entre lesdites couches semi-conductrices actives et ladite plaque de champ.

4. HEMT selon la revendication 1, dans lequel ladite plaque de champ chevauche au moins partiellement ladite grille.

5. HEMT selon la revendication 1, dans lequel ladite couche d'espacement comprend un matériau diélectrique, ou de multiples couches de celui-ci.

6. HEMT selon la revendication 1, comprenant en outre une couche de nucléation (14) entre ledit substrat et ladite couche tampon.

7. HEMT selon la revendication 1, dans lequel ladite plaque de champ réduit le champ électrique de fonctionnement de crête dans ledit HEMT.

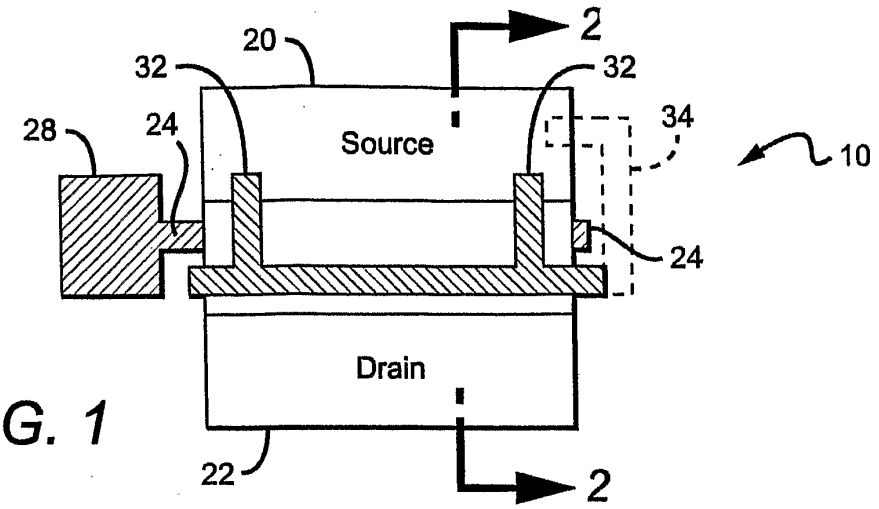
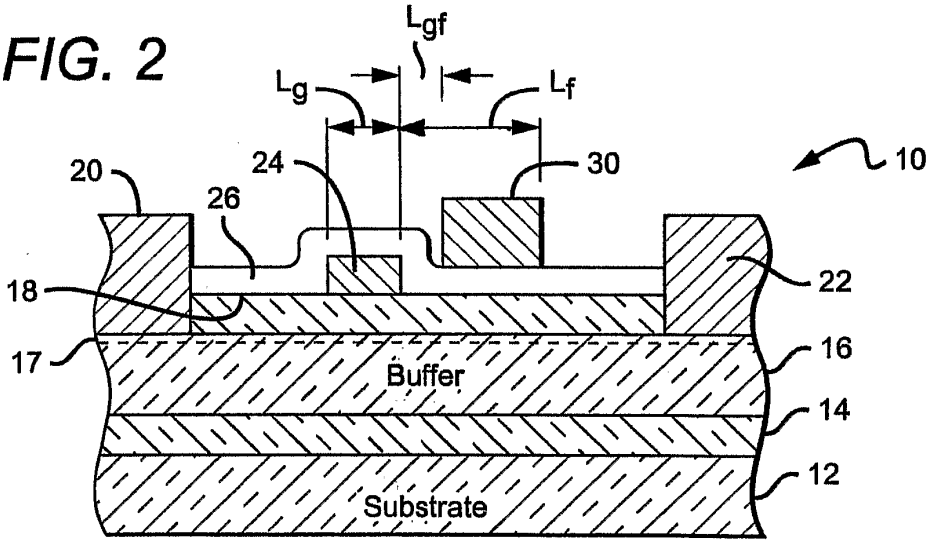


FIG. 1

FIG. 2



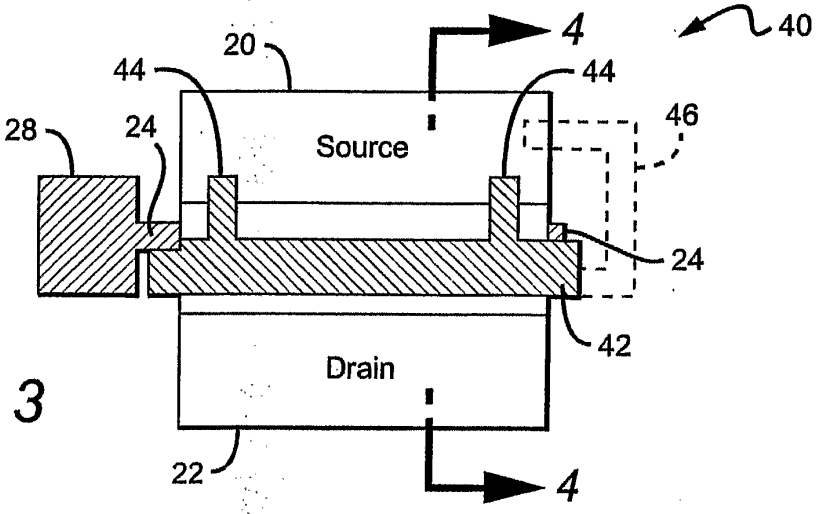


FIG. 3

FIG. 4

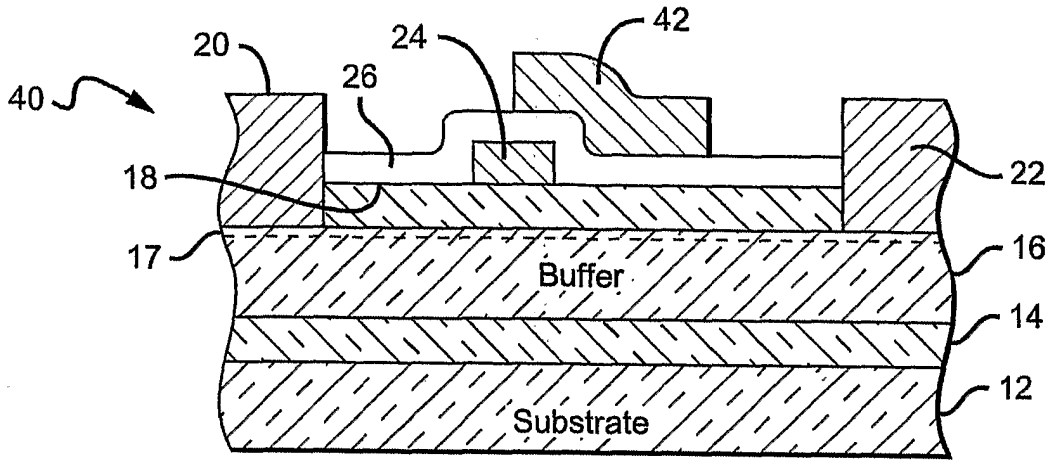


FIG. 5

50

	No FP	No FP connected to gate	FP connected to source
MSG at 4 GHz (dB)	18.6	14.7	19.9
S12 4 GHz	0.0795	0.136	0.0572
S12 compared to none- FP device (%)	100%	171%	72%

FIG. 6

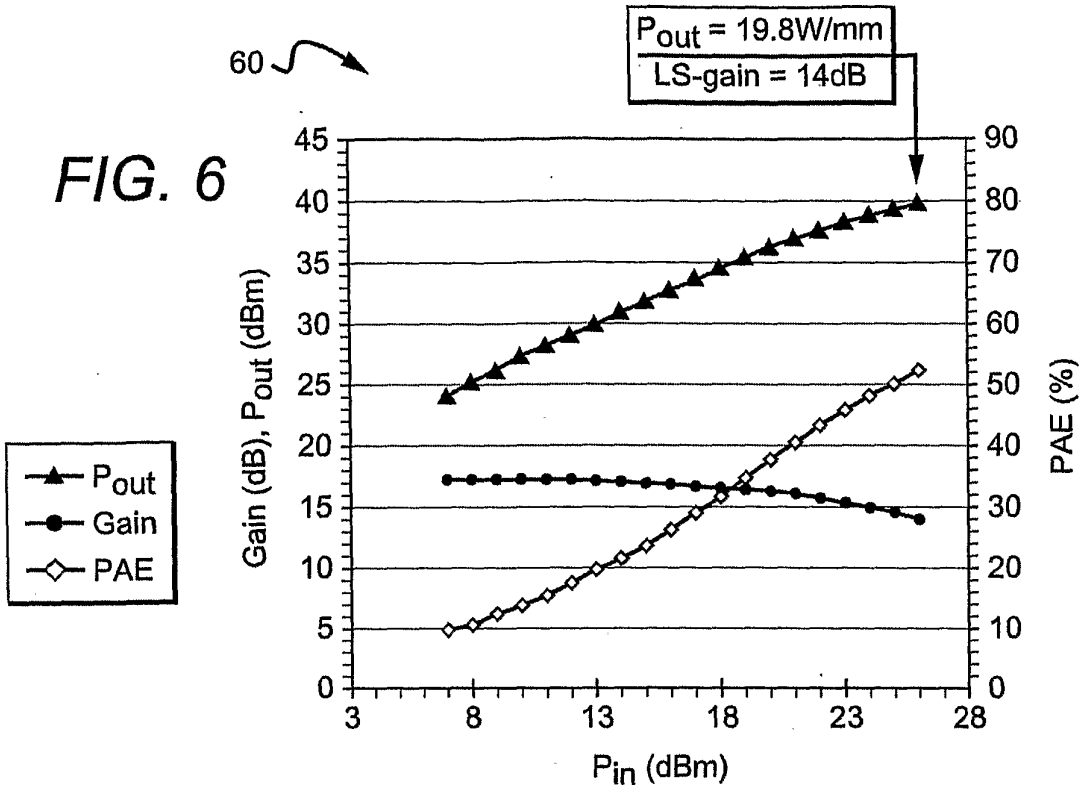

60
Pout = 19.8W/mm
LS-gain = 14dB
Pout
Gain
PAE
Gain (dB), Pout (dBm)
PAE (%)
Pin (dBm)
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
80
90
3
8
13
18
23
28

FIG. 7

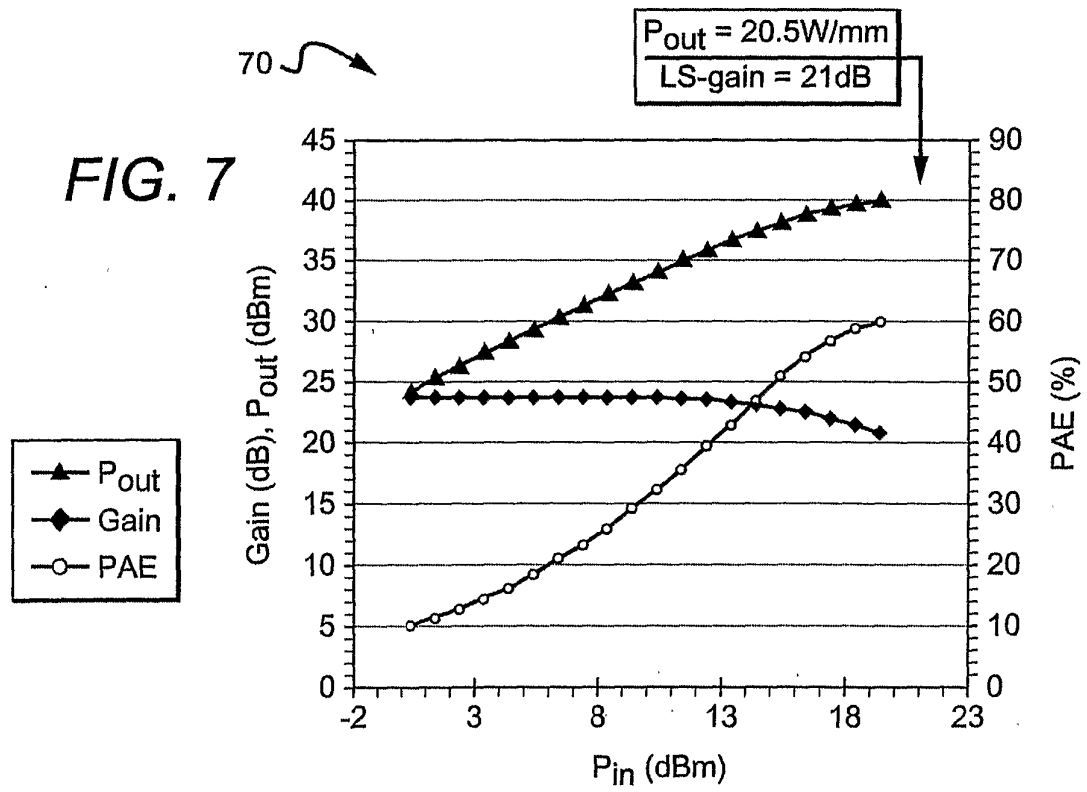

70
Pout = 20.5W/mm
LS-gain = 21dB
Pout
Gain
PAE
Gain (dB), Pout (dBm)
PAE (%)
Pin (dBm)
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
80
90
-2
3
8
13
18
23

FIG. 8

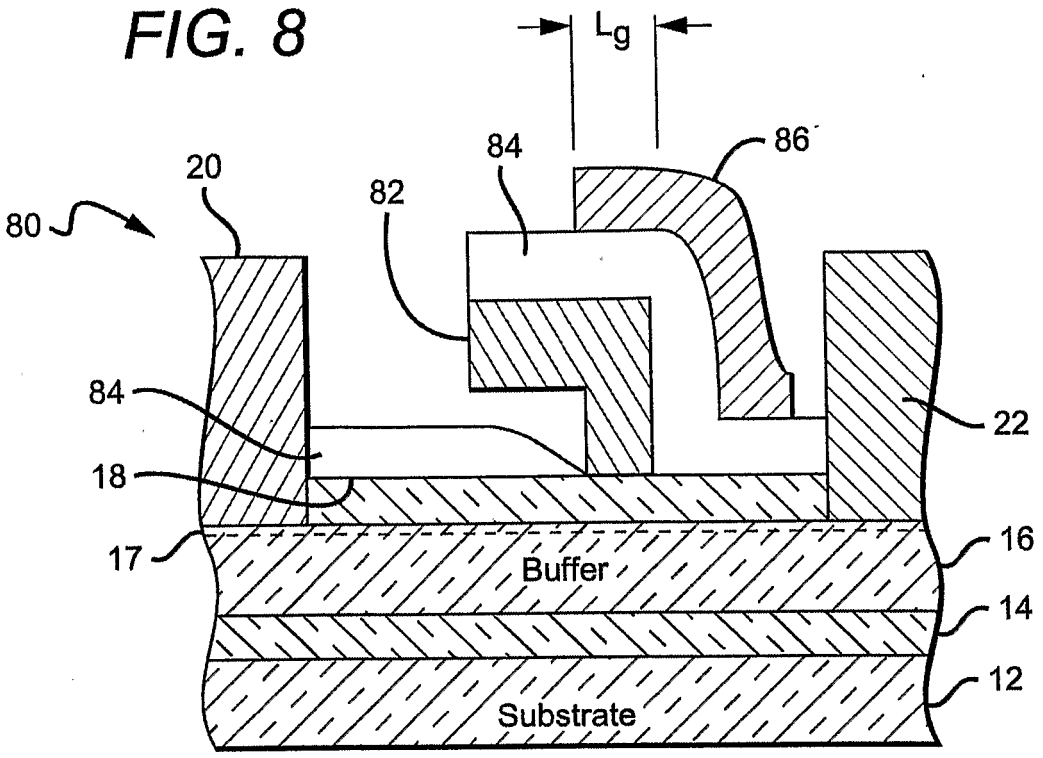
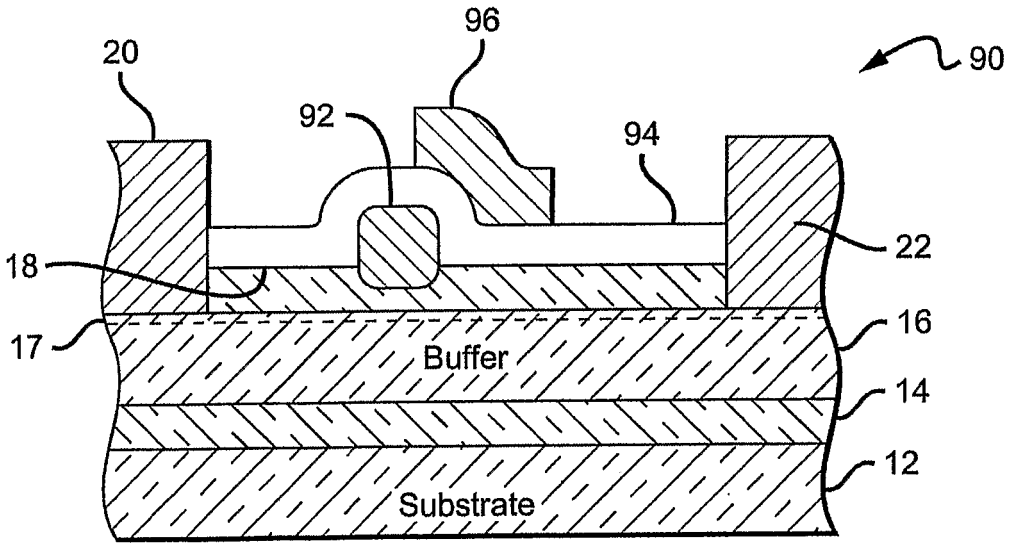

Lg
84
86
20
82
80
84
22
18
16
17
Buffer
14
12
Substrate

FIG. 9


96
20
90
92
94
22
18
16
17
Buffer
14
12
Substrate

REFERENCES CITED IN THE DESCRIPTION

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