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(12) (19) (CA) **Brevet-Patent**

(11) (21) (C) **2,036,595**
(22) 1991/02/19
(43) 1991/08/20
(45) 2000/08/08

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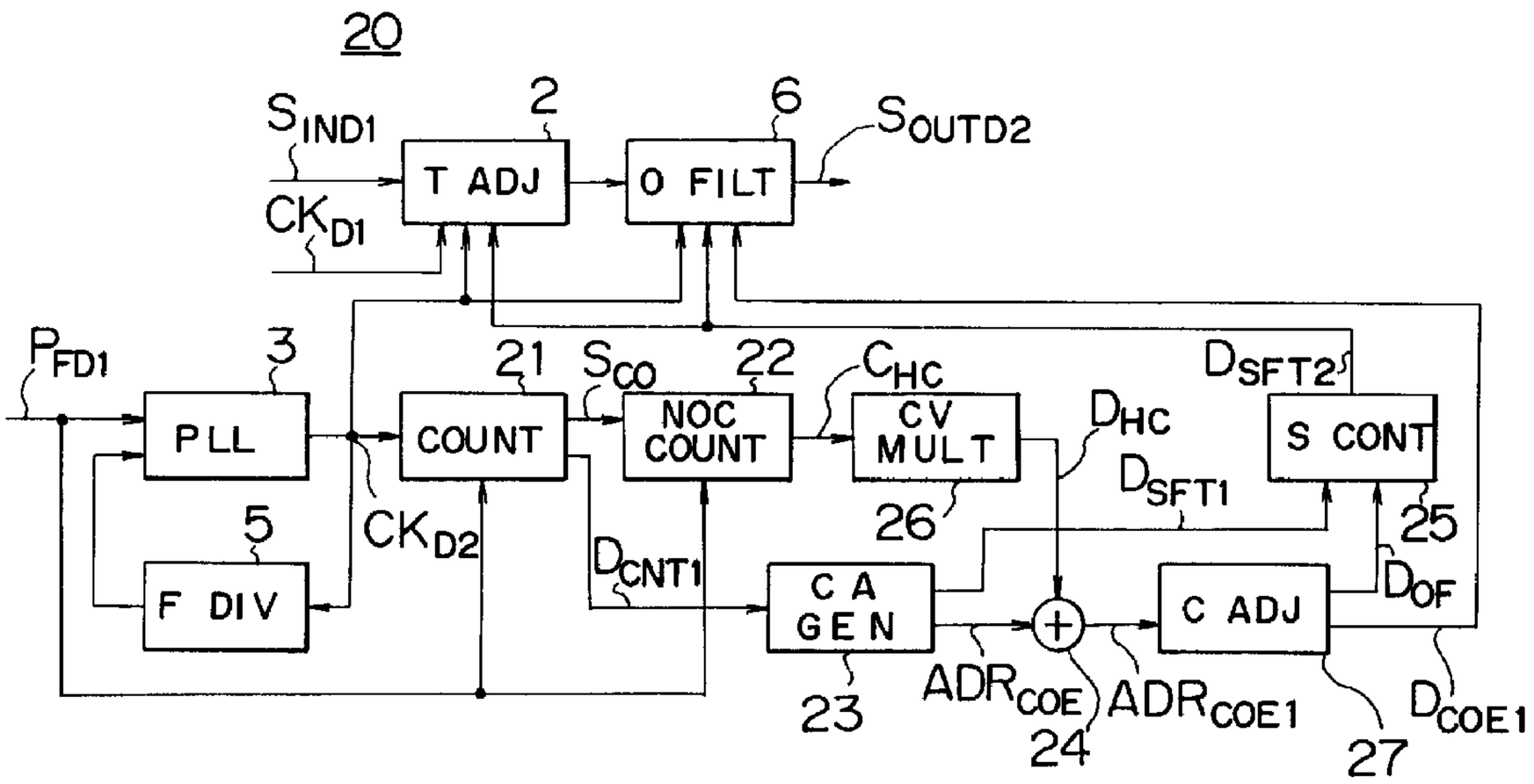
(51) Int.Cl.[5] H03K 5/135, H04N 7/01
(30) 1990/02/19 (039010/90) JP

(54) **CONVERTISSEUR DE FREQUENCE D'ECHANTILLONNAGE POUR SIGNAUX A TAUX D'ECHANTILLONNAGE PARTIEL**

(54) **SAMPLING RATE CONVERTER FOR SIGNALS HAVING A NON-INTEGER SAMPLING RATIO**



(57) In a sampling rate converter which converts a sampling frequency of digital signals sampled at a first sampling frequency into a second sampling frequency, output clocks corresponding to the second sampling frequency are counted in a cyclic fashion from an initial value to a maximum value based on periodicity of the first and second sampling frequencies. Coefficient addresses are generated in accordance to the resulting count value and a coefficient correction value in accordance with a number of counts of the maximum value and the periodicity of the first and second sampling frequencies, the number of the maximum value which is a number of times of counting to the maximum value. The sampling frequency of digital signals sampled at the first sampling frequency is thus converted into the second sampling frequency with a simple construction of counting to the maximum value in accordance to the periodicity of the sampling frequencies.

ABSTRACT OF THE DISCLOSURE

In a sampling rate converter which converts a sampling frequency of digital signals sampled at a first sampling frequency into a second sampling frequency, output clocks corresponding to the second sampling frequency are counted in a cyclic fashion from an initial value to a maximum value based on periodicity of the first and second sampling frequencies. Coefficient addresses are generated in accordance to the resulting count value and a coefficient correction value in accordance with a number of counts of the maximum value and the periodicity of the first and second sampling frequencies, the number of the maximum value which is a number of times of counting to the maximum value. The sampling frequency of digital signals sampled at the first sampling frequency is thus converted into the second sampling frequency with a simple construction of counting to the maximum value in accordance to the periodicity of the sampling frequencies.

SAMPLING RATE CONVERTER FOR SIGNALS HAVING A NON-INTEGER SAMPLING RATIO

BACKGROUND OF THE INVENTION

This present invention relates to a sampling rate converter, and is suitably applied to a case where a sampling frequency of component digital video signals based on D-1(625/50) format is converted to a sampling frequency corresponding to composite digital video signals based on D-2 format, for example.

Heretofore, there used to be a sampling rate converter which is constituted by a digital filter for converting digital signals, which are obtained by sampling analog signals at a predetermined frequency, to an arbitrary sampling frequency.

Such a sampling rate converter is constituted by a high order oversampling filter to strictly observe the Nyquist frequency as a conversion characteristic of the transmission system.

In FIGS. 1A-1D, roughly illustrated is an operation of a sampling rate converter constructed by an oversampling filter having for example. In such an oversampling filter, input digital signals (indicated by character in FIG. 1A) are inputted to the

oversampling filter, the input digital signals being provided by sampling imaginary analog signals S_{VT} as shown in FIG. 1A at a first sampling frequency f_1 (FIG. 1B).

Subsequently, the oversampling filter oversamples input digital signals at a frequency f_{11} 11 times larger as shown in FIG. 1C as well as resamples them at a second sampling frequency f_2 (FIG. 1D)to obtain output digital signals which have values indicated by characters □ in FIG. 1A and are rate converted into frequency f_2.

When a sampling frequency of component digital video signals based on D-1(625/50), format in digital video tape recorder (DVTR) is converted into a sampling frequency corresponding to PAL composite digital video signals based on the D-2(PAL) format, it is not possible to directly convert sampling frequency between digital video signals since the sampling frequency is rate converted from a frequency 13.5 MHz to a frequency 17.734475 MHz. It is thus necessary to build an oversampling filter having approximately a length of an order of about 16500.

Also in the converse case where a sampling frequency of PAL composite digital video signals is

converted into a sampling frequency corresponding to 625/50 component digital video signals, it is necessary to build an oversampling filter in the same circuit scale as the above described case since the sampling frequency is rate converted from a frequency 17.734475 MHz to a frequency 13.5 MHz. It is thus inevitable that the overall circuit scale becomes complicated and large sized.

To solve such a problem, a sampling rate converter has been proposed in which a oversampling filter reduced the circuit scale is built so that on the basis of the relationship of sampling frequencies 13.5 MHz and 17.734475 MHz between 625/50 component digital video signals and PAL composite digital video signals, a oversampling frequency is set, and filter coefficients input changeably to one multiplier corresponding to a magnification of the oversampling to weight the sampling data.

FIG. 2 illustrates a basic construction of a sampling rate converter 1 having changeable coefficient. In a case where in a sampling rate converter 1 as shown in FIG. 2, a sampling frequency of 625/50 component digital video signals is converted into a sampling frequency corresponding to PAL

composite digital video signals, for example, 625/50 component digital video signals S_{IND1} and output clock signals CK_{D1} corresponding to the sampling frequency thereof are inputted to the timing adjusting circuit 2.

This timing adjusting circuit 2 outputs data of the 625/50 component digital video signals S_{IND1} inputted at the rate of the clock signal CK_{D1} at the timing of the rate of the clock signal CK_{D2} so as to exchange the clock as well as control the timing of the data transference described below.

In addition to this, frame pulses P_{FD1} corresponding to one frame of 625/50 component digital video signals S_{IND1} are inputted to reset terminals of a phase locked loop (PLL) circuit 3 and a counter 4.

The output of PLL circuit 3 is feedbacked through a frequency divider 5 with a dividing ratio (= 1/709379) corresponding to the number of samples of one frame (= 709379) of PAL composite digital video signals.

This enables the PLL circuit 3 to correctly synchronize with frame pulses P_{FD1} of 625/50 component digital video signals, and the PLL circuit 3 generates output clock signals CK_{D2} corresponding to the sampling frequency of the PAL composite digital video signals

and supplies them to a count input terminal of a counter 4, the timing adjusting circuit 2 and an oversampling filter 6.

The counter 4 is reset according to frame pulses P_{FD1}, and counts output clock signals CK_{D2}, inputted from the PLL circuit 3, every frame. Consequently, count data D_{CNT} which is zero to 709378 is sequentially sent to a coefficient address control circuit 7.

The coefficient address control circuit 7 generates coefficient address data D_{COE} according to the count data D_{CNT} to read coefficients C_{OEF}, C_{OEFB}, ... from coefficient generating circuits 9A, 9B, ... which are ROM (read only memories), the coefficients C_{OEFA}, C_{OEFB}, ... being to fed to multipliers 8A, 8B, ... which are weighting means of the oversampling filter 6 of which part is illustrated in FIG. 3.

The relationship between coefficients C_{OEFA}, C_{OEFB}, ... supplied to the multipliers 8A, 8B, ... and the coefficient address data D_{COE} is illustrated schematically in FIG. 4. In FIG. 4, a longitudinal" axis represents the coefficient C_{OEF} and lateral axis represents the coefficient address data D_{COE}. The lateral axis also be able to see as a time axis. "N"

is the order of the oversampling filter and is derived from the characteristic of the oversampling filter required. An impulse response characteristic of the oversampling filter is formed by N groups of the coefficient C_{OFF}. It is not that a practical impulse response characteristic is illustrated in FIG. 4, it is illustrated schematically.

"M" represents numbers of division between sampling points to the input signal S_{IND1}, that is a resolution capability, by which the oversampling frequency is decided. The groups of coefficient are divided by M groups so as to store them in the coefficient generating circuits 9A, 9B, ... the number of which are M/N. The address $a_0 \ldots a_n$, $b_0 \ldots b_n$ are apointed with a coefficient address data D_{COE} generated at the rate of the clock signal CK_{D2} in the coefficient address control circuit so that the groups of coefficient C_{OEF} stored is read out.

The relationship between the count data D_{CNT} and the address of the coefficient generating circuits 9A, 9B, ... apointed with the coefficient address data D_{COE} is illustrated in FIG. 5. In the case illustrated in FIG. 5, the oversampling filter is constructed with orders N = 4554, M = 506. The coefficients which form

the impulse response characteristic of the oversampling filter are stored in sequence at the addresses from a_0, b_0, ... i_0 to a_{505}, b_{505}. In the under portion of FIG. 5, the coefficient addresses D_{COE} which are generated at the timings of each of the count data D_{CNT} are illustrated. In FIG. 5, with the count data D_{CNT} exchanged in sequence n, n+1, n+2, ... at the rate of clock signal CK_{D2}, the coefficient address data D_{COE} is generated so that the addresses $a_0 - a_{505}$, $b_0 - b_{505}$, $c_0 - c_{505}$, ... are apointed in sequence [a_0, b_0, c_0, ...], [a_{386}, b_{386}, c_{386}, ...], [a_{266}, b_{266}, c_{266}, ...], ...

The apointment of the address in each of the coefficient generating circuit is performed on the basis of the relationship between the sampling period of 625/50 component digital video signal and the sampling period of PAL composite digital video signal so as to shift by 386 addresses cyclicly among addresses 0 - 505 as following equation.

$$506 * \frac{13.5}{17.7} = 386 \quad \ldots (1)$$

The coefficients C_{OEFA} - C_{OEFI} generated in the coefficient generating circuit 9A - 9I are multiplied by the output data in the multiplier. When the count data D_{CNT} becomes predetermined values, for instance D_{CNT} becoming $D_{CNT} = n + 1$ in FIG. 5, it is necessary to multiply a coefficient corresponding to $D_{CNT} = n + 1$ by the same data as the flip-flop output data multiplied at the timing $D_{CNT} = n$. In this case, the coefficient address control circuit 7 generates a shift control signal D_{SFT} to stop the data transference in the flip-flop circuits 10A - 10I(this means having shifted one block data) so as to be able to multiply in the multiplier using the same flip-flop output data.

The shift control signal D_{SFT} also is provided to the timing adjusting circuit. This results in stopping the exchange of the clock according to stopping the operation of the data transference from the flip-flop circuits 10A - 10I, whereas the exchange of the clock continues in the timing adjusting circuit 2.

As described above, the timing adjusting circuit 2 adjusts timing of inputted 625/50 component digital video signals S_{IND1} to send to the oversampling filter 6 according to the output clock signals CK_{D1}, the output clock signals CK_{D2}, and the shift control data

D_{SFT}.

The oversampling filter 6 performs oversampling by multiplying the 625/50 component digital video signals S_{IND1} thus inputted by coefficients C_{OEFA}, C_{OEFB}, ... according to the shift control data D_{SFT} and the coefficient address data D_{COE}, and provides outputs according to output clock signals CK_{D2}. In this manner, output digital video signals S_{OUTD2} are obtained by converting the sampling frequency of 625/50 component digital video signals to a sampling frequency corresponding to PAL composite digital video signals.

It is to be noted that in the oversampling filter 6 input digital signals S_{IN} are fed to a series circuit flip-flops 10A, 10B, ... having a delay according to output clock signals CK_{D2}. Delayed digital signals sent out from each of the flip-flops 10A, 10B, ... are inputted to subsequent flip-flops 10B, ... and to corresponding multipliers 8A, 8B,....

Predetermined coefficients C_{OEFA}, C_{OEFB}, ... described above are inputted from the coefficient generating circuits 9A, 9B, ... to respective multipliers 8A, 8B, ..., and consequently, the delayed digital signals are multiplied by respective coefficients C_{OEFA}, C_{OEFB}, ...

Results of the multiplication are inputted to each of adders 11A, 11B, ... for providing a total, and the result of this addition is sent out as output digital video signals S_{OUT}.

The sampling rate converter 1 with such a construction has a large scale circuit configuration in which the counter 4 counts a value 0 to 709378. Also, the coefficient address control circuit 7 inevitably has a large scale circuit configuration for processing count data D_{CNT} from the counter 4. Consequently, there is a problem in that the sampling rate converter 1 becomes large sized.

SUMMARY OF THE INVENTION

In view of the foregoing, an object of this invention is to provide a sampling rate converter which is capable of converting a sampling frequency of digital signals sampled at a first sampling frequency to a second sampling frequency with a simple construction.

In accordance with a first aspect of this invention, there is provided a sampling rate converter 20 for converting a sampling frequency of digital signals sampled at a first sampling frequency to a

second sampling frequency, the sampling rate converter including an oversampling filter 6 having coefficient generation means 9A, 9B for generating coefficients C_{OEFA}, C_{OEFB} to be provided to weighting means 8A, 8B according to coefficient addresses D_{COE1}, there are according to the present invention provided for solving such a problem: counting means 21 for counting output clocks CK_{D2} in a cyclic fashion; correction value generation means 22, 26 for generating a coefficient correction value D_{HC} in accordance with a number of counts of a maximum value C_{HC} and the periodicity of the first and second sampling frequencies, the number of counts of the maximum value being obtained by counting maximum value information S_{CO} sent from the counter means 21 every time the counter means counts to the maximum value; and coefficient address generation means 23, 24, 27 for generating the coefficient addresses D_{COE1} in accordance with the counted value D_{CNT1}, inputted from the counter means 21, and the coefficient correction value D_{HC} inputted from the correction value generation means 22, 26.

In thus construction, output clocks CK_{D2} corresponding to the second sampling frequency are counted in the cyclic fashion from the initial value to

the maximum value based on periodicity of the first and second sampling frequencies. Coefficient addresses D_{COE1} are generated in accordance to the resulting count value D_{CNT1} and the coefficient correction value D_{HC} in accordance with the number of counts of the maximum value C_{HC} and the periodicity of the first and second sampling frequencies, the number of the maximum value counts being the number of times of counting to a maximum value. The sampling frequency of digital signals sampled at the first sampling frequency is thus converted to the second sampling frequency with a simple construction of counting from the initial value to the maximum value.

The nature, principle and utility of the invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings in which like parts are designated by like reference numerals or characters.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a timing chart illustrating the oversampling operation;

FIG. 2 is a block diagram showing the conventional

sampling rate converter;

FIG. 3 is a block diagram showing part of the oversampling filter;

FIG. 4 is a graph showing the relationship between the coefficient and the coefficient address data;

FIG. 5 is a schematic diagram showing the relationship between the count data D_{CNT} and the coefficient address data D_{COE};

FIG. 6 is a block diagram showing one embodiment of the sampling rate converter according to this invention; and

FIG. 7 is a schematic diagram showing the shift of the coefficient address data with the correction.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of this invention will be described with reference to the accompanying drawings:

(1) Principle of the Embodiment

In a sampling rate converter of this embodiment, the sampling frequency of component digital video signals based on the D-1(625/50) format in digital • video tape recorder (DVTR) is converted to a sampling frequency corresponding to PAL composite digital video signals based on the D-2(PAL) format.

In practice, the sampling frequency of component digital video signals based on the D-1(625/50) format is defined to 13.5 MHz, and the number of samples per a line of digital video signals is hence 864. The total number of samples of one frame amounts to 540,000.

The sampling frequency of PAL composite digital video signals based on the D-2(PAL) format is 17.734475 MHz which is four times the sub-carrier frequency f_{SC} calculated based on the following equation, provided the horizontal frequency f_h is 15.625 KHz:

$$f_{SC} = (284 - \frac{1}{4})f_h + \frac{50}{2}$$

$$= 4.43361875 \text{ (MHz)} \quad \ldots (2)$$

Accordingly, the number of samples per a line of digital video signals is 1135.0064, and the total number of samples of one frame is 709379.

As described, the ratio in number of samples per a line of the 625/50 component digital video signals over the PAL composite digital video signals is 864:1135.0064, and it is understood that the ratio does

not have an appropriate integer relationship.

When a sampling frequency is converted using an oversampling filter with a sufficient length, the oversampling filter may be of a coefficient switch type construction. In this case, the combination of coefficients given to the oversampling filter must correspond to the phase between the pre-conversion sampling frequency and the pst-conversion sampling frequency.

As already described, there is no relatively small integer ratio between the pre-conversion sampling frequency and the post-conversion sampling frequency, and it is hence necessary to count sampling points per a frame so as to generate a coefficient corresponding to the count value.

The sampling cycle of the 625/50 component digital video signals is computed from the following equation:

$$\frac{1}{13.5\ (\mathrm{MHz})} = 74.074074\ (\mathrm{nsec}) \quad \ldots\ (3)$$

The sampling cycle of the PAL composite digital video signals is computed from the following equation:

$$\frac{1}{17.734475\ (\mathrm{MHz})} = 56.38734724\ (\mathrm{nsec}) \quad \ldots (4)$$

By detecting the time difference between the sampling point corresponding to the sampling frequency of 625/50 component digital video signals and the sampling point corresponding to the sampling frequency of PAL composite digital video signals from the top of a frame, the number of samples of the 625/50 component digital video signals becomes a value given as equation below at a time point of 423 samples of PAL composite digital video signals when counted from the top of the frame:

$$\frac{56.38734724\ (\mathrm{nsec}) * 423}{74.074074\ (\mathrm{nsec})} = 321.9999464 \quad \ldots (5)$$

the sampling points of both become closer in timing.

Sampling points of both which correspond to the

sampling cycles of 625/50 component digital video signals and PAL composite digital video signals become closer every multiple of 423 sample points at the sampling cycle of PAL composite digital video signals.

In this embodiment, coefficient addresses and the data shift control are held between 423 sample points with reference to the sampling cycle of the PAL composite digital video signals. In this manner, correction of time given by the equation below is performed every 423 sample points at the sampling cycle of the PAL composite digital video signals.

$$\begin{aligned} & 56.38734724 \text{ (nsec)} \times 423 \\ & - 74.074074 \text{ (nsec)} \times 322 \\ & = - 0.00396796 \text{ (nsec)} \qquad \ldots (6) \end{aligned}$$

In phase shifting and generation of coefficients, the correction above described is carried out by providing a counter which counts sampling within a small range between 423 sample points. This enables the sampling frequency to be converted at a high accuracy with a simple construction.

(2) Sampling Rate Converter of the Embodiment

In FIG. 6, in which corresponding parts of FIG. 2 are given the same reference numerals, 20 generally designates a sampling rate converter which converts a sampling frequency of 625/50 component digital video signals to a sampling frequency according to PAL composite digital video signals, for example. In this embodiment, frame pulses P_{FD1} which correspond to every one frame of 625/50 component digital video signals S_{IND1} are inputted to a PLL circuit 3, a reset input terminal of a counter 21, and a reset terminal of a number-of-corrections counter 22.

The counter 21 is adopted in place of the conventional counter 4 which counts to 709378 and is designed to count output clock signals CK_{D2} in a cyclic manner from zero to 422 on the basis of the principle stated in connection with the equations (3) to (6) during one frame of 625/50 component digital video signals S_{IND1}.

The counter 21 thus counts output clock signals CK_{D2} during one frame. The counter 21 sends resulting count data D_{CNT1} which is from zero to 422 to a coefficient address generation circuit 23, and also sends a carry signal S_{CO}, which is generated every time the counted value exceeds 422, to the correction

frequency counter 22.

The coefficient address generation circuit 23 generates an coefficient address ADR_{COE} and shift data D_{SFT1} (this signal has the same function as the function of shift control signal D_{SFT}, i.e. data transference function and clock exchange stopping function) in response to the inputted count data D_{CNT1}, and sends them to an adder 24 and a shift control circuit 25, respectively.

During one frame, the number-of-corrections counter 22 counts inputted carry signals S_{CO} to generate number-of-corrections data C_{HC}, which is sent to a corrected value multiplier 26.

The corrected value multiplier 26 calculates number-of-corrections data C_{HC} by multiplying the correction value (= 0.00396795 (nsec)) described in connection with the equation (6) with the number-of-corrections data C_{HC}, the corrected value data D_{HC} corresponding to correction of the coefficient address ADR_{COE} based on the number of corrections. The corrected value data D_{HC} is fed to the adder 24.

The adder 24 adds the coefficient address ADR_{COE} and the corrected value data D_{HC} to produce a corrected coefficient address ADR_{COE1}, which is provided to a

coefficient adjusting circuit 27.

On the basis of the corrected coefficient address ADR_{COE1}, this coefficient adjusting circuit 27 generates coefficient address data D_{COE1} and sends it coefficient generating circuits 9A, 9B, ... of the oversampling filter 6.

Moreover the coefficient adjusting circuit 27 detects whether or not the coefficient address ADR_{COE1} is in overflow comparing with the coefficient address ADR_{COE} before correction so as to send the resultant to the shift control circuit 25 as a overflow data D_{OF}. Hence, the overflow means the fact following. In FIG. 7, when the count data D_{CNT} is $D_{CNT} = n$ the address a_{137} is appointed as the address of the coefficient generating circuit, subsequently when the count data D_{CNT} becomes $D_{CNT} = n + 1$ the address a_0 is appointed by means of correction. On the contrary, when the count data D_{CNT} becomes $D_{CNT} = n + 1$, the address a_{505} is appointed unless the address moves by means of correction.

The overflow means that the address exceeds a round where the accesses of a round is from a_0 to a_{505}. If thus overflow generates, it is needs to process as follow. That is, if there is an address relationship

as FIG. 7, the output data of the flip-flop circuit 10A to be multiplied by the coefficient having the address a_0 needs to data transfer afresh by one clock, unless it is such data as stopped transfering the data which is multiplied by the coefficient. The operation "stop of data transference" and "stop of clock exchange" described above are put a stop to.

The shift control circuit 25 detects whether or not there is need "stop of data transference" and "stop of clock exchange". And sends the resultant signals as shift control signals S_{SFT2} to the timing adjusting circuit 2 and the oversampling filter 6.

Consequently, the timing adjusting circuit 2 controls timing of sending inputted 625/50 component digital video signals S_{IND1} to the oversampling filter 6 according to the output clock signals CK_{D1}, the output clock signals CK_{D2}, and the shift control data D_{SFT2}.

The oversampling filter 6 performs oversampling by multiplying the 625/50 component digital video signals S_{IND1} thus inputted by coefficients C_{OEFA}, C_{OEFB}, ... according to the shift control data D_{SFT2} and the coefficient address data D_{COE1}, and conducts resampling according to the output clock signals CK_{D2} and outputs

the resultant data. In this manner, output digital video signals S_{OUTD2} which are produced by converting the sampling frequency of 625/50 component digital video signals to the sampling frequency of PAL composite digital video signals are obtained.

The oversampling filter 6 has coefficients equal in number to 505 times oversampling filter, and hence has a resolution of 1/505. In fact, the correction (= 0.00396795 (nsec)) stated about the equation (6) is 0.027068 times as large as the resolution. This value means that correction is carried out 45 times (that is, 0.178 (nsec)) at the trailing end of one frame. To do this, the counter 21 and the number-of-corrections counter 22 are controlled to be placed in initialized states by resetting them every frame.

According to the foregoing construction, sampling points are sequentially counted in a small range of 423 sampling points, and the predetermined correction is carried out every 423 sampling points. The sampling rate converter 20 is realized which enables the counter circuit to be built with a simple circuit construction which counts zero to 422, and which is capable of converting a sampling frequency of 625/50 component digital video signals to a sampling frequency according

to PAL composite digital video signals at a high accuracy.

Moreover, according to the foregoing construction, the coefficient address generation circuit 23 is also built with a simple circuit construction by constructing the counter 21 with a simple circuit construction which counts zero to 422. A sampling rate converter is thus realized which is capable of reducing in circuit scale to about 1/1677 of the conventional sampling rate converter 1 (FIG. 2), resulting in a remarkable reduction in overall scale.

(3) Other Embodiments

(3-1) In the embodiment above, a case where a sampling frequency of 825/50 component digital video signals is converted to a sampling frequency according to PAL composite digital video signals is stated but this invention is not limited to this. This invention is suitably applied to a case where a sampling frequency of PAL composite digital video signals is converted to a sampling frequency according to 625/50 component digital video signals.

It is to be understood that in this case an effect similar to that of the preceding embodiment will be achieved by adding the correction (= 0.00396795 (nsec)) described about the equation (6) every 322 sampling points of a sampling cycle of 625/50 component digital video signals according to the principle of this invention stated about the equations (3) to (5).

(3-2) In the preceding embodiments, cases where a sampling frequency of PAL composite digital video signals or 625/50 component digital video signals is converted to a sampling frequency according to 625/50 component digital video signals or PAL composite digital video signals are stated, but this invention is not restricted to these. This invention is suitably

applied to various cases where a sampling frequency of digital signals is converted to a new sampling frequency which is not in a relationship of a simple integer ratio with the sampling frequency.

(3-3) In the preceding embodiments, a case where a range among every 423 sampling points of a sampling cycle of PAL composite digital video signal is counted is stated, but this invention is not limited to this. This invention is suitably applied to a case where a range among every sampling points being integer times as many as 423 is counted.

While there has been described in connection with the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention, and it is aimed, therefore, to cover in the appended claims all such changes and modifications as fall within the true spirit and scope of the invention.

THE EMBODIMENT OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. In a sampling rate converter for converting a sampling frequency of digital signals sampled at a first sampling frequency to a second sampling frequency, and which includes an oversampling filter having coefficient generation means for generating coefficients to be provided to weighting means according to coefficient addresses; the combination of:

means for generating clock pulses at said second sampling frequency;

counting means for generating count data by counting, in response to said clock pulses, in a cyclic fashion from an initial value to a maximum value which is chosen on the basis of the first and second sampling frequencies;

correction value generation means for generating a coefficient correction value in accordance with a number of times said counting means counts said maximum value, the value chosen as said maximum value, and the first and second sampling frequencies; and

coefficient address generation means for generating each of said coefficient addresses in accordance with a respective value of said count data and the corresponding coefficient correction value generated by said correction value generation means.

2. A sampling rate converter according to claim 1, in which said correction value generation means includes:

detection means for detecting said number of times the counting means counts said maximum value during a frame period; and

multiplication means for multiplying said number detected by said detection means by a correction value based on said value chosen as said maximum value and said first and second sampling frequencies, thereby generating said coefficient correction value.

3. A sampling rate converter according to claim 2, in which said detection means for detecting said number of times said maximum value is counted includes a counter which is reset along with said counting means for counting said clock pulses by a signal representing a frame period corresponding to said first sampling frequency.

4. A sampling rate converter according to claim 1, in which said coefficient address generation means includes:

means for generating an initial coefficient address and means for providing shift data based on said count data;

addition means for adding said initial coefficient address and said coefficient correction value;

coefficient adjusting means having means for generating said coefficient address based on an output of said addition means, means for detecting an overflow from said addition means, and means for outputting said coefficient address delayed for a cycle in response to detection of said overflow; and shift control means for modifying said shift data on the basis of said overflow.

5. A sampling rate converter according to claim 1, in which, at each said initial value of said count data, said digital signals sampled at said first sampling frequency are in synchronism with digital signals sampled at said second sampling frequency.

6. A sampling rate converter according to claim 1, in which said first sampling frequency is 13.5 MHz, said second sampling frequency is 17.734475 MHz, and said maximum value is 423.

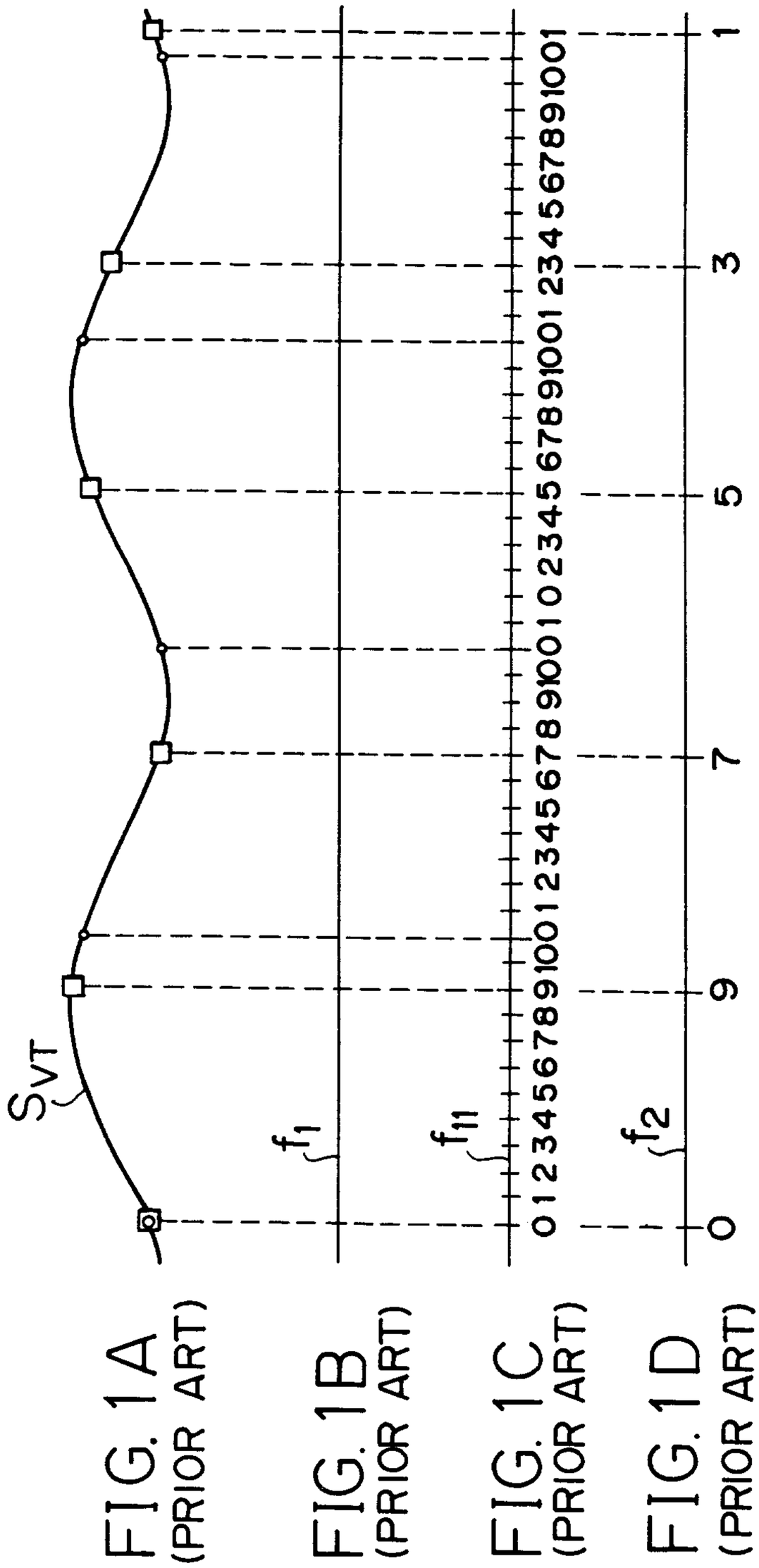


FIG. 1A (PRIOR ART)

FIG. 1B (PRIOR ART)

FIG. 1C (PRIOR ART)

FIG. 1D (PRIOR ART)

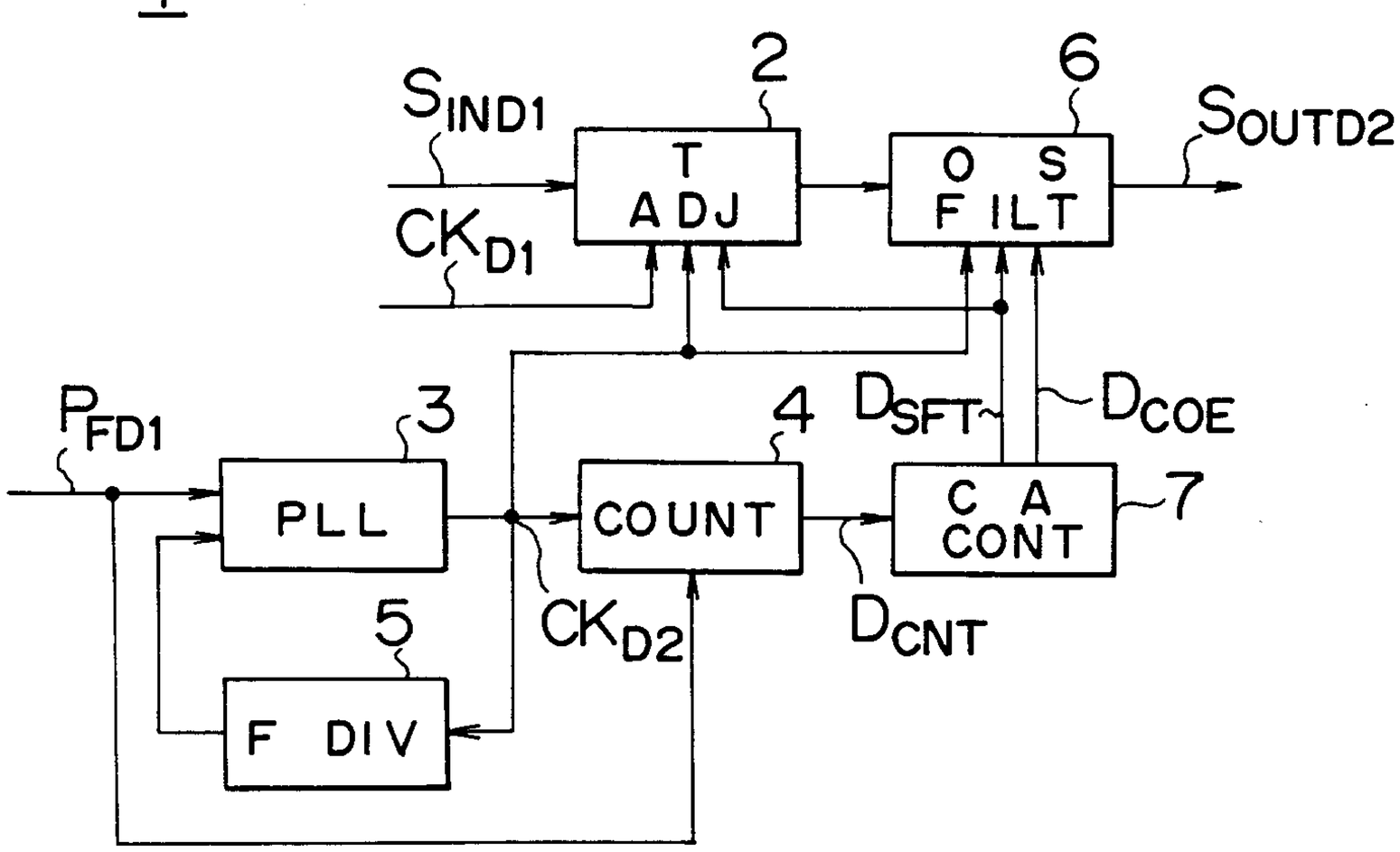


FIG. 2 (PRIOR ART)

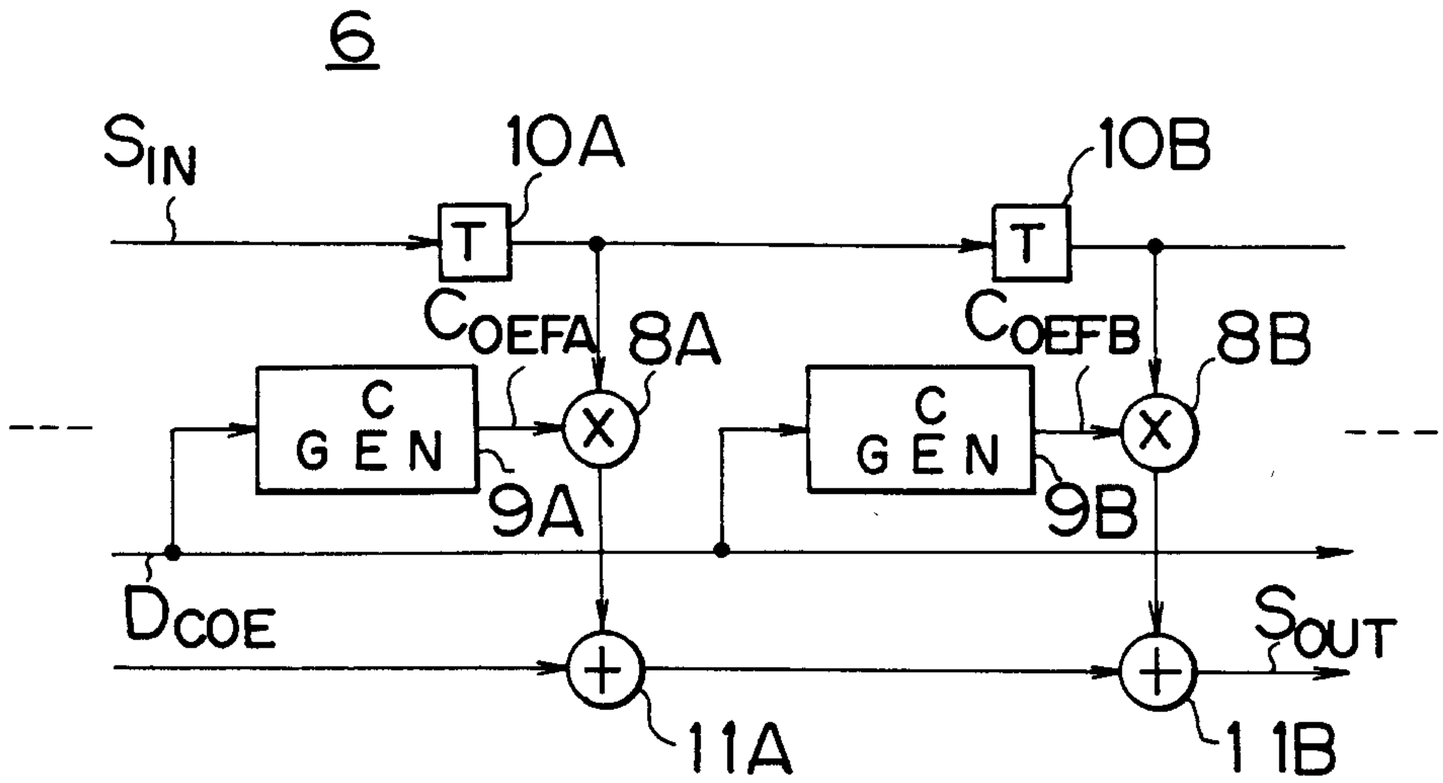


FIG. 3 (PRIOR ART)

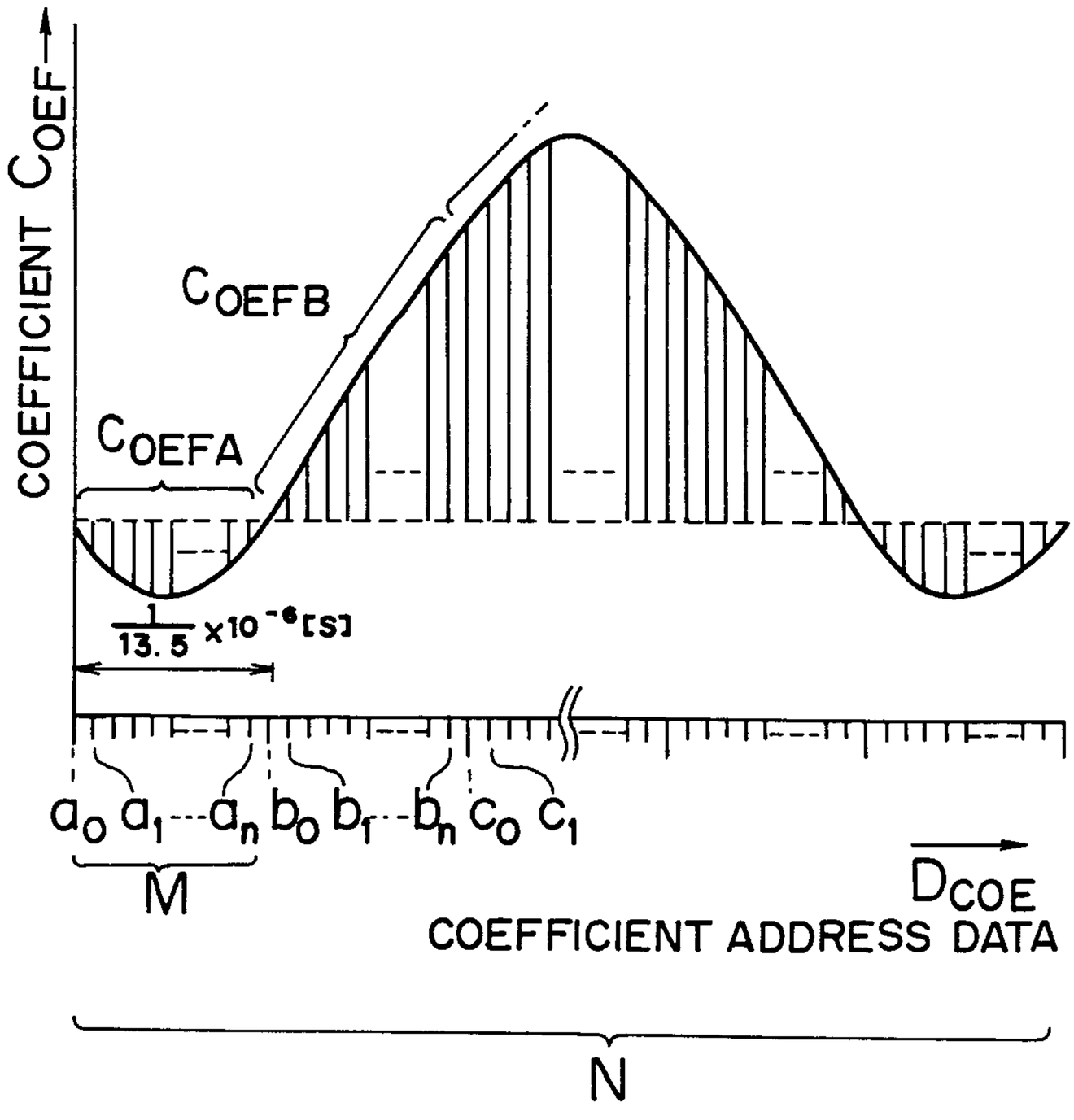


FIG. 4 (PRIOR ART)

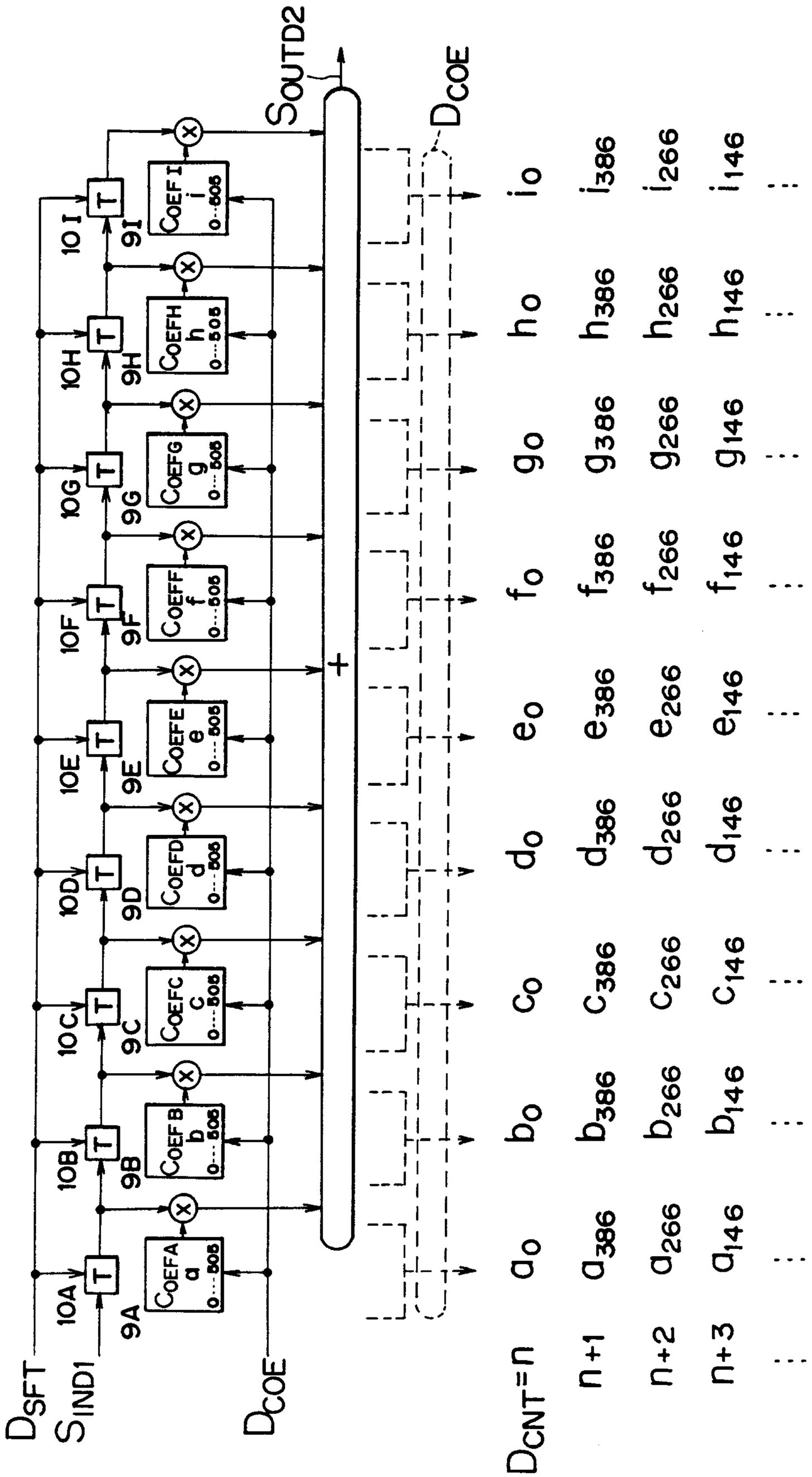


FIG. 5 (PRIOR ART)

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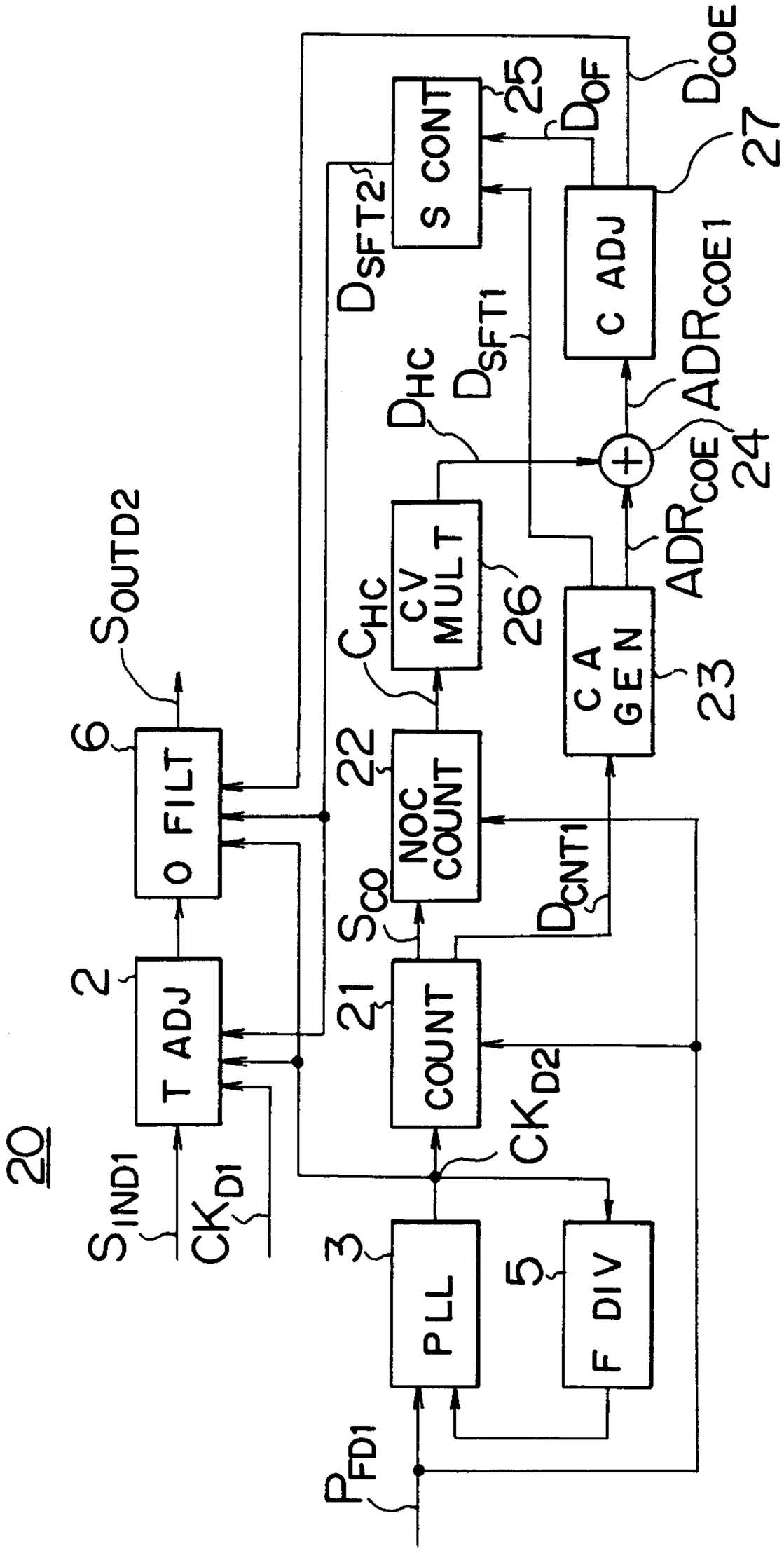

FIG. 6

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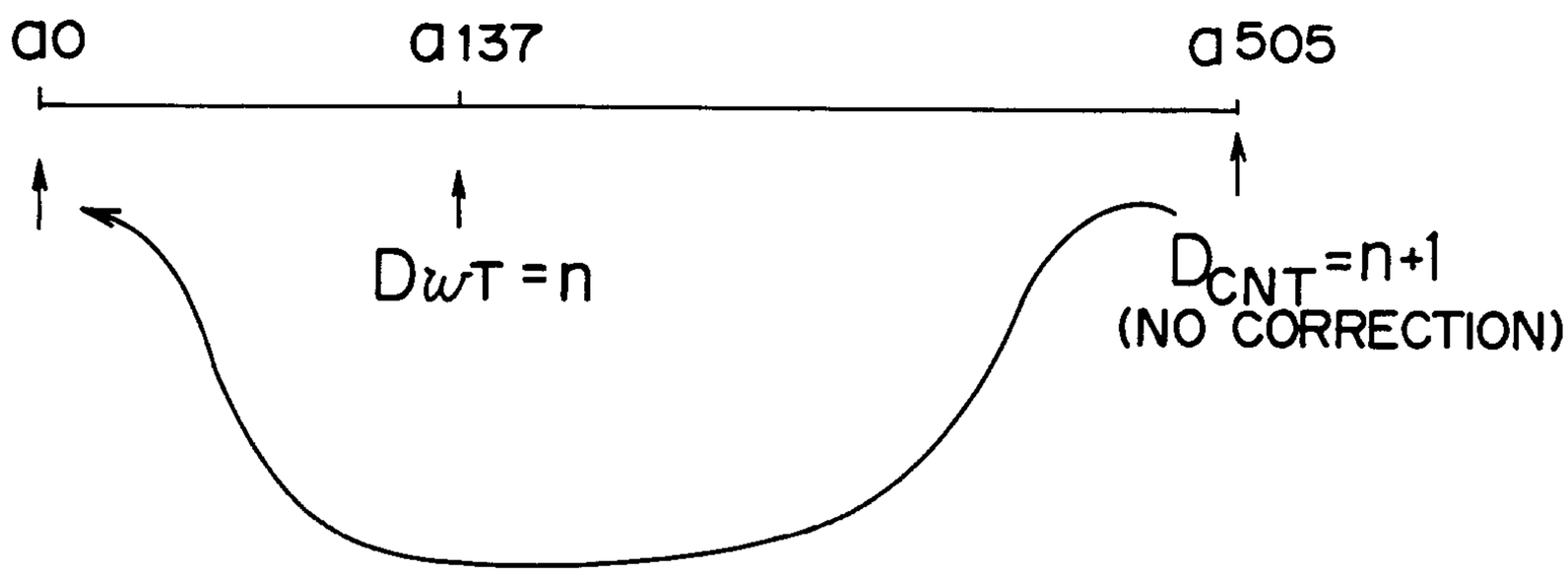

FIG. 7