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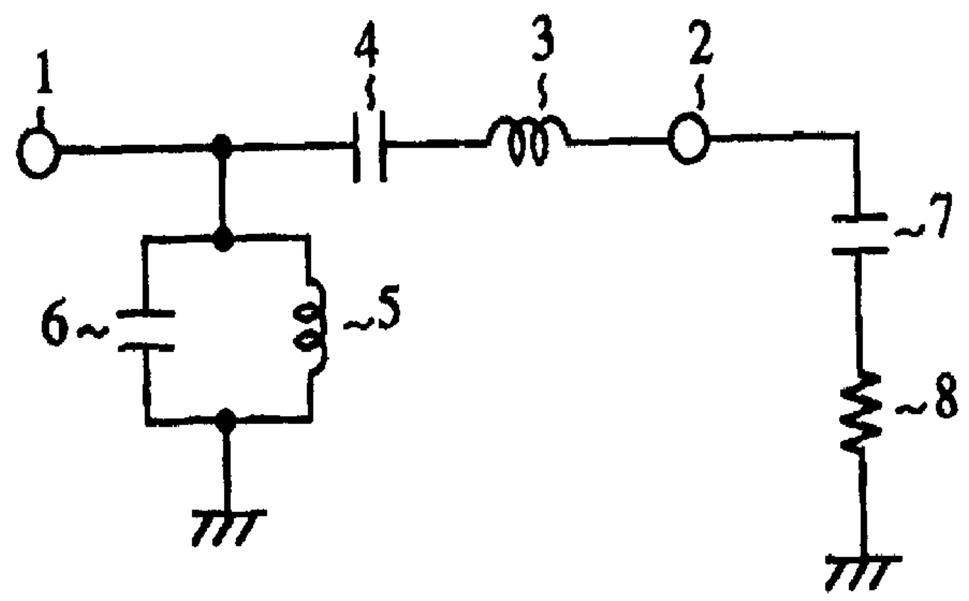
(54) **CIRCUIT D'ADAPTATION D'IMPEDANCE A DEUX FREQUENCES**

(54) **TWO-FREQUENCY IMPEDANCE MATCHING CIRCUIT**



(57) L'invention concerne un circuit d'adaptation d'impédance comprenant une borne de sortie connectée à une charge, une borne d'entrée recevant un signal pour la charge, un résonateur série constitué d'un condensateur série et d'une bobine d'inductance série montée en série avec condensateur série, le résonateur série étant monté en série avec la charge, à partir de la borne d'entrée, un résonateur parallèle constitué d'un condensateur parallèle et une bobine d'inductance parallèle montée en parallèle avec le condensateur parallèle, le résonateur parallèle étant monté en parallèle avec la charge et le résonateur série à partir de la borne d'entrée. Cette configuration résout le problème découlant du fait qu'un circuit d'adaptation d'impédance conventionnel ne peut effectuer l'adaptation de l'impédance à deux fréquences. L'absence de ligne de transmission permet d'obtenir un circuit compact, convenant à une application basse fréquence.

(57) An impedance matching circuit comprises an output terminal connected with a load; an input terminal for receiving a signal for the load; a series resonance circuit consisting of a series capacitor and a series inductor connected in series with the series capacitor, the series resonance circuit being connected in series with the load viewed from the input terminal; and a parallel resonance circuit consisting of a parallel capacitor and a parallel inductor connected in parallel with the parallel capacitor, the parallel resonance circuit being connected in parallel with the load and the series resonance circuit viewed from the input terminal. This configuration solves the problem that the conventional impedance matching circuit cannot perform impedance matching at two frequencies. Since no transmission line is used, the circuit becomes compact for a low-frequency application.

ABSTRACT

A dual-frequency matching circuit of the present invention comprises an output terminal to which a load is connected, an input terminal through which an input signal is input to the load, a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to the series capacitor and disposed in such a manner that it is connected in series to the load when observed from the input terminal side, and a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to the parallel capacitor, and disposed in such a manner that it is connected in parallel to the entire portion of the load and the series resonance circuit when observed from the input terminal side. By this configuration, the problem contained in the conventional matching circuit that the matching of impedance at two arbitrary different frequencies is not made possible can be solved, and that since no transmission line is needed therein, the circuit can be minimized as a whole when frequency at which the matching operation is performed is set to a low frequency band.

TITLE

Dual-Frequency Matching Circuit

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to a dual-frequency matching circuit that enables impedance matching at two separate frequencies simultaneously, and more particularly to an improvement of the matching circuit that can be suitably used in the microwave band.

Background Art

Fig. 9 is a schematic diagram showing a conventional dual-frequency matching circuit cascaded with a field-effect transistor (hereinafter referred to just as an "FET", or an "FET transistor"), as disclosed in the "Dual-frequency matching technique and its application to an octave-band (30-60GHz) MMIC amplifier" by NAKAJIMA, M, MURAGUCHI, in IEICE TRANS, ELECTRON., VOL.E80-C, No.12, December 1997.

In the figure, reference numeral 1 denotes an input terminal of the matching circuit, numeral 2 denotes an output terminal of the matching circuit, numeral 47 denotes a transmission line provided between the input terminal 1 and the output terminal 2, numeral 48 denotes a shorted stub provided between the input terminal 1 and the transmission line 47, the length of which is a quarter-wavelength $\lambda/4$ at a high angular frequency ω_H, numeral 49 denotes an open stub provided between the input terminal 1 and the transmission line 47, and reference numeral 50 denotes an FET transistor, the gate of which is connected to the output terminal 2.

Fig. 10 denotes a Smith Chart for explaining the matching method in the conventional dual-frequency matching circuit. In the figure, reference numeral 51 denotes a load impedance generated in a case

that a low-frequency signal f_L is applied to the FET transistor 50, reference numeral 52 denotes an impedance generated in a case that a high-frequency signal f_H is applied to the FET transistor 50, and reference numeral 53 denotes a constant conductance circle (a constant conductance circle of 0.02S, for example).

First, by setting the length of the transmission line 47 to a predetermined length, the two impedances of the above-mentioned FET transistor are set on to the constant conductance circle 53. Reference numeral 54 denotes a thus obtained transformed impedance of the case that the low-frequency signal f_L is applied, whereas the reference numeral 55 denotes a transformed impedance of the case that the high-frequency signal f_H is applied.

Thereafter, by setting the length of the open stub 49 to a predetermined length, the above-mentioned two impedances are shifted along the constant conductance circle 53 so as to be matched with each other, and reference numeral 56 denotes a point at which they are matched. In this way, the conventional matching circuit enables an impedance matching at two separate frequencies f_L and f_H.

The operation of the above conventional dual-frequency matching circuit is as follows.

When a signal is to be input through the input terminal 1 to the FET transistor 50, no reflected wave due to the input signal is generated at the above two matching frequencies f_L and f_H.

Since the conventional dual-frequency matching circuit is configured as such, two input impedances of the FET transistor 50 at two different frequencies are transformed on to the constant conductance circle 53 only on the basis of the length of the transmission line 47, so that if the length of the transmission line 47 is determined in such a manner that an impedance at one of the two frequencies is shifted on to the constant conductance circle 53,

the other frequency at which the impedance can be shifted on to the constant conductance circle 53 is automatically determined, so that there has been a problem that the matching of impedances at two arbitrarily selected frequencies is not made possible.

Further, as a transmission line 47 is adopted in the conventional dual-frequency matching circuit, if the matching is to be performed in a low-frequency band, a considerably long transmission line is required, so that the size of the frequency-matching circuit as a whole is also made too large.

DISCLOSURE OF THE INVENTION

The present invention has been proposed to solve the problems aforementioned, and it is an object of the present invention to provide a matching circuit capable of performing an impedance matching at two arbitrary frequencies.

In order to achieve the above object, the dual-frequency matching circuit according to the first aspect of the present invention is constructed such that it comprises an output terminal to which a load is connected, an input terminal through which an input signal is input to the load, a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to the series capacitor, and disposed in such a manner as to be connected in series to the load when observed from the input terminal side, and a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to the parallel capacitor, and disposed in such a manner as to be connected in parallel to the entire portion of the series resonance circuit and the load when observed from the input terminal side.

In the dual-frequency matching circuit constructed as above, on condition that the load connected to the output terminal is formed

by a load resistor and a load capacitor mutually connected in series, and that the resistance of the load resistance is R_i, the capacitance of the load capacitor is C_{gs}, two matching angular frequencies are ω_L and ω_H, respectively, and matching admittance is Y_0, the inductance L_1 of the series inductor, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor and the capacitance C_2 of the parallel capacitor are set in such a manner as to satisfy the following Formulae 1:

$$L_1=X_g/(\omega_H-\omega_L)$$

$$C_1=(\omega_H-\omega_L)*C_{gs}/(C_{gs}*\omega_H*\omega_L*X_g-(\omega_H-\omega_L))$$

$$L_2=(\omega_H-\omega_L)*R_i/(\omega_H*\omega_L*Y_o*X_g)$$

$$C_2=Y_o*X_g/((\omega_H-\omega_L)*R_i)$$

$$X_g=(R_i/Y_0-R_i*R_i)^{1/2} \quad \cdots \text{(Formulae 1)}$$

The dual-frequency matching circuit according to the second aspect of the present invention is constructed such that it comprises an output terminal to which a load is connected, an input terminal through which an input signal is input to the load, a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to the parallel capacitor, and disposed in such a manner as to be connected in series to the load when observed from the input terminal side, and a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to the series capacitor, and disposed as being connected in parallel to the load when observed from the input terminal side.

In the dual-frequency matching circuit constructed as above, the load connected to the output terminal is formed by a load resistor and a load capacitor mutually connected in series, wherein on condition that the resistance of the load resistance is R_i, the resistance of the load capacitor is C_{gs}, two matching angular

frequencies are ω_L and ω_H, respectively, and matching impedance is Z_0, the inductance L_1 of the series inductor, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor, and the capacitance C_2 of the parallel capacitor are set in such a manner as to satisfy the following Formulae 2:

$$L_1=(\omega_H*(\beta_L-B_{gl})-\omega_L*(\beta_H+B_{gH}))/((\omega_H*\omega_H-\omega_L*\omega_L)(\beta_L-B_{gl})(\beta_H+B_{gH}))$$

$$C_1=(\omega_H*\omega_H-\omega_L*\omega_L)(\beta_L-B_{gl})(\beta_H+B_{gH})\ /(\omega_H*\omega_L*(\omega_L*(\beta_L-B_{gl})-\omega_H*(\beta_H+B_{gH})))$$

$$L_2=Z_o*(\omega_H*\omega_H-\omega_L*\omega_L)*B_{gH}*B_{gl}/(\omega_H*\omega_L*(\omega_H*\alpha_L*B_{gH}+\omega_L*\alpha_H*B_{gl}))$$

$$C_2=(\omega_L*\alpha_L*B_{gH}+\omega_H*\alpha_H*B_{gl})/(Z_o*(\omega_H*\omega_H-\omega_L*\omega_L)*B_{gH}*B_{gl})$$

$$\alpha=R_i\ /(R_i*R_i+1/(\omega*\omega*C_{gs}*C_{gs}))$$

$$\beta=(1/(\omega*C_{gs}))/(R_i*R_i+1/(\omega*\omega*C_{gs}*C_{gs}))$$

$$B_g=(\alpha/Z_o-\alpha*\alpha)^{1/2} \qquad \cdots \text{(Formulae 2)}$$

The dual-frequency matching circuit according to the third aspect of the present invention is constructed such that it comprises an input terminal to which a load is connected, an output terminal that outputs an output signal on the basis of the load, a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to the series capacitor, and disposed in such a manner as to be connected in series to the load when observed from said output terminal side, and a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to the parallel capacitor, and disposed in such a manner as to be connected in parallel to the load when observed from the output terminal side.

In the dual-frequency matching circuit constructed as above, on condition that the load connected to the input terminal is formed by a load capacitor and a load resistor mutually connected in parallel, one end of the both of which being connected to the input terminal in series, and that the resistance of the load resistance is R_{ds}, the capacitance of the load capacitor is C_{ds}, two matching angular

frequencies are ω_L and ω_H, respectively, and matching impedance is Z_0, the inductance L_1 of the series inductor, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor, and the capacitance C_2 of the parallel capacitor are set in such a manner as to satisfy the following Formulae 3:

$$L_1=R_{ds}*Z_o*B_d/(\omega_H-\omega_L)$$

$$C_1=(\omega_H-\omega_L)/(\omega_H*\omega_L*R_{ds}*Z_o*B_d)$$

$$L_2=(\omega_H-\omega_L)/(\omega_H*\omega_L*B_d)$$

$$C_2=B_d/(\omega_H-\omega_L)-C_{ds}$$

$$B_d=(1/(Z_o*R_{ds})-1/(R_{ds}*R_{ds}))^{1/2} \quad \cdots \text{(Formulae 3)}$$

The dual-frequency matching circuit according to the fourth aspect of the present invention is constructed such that it comprises an input terminal to which a load is connected, an output terminal that outputs an output signal on the basis of the load, a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel with the parallel capacitor, and disposed in such a manner as to be connected in series to the load when observed from the output terminal side, and a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to the series capacitor, and disposed as being connected in parallel to the entire portion of the load and the parallel resonance circuit when observed from the output terminal side.

In the dual-frequency matching circuit constructed as above, on condition that the load connected to the input terminal is formed by a load capacitor and a load resistor mutually connected in parallel, one end of the both of which being connected to the input terminal in series, and that the resistance of the load resistance is R_{ds}, the capacitance of the load capacitor is C_{ds}, two matching angular frequencies are ω_L and ω_H, respectively, and matching impedance is

Z_0, the inductance L_1 of the series inductor, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor, and the capacitance C_2 of the parallel capacitor are set in such a manner as to satisfy the following Formulae 4:

$$L_1=(\omega_L*\alpha_L*X_{dH}+\omega_H*\alpha_H*X_{dL})/(Y_o*(\omega_H*\omega_H-\omega_L*\omega_L)*X_{dH}*X_{dL})$$

$$C_1=Y_o*(\omega_H*\omega_H-\omega_L*\omega_L)*X_{dH}*X_{dL}/(\omega_H*\omega_L*(\omega_H*\alpha_L*X_{dH}+\omega_L*\alpha_{dL}*X_{dL}))$$

$$L_2=(\omega_H*\omega_H-\omega_L*\omega_L)/(\omega_H*\omega_L*(\omega_L/(X_{dH}-\beta_H)+\omega_H/(X_{dL}+\beta_L)))$$

$$C_2=(\omega_H*(X_{dH}-\beta_H)+\omega_L/(X_{dL}+\beta_L))/(\omega_H*\omega_H-\omega_L*\omega_L)$$

$$\alpha=(1/R_{ds})/(1/(R_{ds}*R_{ds})+\omega*\omega*C_{ds}*C_{ds})$$

$$\beta=\omega*C_{ds}/(1/(R_{ds}R_{ds})+\omega*\omega*C_{ds}*C_{ds}))$$

$$X_d=(\alpha/Y_o-\alpha*\alpha)^{1/2} \quad \cdots \text{(Formulae 4)}$$

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram showing a dual-frequency matching circuit according to the first embodiment of the present invention and a load connected thereto.

Fig. 2 is a Smith Chart for explaining the role of each of the circuit elements when the matching operation at two angular frequencies ω_H and ω_L are carried out in the dual-frequency matching circuit of the first embodiment.

Fig. 3 is a schematic diagram showing a dual-frequency matching circuit according to the second embodiment of the present invention and a load connected thereto.

Fig. 4 is a Smith Chart for explaining the role of each of the circuit elements when the matching operation at two angular frequencies ω_H, ω_L are carried out in the dual-frequency matching circuit of the second embodiment.

Fig. 5 is a schematic diagram showing a dual-frequency matching circuit according to the third embodiment of the present invention and a load connected thereto.

Fig. 6 is a Smith Chart for explaining the role of each of the circuit elements when the matching operation at two angular frequencies ω_H and ω_L are carried out in the dual-frequency matching circuit of the third embodiment.

Fig. 7 is a schematic diagram showing a dual-frequency matching circuit according to the fourth embodiment of the present invention and a load connected thereto.

Fig. 8 is a Smith Chart for explaining the role of each of the circuit elements when the matching operation at two angular frequencies ω_H and ω_L are carried out in the dual-frequency matching circuit of the fourth embodiment.

Fig. 9 is a schematic diagram of a conventional dual-frequency matching circuit and an FET transistor connected thereto.

Fig. 10 is a Smith Chart for explaining the matching method in the conventional dual-frequency matching circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

Several embodiments for carrying out best the present invention are now explained as in the followings.

[First Embodiment]

Fig. 1 is a schematic diagram showing a dual-frequency matching circuit and a load connected thereto according to a first embodiment of the present invention.

In the figure, reference numeral 1 denotes an input terminal of the matching circuit, numeral 2 denotes an output terminal of the matching circuit, numeral 3 denotes a series inductor connected between the input terminal 1 and the output terminal 2, numeral 4 denotes a series capacitor connected between the series inductor 3 and the input terminal 1, numeral 5 denotes a parallel inductor whose one end is connected between the series capacitor 4 and the input

terminal 1, while the other end thereof is connected to the ground potential, and reference numeral 6 denotes a parallel capacitor whose one end is connected between the series capacitor 4 and the input terminal 1, while the other end thereof is connected to the ground potential.

Further, reference numeral 7 denotes a load capacitor, one end of which is connected to the output terminal 2, and numeral 8 denotes a load resistance, one end of which is connected to the other end of the load capacitor 7, while the other end thereof is connected to the ground potential. It should be noted that in the following explanation of the present embodiment, the load resistance 8 is regarded as being smaller than the matching impedance (for example of 50Ω generally used for a transmission line of a microwave). Further, note that if an equivalent circuit is to be replaced for a circuit in which the load capacitor 7 and the load resistance 8 are connected in series, a circuit, in which an FET transistor whose source electrode is grounded is used in the microwave band, can be represented as an equivalent circuit when observed from the gate electrode of the FET transistor.

Fig. 2 is a Smith Chart for explaining the role of each of the circuit elements shown in Fig. 1 such as the series inductor 3, the series capacitor 4, the parallel inductor 5, and the parallel capacitor 6, when performing an impedance matching operation at two angular frequencies ω_H and ω_L in the dual-frequency matching circuit according to the first embodiment.

In Fig. 2, reference numeral 9 denotes a load impedance $Z_L(\omega_L)$ in a case that a signal of low angular frequency ω_L is applied to the load resistance 8 and the load capacitor 7, reference numeral 10 denotes a load impedance $Z_L(\omega_H)$ in a case that a signal of high angular frequency ω_H is applied to the load resistance 8 and the load

capacitor 7, and reference numeral 11 denotes a constant conductance circle (a constant conductance circle of 0.02S, for example), which is regulated by the above matching impedance.

Here, it is arranged such that the series resonance circuit formed by the series inductor 3 and the series capacitor 4 becomes inductive at two angular frequencies, and that due to this the conductance component of the admittance, which is obtained by observing from the input terminal 1 side the series resonance circuit formed by these circuit elements 3 and 4, and the total load formed by the load capacitor 7 and the load resistance 8 at two different angular frequencies ω_H and ω_L, is shifted on to the constant conductance circle 11. Reference numeral 12 denotes a thus obtained transformed impedance of the case in which a signal of low angular frequency ω_L is applied, whereas numeral 13 denotes a transformed impedance of the case in which a high angular frequency ω_H is applied, which is also obtained by this operation. The value of the inductance L_1 of the series inductor and that of the capacitance C_1 of the series capacitor are shown in the Formulae 5 below.

Further, it is arranged such that the parallel resonance circuit formed by the parallel inductor 5 and the parallel capacitor 6 becomes inductive at a low angular frequency ω_L, and capacitive at a high angular frequency ω_H, and that the two impedances are, due to this, shifted along the constant conductance circle 11 so as to be matched with each other. Reference numeral 14 denotes a matching point obtained by this matching operation. The value of the inductance L_2 of the parallel inductor and that of the capacitance C_2 of the parallel capacitor are shown also in the Formulae 5 below.

$$L_1 = X_g / (\omega_H - \omega_L)$$

$$C_1 = (\omega_H - \omega_L) * C_{gs} / (C_{gs} * \omega_H * \omega_L * X_g - (\omega_H - \omega_L))$$

$$L_2 = (\omega_H - \omega_L) * R_i / (\omega_H * \omega_L * Y_o * X_g)$$

$$C_2=Y_o*X_g/((\omega_H-\omega_L)*R_i)$$

$$X_g=(R_i/Y_0-R_i*R_i)^{1/2} \quad \cdots \text{(Formulae 5)}$$

As is obvious from the Formulae 5, the two matching angular frequencies ω_L, ω_H can be set as individually separate angular frequencies from each other.

The operation of the matching circuit according to the present invention is as follows.

When a signal is to be input through the input terminal 1 to the load, no reflected wave due to the input signal is generated at the two matching angular frequencies ω_L and ω_H.

As explained hereinabove, since according to the first embodiment of the present invention, an impedance matching operation is performed by a dual-frequency matching circuit which is configured as comprising the output terminal 2 to which the loads 7 and 8 are connected, the input terminal 1 through which an input signal to the loads 7 and 8 is input, and the series resonance circuit, which is composed of the series capacitor 4 and the series inductor 3 connected to the series capacitor 4 and disposed in such a manner that it is connected in series to the loads 7 and 8 when observed from the input terminal 1 side, and the parallel resonance circuit, which is composed of the parallel capacitor 6 and the parallel inductor 5 connected in parallel to the parallel capacitor 6, and disposed in such a manner that it is connected in parallel to the entire portion of the loads 7 and 8 and the series resonance circuit formed by the capacitor 4 and the inductor 3 when observed from the input terminal 1 side, the matching operation can be performed with an input resistance (Ri) of the loads 7 and 8 which is smaller than the matching impedance at arbitrarily selected two frequencies.

Particularly, on condition that the resistance of the load

resistance 8 is Ri, the capacitance of the load capacitor 7 is C_{gs}, two matching angular frequencies are ω_L and ω_H, and the matching admittance is Y_0, since the inductance L_1 of the series inductance, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor, and the capacitance C_2 of the parallel capacitor are set in such a manner as to satisfy the above Formulae 5, the matching operation can be performed optimally at the target matching impedance value.

Further, since there is no need to use a transmission line as one of the matching elements, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

[Second Embodiment]

Fig. 3 is a schematic diagram showing a dual-frequency matching circuit and a load connected thereto according to a second embodiment of the present invention.

In the figure, reference numeral 15 denotes a parallel inductor provided between the input terminal 1 and the output terminal 2, numeral 16 denotes a parallel capacitor provided between the input terminal 1 and the output terminal 2, numeral 17 denotes a series inductor whose one end is connected between the output terminal 2 and the parallel inductor 15, numeral 18 denotes a series capacitor whose one end is connected to the other end of the series inductor 17, while the other end thereof is connected to the ground potential. Other portions are same as those of the first embodiment, so that the detailed explanation thereabout is omitted here by simply putting the same reference numerals.

It should be noted that in the following explanation of the

present embodiment, the load resistance 8 is regarded as being smaller than the matching impedance (for example of 50Ω generally used for a transmission line of a microwave).

Fig. 4 is a Smith Chart for explaining the role of each of the circuit elements shown in Fig. 5, such as the series inductor 17, the series capacitor 18, the parallel inductor 15 and the parallel capacitor 16 when performing an impedance matching operation at two angular frequencies ω_H and ω_L in the dual-frequency matching circuit according to the second embodiment.

In Fig. 4, reference numeral 19 denotes a load impedance $Z_L(\omega_L)$ in a case that a low angular frequency signal ω_L is applied to the load resistance 8 and the load capacitor 7, reference numeral 20 denotes a load impedance $Z_L(\omega_H)$ in a case that a high angular frequency signal ω_H is applied to the load resistance 8 and the load capacitor 7, and reference numeral 21 denotes a constant resistance circle (a constant resistance circle of 50Ω, for example), which is regulated by the matching impedance.

Here, it is arranged such that the series resonance circuit formed by the series inductor 17 and the series capacitor 18 becomes inductive at a low angular frequency ω_L and capacitive at a high angular frequency ω_H, and that the two impedances are, due to this, shifted on to the constant resistance circle 21. Reference numeral 22 denotes a thus obtained transformed impedance of the case that signal of a low angular frequency ω_L is applied, whereas reference numeral 23 denotes a transformed impedance of the case that a signal of high angular frequency ω_H is applied, which is also obtained by this operation. The value of the inductance L_1 of the series inductor and that of the capacitance C_1 of the series capacitor are shown in the Formulae 6 below.

Further, it is arranged such that the parallel resonance circuit

formed by the parallel inductor 15 and the parallel capacitor 16 becomes inductive at a low angular frequency ω_L, and capacitive at a high angular frequency ω_H, and that the two impedances are, due to this, shifted along the constant resistance circle 21 so as to be matched with each other. Reference numeral 24 denotes a matching point obtained by this matching operation. The value of the inductance L_2 of the parallel inductor and that of the capacitance C_2 of the parallel capacitor are shown also in the Formulae 6 below.

$$L_1=(\omega_H*(\beta_L-B_{gL})-\omega_L*(\beta_H+B_{gH}))/((\omega_H*\omega_H-\omega_L*\omega_L)(\beta_L-B_{gL})(\beta_H+B_{gH}))$$

$$C_1=(\omega_H*\omega_H-\omega_L*\omega_L)(\beta_L-B_{gL})(\beta_H+B_{gH})\ /(\omega_H*\omega_L*(\omega_L*(\beta_L-B_{gL})-\omega_H*(\beta_H+B_{gH})))$$

$$L_2=Z_o*(\omega_H*\omega_H-\omega_L*\omega_L)*B_{gH}*B_{gL}/(\omega_H*\omega_L*(\omega_H*\alpha_L*B_{gH}+\omega_L*\alpha_H*B_{gL}))$$

$$C_2=(\omega_L*\alpha_L*B_{gH}+\omega_H*\alpha_H*B_{gL})/(Z_o*(\omega_H*\omega_H-\omega_L*\omega_L)*B_{gH}*B_{gL})$$

$$\alpha=R_i\ /(R_i*R_i+1/(\omega*\omega*C_{gs}*C_{gs}))$$

$$\beta=(1/(\omega*C_{gs}))/(R_i*R_i+1/(\omega*\omega*C_{gs}*C_{gs}))$$

$$B_g=(\alpha/Z_o-\alpha*\alpha)^{1/2} \qquad \cdots \text{(Formulae 6)}$$

As is obvious from the Formulae 6, the two matching angular frequencies ω_L and ω_H can be set as individually separate angular frequencies from each other.

The operation of the matching circuit according to the present invention is equivalent to that of the first embodiment, so that the detailed explanation thereof is omitted here.

As explained hereinabove, since according to the second embodiment of the present invention, an impedance matching operation is performed by a dual-frequency matching circuit which is configured as comprising the output terminal 2 to which the loads 7 and 8 are connected, an input terminal 1 through which an input signal to the loads 7 and 8 is input, the parallel resonance circuit, which is composed of the parallel capacitor 16 and the parallel inductor 15 connected to the parallel capacitor 16, and disposed in such a manner

that it is connected in series to the loads 7 and 8 when observed from the input terminal 1 side, and a series resonance circuit, which is composed of a series capacitor 18 and a series inductor 17 connected in series to the series capacitor 18, and disposed in such a manner that it is connected in parallel to the loads 7 and 8 when observed from the input terminal 1 side, the matching operation can be performed with an input resistance (Ri) of the loads 7 and 8 which is larger than the matching impedance at arbitrarily selected two frequencies.

Particularly, on condition that the resistance of the load resistance 8 is Ri, the capacitance of the load capacitor 7 is C_{gs}, two matching angular frequencies are ω_L and ω_H, respectively, and the matching impedance is Z_0, since the inductance L_1 of the series inductor, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor, and the capacitance C_2 of the parallel capacitor are set in such a manner as to satisfy the above Formulae 6, the matching operation can be performed optimally at the target matching impedance value.

Further, since there is no need to use a transmission line as each of the inductor 15 and 17, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

[Third Embodiment]

Fig. 5 is a schematic diagram showing a dual-frequency matching circuit and a load connected thereto according to a third embodiment of the present invention and a load therein.

In the figure, reference numeral 25 denotes a series inductor connected between the input terminal 1 and the output terminal 2,

numeral 26 denotes a series capacitor provided between the serial inductor 25 and the input terminal 1, numeral 27 denotes a parallel inductor whose one end is connected between the series capacitor 26 and the input terminal 1, while the other end thereof is connected to the ground potential, and numeral 28 denotes a parallel capacitor whose one end is connected between the series capacitor 26 and the input terminal 1, while the other end thereof is connected to the ground potential.

Further, reference numeral 29 denotes a load capacitor whose one end is connected to the input terminal 1, while the other end is connected to the ground potential, and numeral 30 denotes a load resistor whose one end is connected to the input terminal 1, while the other end is connected to the ground potential.

It should be noted that in the following explanation of the present embodiment the load resistance 30 is regarded as being larger than the matching impedance (for example of 50Ω generally used for a transmission line of a microwave). Further, note that if an equivalent circuit is to be replaced for a circuit in which the load capacitor 29 and the load resistance 30 are connected in parallel, a circuit, in which an FET transistor whose source electrode is grounded is used in the microwave band, can be represented as an equivalent circuit when observed from the drain electrode of the FET transistor. Other portions are same as those of the first embodiment, so that the detailed explanation thereabout is omitted here by simply putting the same reference numerals.

Fig. 6 is a Smith Chart for explaining the role of each of the circuit elements as shown in Fig. 5, such as the series inductor 25, the series capacitor 26, the parallel inductor 27 and the parallel capacitor 28 when performing an impedance matching operation at two angular frequencies ω_H and ω_L in the dual-frequency matching circuit

according to the third embodiment.

In Fig. 5, reference numeral 31 denotes a load impedance $Z_L(\omega_L)$ in a case that a signal of low angular frequency ω_L is applied to the load resistance 30 and the load capacitor 29, reference numeral 32 denotes a load impedance $Z_L(\omega_H)$ in a case that a signal of high angular frequency signal ω_H is applied to the load resistance 30 and the load capacitor 29, and reference numeral 33 denotes a constant resistance circle (a constant resistance circle of 50Ω, for example), which is regulated by the matching impedance.

Here, it is arranged such that the parallel resonance circuit formed by the parallel inductor 27 and the parallel capacitor 28 becomes inductive at a low angular frequency ω_L and capacitive at a high angular frequency ω_H, and that due to this the admittance, which is obtained by observing from the output terminal 2 side the parallel resonance circuit and the load, is shifted on to the constant resonance circle 33. Reference numeral 34 denotes a thus obtained transformed impedance of the case in which a signal of low angular frequency ω_L is applied, whereas numeral 35 denotes a transformed impedance of the case in which a signal of high angular frequency ω_H is applied, which is also obtained by this operation. The value of the inductance L_2 of the parallel inductor 27 and that of the capacitance C_1 of the parallel capacitor 28 are shown in the Formulae 7 below.

Further, it is arranged such that the series resonance circuit formed by the series inductor 25 and the series capacitor 26 becomes inductive at a low angular frequency ω_L and capacitive at a high angular frequency ω_H, and that the two impedances are, due to this, shifted along the constant resistance circle 33 so as to be matched with each other. Reference numeral 36 denotes a matching point obtained by this matching operation. The value of the inductance

L_1 of the series inductor and that of the capacitance C_1 of the series capacitor are shown also in the Formulae 7 below.

$$L_1=R_{ds}*Z_o*B_d/(\omega_H-\omega_L)$$

$$C_1=(\omega_H-\omega_L)/(\omega_H*\omega_L*R_{ds}*Z_o*B_d)$$

$$L_2=(\omega_H-\omega_L)/(\omega_H*\omega_L*B_d)$$

$$C_2=B_d/(\omega_H-\omega_L)-C_{ds}$$

$$B_d=(1/(Z_o*R_{ds})-1/(R_{ds}*R_{ds}))^{1/2} \quad \cdots \text{(Formulae 7)}$$

As is obvious from the Formulae 7, the two matching angular frequencies ω_L and ω_H can be set as individually separate angular frequencies from each other.

The operation of the matching circuit according to the third embodiment of the present invention is as follows.

When a signal from an FET transistor or the like is to be output from the output terminal 2, no reflected wave is generated at least on the basis of the output signal at the two matching frequencies.

As explained hereinabove, since according to the third embodiment of the present invention, an impedance matching operation is performed by a dual-frequency matching circuit which is so configured as comprising the input terminal 1 to which the loads 29 and 30 are connected, the output terminal 2 that outputs an output signal on the basis of the loads 29 and 30, the series resonance circuit, which is composed of the series capacitor 26 and the series inductor 25 connected in series to the series capacitor 26, and disposed in such a manner that it is connected in series to the loads 29 and 30 when observed from the output terminal 2 side, and a parallel resonance circuit, which is composed of the parallel capacitor 28 and the parallel inductor 27 connected in parallel to the parallel capacitor 28, and disposed in such a manner that it is connected to the loads 29 and 30 in parallel when observed from the output terminal

2 side, the matching operation can be performed with an output resistance (R_{ds}) of the loads 29 and 30 which is larger than the matching impedance at arbitrarily selected two frequencies.

Particularly, on condition that the resistance of the load resistance 30 is R_{ds}, the capacitance of the load capacitor 29 is C_{ds}, two matching angular frequencies are ω_L and ω_H, respectively, and the matching impedance is Z_0, since the inductance L_1 of the series inductor, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor, and the capacitance C_2 of the parallel capacitor are set in siuch a manner as to satisfy the above Formulae 7, the matching operation can be performed optimally at the target matching impedance value.

Further, since there is no need to use a transmission line as each of the inductor 25 and 27, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

[Fourth Embodiment]

Fig. 7 is a schematic diagram showing a dual-frequency matching circuit and a load connected thereto according to a fourth embodiment of the present invention.

In the figure, reference numeral 37 denotes a parallel inductor disposed between the input terminal 1 and the output terminal 2, numeral 38 denotes a parallel capacitor disposed between the input terminal 1 and the output terminal 2, numeral 39 denotes a series inductor whose one end is connected between the output terminal 2 and the parallel inductor 37, and reference numeral 40 denotes a series capacitor whose one end is connected to the other end of the series inductor 39, while the other end thereof is connected to the

ground potential. Other portions are same as those of the third embodiment, so that the detailed explanation thereabout is omitted here by simply putting the same reference numerals. It should be noted that the following explanation of the present embodiment the load resistance 30 is regulated as being smaller than the matching impedance (for example of 50Ω generally used for a transmission line of a microwave).

Fig. 8 is a Smith Chart for explaining the role of each of the circuit elements shown in Fig. 7, such as the series inductor 39, the series capacitor 40, the parallel inductor 37 and the parallel capacitor 38 when performing an impedance matching operation at two angular frequencies ω_H and ω_L in the dual-frequency matching circuit according to the fourth embodiment.

In Fig. 8, reference numeral 41 denotes a load impedance $Z_L(\omega_L)$ in a case that a signal of low angular frequency ω_L is applied to the load resistance 30 and the load capacitor 29, reference numeral 42 denotes a load impedance Z_L (ω_H) in a case in that a signal of high angular frequency ω_H is applied to the load resistance 30 and the load capacitor 29, and reference numeral 43 denotes a constant conductance circle (a constant conductance circle of 0.02S, for example), which is regulated by the matching impedance.

Here, it is arranged such that the parallel resonance circuit formed by the parallel inductor 37 and the parallel capacitor 38 becomes inductive at a low angular frequency ω_L and capacitive at a high angular frequency ω_H, and that the two impedances are, due to this, shifted on to the constant conductance circle 43. Reference numeral 44 denotes a thus obtained transformed impedance of the case that a signal of low angular frequency ω_L is applied, whereas numeral 45 denotes a transformed impedance of the case that a signal of high angular frequency ω_H is applied, which is also obtained by this

operation. The value of the inductance L_2 of the parallel inductor L_2 and that of the capacitance of the parallel capacitor C_2 are shown in the Formulae 8 below.

Further, it is arranged such that the series resonance circuit formed by the series inductor 39 and the series capacitor 40 becomes inductive at a low angular frequency ω_L and capacitive at a high angular frequency ω_H, and that due to this the two impedances are shifted along the constant conductance circle 43 so as to be matched with each other. Reference numeral 46 denotes a matching point obtained by this matching operation. The value of the inductance L_1 of the series inductor and that of the capacitance C_1 of the series capacitor are shown also in the Formulae 8 below.

$$L_1=(\omega_L*\alpha_L*X_{dH}+\omega_H*\alpha_H*X_{dL})/(Y_o*(\omega_H*\omega_H-\omega_L*\omega_L)*X_{dH}*X_{dL})$$

$$C_1=Y_o*(\omega_H*\omega_H-\omega_L*\omega_L)*X_{dH}*X_{dL}/(\omega_H*\omega_L*(\omega_H*\alpha_L*X_{dH}+\omega_L*\alpha_{dL}*X_{dL}))$$

$$L_2=(\omega_H*\omega_H-\omega_L*\omega_L)/(\omega_H*\omega_L*(\omega_L/(X_{dH}-\beta_H)+\omega_H/(X_{dL}+\beta_L)))$$

$$C_2=(\omega_H*(X_{dH}-\beta_H)+\omega_L/(X_{dL}+\beta_L))/(\omega_H*\omega_H-\omega_L*\omega_L)$$

$$\alpha=(1/R_{ds})/(1/(R_{ds}*R_{ds})+\omega*\omega*C_{ds}*C_{ds})$$

$$\beta=\omega*C_{ds}\ /(1/(R_{ds}R_{ds})+\omega*\omega*C_{ds}*C_{ds}))$$

$$X_d=(\alpha/Y_o-\alpha*\alpha)^{1/2} \qquad \cdots \text{(Formulae 8)}$$

As is obvious from the Formulae 8, the two matching angular frequencies ω_L, ω_H can be set as individually separate angular frequencies from each other.

The operation of the matching circuit according to the present invention is equivalent to that of the third embodiment, so that the detailed explanation thereof is omitted here.

As explained hereinabove, since according to the fourth embodiment of the present invention, an impedance matching operation is performed by a dual-frequency matching circuit which is so configured as comprising an input terminal 1 to which the loads 29

and 30 are connected, an output terminal 2 that outputs an output signal on the basis of the loads 29 and 30, a parallel resonance circuit that is composed of a parallel capacitor 38 and a parallel inductor 37 connected to the parallel capacitor 38, and disposed in such a manner that it is connected in series to the loads 29 and 30 when observed from the output terminal 2 side, and a series resonance circuit that is composed of the series capacitor 40 and the series inductor 39 connected to this series capacitor 40, and disposed in such a manner that it is connected in parallel to the entire portion of the loads 29 and 30 and the parallel resonance circuit formed by the circuit elements 37 and 38 when observed from the output terminal 2 side, the matching operation can be performed with an output resistance (R_{ds}) of the loads 29 and 30 which is smaller than the matching impedance at arbitrarily selected two frequencies.

Particularly, on condition that the resistance of the load resistance 30 is R_{ds}, the capacitance of the load capacitor 29 is C_{ds}, two matching angular frequencies are ω_L and ω_H, respectively, and the matching admittance is Y_0, since the inductance L_1 of the series inductor, the capacitance C_1 of the series capacitor, the inductance L_2 of the parallel inductor, and the capacitance C_2 of the parallel capacitor are set in such a manner as to satisfy the above Formulae 8, the matching operation can be performed optimally at the target matching impedance value.

Further, since there is no need to use a transmission line as each of the inductor 37 and 39, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

As is explained heretofore, since the dual-frequency matching circuit according to the present invention comprises an output

terminal to which a load is connected, an input terminal through which an input signal is input to the load, a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to the series capacitor and disposed in such a manner as to be connected in series to the load when observed from the input terminal side, and a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to the parallel capacitor, and disposed in such a manner as to be connected in parallel to the entire portion of the series resonance circuit and the load when observed from the input terminal side, the matching operation can be performed with an input resistance (Ri) of the load which is smaller than the matching impedance at arbitrarily selected two frequencies. Further, since there is no need to use a transmission line as one of the matching elements, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

Since the dual-frequency matching circuit according to the present invention comprises an output terminal to which the load is connected, an input terminal 1 through which an input signal to the load is input, a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to the parallel capacitor and disposed in such a manner as to be connected in series to the loads and when observed from the input terminal side, and a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to the series capacitor, and disposed in such a manner as to be connected in parallel to the load when observed from the input terminal side, the matching operation can be performed with an input resistance (Ri)

of the load which is larger than the matching impedance at arbitrarily selected two frequencies. Further, since there is no need to use a transmission line as each of the inductor, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

Since the dual-frequency matching circuit according to the present invention comprises an input terminal through which the total load is connected, an output terminal that outputs an output signal on the basis of the load, a series resonance circuit, which is composed of a series capacitor and a series inductor connected to the series capacitor and disposed in such a manner as to be connected in series to the load and when observed from the output terminal side, and a parallel resonance circuit, which is composed of the parallel capacitor and the parallel inductor connected in series to the parallel capacitor and disposed in such a manner as to be connected in parallel with the load when observed from the output terminal side, the matching operation can be performed with an output resistance (R_{ds}) of the load which is larger than the matching impedance at arbitrarily selected two frequencies. Further, since there is no need to use a transmission line as each of the inductor, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

Since the dual-frequency matching circuit according to the present invention comprises an input terminal through which the total load is connected, an output terminal that outputs an output signal on the basis of the load, a parallel resonance circuit, which is

composed of a parallel capacitor and a parallel inductor connected to the parallel capacitor and disposed in such a manner as to be connected in series to the load when observed from the output terminal side, and a series resonance circuit, which is composed of the series capacitor and the series inductor and disposed in such a manner as to be connected in parallel to the entire portion of the load and the parallel resonance circuit when observed from the output terminal side, the matching operation can be performed with an input resistance (R_{ds}) of the load which is larger than the matching impedance at arbitrarily selected two frequencies. Further, since there is no need to use a transmission line as each of the inductor, even though the frequency at which the matching operation is performed is set to a low frequency band, a considerably long transmission line is no longer needed, so that the circuit can be minimized when applied in the low frequency band.

Industrial Applicability

As explained heretofore, a dual-frequency matching circuit according to the present invention enables impedance matching at two separate frequencies simultaneously, so that it can be suitably used in the microwave band.

What is claimed is;

1. A dual-frequency matching circuit comprising:

an output terminal to which a load is connected,

an input terminal through which an input signal is input to the load,

a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to said series capacitor and disposed as being connected in series to the load when observed from the input terminal side, and

a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to said parallel capacitor, and disposed as being connected in parallel to the entire portion of said load and said series resonance circuit when observed from the input terminal side.

2. A dual-frequency matching circuit according to claim 1, wherein on condition that said load is formed by a load resistor and a load capacitor mutually connected in series, and that the resistance of said load resistance is Ri, the capacitance of the load capacitor is C_{gs}, two matching angular frequencies are ω_L and ω_H, respectively, and matching admittance is Y_0, the inductance L_1 of said series inductor, the capacitance C_1 of said series capacitor, the inductance L_2 of said parallel inductor, and the capacitance C_2 of said parallel capacitor are set in such a manner as to satisfy the following formulae:

$$L_1=X_g/(\omega_H-\omega_L)$$

$$C_1=(\omega_H-\omega_L)*C_{gs}/(C_{gs}*\omega_H*\omega_L*X_g-(\omega_H-\omega_L))$$

$$L_2=(\omega_H-\omega_L)*R_i/(\omega_H*\omega_L*Y_o*X_g)$$

$$C_2=Y_o*X_g/((\omega_H-\omega_L)*R_i)$$

$$X_g=(R_i/Y_0-R_i*R_i)^{1/2}$$

3. A dual-frequency matching circuit comprising:

an output terminal to which a load is connected,

an input terminal through which an input signal is input to the load,

a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to said parallel capacitor and disposed as being connected in series to the load when observed from the input terminal side, and

a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to said series capacitor and disposed as being connected in parallel to the load when observed from the input terminal side.

4. A dual-frequency matching circuit according to claim 3, wherein on condition that said load is formed by a load resistor and a load capacitor mutually connected in series, and that the resistance of the load resistance is Ri, the capacitance of the load capacitor is C_{gs}, two matching angular frequencies are ω_L and ω_H, respectively, and matching impedance is Z_0, the inductance L_1 of said series inductor, the capacitance C_1 of said series capacitor, the inductance L_2 of said parallel inductor, and the capacitance C_2 of said parallel capacitor are set in such a manner as to satisfy the following formulae:

$$L_1=(\omega_H*(\beta_L-B_{gL})-\omega_L*(\beta_H+B_{gH}))/((\omega_H*\omega_H-\omega_L*\omega_L)(\beta_L-B_{gL})(\beta_H+B_{gH}))$$

$$C_1=(\omega_H*\omega_H-\omega_L*\omega_L)(\beta_L-B_{gL})(\beta_H+B_{gH})\ /(\omega_H*\omega_L*(\omega_L*(\beta_L-B_{gL})-\omega_H*(\beta_H+B_{gH})))$$

$$L_2=Z_o*(\omega_H*\omega_H-\omega_L*\omega_L)*B_{gH}*B_{gL}/(\omega_H*\omega_L*(\omega_H*\alpha_L*B_{gH}+\omega_L*\alpha_H*B_{gL}))$$

$$C_2=(\omega_L*\alpha_L*B_{gH}+\omega_H*\alpha_H*B_{gL})/(Z_o*(\omega_H*\omega_H-\omega_L*\omega_L)*B_{gH}*B_{gL})$$

$$\alpha=R_i\ /(R_i*R_i+1/(\omega*\omega*C_{gs}*C_{gs}))$$

$$\beta=(1/(\omega*C_{gs}))/(R_i*R_i+1/(\omega*\omega*C_{gs}*C_{gs}))$$

$$B_g=(\alpha/Z_o-\alpha*\alpha)^{1/2}$$

5. A dual-frequency matching circuit comprising:

an input terminal to which a load is connected,

an output terminal that outputs an output signal on the basis of the load,

a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to said series capacitor and disposed as being connected in series to the load when observed from the output terminal side, and

a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to said parallel capacitor and disposed as being connected in parallel to the load when observed from the output terminal side.

6. A dual-frequency matching circuit according to claim 5, wherein on condition that the load is formed by a load capacitor and a load resistor mutually connected in parallel, one end of said both load capacitor and load resistor being connected to the input terminal in series, and that the resistance of said load resistance is R1, the capacitance of the load capacitor is C_{gs}, two matching angular frequencies are ω_L and ω_H, respectively, and matching admittance is Y_0, the inductance L_1 of said series inductor, the capacitance C_1 of said series capacitor, the inductance L_2 of said parallel inductor, and the capacitance C_2 of said parallel capacitor are set in such a manner as to satisfy the following formulae:

$$L_1=R_{ds}*Z_o*B_d/(\omega_H-\omega_L)$$

$$C_1=(\omega_H-\omega_L)/(\omega_H*\omega_L*R_{ds}*Z_o*B_d)$$

$$L_2=(\omega_H-\omega_L)/(\omega_H*\omega_L*B_d)$$

$$C_2=B_d/(\omega_H-\omega_L)-C_{ds}$$

$$B_d=(1/(Z_o*R_{ds})-1/(R_{ds}*R_{ds}))^{1/2}$$

7. A dual-frequency matching circuit comprising:

an input terminal to which a load is connected,

an output terminal that outputs an output signal on the basis of the load,

a parallel resonance circuit, which is composed of a parallel capacitor and a parallel inductor connected in parallel to said parallel capacitor and disposed as being connected in series to the load when observed from said output terminal side, and

a series resonance circuit, which is composed of a series capacitor and a series inductor connected in series to said series capacitor and disposed as being connected in parallel to the load and said parallel resonance circuit when observed from the output terminal side.

8. A dual-frequency matching circuit according to claim 7, wherein on condition that the load is formed by a load capacitor and a load resistor mutually connected in parallel, one end of said both load capacitor and load resistor being connected to the input terminal in series, and that the resistance of said load resistance is Ri, the capacitance of the load capacitor is C_{gs}, two matching angular frequencies are ω_L and ω_H, respectively, and matching admittance is Y_0, the inductance L_1 of said series inductor, the capacitance C_1 of said series capacitor, the inductance L_2 of said parallel inductor, and the capacitance C_2 of said parallel capacitor are set in such a manner as to satisfy the following formulae:

$$L_1=(\omega_L*\alpha_L*X_{dH}+\omega_H*\alpha_H*X_{dL})/(Y_o*(\omega_H*\omega_H-\omega_L*\omega_L)*X_{dH}*X_{dL})$$

$$C_1=Y_o*(\omega_H*\omega_H-\omega_L*\omega_L)*X_{dH}*X_{dL}/(\omega_H*\omega_L*(\omega_H*\alpha_L*X_{dH}+\omega_L*\alpha_{dL}*X_{dL}))$$

$$L_2=(\omega_H*\omega_H-\omega_L*\omega_L)/(\omega_H*\omega_L*(\omega_L/(X_{dH}-\beta_H)+\omega_H/(X_{dL}+\beta_L)))$$

$$C_2=(\omega_H*(X_{dH}-\beta_H)+\omega_L/(X_{dL}+\beta_L))/(\omega_H*\omega_H-\omega_L*\omega_L)$$

$$\alpha = (1/R_{ds}) / (1/(R_{ds} * R_{ds}) + \omega * \omega * C_{ds} * C_{ds})$$

$$\beta = \omega * C_{ds} / (1/(R_{ds} R_{ds}) + \omega * \omega * C_{ds} * C_{ds}))$$

$$X_d = (\alpha / Y_o - \alpha * \alpha)^{1/2}$$

FIG.1

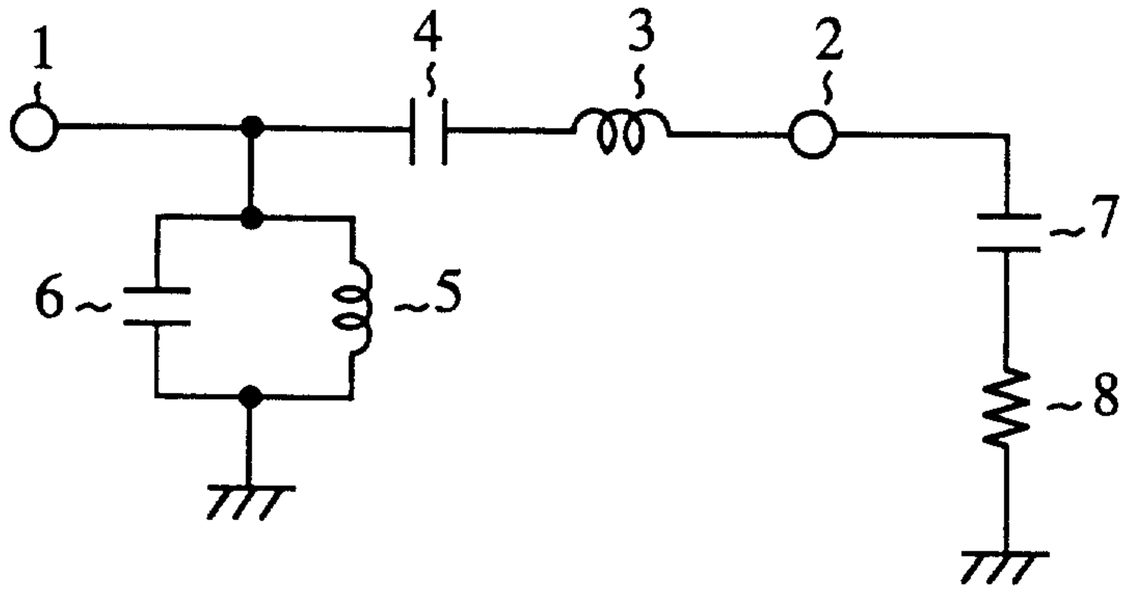


FIG.2

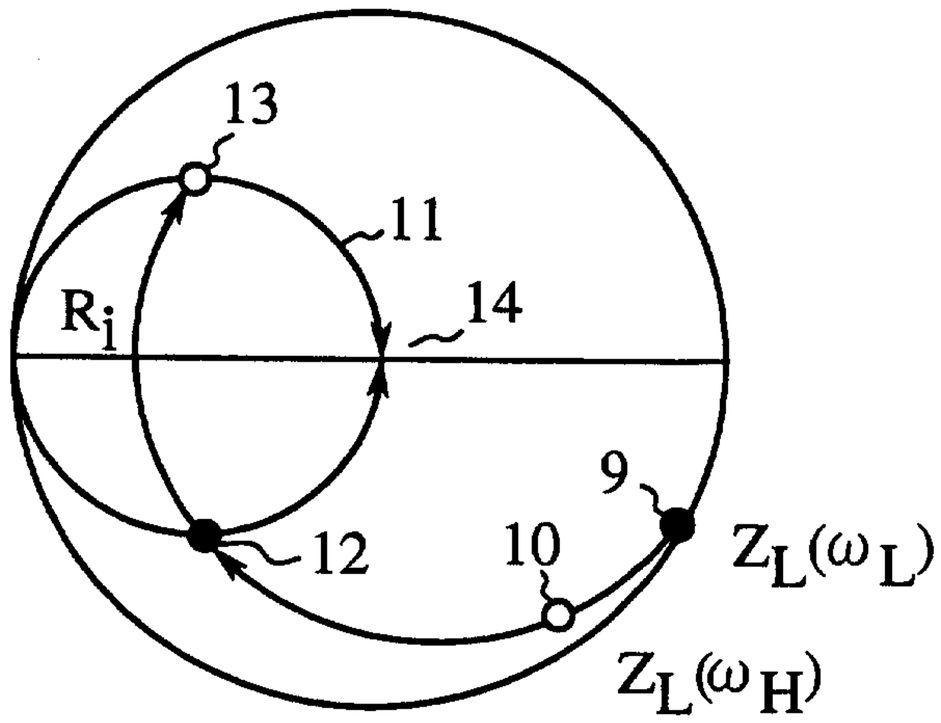


FIG.3

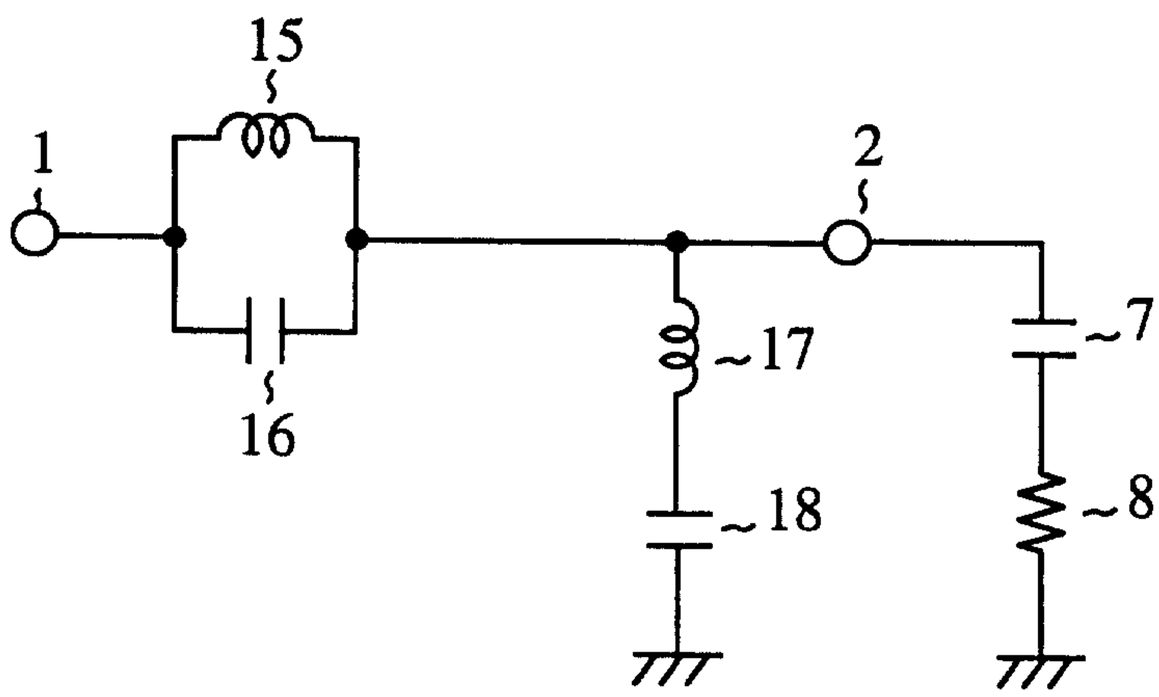


FIG.4

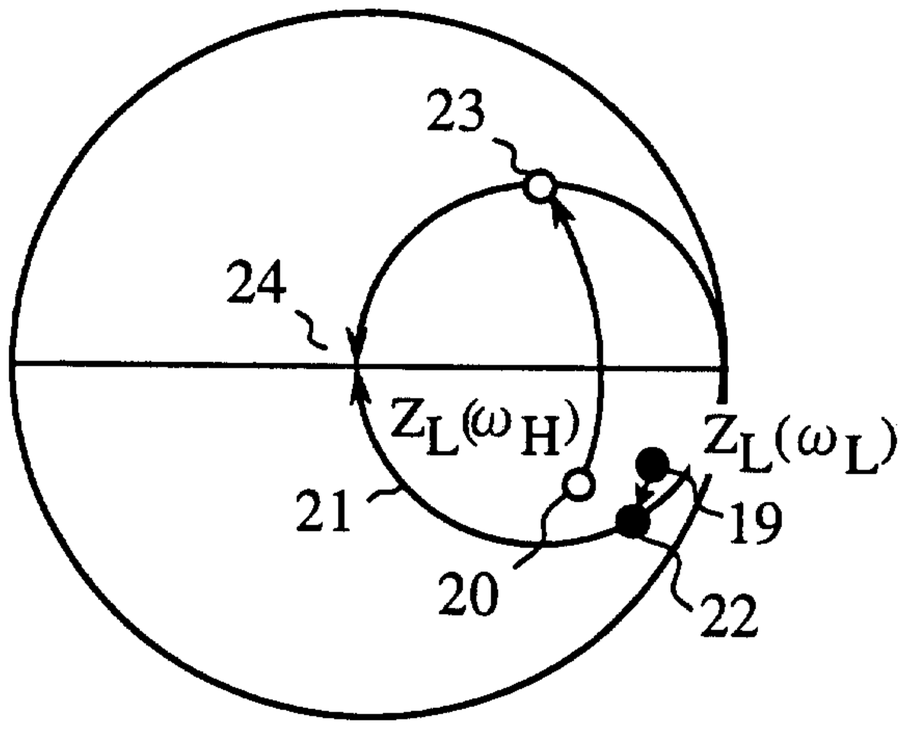


FIG.5

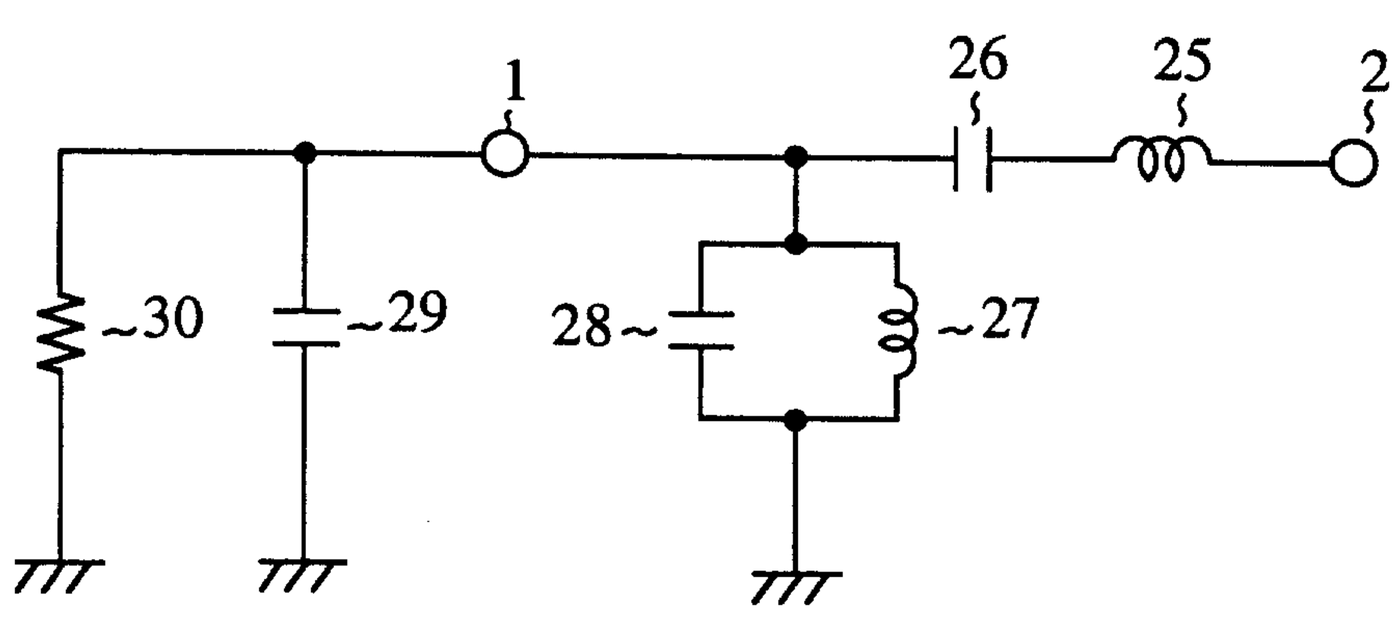


FIG.6

FIG.7

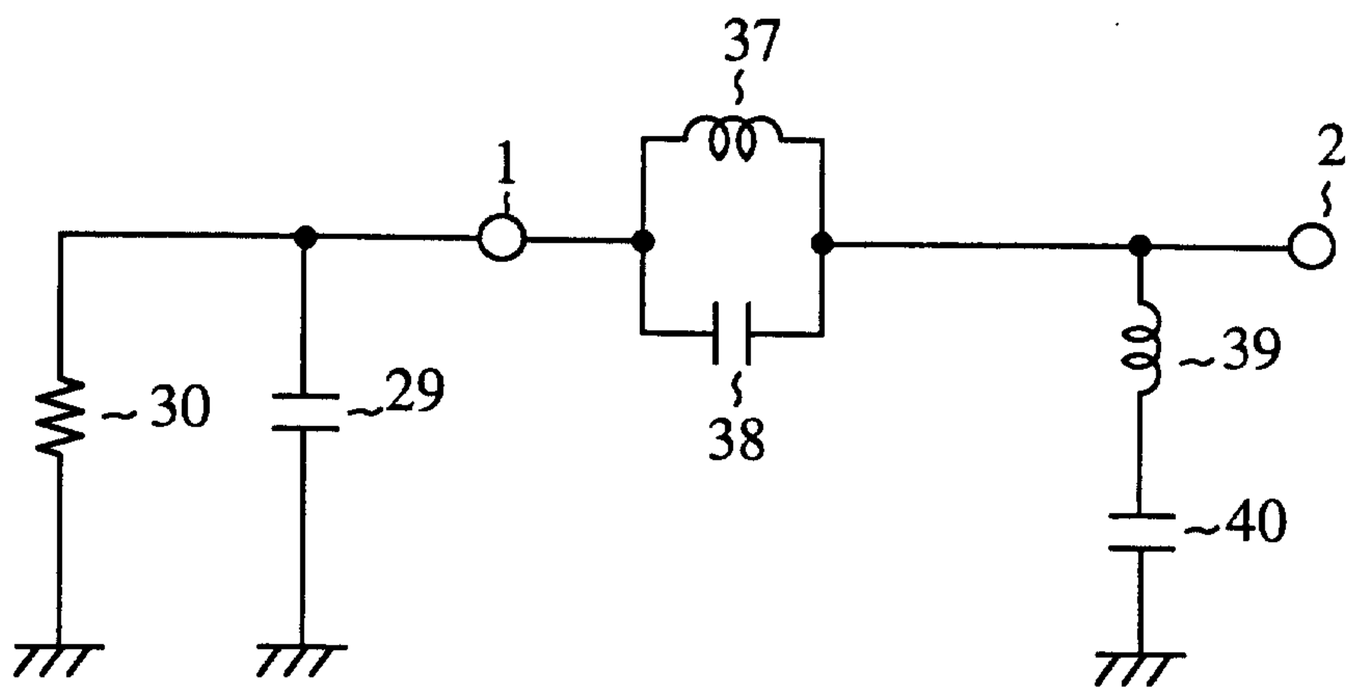


FIG.8

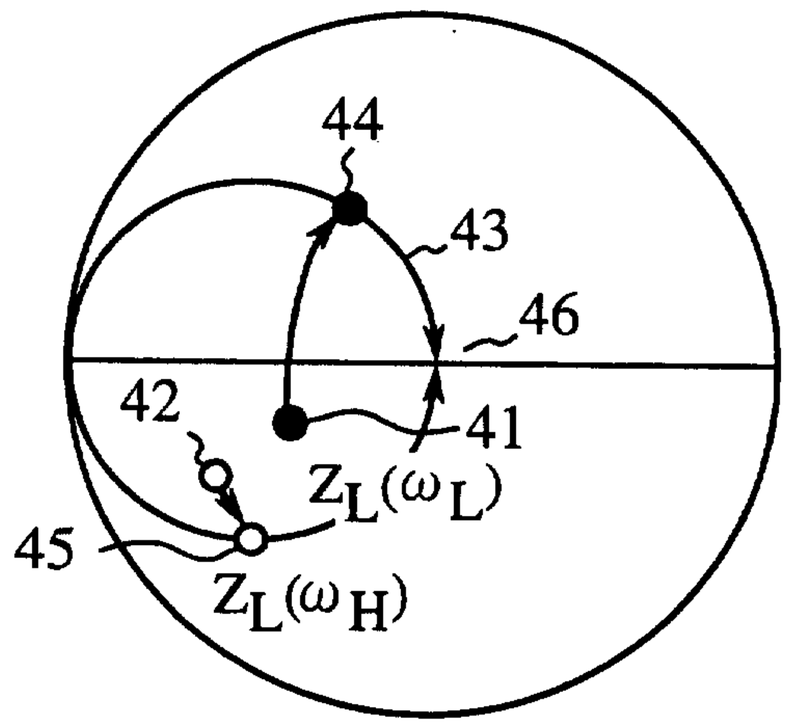


FIG.9

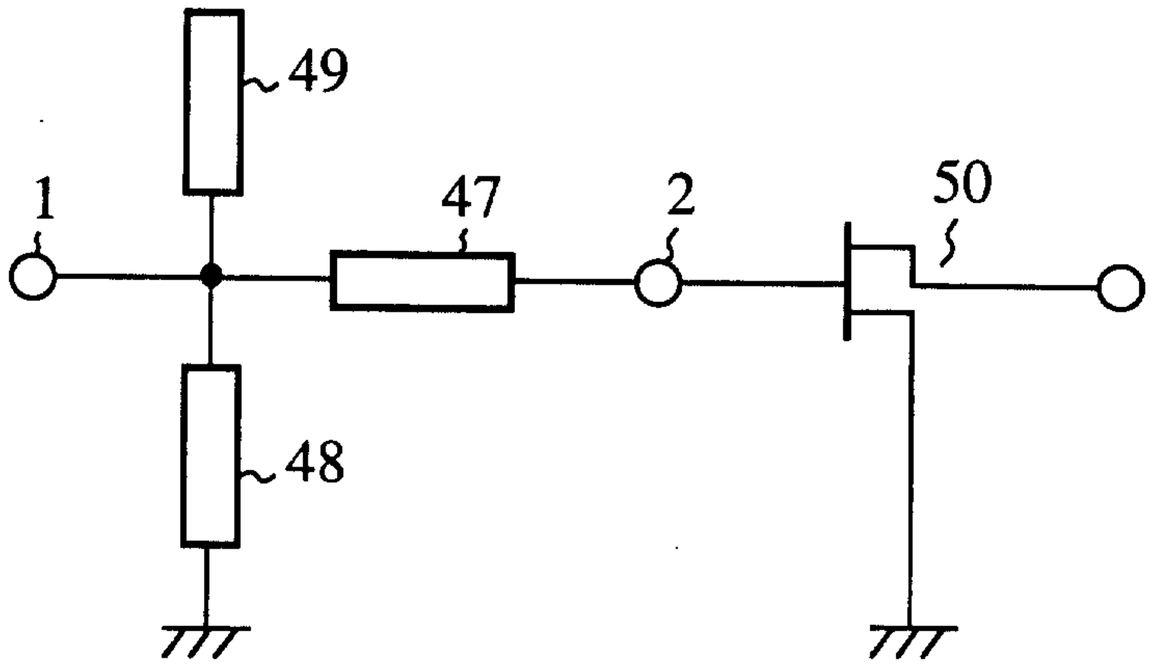


FIG.10

