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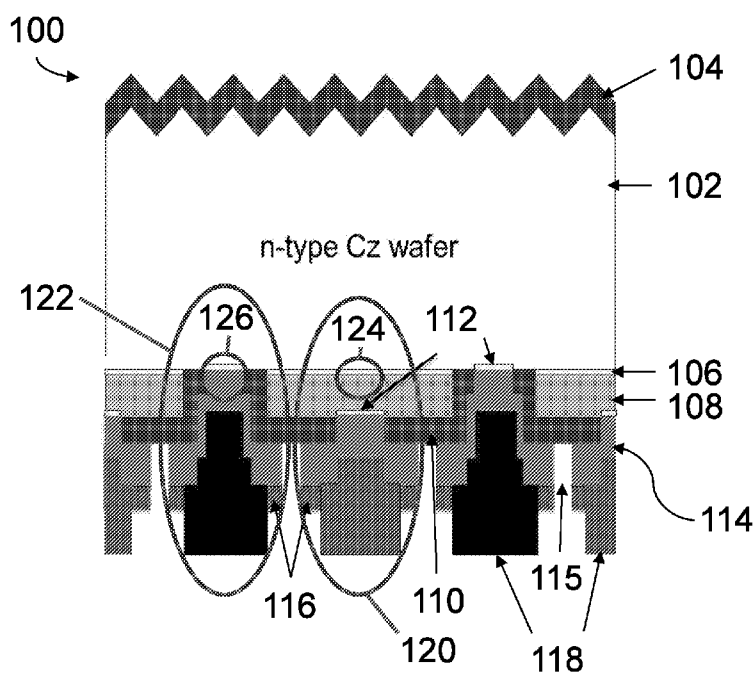


Figure 1

(57) Abstract: A method for fabricating a solar cell (100) is disclosed. The method comprises depositing sequentially a rear surface dielectric tunnel layer (106), a first doped semiconductor layer (108), a dielectric tunnel layer (112) and a second doped semiconductor layer (114) to form a plurality of interdigitated contacts. The interdigitated contacts comprise alternating tunnel junction augmented passivated contacts (120) and conventional passivated contacts (122). Each tunnel junction augmented passivated contact (120) comprises the rear surface dielectric tunnel layer (106), the first doped semiconductor layer (108) and the second doped semiconductor layer (114). Each conventional passivated contact (122) comprises the second doped semiconductor layer (108) and the dielectric tunnel layer (112). Conventional passivated contacts (122) are formed at openings (302) of the first doped semiconductor layer (108) and openings (302) of the rear surface dielectric tunnel layer (106). A tandem solar cell with said solar cell as bottom cell is also disclosed.



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Solar cell and Method for fabricating a solar cell

Technical Field

The present disclosure relates to a solar cell and also a method for fabricating a solar cell, in particular, an all-back-contact (ABC) solar cell with tunnel layer passivated contacts.

Background

The photovoltaic market is currently dominated by wafer based, crystalline silicon (Si) solar cells. In order to realise Si solar cells having an ultra-high efficiency which reaches the theoretical Auger efficiency limit of 29%, an all-back-contact (ABC) solar cell architecture may be deployed. By using the ABC solar cell architecture, which involves placing both electron extraction contacts and hole extraction contacts on a rear side of the solar cell, no metal contacts at the front side of the solar cells are used. This minimizes any front-side shading effects and leads to a high efficiency potential by gaining short-circuit current due to a higher photon absorption, which results in a higher excess carrier generation rate within the silicon wafer of the ABC solar cell.

However, using an ABC solar cell architecture typically comes with a cost of introducing additional complex steps in fabricating these solar cells. For example, multiple functional layers have to be deposited and patterned on the rear side of these solar cells in order to form both electron extraction and hole extraction contacts on the rear side of the solar cell.

It is therefore desirable to provide a simple method for fabricating an ABC solar cell and an ABC solar cell which address the problems of the prior art and/or provides the public with a useful alternative.

Furthermore, other desirable features and characteristics will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and this background of the disclosure.

Summary

In accordance with a first aspect there is provided a method for fabricating a solar cell, the solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side, the method comprising:

5 (i) depositing a rear surface dielectric tunnel layer on a surface of the rear side of the silicon wafer;

(ii) depositing a first doped semiconductor layer on the rear surface dielectric tunnel layer;

(iii) depositing a dielectric tunnel layer on the first doped semiconductor layer; and

10 (iv) depositing a second doped semiconductor layer on the dielectric tunnel layer to form a plurality of interdigitated contacts on the rear side of the silicon wafer, the second doped semiconductor layer having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the plurality of interdigitated contacts comprises alternating tunnel
15 junction augmented passivated contacts and conventional passivated contacts, each of the tunnel junction augmented passivated contacts comprises the rear surface dielectric tunnel layer, the first doped semiconductor layer and the second doped semiconductor layer, and each of the conventional passivated contacts comprises the dielectric tunnel layer and the second doped semiconductor layer, the conventional passivated contacts
20 being formed at openings of the first doped semiconductor layer and openings of the rear surface dielectric tunnel layer.

In particular, the first doped semiconductor layer and the second doped semiconductor layer are of opposite polarity, and each of the doped semiconductor layers deposited is part of a corresponding contact passivation layer stack, i.e. of the tunnel junction
25 augmented passivated contacts as well as of the conventional passivated contacts respectively. The contact passivation layer stack of the tunnel junction augmented passivated contacts comprises the rear surface dielectric tunnel layer and the first doped semiconductor layer (e.g. hole extracting), while the contact passivation layer stack of the conventional passivated contacts comprises the dielectric tunnel layer and the
30 second doped semiconductor layer (e.g. electron extracting). Therefore, by forming the conventional passivated contacts in the openings of the first doped semiconductor layer and the openings of the rear surface dielectric tunnel layer, alternating electron and hole extracting interdigitated contacts can be formed. Further, each of the tunnel junction

augmented passivated contacts comprises a tunnel junction formed by the first doped semiconductor layer and the second doped semiconductor layer. In some embodiments as described below, the tunnel junction comprises the first doped semiconductor layer, the dielectric tunnel layer and the second doped semiconductor layer. As will be shown in Figure 1, this tunnel junction is formed on the contact passivation layer stack and it comprises the first doped semiconductor layer which also forms part of the contact passivation layer stack (i.e. the first doped semiconductor layer and the rear surface dielectric tunnel layer) of the tunnel junction augmented passivated contact. Holes (e.g. if the first doped semiconductor layer is p-doped) or electrons (e.g. if the first doped semiconductor layer is n-doped) can then be extracted via the tunnel junction from the contact passivation layer stack of the tunnel junction augmented passivated contact. In this way, the second doped semiconductor layer is formed at the top of both the tunnel junction augmented passivated contacts and the conventional passivated contacts on the rear side of the Si wafer so that an interdigitated metal layer grid which is subsequently deposited to form electrical contacts for these interdigitated contacts of the solar cell can contact the same second doped semiconductor layer. This significantly minimizes the number and complexity of patterning steps in order to realize an ABC tunnel layer contact passivated silicon wafer based solar cell. The deposition of the aforementioned layers can be performed on a full area of the rear side of the silicon wafer without having to adhere to tight alignment tolerances. The aforementioned method also minimizes / eliminates the use of masking layers which are required to be subsequently removed, thereby significantly reduces the number of process steps in the fabrication of the ABC Si wafer based solar cell.

Further, in addition to using the ABC solar cell architecture, the described embodiment incorporates contact passivation layer stacks for each of the interdigitated contacts in the above steps. By deploying contact passivation layer stacks in each of the interdigitated contacts, recombination at these contacts can be minimised to improve the open-circuit voltage and thus the efficiency of the ABC solar cell. In particular, the contact passivation layer stacks in the above embodiment are formed by depositing a dielectric tunnel layer (e.g. either a wet-chemically formed or a thermally grown or an ozone assisted grown ultra-thin SiO_x or any atomic layer deposited ultra-thin tunnel layer, like AlO_x , SiN_x , TiO_x , etc..) and depositing a doped semiconductor layer on top of it (e.g. highly-doped polysilicon (poly-Si) deposited using low pressure chemical vapor deposition (LPCVD) or

plasma-enhanced chemical vapor deposition (PECVD)). The doped semiconductor layers of the contact passivation layer stacks of the interdigitated contacts (one for electron extraction and one for hole extraction) is then in one case contacted directly by a metal contact (for one polarity, for example for electron extraction) to form the conventional passivated contacts and in the other case via a tunnel junction for the other polarity (for example hole extraction) to form the tunnel junction augmented passivated contacts. The contact passivation layer stack of the interdigitated contacts not only provides an excellent surface passivation towards the crystalline silicon wafer (with recombination current densities j_0 in the order of a few fs cm^{-2} only), but also provides a reasonable low contact resistivity (in the order of some ten or some hundred $\text{m}\Omega \text{ cm}^2$) and thus enables a high excess carrier extraction selectivity (i.e. are able to extract only electrons or only holes at the contact, with an excess carrier extraction selectivity higher than 12).

By combining the architecture of an all-back-contact (ABC) solar cell with the tunnel junction augmented passivated contacts and conventional passivated contacts, the resulting all-back-contact (ABC) solar cell architecture of the present embodiment not only minimizes optical losses (having no front-contact and thus no shadowing effect, i.e. enabling an ultra-high short-circuit current), but also significantly minimizes recombination at the metal contacts (i.e. enabling an ultra-high open-circuit voltage), so as to achieve an ultra-high efficiency solar cell. Furthermore, by deploying a tunnel junction in order to extract one polarity (either electrons or holes), the amount of processing steps and alignments needed in order to form an ABC cell are significantly reduced, as further detailed below.

Each of the tunnel junction augmented passivated contacts may comprise the dielectric tunnel layer sandwiched between the first doped semiconductor layer and the second doped semiconductor layer. By including the dielectric tunnel layer in the tunnel junction augmented passivated contacts, the amount of processing steps and alignments needed in order to form an ABC cell can be further reduced, as compared to an embodiment which includes the tunnel junction augmented passivated contact without the dielectric tunnel layer, as described below.

The method may comprise forming openings in the dielectric tunnel layer prior to depositing the second doped semiconductor layer such that each of the tunnel junction

augmented passivated contacts formed comprises the second doped semiconductor layer deposited directly on the first doped semiconductor layer.

The method may comprise forming the openings of the rear surface dielectric layer or the openings of the first doped semiconductor layer using a femtosecond laser having an ultraviolet wavelength. Forming the openings of the rear surface dielectric layer or the openings of the first doped semiconductor layer using the femtosecond laser minimizes / eliminates the use of masking layers which are required to be subsequently removed, thereby significantly reducing the number of process steps in the fabrication of the ABC Si wafer based solar cell. Further, by using a femtosecond laser having an ultraviolet wavelength for forming the aforementioned openings, surface damage created by the femtosecond laser is minimized.

The method may comprise depositing an intermediate dielectric layer between each of the alternating tunnel junction augmented passivated contacts and the conventional passivated contacts, wherein the tunnel junction augmented passivated contacts and the conventional passivated contacts are formed at openings of the intermediate dielectric layer. The intermediate dielectric layer advantageously isolates the alternating tunnel junction augmented passivated contacts and the conventional passivated contacts to minimize shunting between these alternating contacts. This also enables the interdigitated metal layer grid, which is subsequently deposited to form electrical contacts for these interdigitated contacts of the solar cell, to have the same surface area for both polarities to extract carriers.

The method may comprise: depositing a contact dielectric layer on the plurality of interdigitated contacts; and depositing an interdigitated metal layer grid on the contact dielectric layer to form electrical contacts for the plurality of interdigitated contacts.

The silicon wafer may be n-doped, and depositing the first doped semiconductor layer may comprise depositing a p-doped polysilicon layer and depositing the second-doped semiconductor layer may comprise depositing an n-doped polysilicon layer.

Depositing the second doped semiconductor layer may comprise depositing the second doped semiconductor layer on an entire area of the rear side of the silicon wafer, and the method may comprise forming isolation trenches in the second doped semiconductor layer to form the plurality of interdigitated contacts.

The method may comprise texturing the front side of the silicon wafer.

The method may comprise texturing the rear side of the silicon wafer.

In accordance with a second aspect, there is provided a solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side, the solar cell comprising:

a rear surface dielectric tunnel layer deposited on a surface of the rear side of the silicon wafer;

a first doped semiconductor layer deposited on the rear surface dielectric tunnel layer;

a dielectric tunnel layer deposited on the first doped semiconductor layer; and

a second doped semiconductor layer deposited on the dielectric tunnel layer to form a plurality of interdigitated contacts on the rear side of the silicon wafer, the second doped semiconductor layer having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the plurality of interdigitated contacts comprises alternating tunnel junction augmented passivated contacts and conventional passivated contacts, each of the tunnel junction augmented passivated contacts comprises the rear surface dielectric tunnel layer, the first doped semiconductor layer and the second doped semiconductor layer, and each of the conventional passivated contacts comprises the dielectric tunnel layer and the second doped semiconductor layer, the conventional passivated contacts being formed at openings of the first doped semiconductor layer and openings of the rear surface dielectric tunnel layer.

Thus, the described embodiment provides a solar cell. In particular, the solar cell comprises a plurality of interdigitated contacts formed at the rear side of the solar cell.

As described above, the first doped semiconductor layer and the second doped semiconductor layer are of opposite polarity, and each of these semiconductor layers deposited is part of a contact passivation layer stack of the tunnel junction augmented passivated contacts and the conventional passivated contacts respectively. Therefore, by forming the conventional passivated contacts in the openings of the first doped semiconductor layer and the openings of the rear surface dielectric tunnel layer, alternating electron and hole extracting interdigitated contacts can be formed. Further, each of the tunnel junction augmented passivated contacts comprises a tunnel junction,

where the tunnel junction comprises the first doped semiconductor layer and the second doped semiconductor layer. Holes (e.g. if the first doped semiconductor layer is p-doped) or electrons (e.g. if the first doped semiconductor layer is n-doped) can be extracted via the tunnel junction from the contact passivation layer stack of the tunnel junction augmented passivated contact. In this way, the second doped semiconductor layer is formed at the top of both the tunnel junction augmented passivated contacts and the conventional passivated contacts on the rear side of the Si wafer so that an interdigitated metal layer grid which is subsequently deposited to form electrical contacts for these interdigitated contacts of the solar cell can contact the same second doped semiconductor layer. This significantly minimizes the number and complexity of patterning steps in order to realize an ABC tunnel layer contact passivated silicon wafer based solar cell. The deposition of the aforementioned layers can also be performed on a full area of the rear side of the silicon wafer without having to adhere to tight alignment tolerances.

Further, by deploying contact passivation layer stacks in each of the interdigitated contacts, recombination at these contacts can be minimised to improve the open-circuit voltage and thus the efficiency of the ABC solar cell. The contact passivation layer stacks of the interdigitated contacts not only provide an excellent surface passivation towards the crystalline silicon wafer (with recombination current densities j_0 in the order of a few fs cm^{-2} only), but also provide a reasonable low contact resistivity (in the order of some ten or some hundred $\text{m}\Omega \text{ cm}^2$) and thus enable a high excess carrier extraction selectivity (i.e. are able to extract only electrons or only holes at the contact, with an excess carrier extraction selectivity higher than 12).

Each of the tunnel junction augmented passivated contacts may comprise the dielectric tunnel layer sandwiched between the first doped semiconductor layer and the second doped semiconductor layer.

The solar cell may comprise openings formed in the dielectric tunnel layer prior to the second doped semiconductor layer being deposited on the dielectric tunnel layer, such that each of the tunnel junction augmented passivated contacts formed may comprise the second doped semiconductor layer deposited directly on the first doped semiconductor layer.

The openings of the rear surface dielectric layer or the openings of the first doped semiconductor layer may be formed using a femtosecond laser having an ultraviolet wavelength.

5 The solar cell may comprise an intermediate dielectric layer deposited between each of the alternating tunnel junction augmented passivated contacts and the conventional passivated contacts, wherein the tunnel junction augmented passivated contacts and the conventional passivated contacts are formed at openings of the intermediate dielectric layer. The intermediate dielectric layer advantageously minimizes shunting between the alternation tunnel junction augmented passivated contacts and the conventional
10 passivated contacts.

The solar cell may comprise: a contact dielectric layer deposited on the plurality of interdigitated contacts; and an interdigitated metal layer grid deposited on the contact dielectric layer to form electrical contacts for the plurality of interdigitated contacts.

15 The silicon wafer may be n-doped, and the first doped semiconductor layer may comprise a p-doped polysilicon layer and the second doped semiconductor layer may comprise an n-doped polysilicon layer.

The second doped semiconductor layer may be deposited on an entire area of the rear side of the silicon wafer, and the solar cell may comprise isolation trenches formed in the second doped semiconductor layer for forming the plurality of interdigitated contacts.

20 The front side of the silicon wafer may be textured.

The rear side of the silicon wafer may be textured.

In accordance with a third aspect, there is provided a tandem solar cell comprising:

- a top solar cell; and
- a bottom solar cell, wherein the bottom solar cell comprises a silicon wafer having
25 a front side arranged to receive incident light via the top solar cell and a rear side, the bottom solar cell comprising:
 - a rear surface dielectric tunnel layer deposited on a surface of the rear side of the silicon wafer;
 - a first doped semiconductor layer deposited on the rear surface dielectric tunnel
30 layer;

a dielectric tunnel layer deposited on the first doped semiconductor layer; and
a second doped semiconductor layer deposited on the dielectric tunnel layer to form a plurality of interdigitated contacts on the rear side of the silicon wafer, the second doped semiconductor layer having a doping of an opposite polarity to the first doped semiconductor layer,

5 wherein the plurality of interdigitated contacts comprises alternating tunnel junction augmented passivated contacts and conventional passivated contacts, each of the tunnel junction augmented passivated contacts comprises the rear surface dielectric tunnel layer, the first doped semiconductor layer and the second doped semiconductor layer, and each of the conventional passivated contacts comprises the dielectric tunnel layer and the second doped semiconductor layer, the passivated contacts being formed at openings of the first doped semiconductor layer and openings of the rear surface dielectric tunnel layer.

Thus, the described embodiment provides a tandem solar cell. In particular, the tandem solar cell comprises a bottom solar cell where the bottom solar cell includes a plurality of interdigitated contacts formed at the rear side of the bottom solar cell. As described above, the first doped semiconductor layer and the second doped semiconductor layer are of opposite polarity, and each of these semiconductor layers deposited is part of a contact passivation layer stack of the tunnel junction augmented passivated contacts and the conventional passivated contacts respectively. Therefore, by forming the conventional passivated contacts in the openings of the first doped semiconductor layer and the openings of the rear surface dielectric tunnel layer, alternating electron and hole extracting interdigitated contacts can be formed. Further, each of the tunnel junction augmented passivated contacts comprises a tunnel junction formed by the first doped semiconductor layer and the second doped semiconductor layer. Holes (e.g. if the first doped semiconductor layer is p-doped) or electrons (e.g. if the first doped semiconductor layer is n-doped) can be extracted via the tunnel junction from the contact passivation layer stack of the tunnel junction augmented passivated contact. In this way, the second doped semiconductor layer is formed at the top of both the tunnel junction augmented passivated contacts and the conventional passivated contacts on the rear side of the Si wafer so that an interdigitated metal layer grid which is subsequently deposited to form electrical contacts for these interdigitated contacts of the solar cell can contact the same second doped semiconductor layer. This significantly minimizes the number and

complexity of patterning steps in order to realize an ABC tunnel layer contact passivated silicon wafer based solar cell, which may form a bottom solar cell of the tandem solar cell. The deposition of the aforementioned layers can also be performed on a full area of the rear side of the silicon wafer without having to adhere to tight alignment tolerances.

- 5 Further, by deploying contact passivation layer stacks in each of the interdigitated contacts, recombination at these contacts can be minimised to further improve the open-circuit voltage and thus the efficiency of the ABC solar cell. The contact passivation layer stack of the interdigitated contacts not only provides an excellent surface passivation towards the crystalline silicon wafer (with recombination current densities j_0 in the order
10 of a few fs cm^{-2} only), but also provides a reasonable low contact resistivity (in the order of some ten or some hundred $\text{m}\Omega \text{ cm}^2$) and thus enables a high excess carrier extraction selectivity (i.e. are able to extract only electrons or only holes at the contact, with an excess carrier extraction selectivity higher than 12).

- 15 The top solar cell and the bottom solar cell may be integrated to form a three-terminal tandem solar cell structure.

- It should be appreciated that features relating to one aspect may be applicable to the other aspects. Embodiments therefore provide a method for fabricating an ABC solar cell with interdigitated contacts, where the interdigitated contacts comprise alternating tunnel junction augmented passivated contacts and conventional passivated contacts. By
20 forming the conventional passivated contacts in openings of the first doped semiconductor layer and in the openings of the rear surface dielectric tunnel layer, the alternating tunnel junction augmented passivated contacts and the conventional passivated contacts can be formed upon the deposition of the second doped semiconductor layer, thereby minimizes the number and complexity of patterning steps
25 in order to realize an ABC contact passivated silicon wafer based solar cell. The deposition of the aforementioned layers can be performed on a full area of the rear side of the silicon wafer without adhering to tight alignment tolerances. The method as described also minimizes the use of masking layers which are required to be subsequently removed, thereby reducing the number of process steps in the fabrication
30 of the Si wafer based solar cell. Further, in addition to using the ABC solar cell architecture, the aforementioned method incorporates contact passivation. By deploying contact passivation, in the form of contact passivation layer stacks comprised in the

tunnel junction augmented passivated contacts and the conventional passivated contacts, there is no diffused area within the wafer underneath the solar cell contacts, which enables the solar cell to reach higher open-circuit voltages due to reduced contact and bulk recombination. Thus, as compared to conventionally diffused ABC solar cells, the efficiency potential of the solar cell is higher, and the resulting process sequence to realize such cells is leaner (i.e. requiring less process steps).

Brief description of the drawings

Embodiments will now be described, by way of example only, with reference to the following drawings, in which:

- 10 Figure 1 is a schematic structure of a solar cell in accordance with an embodiment;

Figure 2 is a flowchart showing steps of a method for fabricating the solar cell of Figure 1 in accordance with a first embodiment;

Figures 3A to 3L are schematic diagrams which illustrate the method of Figure 2 for fabricating the solar cell of Figure 1;
- 15 Figure 4 is a flowchart showing steps of a method for fabricating a solar cell similar to the solar cell of Figure 1 but without a contact dielectric layer, in accordance with a second embodiment;

Figures 5A to 5G are schematic diagrams which illustrate the method of Figure 4 for fabricating the solar cell of Figure 1 but without the contact dielectric layer;
- 20 Figures 6A and 6B show schematic structures of two different test samples which have been processed to measure their corresponding tunneling resistances;

Figures 7A and 7B show measured dark current-voltage (I-V) curves of the structures of Figures 6A and 6B respectively for measuring their corresponding tunneling resistances;
- 25 Figures 8A, 8B and 8C show schematics of structures where each structure comprises a p^+ poly-Si/SiO_x/n⁺ poly-Si tunnel junction which is optimized for use in the methods of Figures 2 and 4, where Figure 8A shows a structure comprising the SiO_x/ p^+ poly-Si/SiO_x/n⁺ poly-Si tunnel junction deposited on both sides of an n-type Si wafer and with an additional SiN_x passivation layer on each side, Figure 8B shows a structure comprising the SiO_x/ p^+ poly-Si/SiO_x/n⁺ poly-Si tunnel junction deposited on both sides of

an n-type Si wafer, and Figure 8C shows a structure comprising the SiO_x/p^+ poly-Si/ SiO_x/n^+ poly-Si tunnel junction deposited on both sides of a p-type Si wafer with an additional metal contact layer deposited on each side;

Figures 9A and 9B illustrate experimental findings of a performance of a n^+ -poly-Si/ SiO_x/p^+ -poly-Si tunnel junction, where Figure 9A shows an Electrochemical Capacitance-Voltage (ECV) profiling of the n^+ -poly-Si/ SiO_x/p^+ -poly-Si tunnel junction and Figure 9B shows a dark I-V curve of the n^+ -poly-Si/ SiO_x/p^+ -poly-Si tunnel junction after applying a short high temperature firing process step as used during conventional high-temperature screen printing;

Figures 10A, 10B and 10C show schematic structures for use in investigating a minority carrier lifetime for a SiO_x/p^+ -poly-Si/ SiO_x/n^+ -poly-Si tunnel junction, where Figure 10A shows a structure comprising a diffusion optimized SiO_x/p^+ -poly-Si contact passivation layer stack on a n-doped Si wafer, Figure 10B shows a structure comprising a SiO_x/p^+ -poly-Si contact passivation layer stack, being additionally SiN_x passivated, on a p-doped Si wafer, and Figure 10C shows a structure comprising the SiO_x/p^+ -poly-Si/ SiO_x/n^+ -poly-Si tunnel junction on a rear side of a p-doped Si wafer, suited for dark-IV tunneling resistance measurements;

Figures 11A and 11B illustrate experimental findings of minority carrier lifetime for the structures of Figures 10A, 10B and 10C, where Figure 10A shows the experimental findings for the structure of Figure 10A, and Figure 10B shows the experimental findings for the structures of Figures 10B and 10C;

Figure 12 shows photoluminescence (PL) images and optical microscope images of the area after laser ablation processes used in the method of Figure 2;

Figures 13A, 13B and 13C illustrate experimental findings in relation to conventional high-temperature screen printing on top of a n^+ -poly-Si/ SiO_x/p^+ -poly-Si tunnel junction, where Figure 13A shows a schematic of a biPoly test-cell with a front-side (250nm thick) n^+ -poly-Si/ SiO_x and a rear-side n^+ -poly-Si/ SiO_x/p^+ -poly-Si/ SiO_x passivated contact, Figure 13B shows a PL image measured of a sample with screen-printed contact on the n^+ -poly-Si/ SiO_x/p^+ -poly-Si tunnel junction, and Figure 13C shows measured I-V graph of the double side contact passivated test cell with a rear-side n^+ -poly-Si/ SiO_x/p^+ -poly-Si/ SiO_x tunnel junction; and

Figure 14 shows a schematic of a three-terminal (3T) tandem solar cell comprising a thin-film top solar cell and a silicon wafer based bottom solar cell where the bottom solar cell has a similar structure to the solar cell of Figure 1 but without the textured front surface and the front side passivation layer, in accordance with an embodiment.

5 Detailed description

An exemplary embodiment relates to a method for fabricating a solar cell, in particular, an all-back contact (ABC) solar cell with tunnel layer passivated contacts, and the solar cell thereof.

Figure 1 is a schematic structure of the solar cell 100 in accordance with an embodiment.

10 This solar cell 100 can either be deployed as a single-junction, ultra-high efficiency solar cell, or be adapted to be deployed as a high efficiency silicon bottom cell for further thin-film on silicon tandem device integration as discussed later in relation to Figure 14.

The solar cell 100 comprises an n-type Czochralski (Cz) grown monocrystalline Si wafer 102 with a front side passivation layer 104 deposited on a textured front side of the Si wafer 102. The front side passivation layer comprises a silicon nitride (SiN_x) layer or any other suitable front-side passivation stack. On a rear side of the Si wafer 102, a rear surface dielectric tunnel layer 106 is deposited on a surface of the rear side of the Si wafer 102. The rear surface dielectric tunnel layer 106 may comprise silicon oxide (SiO_x), aluminium oxide (AlO_x), titanium oxide (TiO_x) or SiN_x . The solar cell comprises a first
15 doped semiconductor layer 108 deposited on the rear surface dielectric tunnel layer 106. In the present embodiment, the first doped semiconductor layer 108 comprises a p^+ doped (e.g. boron doped) polysilicon (poly-Si) layer. As shown in Figure 1, the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108 each comprises openings. The openings of the rear surface dielectric tunnel layer 106 and the
20 openings of the first doped semiconductor layer 108 may be formed in-situ as a result of depositing the dielectric tunnel layer 106 and the first doped semiconductor layer 108 using a shadow mask or may be formed by ablation using a femtosecond laser. As shown in Figure 1, the openings of the rear surface dielectric tunnel layer 106 and the openings of the first doped semiconductor layer 108 are formed at the same positions and they
25 overlap completely. The solar cell 100 further comprises an intermediate dielectric layer 110 deposited on the first doped semiconductor layer 108. The intermediate dielectric layer 110 may comprise a silicon nitride (SiN_x) layer. Similar to the rear surface dielectric
30

tunnel layer 106 and the first doped semiconductor layer 108, the intermediate dielectric layer 110 comprises openings. The openings of the intermediate dielectric layer 110 may be formed in-situ as a result of depositing the intermediate dielectric layer 110 using a shadow mask or may be formed by ablation using a femtosecond laser. A portion of the openings of the intermediate dielectric layer 110 are formed within the openings of the rear surface dielectric tunnel layer 104 and the openings of the first doped semiconductor layer 106, while a portion of the openings of the intermediate dielectric layer 110 are formed on the first doped semiconductor 106 in between adjacent openings of the rear surface dielectric tunnel layer 104 and the openings of the first doped semiconductor layer 106. The solar cell 100 further comprises a dielectric tunnel layer 112 deposited within the openings of the intermediate dielectric layer 110. In another embodiment (not shown in Figure 1), the solar cell 100 comprises a dielectric tunnel layer 112 deposited across an entire area of the rear side of the Si wafer 102. In any case, the solar cell 100 further comprises a second doped semiconductor layer 114 deposited on the dielectric tunnel layer 112. The second doped semiconductor layer 114 are patterned (e.g. either by shadow mask or by laser ablation) so that isolation trenches 115 are formed within the second doped semiconductor layer 114. The second doped semiconductor layer 114 is of an opposite polarity to the first doped semiconductor layer 108. In this case, the second doped semiconductor layer 114 may comprise an n^+ doped (e.g. phosphorous doped) polysilicon (poly-Si) layer. As shown in Figure 1, portions of the second doped semiconductor layer 114 are deposited on the dielectric tunnel layer 112 at the openings of the rear surface dielectric tunnel layer 106 and the openings of the first doped semiconductor layer 108, while portions of the second doped semiconductor layer 114 are deposited on the dielectric tunnel layer 112 at the openings of the intermediate dielectric layer 110. The solar cell 100 comprises a contact dielectric layer 116 optionally deposited on the second doped semiconductor layer 114. The solar cell 100 further comprises an interdigitated metal layer grid 118 deposited on the contact dielectric layer 116. The interdigitated metal layer grid 118 deposited using a conventional high-temperature fire-through screen printing paste so that the interdigitated metal layer grid 118 deposited is in electrical contact with the second doped semiconductor layer 114. As shown in Figure 1, the solar cell 100 comprises a plurality of interdigitated contacts formed on the rear side of the Si wafer 102. The plurality of interdigitated contacts comprises alternating tunnel junction augmented passivated contacts 120 and conventional passivated contacts 122. Each of the tunnel junction augmented passivated

contacts 120 comprises the rear surface dielectric tunnel layer 106, the first doped semiconductor layer 108, the dielectric tunnel layer 112 and the second doped semiconductor layer 114, and each of the conventional passivated contacts 122 comprises the dielectric tunnel layer 112 and the second doped semiconductor layer 114, where the conventional passivated contacts 122 are formed at the openings of the first doped semiconductor layer 108 and at the openings of the rear surface dielectric tunnel layer 106.

Further, each of the tunnel junction augmented passivated contacts 120 and conventional passivated contacts 122 comprises a contact passivation layer stack 124, 126. The contact passivation layer stack functions as a tunnel layer passivated contact on the surface of the rear side of the Si wafer 102. As shown in Figure 1, the contact passivation layer stack 124 of the tunnel junction augmented passivated contacts 120 comprises the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108 (e.g. hole extracting) while the contact passivation layer stack 126 of the conventional passivated contacts 122 comprises the dielectric tunnel layer 112 and the second doped semiconductor layer 114 (e.g. electron extracting). Given that the first doped semiconductor layer 108 and the second doped semiconductor layer 114 are of opposite polarity, the alternating tunnel junction augmented passivated contacts 120 and conventional passivated contacts 122 therefore comprise alternating electron and hole extracting tunnel layer passivated contacts. Further, each of the tunnel junction augmented passivated contacts 120 comprises a tunnel junction formed by the first doped semiconductor layer 108, the dielectric tunnel layer 112 and the second doped semiconductor layer 114. In some embodiments as described below, the tunnel junction comprises the first doped semiconductor layer 108 and the second doped semiconductor layer 114, but without the dielectric tunnel layer 112. In this embodiment, holes (since the first doped semiconductor layer 108 is p-doped) can be extracted via the tunnel junction from the contact passivation layer stack 124 of the tunnel junction augmented passivated contact 120. In this way, the second doped semiconductor layer 114 is formed at the top of both the tunnel junction augmented passivated contacts 120 and the conventional passivated contacts 122 on the rear side of the Si wafer 102 so that the interdigitated metal layer grid 118 which is subsequently deposited to form electrical contacts for these interdigitated contacts of the solar cell can contact the same second doped semiconductor layer. This significantly minimizes the number and complexity of

patterning steps in order to realize an ABC tunnel layer contact passivated silicon wafer based solar cell.

Figure 2 is a flowchart showing steps of a method 200 for fabricating the solar cell 100 of Figure 1 in accordance with a first embodiment. Figures 3A to 3L are schematic diagrams which illustrate the method 200 of Figure 2. Figures 3A to 3L provide clarity to the steps of the method 200 and are therefore discussed in conjunction with Figure 2 below. In the first embodiment, laser ablation is used to form the openings of the rear surface dielectric tunnel layer 106, the openings of the first doped semiconductor layer 108, the openings of the intermediate dielectric layer 110, and the openings of the contact dielectric layer 116. Selective etching (e.g. chemical and/or physical) is used to form the isolation trenches of the second doped semiconductor layer 114. Details of these are discussed further below.

In this embodiment, an n-type Czochralski grown monocrystalline silicon (Si) wafer is used as a starting substrate for fabricating the solar cell. As would be appreciated by the skilled person in the art, preparatory steps (e.g. cleaning the Si wafer surface) may be necessary before each fabrication step, and these preparatory steps have been omitted for clarity and succinctness of the present method 200.

In a step 202, the front side of the Si wafer 102 of the solar cell 100 is textured. Texturing the front side of the Si wafer 102 may comprise etching the front side of the Si wafer 102, for example using a wet chemical etch. Please note, that this is not necessarily the first process step, it could also be performed at a later stage.

In a step 204, the front side passivation layer 104 is deposited on the textured front side of the Si wafer 102. The front side passivation layer 104 may comprise SiN_x or any other front-side passivation stack. A schematic of the resultant structure of the solar cell 100 after deposition of the front side passivation layer 104 is shown in Figure 3A. Please note, that this process step could also be performed at a later stage.

In a step 206, the rear surface dielectric tunnel layer 106 is deposited on the rear side of the Si wafer 102. The deposition of the rear surface dielectric tunnel layer 106 comprises a single-side full-area deposition as shown in Figure 3B. The rear surface dielectric tunnel layer 106 may comprise aluminium oxide (AlO_x), SiN_x or TiO_x deposited by atomic

layer deposition (ALD) or silicon oxide (SiO_x) deposited by chemical vapour deposition (PECVD or LPCVD)

After the deposition of the rear surface dielectric tunnel layer 106 in the step 206, a first doped semiconductor layer 108 is deposited on the rear surface dielectric tunnel layer 106 in a step 208. Similar to the step 206, the deposition of the first doped semiconductor layer 108 comprises a single-side full-area deposition as shown in Figure 3C. The first doped semiconductor layer 108 comprises p^+ doped poly-Si for the purpose of forming a contact that can selectively extract holes. The first doped semiconductor layer 108 may be deposited by PECVD or LPCVD. In an embodiment where the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108 are both deposited by PECVD or LPCVD, the steps 204 and 206 are effectively combined into one process step since these two layers can be deposited using the same CVD machine (e.g. by introducing process gases for the deposition of the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108 one after the other).

After the deposition of the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108, openings in the rear surface dielectric tunnel layer 106 and openings in the first doped semiconductor layer 108 are formed in a step 210. The openings 302 in each of these layers 106, 108 are formed by laser ablation. This is shown in Figure 3D. As shown in Figure 3D, the openings of the rear surface dielectric tunnel layer 106 and openings of the first doped semiconductor layer 108 are formed at identical positions and they overlap completely with each other. The openings 302 are formed to accommodate the conventional passivated contacts 122 for electron (i.e. majority carrier) extraction. Typically, these openings 302 cover about 5% - 30% of the total rear side surface of the Si wafer 102. The laser ablation used in forming the openings 302 is required to create as little laser induced surface damage as possible. In the present embodiment, a femtosecond (fs) laser having an ultraviolet wavelength is used. It is shown that by using a femtosecond (fs) laser having an ultraviolet wavelength, it is possible to form local openings 302 in the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108 (e.g. a SiO_x /poly-Si contact passivation layer stack) with minimal damage. This is discussed later in relation to Figure 12. In an embodiment, an additional wet-chemical post-treatment can be used to remove some remaining surface induced damage due to the laser ablation process.

In a step 212, after forming the openings 302 in the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108, the intermediate dielectric layer 110 is deposited on the first doped semiconductor layer 108. The deposition of the intermediate dielectric layer 110 comprises a full-area deposition on the rear side of the Si wafer 102.

5 This is shown in Figure 3E. The intermediate dielectric layer 110 comprises a silicon nitride (SiN_x) layer.

In a step 214, openings are formed in the intermediate layer 110. Similar to the step 210, the openings can be formed using femtosecond (fs) laser ablation with an ultraviolet wavelength. As shown in Figure 3F, there are two types of openings 304, 306 formed in
10 the intermediate layer 110. The openings 304 are formed within the openings 302 of the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108. The formation of the openings 304 thus requires an alignment step. As shown in Figure 3F, the openings 304 expose a portion of the Si wafer 102. On the other hand, the openings 306 formed are located between the openings 304. There is no requirement on a specific
15 location of these openings 306 and the alignment of these openings 306 are therefore non-critical. The openings 306 formed expose the first doped semiconductor layer 108 as shown in Figure 3F. Since the openings 304 and 306 can be formed in a single setting without a need to reposition the Si wafer 102 between each of the opening formation steps, no re-alignment of the Si wafer 102 is required as the laser ablation program can
20 be configured to align the two openings of the rear side of the Si wafer 102 automatically. Similar to the step 210, laser ablation has been shown to be effective in forming local openings 304, 306 in the intermediate dielectric layer 110. This is also discussed in relation to Figure 12.

After the openings 304, 306 are formed in the intermediate dielectric layer 110, the
25 dielectric tunnel layer 112 is deposited in a step 216. This is shown in Figure 3G. The dielectric tunnel layer 112 can be either grown only in the local area within the openings 304, 306 as shown, or can be deposited as a single-side full-area deposition on the rear side of the Si wafer 102 (not shown). For example, in case of using a thermally grown SiO_x to form the intermediate dielectric layer 110, i.e. using PECVD or LPCVD, the SiO_x
30 will grow only locally inside the openings. However, if atomic layer deposition technology is used in order to form the intermediate dielectric layer 110, it will be a rear-side full-area deposition.

After the deposition of the dielectric tunnel layer 112 in the step 216, the second doped semiconductor layer 114 is deposited on the dielectric tunnel layer 112 in a step 218. The deposition of the second doped semiconductor layer 114 comprises a single-side full-area deposition as shown in Figure 3H. The dielectric tunnel layer 112 together with the second doped semiconductor layer 114 formed a second type of contact passivation layer stack (i.e. electron extracting tunnel layer and capping layer). The dielectric tunnel layer 112 comprises silicon oxide (SiO_x) deposited, for example, by chemical vapour deposition (PECVD or LPCVD). The second doped semiconductor layer 114 comprises n^+ doped poly-Si for the purpose of forming a contact that can selectively extract electrons. The second doped semiconductor layer 114 may be deposited by PECVD or LPCVD. In an embodiment where the dielectric tunnel layer 112 and the second doped semiconductor layer 114 are deposited by PECVD or LPCVD, the steps 216 and 218 are effectively combined into one process step since these two layers can be deposited using the same CVD machine in a similar manner as the steps 206 and 208. As shown in Figure 3H, as a result of the openings 304 and 306 formed in the intermediate dielectric layer 110, three different contact areas are formed. A first type of contact area is formed at locations 307 where either the dielectric tunnel layer 112 / the second doped semiconductor layer 114 stack (in case of forming a full-area dielectric tunnel layer 112) or the second doped semiconductor layer 114 (in case of forming a local-area dielectric tunnel layer 112 only in the openings) is in contact with the intermediate dielectric layer 110, this first type of contact area is irrelevant for device performance of the solar cell 100. A second type of contact area is formed at locations 308 where the dielectric tunnel layer 112 / the second doped semiconductor layer 114 stack is in contact with the Si wafer 102. This second type of contact area is formed at the openings 304 as shown in Figure 3H. This second type of contact area forms part of the electron-extracting conventional passivated contact 122 (i.e. within the openings 304). A third type of contact area is formed at locations 309 where the dielectric tunnel layer 112 / the second doped semiconductor layer 114 stack is in contact with the rear surface dielectric tunnel layer 106 / first doped semiconductor layer 108 stack. This third type of contact area is formed at the openings 306 of the intermediate dielectric layer 110. This third type of contact area forms part of the hole-extracting tunnel junction augmented passivated contact 120 (i.e. within the openings 306).

For the present embodiment, the quality of the resulting tunnel junction augmented passivated contacts 120 formed (which comprises the rear surface dielectric tunnel layer 106 / the first doped semiconductor layer 108 / the dielectric tunnel layer 112 / the second doped semiconductor layer 114 stack) is critical for effectively converting minority hole current into a majority electron current. This requires that the effective doping of the first doped semiconductor layer 108 (e.g. p^+ doped poly-Si) and the second doped semiconductor layer 114 (e.g. n^+ doped poly-Si) to be sufficiently high in order to form an ohmic tunnel junction (in contrast to a rectifying p/n junction). As discussed below (see e.g. Figure 9A), it has been successfully demonstrated that a high quality tunnel junction with sufficiently high doped poly-Si capping layers can be formed, clearly showing an ohmic (linear) behaviour (see e.g. Figure 9B). It is shown that these tunnel junctions maintain high passivation quality as demonstrated by the high minority carrier lifetime and a correspondingly high implied open circuit voltage, for example, as shown in relation to Figures 11A and 11B.

In a step 220, the contact dielectric layer 116 is deposited on the second doped semiconductor layer 114. The deposition of the contact dielectric layer 116 comprises a full area deposition on the rear side of the Si wafer 112. This is shown in Figure 3I. The contact dielectric layer 116 comprises silicon nitride (SiN_x) which acts as a passivation layer. After deposition of the contact dielectric layer 116 in the step 220, openings/isolation trenches are required to be formed in the contact dielectric layer 116 and the second doped semiconductor layer 114 in order to separate the hole extracting contact (i.e. the tunnel junction augmented passivated contacts 120 formed at the openings 306) and the electron extracting contacts (i.e. the conventional passivated contacts 122 formed at the openings 304). In a step 222, openings 310 are formed in the contact dielectric layer 116. The openings 310 are formed between the openings 304 and 306. This is shown in Figure 3J. The openings 310 are formed by ablation using a femtosecond laser having an ultraviolet wavelength, in a similar manner as forming openings 304 in the intermediate dielectric layer 110. In a step 224, isolation trenches 312 are formed in the second doped semiconductor layer 114. This is shown in Figure 3K. The isolation trenches 312 are formed at positions of the openings 310 (i.e. the exposed area of the second doped semiconductor layer 114 after performance of the step 222). The isolation trenches 312 are formed by selective etching, for example by using wet chemical etching (e.g. potassium hydroxide (KOH)) or dry etching or a

combination of both. Similar to forming the openings 306, alignment for the formation of the openings 310 and the isolation trenches 312 is not critical for the steps 222 and 224.

In a step 226, an interdigitated metal layer grid 118 is deposited on the contact dielectric layer 116 to form electrical contacts for the interdigitated contacts. The interdigitated metal layer grid 118 forms an interdigitated contact grid for the solar cell 100. This is shown in Figure 3L. The interdigitated metal layer grid 118 (i.e. the interdigitated metal contact grid) is screen printed on top of the contact dielectric layer 116 using conventional screen printing technology, e.g. using a conventional high-temperature fire-through screen printing paste.

As outlined in the method 200 above, the ABC contact passivated solar cell 100 can be fabricated in a streamlined process with a total of ten method steps by using femtosecond laser ablation for patterning of the deposited layers. Two of the ten method steps are for providing the single-side textured and passivated wafer (i.e. the steps 202 and 204), seven of the ten method steps are to form the electron and hole extracting contacts including forming the contact passivation layer stacks of the interdigitated contacts and the tunnel junction for the tunnel junction augmented passivated contacts on the rear side of the Si wafer 102 (i.e. the steps 206 to 224 – this includes combining the deposition steps 206 and 208, and combining the deposition steps 216 and 218 as outlined above in an embodiment where the rear surface dielectric tunnel layer and the first doped semiconductor layer can be deposited by CVD in a single process step, and where the dielectric tunnel layer 112 and the second doped semiconductor layer 114 can be deposited by CVD in a single process step, and combining the steps 222 and 224 in forming the openings/isolation trenches in the contact dielectric layer and the second doped semiconductor layer in a single ablation/etching step), and one of the ten method steps is to deposit the interdigitated metal layer grid 118 for forming electrical contacts for the interdigitated contacts in the step 226.

By realizing the ABC solar cell architecture using sequential damage-free laser patterning steps to form openings in the deposited layers as described in the first embodiment, the method 200 is capable of using full-area deposition of contact passivation layer stacks so that no masking / mask removal process steps are required. In this way, the ABC contact passivated solar cells can be realized without any need of local alignment / masking. In addition, by deploying contact passivation, there is no

diffused area within the wafer underneath the solar cell contacts. This enables the solar cell 100 of the present embodiment to reach higher open-circuit voltages due to reduced contact and bulk recombination. Thus, as compared to conventionally diffused ABC solar cells, the efficiency potential of the solar cell is higher, and the resulting process sequence to realize such cells is leaner (i.e. requiring less process steps). Further, by using the tunnel junction augmented passivated contact structure in the solar cell 100, it allows conventional high-temperature screen printing for both polarities in one process step (see Figures 13A, 13B and 13C and their description below).

To sum up, as compared to a conventional ABC solar cell, the present embodiment uses (1) poly-Si contact passivation layers, (2) local laser ablation, (3) an intermediate dielectric layer 110, and (4) conventional high temperature screen printing. In relation to (1), by deploying poly-Si contact passivation layers (i.e. the SiO_x layer of the contact passivation layer stack) instead of “conventional” heterojunction layers or “conventional” locally diffused areas within the Si wafer to form the ABC solar cells, a significant cost advantage can be achieved (e.g. the TCO used in ABC solar cells with heterojunction contacts is far more expensive than the poly-Si used in the present conventional passivated contacts and tunnel junction augmented passivated contacts) and the amount of process steps needed can be significantly reduced while achieving a similar solar cell efficiency (contact passivation is as effective as heterojunction passivation, both methods are more effective than local diffusion). In relation to (2), by deploying local laser ablation instead of conventional shadow masking, the requirement for alignment during the fabrication process is reduced. In relation to (3), by deploying the intermediate dielectric layer 110 (e.g. SiN_x passivation layer) deposited between the tunnel junction augmented passivated contacts 120 and the conventional passivated contacts 122, electron and hole transport in these contacts can be decoupled. This enables the two contacts for electron and hole extraction to be of the same width which advantageously simplifies the contact printing process. This is also advantageous as it reduces ohmic loss related to current transport across the interdigitated contacts. In relation to (4), the conventional high temperature screen printing, which is already deployed in any production line, can be utilized. In other words, the solar cell architecture and the method of the present embodiment can be deployed readily in an industrial setting.

Figure 4 is a flowchart showing steps of a method 400 for fabricating a solar cell similar to the solar cell 100 of Figure 1 but without the contact dielectric layer 116, in accordance

with a second embodiment. Figures 5A to 5G are schematic diagrams which illustrate the method 400 of Figure 4. Figures 5A to 5G provide clarity to the steps of the method 400 and are therefore discussed in conjunction with Figure 4 below.

5 In this second embodiment, conventional shadow masks are used for all thin-film layer depositions. By doing so, the openings of the rear surface dielectric tunnel layer 106, the openings of the first doped semiconductor layer 108, the openings of the intermediate dielectric layer 110 and the isolation trenches 312 of the second doped semiconductor layer 114 are formed in-situ during the deposition processes using the shadow masks. It is also noted that the solar cell 100 formed using this second embodiment as described
10 does not include the contact dielectric layer 116. Nonetheless, it should be appreciated the contact dielectric layer 116 can be easily incorporated in the method 400 if required.

In contrast to the first embodiment as described in relation to the method 200, the method 400 of the second embodiment therefore does not require separate process steps for the formation of the openings/isolation trenches in the rear surface dielectric tunnel layer
15 106, the first doped semiconductor layer 108, the intermediate dielectric layer 110 and the second doped semiconductor layer 114. As shown in Figure 4, the steps 210, 214, 222 and 224 can therefore be eliminated from the method 400. The required method steps can therefore be further reduced in this second embodiment as compared to the first embodiment. However, the method 400 requires an alignment of three different
20 shadow masks during the deposition of the first rear surface dielectric tunnel layer 106 / first doped semiconductor layer 108 contact passivation layer stack, the intermediate dielectric layer 110, and the dielectric tunnel layer 112 / second doped semiconductor layer 114 contact passivation layer stack.

The steps 202, 204, 206, 208, 212, 216, 218, 226 comprised in the method 400 are
25 similar to those as described above for the method 200 and will therefore not be repeated here in their entirety. A brief description of the method 400 in relation to the schematics as shown in Figures 5A to 5G is provided below for completeness.

The steps 202 and 204 are performed to produce a front side textured passivated Si wafer 102 as shown in Figure 5A. Similar to the first embodiment, the front side
30 passivation layer 104 comprises a SiN_x layer. Please note again, that these process steps do not necessarily have to be performed at the beginning of the method 400, they can alternatively also be performed later. The steps 206 and 208 of the method 400 are

then performed to deposit the rear surface dielectric tunnel layer 106 (see Figure 5B) and the first doped semiconductor layer 108 (see Figure 5C) on the rear side of the Si wafer 102 respectively. The deposition of the rear surface dielectric tunnel layer 106 / the first doped semiconductor layer 108 (i.e. the hole extracting contact passivation layer stack) is performed using a shadow mask, where the openings 302 in the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108 are formed in-situ during the deposition steps 206 and 208. After the deposition of the rear surface dielectric tunnel layer 106 and the first doped semiconductor layer 108 in the steps 206 and 208, the intermediate dielectric layer 110 is deposited on the first doped semiconductor layer 108 in the step 212. The deposition of the intermediate dielectric layer 110 is again performed using a shadow mask. The openings 304 and 306 are formed in-situ during the deposition of the intermediate dielectric layer 110 using shadow mask deposition. This is shown in Figure 5D. After the deposition of the intermediate dielectric layer 110 in the step 212, the dielectric tunnel layer 112 and the second doped semiconductor layer 114 are deposited in the steps 216 and 218 respectively. The dielectric tunnel layer 112 and the second doped semiconductor layer 114 are deposited using a shadow mask. This is shown in Figure 5E (where the dielectric tunnel layer 112 is deposited) and Figure 5F (where the second doped semiconductor layer 114 is deposited). The isolation trenches 312 of the second doped semiconductor layer 114 are formed in-situ during the shadow mask deposition of the second doped semiconductor layer 114 in the step 218. After the deposition of the second doped semiconductor layer 114 in the step 218, the interdigitated metal layer grid 118 is deposited on the second doped semiconductor layer 114 in the step 226. This is shown in Figure 5G. The interdigitated metal layer grid 118 is screen printed on top of the second doped semiconductor layer 114 to form the plurality of interdigitated contacts. As no contact dielectric layer 116 is deposited in this second embodiment, a non-fire through paste is used for screen printing the interdigitated metal layer grid 118 to form electrical contacts for the interdigitated contacts.

As compared to the first embodiment, the method 400 of the second embodiment requires a total of six method steps to form an ABC contact passivated solar cell 100. Two of the six method steps are for providing the front-side textured and passivated Si wafer (i.e. the steps 202 and 204), the rest of the method steps are used to form the ABC interdigitated contacts (i.e. the steps 206, 208, 212, 216, 218 and 226 – this includes combining the deposition steps 206 and 208, and combining the deposition steps 216

and 218 in an embodiment where the rear surface dielectric tunnel layer and the first doped semiconductor layer can be deposited by CVD in a single process step, and where the dielectric tunnel layer 112 and the second doped semiconductor layer 114 can be deposited by CVD in a single process step).

- 5 Although the method 400 of the second embodiment uses fewer process steps, the method 400 requires alignment of the shadow masks. Furthermore, using shadow masks in industrial production of solar cells may be challenging. For example, using shadow masks involve additional steps for cleaning the shadow masks and aligning the shadow masks. Nonetheless, the solar cell architecture (i.e. solar cell 100) which employs tunnel
10 junction augmented passivated contacts and conventional passivated contacts still minimizes the amount of patterning and alignments needed for processing these all-back-contact (ABC) solar cells (as compared to conventional heterojunction ABC solar cells), while at the same time guarantying high open-circuit voltage potential due to the deployment of contact passivation. In particular, by additionally deploying a tunnel
15 junction for one of the electron and hole extracting passivated contacts of the ABC solar cell, self-aligned contact passivation layer stacks for interdigitated selective electron and hole extraction are formed.

- When the interdigitated passivated contacts (formed by PECVD or LPCVD) are formed in combination with local-area femtosecond laser ablation, a simple processing for the
20 patterning of the interdigitated passivated contacts can be achieved, requiring only 1 alignment, without having to adhere to tight alignment tolerances. This allows a significant reduction in the number of patterning steps for fabricating of an ABC solar cell to such an extent that there are only ten or six process steps required, respectively, and no masking and subsequent mask-removal of the deposited thin-film layers is necessary.

- 25 Further, similar to the first embodiment, the use of the intermediate dielectric layer 110 (e.g. a SiN_x passivation layer) allows the electron collecting regions to be separated from the hole collecting regions so that local internal shunting can be avoided, and that the interdigitated metal layer grid 118 can have the same surface area for extracting carriers from the passivated contacts of both polarities.

- 30 In addition, it is noted that most all-back-contact solar cells use conventional diffusion in order to form the solar cell contacts. In this case, structuring has to be performed within the wafer (i.e. in the formation of highly p- and n- doped regions within the wafer), which

requires a significant number of masking steps. In other words, a comparable amount of structuring is required if the interdigitating sequence of n-doped and p-doped heterojunction layers at the rear side of the wafer is to be realized. In contrast, by fabricating the solar cell 100 using the methods 200 and 400 as aforementioned described, no structuring of the Si wafer 102 is required. This significantly reduces the number of processing steps for fabricating the ABC solar cell 100.

Figures 6A – 6B, 7A – 7B, 8A – 8B, 9A – 9C, 10A – 10B, 11, 12 and 13A – 13C provide experimental results in relation to several method steps in the methods 200, 400. In particular, it is demonstrated that a working n⁺-poly-Si/SiO_x/p⁺-poly-Si tunnel junction with a tunnel resistance of 0.52 Ω.cm² has been developed. Further, it is shown that the required laser patterning processes with minimum damage used in the first embodiment has been established. It is also demonstrated that the n⁺-poly-Si/SiO_x/p⁺-poly-Si tunnel junction can be contacted by conventional fire-through screen printing and hence is compatible with industrial processes.

Figures 6A and 6B show schematic structures of two different test samples which have been processed to measure a corresponding tunneling resistance of the tunnel junction formed by the first doped semiconductor layer 108 (e.g. p⁺-poly-Si) / the dielectric tunnel layer 112 (e.g. SiO_x) / the second doped semiconductor layer 114 (i.e. n⁺ poly-Si) stack.

As previously described, the quality of the tunnel junction augmented passivated contact is important for the performance of the solar cell 100. In order to test a quality of the tunnel junctions formed in the tunnel junction augmented passivated contacts, test samples as shown in Figures 6A and 6B are fabricated. Figure 6A shows a symmetric test-structure 600 to measure the effective contact resistance of a conventional hole extracting SiO_x/p⁺-poly-Si passivated contact. The SiO_x/p⁺-poly-Si contact passivating tunnel junction comprises a p-type Si wafer 602, a SiO_x layer 604 deposited on the p-type Si wafer 602, a p⁺-poly-Si layer 606 deposited on the SiO_x layer 604 and a silver metal layer 608 deposited on the p⁺-poly-Si layer 606. As shown in Figure 6A, this multi-layer stack is deposited symmetrically on both sides of the p-type Si wafer 602.

Figure 6B shows a test-structure 610, deploying a conventional hole extracting SiO_x/p⁺-poly-Si passivated contact at one side, and a tunnel junction augmented hole extracting SiO_x/p⁺-poly-Si/SiO_x/n⁺-poly-Si passivated contact at the other side. By measuring the total series resistance of this structure and subtracting the series resistance of the wafer

as well as the effective contact resistance of a conventional hole extracting $\text{SiO}_x/\text{p}^+\text{-poly-Si}$ passivated contact as measured with the test structure 600, the tunneling resistance of the $\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ tunnel junction can be determined.

Figures 7A and 7B show measured dark current-voltage (I-V) curves of the structures 600, 610 of Figures 6A and 6B respectively. The I-V curves as shown in Figures 7A and 7B are used to measure the corresponding tunneling resistance of the $\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ tunnel junction (i.e. extracted from the total series resistance of the structures 600, 610).

As shown in Figures 7A and 7B, the measured dark I-V curves comprise a straight line for both structures 600 and 610. This shows that both the structures 600, 610 display an ohmic behaviour in the vicinity of 0 V. The measured dark I-V curves also allows the total series resistance of the structures 600 and 610 to be calculated and thus the associated tunneling resistance of the tunnel junction in the structure 610 to be extracted. The corresponding tunneling resistance extracted is in the range $\sim 0.5 \text{ Ohm}\cdot\text{cm}^2$. This range is already well suited for full-area device integration but may still be further optimized for the methods 200, 400. Further, since the $\text{SiO}_x/\text{p}^+\text{-poly-Si}$ layers deposited on top of the p-doped Si wafer 602 do form an ohmic contact, upon the addition of the SiO_x layer 612 and the $\text{n}^+\text{-poly Si}$ layer 614 deposited on the rear side of the p-type Si wafer 602 in the structure 610, the ohmic behaviour is conserved as observed only if the $\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ structure is indeed forming a tunnel junction.

Given that the measured dark I-V curves show straight lines as shown in Figures 7A and 7B, it is therefore experimentally demonstrated that a tunnel junction $\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ is formed. As demonstrated in Figure 7B using the structure 610, the tunneling properties of the tunnel junction $\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ remain (albeit with an increased tunnel resistance R_{series}), even if there is an additional ultra-thin SiO_x tunnel layer sandwiched in between the $\text{p}^+\text{-poly-Si}$ and the $\text{n}^+\text{-poly-Si}$ layers. Thus it is not necessary to use a $\text{p}^+\text{-poly-Si}/\text{n}^+\text{-poly-Si}$ tunnel junction without an interfacial SiO_x interlayer for forming the tunnel junction augmented passivated contacts 120 of the solar cell 100 (this significantly reduces the required process steps, however, may be at the expense of a slightly increased tunneling resistance).

Figures 8A, 8B and 8C show schematics of structures 800, 820, 830 where each comprises a $\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ tunnel junction which is optimized for use in the

methods of Figures 2 and 4, where Figure 8A shows a structure 800 comprising the tunnel junction augmented hole extracting $\text{SiO}_x/\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ passivated contact deposited on both sides of an n-type Si wafer and with additional SiN_x passivation layers, Figure 8B shows a structure 820 comprising the tunnel junction augmented hole extracting $\text{SiO}_x/\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ passivated contact deposited on both sides of an n-type Si wafer, and Figure 8C shows a structure 830 comprising the tunnel junction augmented hole extracting $\text{SiO}_x/\text{p}^+\text{-poly-Si}/\text{SiO}_x/\text{n}^+\text{-poly-Si}$ passivated contact deposited on both sides of a p-type Si wafer with additional metal contact layers.

As shown in Figure 8A, the structure 800 comprises an n-type Si wafer 802, a SiO_x layer 804 deposited on the n-type Si wafer 802, a p^+ poly-Si layer 806 deposited on the SiO_x layer 804, a second SiO_x layer 808 deposited on the p^+ poly-Si layer 806, an n^+ poly-Si layer 810 deposited on the second SiO_x layer 808, and a SiN_x passivation layer 812 deposited on n^+ poly-Si layer 810. As shown in Figure 8A, this multi-layer stack is deposited symmetrically on both sides of the n-type Si wafer 802. The structure 800 corresponds to the rear side tunnel junction augmented passivated contact of the solar cell 100. This structure 800 and its variations are used to investigate the passivation properties of the tunnel junction augmented passivated contact at different stages of processing (structures 800 and 820) as well as the resistance properties of the tunnel junction augmented passivated contact (structure 830). For example, a variation to the structure 800 is shown in Figure 8B. The structure 820 of Figure 8B is similar to the structure 800 except that it does not include the SiN_x layers 812 formed on both sides of the n-type Si wafer 802. Another variation to the structure 800 is shown in Figure 8C. The structure 830 of Figure 8C is similar to the structure 800 except that it does not include the SiN_x layers 812 formed on both sides of the n-type Si wafer 802, but deploys metal layers 834 instead.

Figures 9A and 9B illustrate experimental findings of a performance of an $\text{n}^+\text{-poly-Si}/\text{SiO}_x/\text{p}^+\text{-poly-Si}$ tunnel junction, where Figure 9A shows an Electrochemical Capacitance-Voltage (ECV) profiling of the $\text{n}^+\text{-poly-Si}/\text{SiO}_x/\text{p}^+\text{-poly-Si}$ tunnel junction and Figure 9B shows a dark I-V curve of the $\text{n}^+\text{-poly-Si}/\text{SiO}_x/\text{p}^+\text{-poly-Si}$ tunnel junction. The ECV profiling was performed using the structure 820 of Figure 8B and the dark I-V curve was performed using the structure 830 of Figure 8C.

As shown in Figures 9A and 9B, a high-performance tunnel junction augmented passivated contact, n^+ -poly-Si/SiO_x/p⁺-poly-Si/SiO_x has been developed. For example, the ECV profiling of the n^+ -poly-Si/SiO_x/p⁺-poly-Si/SiO_x tunnel junction shows that high doping concentrations (10^{20} cm^{-3}) are achieved at both n^+ poly-Si and p⁺ poly-Si regions, where the tunnel junction exhibits a very sharp transition between the n^+ poly-Si and p⁺ poly-Si regions. From the dark I-V curve of Figure 9B, it can be calculated that the n^+ -poly-Si/SiO_x/p⁺-poly-Si/SiO_x tunnel junction has a moderate tunnel resistivity ($\sim 0.52 \Omega \cdot \text{cm}^2$) despite the fact that there is an interfacial SiO_x located in between the two n^+ poly-Si and p⁺ poly-Si regions.

Further, using the structure 800 of Figure 8A, an implied open-circuit voltage of 715 mV has been measured. All test structures 800, 820, 830 were fabricated using low pressure chemical vapour deposition (LPCVD) process which is a double-side deposition process. Further development is being made to deposit the n^+ -poly-Si/SiO_x/p⁺-poly-Si/SiO_x tunnel junction using the PECVD process (a single-side deposition process, instead of a double-side deposition process).

Figures 10A, 10B and 10C show schematic structures 1000, 1010, 1020 for use in investigating minority carrier lifetime of a hole extracting tunnel layer augmented SiO_x/p⁺-poly-Si/SiO_x/n⁺-poly-Si passivated contact, where Figure 10A shows a structure 1000 comprising a diffusion optimized SiO_x/p⁺-poly-Si hole extracting passivated contact, additionally passivated by SiN_x, symmetrically deposited on an n-doped Si wafer in order to measure its minority carrier lifetime, Figure 10B shows a similar structure 1010 without the SiN_x passivation layer but deposited on a p-doped Si wafer, comprising a SiO_x/p⁺-poly-Si contact passivation layer stack on a p-doped Si wafer, and Figure 10C shows a similar structure 1020 to the structure 1010, additionally forming a rear-side p⁺-poly-Si/SiO_x/n⁺-poly-Si tunnel junction.

As shown in Figure 10A, the structure 1000 comprises an n-type Si wafer 1002, a SiO_x layer 1004 deposited on the n-type Si wafer 1002, a p⁺ poly-Si layer 1006 deposited on the SiO_x layer 1004 and a SiN_x passivation layer 1008 deposited on the p⁺ poly-Si layer 1006. As shown in Figure 10A, this multi-layer stack is deposited symmetrically on both sides of the n-type Si wafer 1002. The structure 1010 of Figure 10B is similar to the structure 1000 except that it does not include the SiN_x layers 1008 and that the SiO_x and the p⁺ poly-Si layers are formed on a p-type Si wafer 1012. The structure 1020 of Figure

10C is similar to the structure 1010 except that it further comprises a second SiO_x layer 1022 deposited on the p⁺ poly-Si layer 1006, an n⁺ poly-Si layer 1024 deposited on the second SiO_x layer 1022 on a rear side of the p-type Si wafer 1012.

Figures 11A and 11B illustrate experimental findings in relation to intensity-dependent minority carrier lifetimes (as a function of the excess minority carrier density within the sample) for the structures of Figures 10A, 10B and 10C, where Figure 11A shows the experimental findings for the structure of Figure 10A, and Figure 11B shows the experimental findings for the structures of Figures 10B and 10C.

As shown in the results of Figures 11A and 11B, by employing SiO_x/poly-Si contact passivation layers, it is possible to obtain a high minority carrier lifetime. For example, an implied open-circuit voltages $iV_{oc} \geq 700\text{mV}$ can be obtained for SiO_x/poly-Si contact passivation layers deposited on a n-type or p-type crystalline Si wafer. As shown in Figure 11B, this high minority carrier lifetime persists (or even improves!) after including a p⁺-poly-Si/SiO_x/n⁺-poly-Si tunnel junction (see e.g. structure 1020). It is noted that the structure 1020 is a pre-cursor (i.e. before metallization) of the structure 610 shown in Fig. 6B which is used to measure the tunneling resistance. Please note, the “older” structures 1000, 1010, 1020 utilized a different diffusion recipe for the hole extracting SiO_x/p⁺-poly-Si passivated contact as compared to the more optimized “newer” test-structure 800 described before.

A summary of the minority carrier lifetimes for the different structures 1000, 1010, 1020 of Figures 10A, 10B and 10C respectively is included in the Table 1 below.

	Lifetime (ms)	iV_{oc} (mV)	J_0 (fA cm ⁻²)
Structure 1000	2523	725	7
Structure 1010	351	688	46.7
Structure 1020	490	697	35.5

Table 1: Summary of the minority lifetime measurements for the structures of Figures 10A, 10B and 10C.

Figure 12 shows photoluminescence (PL) images and optical microscope images of the area after laser ablation processes used in the method of Figure 2. As shown in Figure 12, the images are classified in different rows used to investigate the effects of laser ablation for forming the openings 302, 304 and 306 in the method 200.

In order to successfully fabricate the solar cell 100 using the method 200, damage-free (or minimal damage) laser patterning steps have to be established. For each laser ablation step (e.g. the steps 210, 214, 222, 224 of the method 200), an optimal laser fluence has to be identified in order to ablate the targeted thin-film layer with minimum damage. The PL images are used as an indicator for any effects on the minority carrier lifetime of relevant regions both after ablation and after re-passivation. The optical microscope images are used to investigate whether the SiN_x layer is fully removed by the laser ablation. As shown by the PL images in Figure 12, the minority carrier lifetime of the laser ablated regions is preserved after ablation or can be recovered after re-passivation.

Laser opening 302 (i.e. the step 210 of Figure 2; with reference to Figures 3D and 3E)

As shown in the first row of Figure 12, by using a femtosecond laser at an ultraviolet wavelength, it is possible to damage-free locally form openings in a $\text{SiO}_x/\text{poly-Si}$ contact passivation stack (e.g. the rear surface dielectric tunnel layer 106 / the first doped semiconductor layer 108 stack). Additional wet-chemical post-treatment to the laser ablated region may be required to remove some remaining surface induced damage due to the laser ablation process. With optimized laser fluence and post ablation treatment to remove laser induced damage, the minority carrier lifetime of the local ablated region can be recovered after subsequent SiN_x layer deposition (as indicated in Figure. 12 – at a fluence of 0.10 J/cm^2 after re-passivation).

Laser opening 304 (i.e. the step 214 of Figure 2; with reference to Figures 3F to 3H)

As shown in the second row of Figure 12, by using a femtosecond laser at an ultraviolet wavelength, it is possible to damage-free locally form openings in a SiN_x layer (e.g. the intermediate dielectric layer 110). Additional wet-chemical post-treatment to the laser ablated region may be required to remove some remaining surface induced damage due to the laser ablation process. With optimized laser fluence and post ablation treatment to remove laser induced damage, the minority carrier lifetime of the locally ablated region can be recovered after subsequent deposition of a second contact passivation stack (i.e. SiO_x/n^+ poly-Si passivation stack – e.g. the dielectric tunnel layer 112 / the second doped semiconductor layer 114 stack). The optimized laser fluence as shown is 0.10 J/cm^2 after re-passivation.

Laser opening 306 (i.e. the step 214 of Figure 2; with reference to Figures 3F to 3H)

As shown in the third row of Figure 12, a laser ablation process window which is capable of locally ablating the overlaying SiN_x layer to form openings in the SiN_x layer (e.g. the intermediate dielectric layer 110 at positions above the first doped semiconductor layer 108) without damaging the underneath poly-Si layer has been identified and optimised. By using a femtosecond laser at an ultraviolet wavelength, the onset fluence of the optimized process window is 0.048 J/cm^2 . Within the optimized process window, the minority carrier lifetime of the laser ablated region is preserved as indicated by the PL images. As shown by the optical microscopy images in Figure 12, the SiN_x layer has also been fully ablated within the optimized process window for a laser fluence of 0.048 J/cm^2 to 0.075 J/cm^2 .

Laser opening 310 (i.e. the step 222 of Figure 2; Figure 3J)

The results for forming openings 310 of the contact dielectric layer 116 by laser ablation is not shown in Figure 12. However, the laser ablation process to form the openings 310 is very similar to that use to form the openings 306 as outlined above. Therefore, the optimized process window for a laser fluence of 0.048 J/cm^2 to 0.075 J/cm^2 is expected to work. However, the optimum laser fluence conditions may still differ slightly, as SiN_x is now ablated on top of poly-Si as compared to being ablated on top of a silicon wafer. A corresponding laser fluence optimization is still to be undertaken. It is noted that femtosecond laser ablation is only applicable to damage free ablate the SiN_x contact dielectric layer 116 on top of the second doped semiconductor layer 114 (i.e. n^+ poly-Si layer) in the step 222 of Figure 2. Forming the isolation trenches 312 in the second doped semiconductor layer 114 (i.e. n^+ poly-Si layer) with the help of laser ablation was not possible. In order to form the isolation trenches 312 in the second doped semiconductor layer 114 (i.e. n^+ poly-Si layer), selective KOH etching can be applied.

Figures 13A, 13B and 13C illustrate experimental findings in relation to conventional high-temperature screen printing on top of the n^+ -poly-Si/ SiO_x / p^+ -poly-Si tunnel junction, where Figure 13A shows a schematic of a double side contact passivated test-cell with a front-side (250nm thick!) conventional n^+ -poly-Si/ SiO_x passivated contact, and a rear-side n^+ -poly-Si/ SiO_x / p^+ -poly-Si/ SiO_x tunnel layer augmented passivated contact, Figure 13B shows a PL image measured of a sample with a rear-side screen-printed contact contacting the n^+ -poly-Si/ SiO_x / p^+ -poly-Si tunnel junction, and Figure 13C shows

measured I-V graph of the double side contact passivated test cell exhibiting a rear-side hole extracting tunnel junction augmented n^+ -poly-Si/SiO_x/p⁺-poly-Si/SiO_x passivated contact.

As shown in Figure 13A, the double side contact passivated test cell structure 1300
5 comprises an n-type Si wafer 1302, a SiO_x layer 1304 deposited on a front side of the n-doped Si wafer 1302, a n^+ poly-Si layer 1306 deposited on the SiO_x layer 1304 and a SiN_x passivation layer 1308 deposited on the n^+ poly-Si layer 1306. On a rear side of the n-type Si wafer 1302, a SiO_x layer 1310 is deposited on a surface of the rear side of the n-type Si wafer 1302, a p^+ poly-Si layer 1312 is deposited on the SiO_x layer 1310,
10 followed by another SiO_x layer 1314 deposited on the p^+ poly-Si layer 1312. An n^+ poly-Si layer 1316 is deposited on the SiO_x layer 1314 before being capped by a SiN_x passivation layer 1318 deposited on the n^+ poly-Si layer 1316. Metal contacts 1320 are then deposited on each of the front side and the rear side of the cell structure 1300 by conventional high-temperature screen printing.

15 As demonstrated by the experimental results of Figures 13B and 13C using a double side contact passivated test cell, conventional high-temperature screen printing can be used to contact both the electron-extracting regions via a n^+ -poly-Si/SiO_x conventional passivated contact, and the hole-extracting regions via a n^+ -poly-Si/SiO_x/p⁺-poly-Si/SiO_x tunnel junction augmented passivated contact. For example, the PL image as shown in
20 Figure 13B shows no visible damage on a region of the sample with screen-printed contact on the n^+ -poly-Si/SiO_x/p⁺-poly-Si/SiO_x tunnel junction of Figure 13A. Further, Figure 13C shows that the double side contact passivated cell structure 1300 exhibits an open-circuit voltage (V_{OC}) of 686.1 mV with a current density (j_{sc}) of 30.8 mA/cm². The measured efficiency as shown in Figure 13C is 16.4%. It is noted that the j_{sc} and
25 efficiency are low in the present test structure 1300 because there is significant parasitic absorption in the front n^+ poly-Si layer 1306. Furthermore, V_{OC} is constrained by the front-side, due to screen printing on the textured n^+ poly-Si layer 1306. In the targeted contact passivated all-back-contact configuration of the solar cell 100, both the tunnel junction augmented passivated contacts 120 and the conventional passivated contacts 122 will
30 be at the rear side of the Si wafer 102 and there will be no parasitic absorption at the front side, thus a V_{OC} of ~715mV can be expected. It is noted that current technology does not allow contacting hole-extracting p^+ -poly-Si/SiO_x conventional passivated contacts by means of screen conventional high temperature printing. The n^+ -poly-

Si/SiO_x/p⁺-poly-Si tunnel junction of the hole extracting tunnel junction augmented n⁺-poly-Si/SiO_x/p⁺-poly-Si/SiO_x passivated contact in the architecture of the solar cell 100 therefore makes conventional screen printing possible. This is advantageous as the solar cell architecture 100 can be easily applied in an industrial setting.

- 5 The solar cell 100 of the present embodiments may be deployed as a bottom cell for three-terminal (3T) tandem solar cell integration. Although the Si wafer 102 of the solar cell 100 of the present embodiments comprises a textured passivated front side, in a variation, the solar cell 100 comprises a non-textured (or planar) front side for better 3T tandem solar cell integration. In a variation, the solar cell 100 may comprise a textured
10 rear side for better 3T tandem solar cell integration (i.e. instead of the planar rear side of the Si wafer 102 as shown in Figure 1).

Figure 14 shows a schematic of a three-terminal (3T) tandem solar cell 1400 comprising a top solar cell 1402 and a bottom solar cell 1404 in accordance with an embodiment. The bottom solar cell 1404 employs a similar structure 100 as shown in Figure 1, except
15 for the textured front side of the Si wafer 102 and the front side passivation layer 104. In this embodiment, the n-type crystalline Cz Si wafer 102 has a planar front side without the deposited front side passivation layer 104. The rest of the structures of the bottom solar cell 1404 are similar to those of the solar cell 100 and their descriptions are not repeated here. In the present embodiment, the planar front-side of the n-type Si wafer
20 102 advantageously simplifies formation of the top solar cell 1402 (for example, a thin film top solar cell 1406).

In order to form the 3T tandem solar cell 1400, once the bottom Si solar cell 1402 has been fabricated, several coupling layers 1408 may be deposited on the front-side of the bottom Si solar cell 1402. The thin film top solar cell 1406 (e.g. a thin-film perovskite
25 solar cell, consisting of an hole transport layer, a perovskite absorber layer and an electron transport layer) for forming the device integrated top solar cell 1402 is then deposited on top of the coupling layers 1408 using a process that does not damage the underlying coupling layer 1408 and the bottom Si solar cell 1402. A top transparent electrode 1410 (e.g. a transparent conductive oxide (TCO)) is then deposited on the thin
30 film top solar cell 1406. The top transparent electrode 1410 has a low sheet resistance and a high transparency. Metal gridlines 1412 are then deposited on the top transparent electrode 1410 to minimise series resistance through the top transparent electrode 1410.

Further, although SiO_x which has a moderate positive charge density has been used as the tunnel layer in the previously described embodiment, in a variation, the rear side dielectric tunnel layer 106 and/or the dielectric tunnel layer 112 can be formed by atomic layer deposited AlO_x or TiO_x (exhibiting a high negative interface charge, i.e. aiming at selective hole extraction) or by LPCVD deposited or atomic layer deposited SiN_x (exhibiting a high positive interface charge, i.e. aiming at selective electron extraction).

Other alternative embodiments include (1) using a p-doped Si wafer instead an n-doped Si wafer, (2) using an n^+ -poly-Si/ SiO_x / p^+ -poly-Si tunnel junction instead of a $\text{p}^+/\text{SiO}_x/\text{n}^+$ tunnel junction (i.e. the first doped semiconductor layer 108 is an n^+ poly-Si layer instead of a p^+ poly-Si layer, and that the second doped semiconductor layer 114 is a p^+ poly-Si layer instead of an n^+ poly-Si layer), and (3) excluding the contact dielectric layer 116 (e.g. the architecture of the solar cell formed by the method 400).

In a variation, each of the tunnel junction augmented passivated contacts 120 of the solar cell 100 comprises the rear surface dielectric tunnel layer 106, the first doped semiconductor layer 108 and the second doped semiconductor layer 114. In other words, the tunnel junction augmented passivated contact 120 in this variation does not include the dielectric tunnel layer 112. The performance of the tunnel junction augmented passivated contact 120 may be improved without the sandwiched dielectric tunnel layer 112 (e.g. the SiO_x interlayer). To form the tunnel junction augmented passivated contact 120 without the sandwiched dielectric tunnel layer 112, additional process steps are however required. For example, instead of forming openings 304 and 306 in the intermediate dielectric layer 110 at the step 214 and then depositing the dielectric tunnel layer 112 in the step 216 as discussed in relation to Figure 2, in this variation, the openings 304 are first formed in the intermediate dielectric layer 110 followed by depositing the dielectric tunnel layer 112 and subsequently forming the openings 306 in the intermediate dielectric layer 110 (or forming the openings 306 in both the dielectric tunnel layer 112 and the intermediate dielectric layer 110 if the dielectric tunnel layer 112 is full-area deposited on the rear side of the Si wafer 102). Therefore, compared to the method 200 which includes forming the openings 304 and 306 in one step (i.e. the step 214), an additional alignment step has to be performed in this variation in order to form the openings 306 in correction positions in relation to the openings 304.

In a variation, the steps 202 and 204 for texturing and passivating the front side of the Si wafer 102 are not performed as the first two method steps. In case of using LPCVD, which is a well established double-side deposition process technology for contact passivation already used in solar cell production, these steps may be performed at a later stage of the solar cell fabrication process. For example, texturing and passivating the front side of the Si wafer 102 in the method 200 can be performed after depositing the contact dielectric layer 116 in the step 220 where the contact dielectric layer 116 acts as a masking layer (when deposited on a full-area of the rear side of the Si wafer 102). Once the rear-side is masked, etching off of all unwanted front side deposited layers can be performed (e.g. if LPCVD, which is a double side deposition technology, is used in previously deposition steps such as the steps 206, 208, 212, 216 or 218, prior layers would have been deposited on both the front and rear side of the Si wafer 102), thereby also texturing the Si wafer 102 (c.f. the step 202). Since the masking layer for the etching process could at the same time constitute the contact dielectric layer 116, it will not have to be removed. In this case, following the texturing of the front side of the Si wafer 102, deposition of the front-side passivation layer 104 (i.e. the step 204) can be performed. After the deposition of the front-side passivation layer 104, the steps 222 to 226 as shown in Figure 2 can be performed to complete the fabrication of the solar cell 100. In other words, the steps 202 and 204 can be inserted between the steps 220 and 222 in the method 200.

Similar to the above, in a variation, the steps 202 and 204 can also be performed between the steps 218 and 226 of the method 400 as shown in Figure 4. In this case, given that the solar cell fabricated by the method 400 does not include the contact passivation layer 116, a masking layer will be deposited on the rear side of the Si wafer 102 before etching off all unwanted front side deposited layers (e.g. if LPCVD is performed for any of the prior deposition steps i.e. the steps 204, 206, 208, 212, 216 or 218). This etching process also textures a front side of the Si wafer 102 (i.e. the step 202). Following the texturing of the front side of the Si wafer 102, deposition of the front-side passivation layer 104 (i.e. the step 204) can be performed. In this embodiment however, no contact passivation layer 116 is deposited at the rear side of the Si wafer 102. Therefore, an additional process step of removal of the masking layer is required. Removal of the masking layer is preferably done before the deposition of the front-side passivation layer 104. After the removal of the masking layer, the step 226 as shown in

Figure 4 can be performed to complete the fabrication of the solar cell. In other words, the steps 202 and 204 (and an additional step for removing the masking layer) can be inserted between the steps 218 and 226 in the method 400.

Further work may be carried out in relation to the aforementioned process methods 200, 5 400. In particular, it may be feasible to deploy single side deposited PECVD layers to form the tunnel junction. The formation of the tunnel junction augmented passivated contact may be further optimized to reduce its tunneling resistance, for example by optimizing the doping profile within the contact passivation layers and/or by removing the SiO_x dielectric tunnel layer which is sandwiched in between the two doped 10 semiconductor layers. Alternatively, an ultra-thin conductive (TCO) interlayer could be deposited in between the two poly-Si layers, in order to further improve the tunnel junction properties

Although only certain embodiments of the present invention have been described in detail, many variations are possible in accordance with the appended claims. For 15 example, features described in relation to one embodiment may be incorporated into one or more other embodiments and vice versa.

Claims

1. A method of fabricating a solar cell, the solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side, the method comprising:

5 (i) depositing a rear surface dielectric tunnel layer on a surface of the rear side of the silicon wafer;

(ii) depositing a first doped semiconductor layer on the rear surface dielectric tunnel layer;

(iii) depositing a dielectric tunnel layer on the first doped semiconductor layer; and

10 (iv) depositing a second doped semiconductor layer on the dielectric tunnel layer to form a plurality of interdigitated contacts on the rear side of the silicon wafer, the second doped semiconductor layer having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the plurality of interdigitated contacts comprises alternating tunnel
15 junction augmented passivated contacts and conventional passivated contacts, each of the tunnel junction augmented passivated contacts comprises the rear surface dielectric tunnel layer, the first doped semiconductor layer and the second doped semiconductor layer, and each of the conventional passivated contacts comprises the dielectric tunnel layer and the second doped semiconductor layer, the conventional passivated contacts
20 being formed at openings of the first doped semiconductor layer and openings of the rear surface dielectric tunnel layer.

2. The method of claim 1, wherein each of the tunnel junction augmented passivated contacts further comprises the dielectric tunnel layer sandwiched between the first doped
25 semiconductor layer and the second doped semiconductor layer.

3. The method of claim 1, further comprising forming openings in the dielectric tunnel layer prior to (iv) depositing the second doped semiconductor layer such that each of the tunnel junction augmented passivated contacts formed comprises the second doped
30 semiconductor layer deposited directly on the first doped semiconductor layer.

4. The method of any one of claims 1 to 3, further comprising forming the openings of the rear surface dielectric layer or the openings of the first doped semiconductor layer using a femtosecond laser having an ultraviolet wavelength.

5. The method of any one of claims 1 to 4, further comprising depositing an intermediate dielectric layer between each of the alternating tunnel junction augmented passivated contacts and the conventional passivated contacts, wherein the tunnel junction augmented passivated contacts and the conventional passivated contacts are formed at openings of the intermediate dielectric layer.
6. The method of any one of claims 1 to 5, further comprising:
depositing a contact dielectric layer on the plurality of interdigitated contacts; and
depositing an interdigitated metal layer grid on the contact dielectric layer to form electrical contacts for the plurality of interdigitated contacts.
7. The method of any one of the preceding claims, wherein the silicon wafer is n-doped, (ii) depositing the first doped semiconductor layer comprises depositing a p-doped polysilicon layer and (iv) depositing the second-doped semiconductor layer comprises depositing an n-doped polysilicon layer.
8. The method of any one of the preceding claims, wherein (iv) depositing the second doped semiconductor layer further comprises depositing the second doped semiconductor layer on an entire area of the rear side of the silicon wafer, the method further comprising forming isolation trenches in the second doped semiconductor layer to form the plurality of interdigitated contacts.
9. The method of any one of the preceding claims, further comprising texturing the front side of the silicon wafer.
10. The method of any one of the preceding claims, further comprising texturing the rear side of the silicon wafer.
11. A solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side, the solar cell comprising:
a rear surface dielectric tunnel layer deposited on a surface of the rear side of the silicon wafer;

a first doped semiconductor layer deposited on the rear surface dielectric tunnel layer;

a dielectric tunnel layer deposited on the first doped semiconductor layer; and

a second doped semiconductor layer deposited on the dielectric tunnel layer to
5 form a plurality of interdigitated contacts on the rear side of the silicon wafer, the second doped semiconductor layer having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the plurality of interdigitated contacts comprises alternating tunnel
junction augmented passivated contacts and conventional passivated contacts, each of
10 the tunnel junction augmented passivated contacts comprises the rear surface dielectric tunnel layer, the first doped semiconductor layer and the second doped semiconductor layer, and each of the conventional passivated contacts comprises the dielectric tunnel layer and the second doped semiconductor layer, the conventional passivated contacts being formed at openings of the first doped semiconductor layer and openings of the rear
15 surface dielectric tunnel layer.

12. The solar cell of claim 11, wherein each of the tunnel junction augmented passivated contacts further comprises the dielectric tunnel layer sandwiched between the first doped semiconductor layer and the second doped semiconductor layer.

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13. The solar cell of claim 11, further comprising openings formed in the dielectric tunnel layer prior to the second doped semiconductor layer being deposited on the dielectric tunnel layer, such that each of the tunnel junction augmented passivated contacts formed comprises the second doped semiconductor layer deposited directly on the first doped
25 semiconductor layer.

14. The solar cell of any one of claims 11 to 13, wherein the openings of the rear surface dielectric layer or the openings of the first doped semiconductor layer are formed using a femtosecond laser having an ultraviolet wavelength.

30

15. The solar cell of any one of claims 11 to 14, further comprising an intermediate dielectric layer deposited between each of the alternating tunnel junction augmented passivated contacts and the conventional passivated contacts, wherein the tunnel

junction augmented passivated contacts and the conventional passivated contacts are formed at openings of the intermediate dielectric layer.

16. The solar cell of any one of claims 11 to 15, further comprising:

- 5 a contact dielectric layer deposited on the plurality of interdigitated contacts; and
 an interdigitated metal layer grid deposited on the contact dielectric layer to form electrical contacts for the plurality of interdigitated contacts.

17. The solar cell of any one of claims 11 to 16, wherein the silicon wafer is n-doped, the
10 first doped semiconductor layer comprises a p-doped polysilicon layer and the second doped semiconductor layer comprises an n-doped polysilicon layer.

18. The solar cell of any one of claims 11 to 17, wherein the second doped semiconductor layer is deposited on an entire area of the rear side of the silicon wafer, the solar cell
15 further comprises isolation trenches formed in the second doped semiconductor layer for forming the plurality of interdigitated contacts.

19. The solar cell of any one of claims 11 to 18, wherein the front side of the silicon wafer is textured.

20

20. The solar cell of any one of claims 11 to 19, wherein the rear side of the silicon wafer is textured.

21. A tandem solar cell comprising:

- 25 a top solar cell; and
 a bottom solar cell, wherein the bottom solar cell comprises a silicon wafer having a front side arranged to receive incident light via the top solar cell and a rear side, the bottom solar cell comprising:
 a rear surface dielectric tunnel layer deposited on a surface of the rear
30 side of the silicon wafer;
 a first doped semiconductor layer deposited on the rear surface dielectric tunnel layer;
 a dielectric tunnel layer deposited on the first doped semiconductor layer;
and

a second doped semiconductor layer deposited on the dielectric tunnel layer to form a plurality of interdigitated contacts on the rear side of the silicon wafer, the second doped semiconductor layer having a doping of an opposite polarity to the first doped semiconductor layer,

5 wherein the plurality of interdigitated contacts comprises alternating tunnel junction augmented passivated contacts and conventional passivated contacts, each of the tunnel junction augmented passivated contacts comprises the rear surface dielectric tunnel layer, the first doped semiconductor layer and the second doped semiconductor layer, and each of the conventional passivated contacts comprises the dielectric tunnel
10 layer and the second doped semiconductor layer, the conventional passivated contacts being formed at openings of the first doped semiconductor layer and openings of the rear surface dielectric tunnel layer.

22. The tandem solar cell of claim 21, wherein the top solar cell and the bottom solar cell
15 are integrated to form a three-terminal tandem solar cell structure.

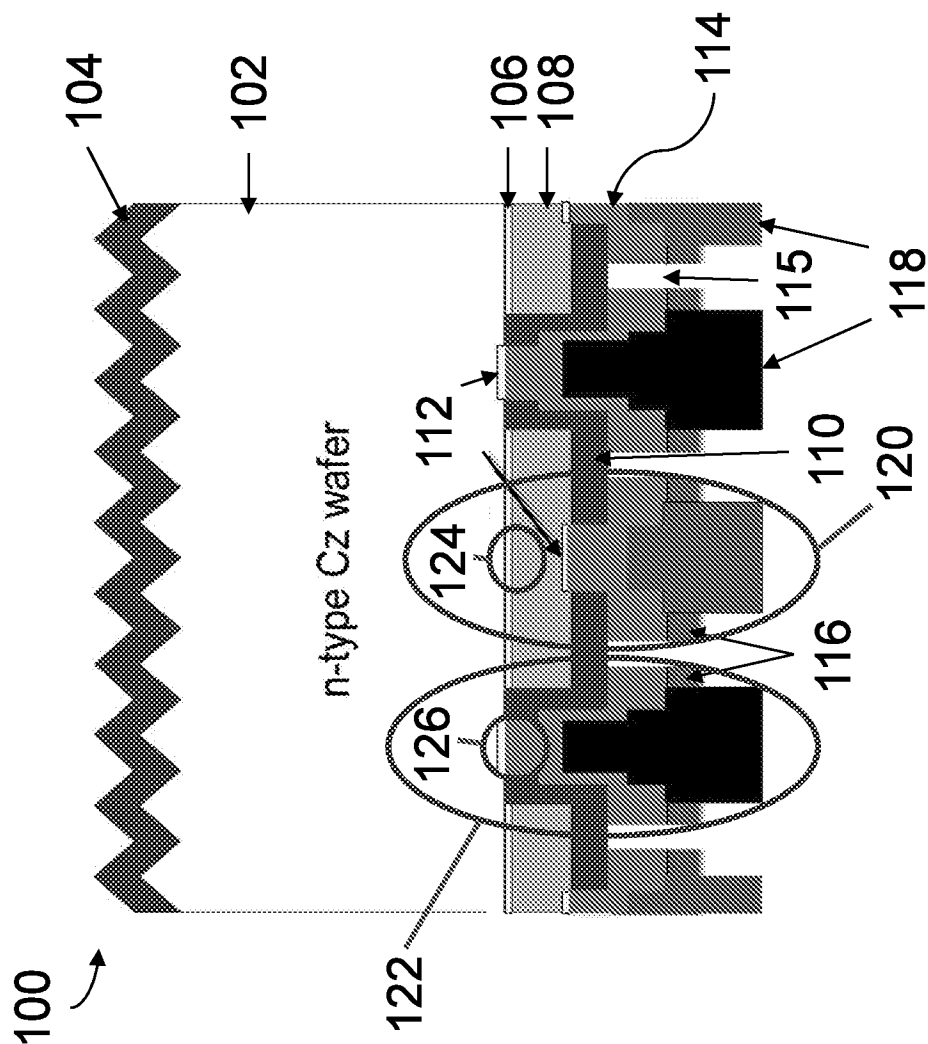


Figure 1

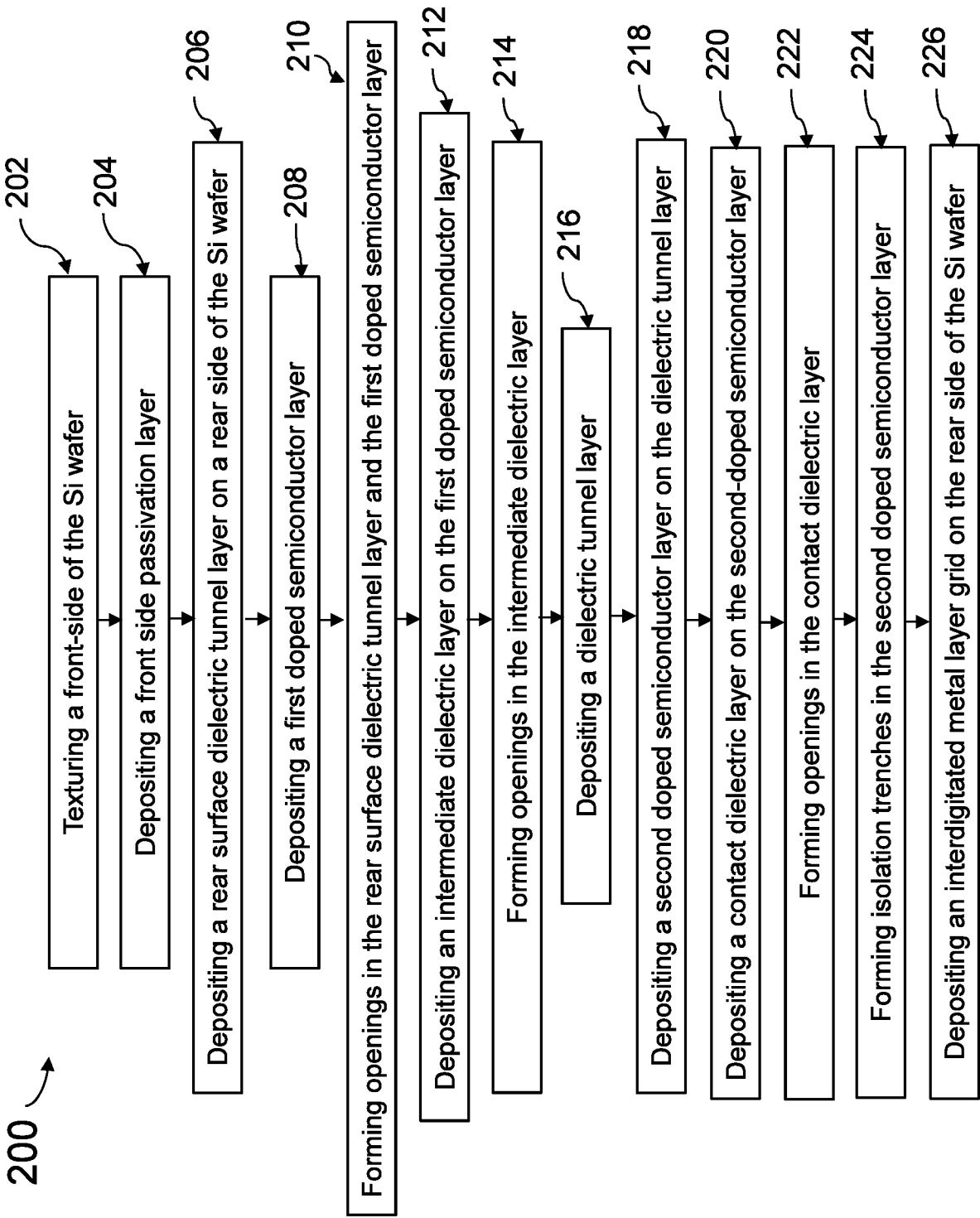


Figure 2

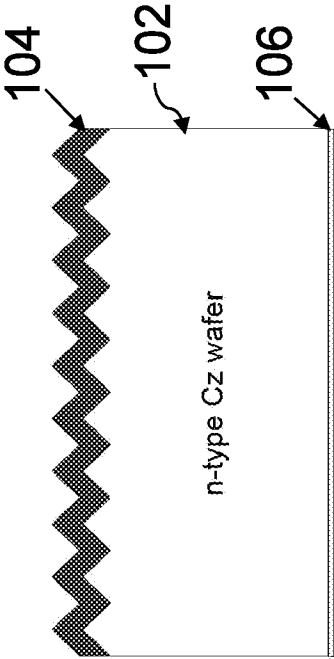


Figure 3A

Figure 3B

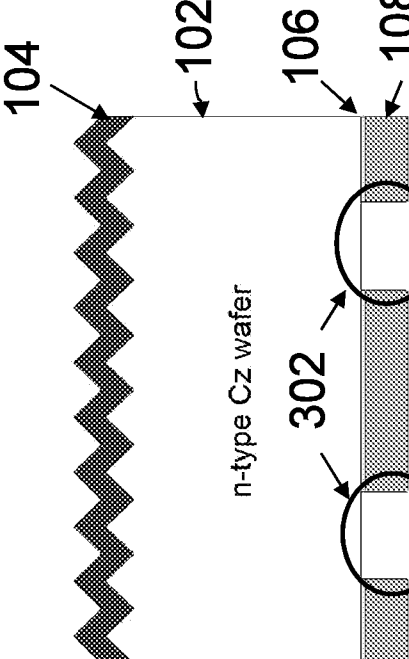
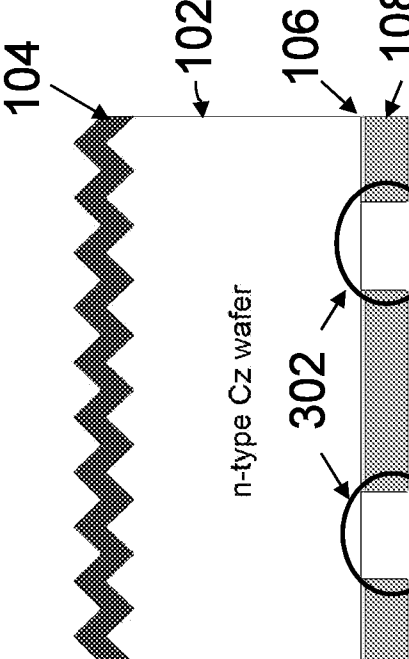


Figure 3C

Figure 3D



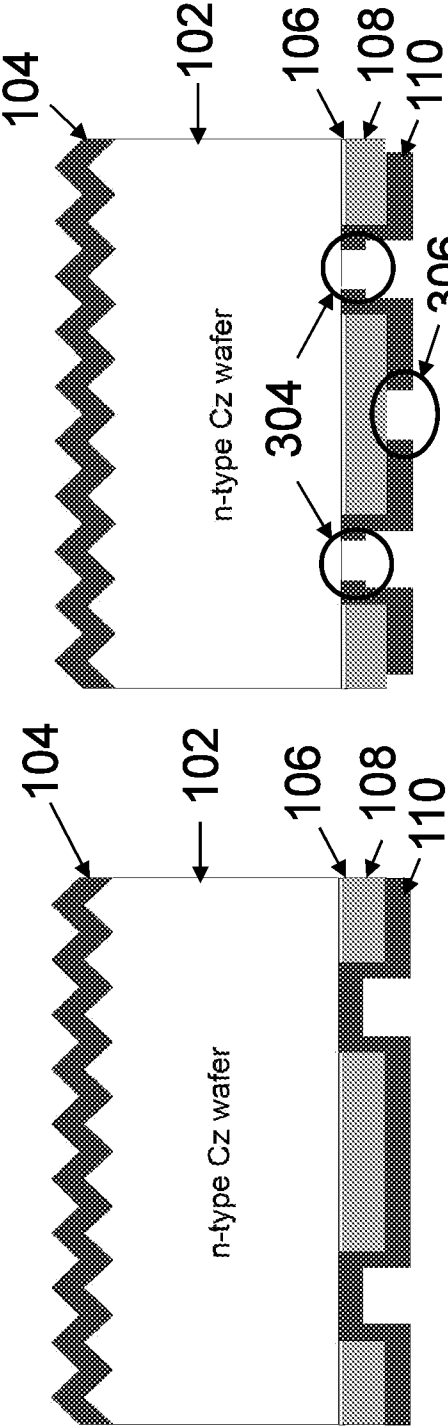


Figure 3F

Figure 3E

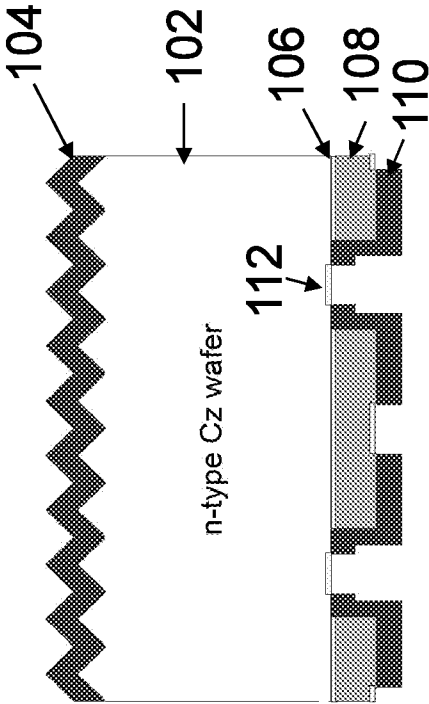


Figure 3G

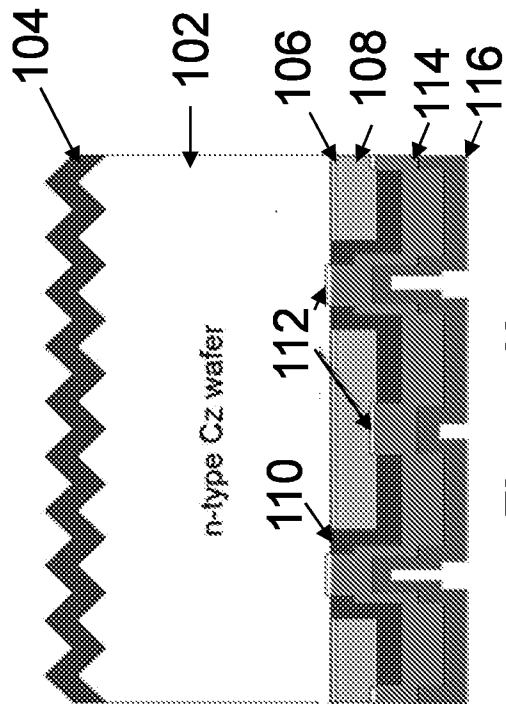


Figure 31

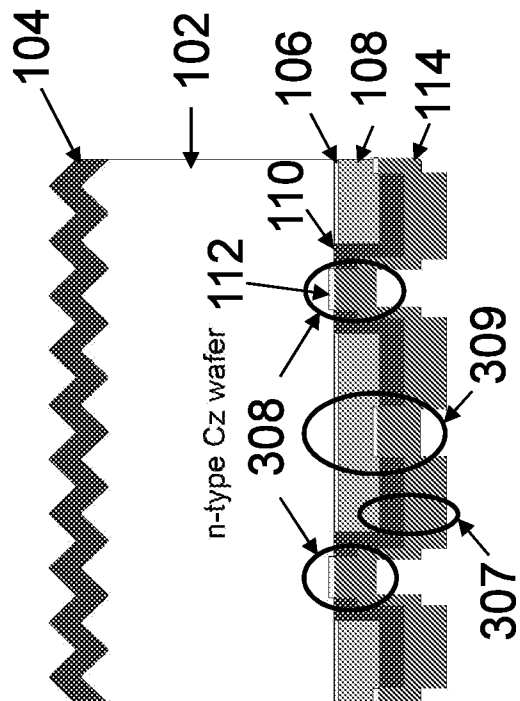


Figure 3H

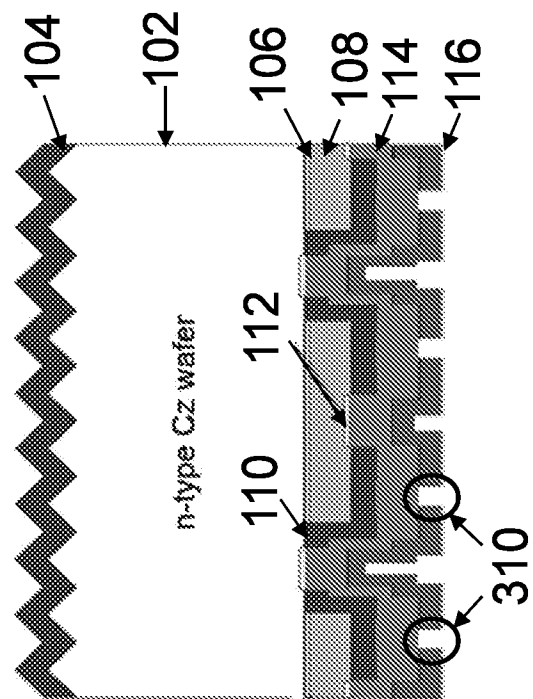
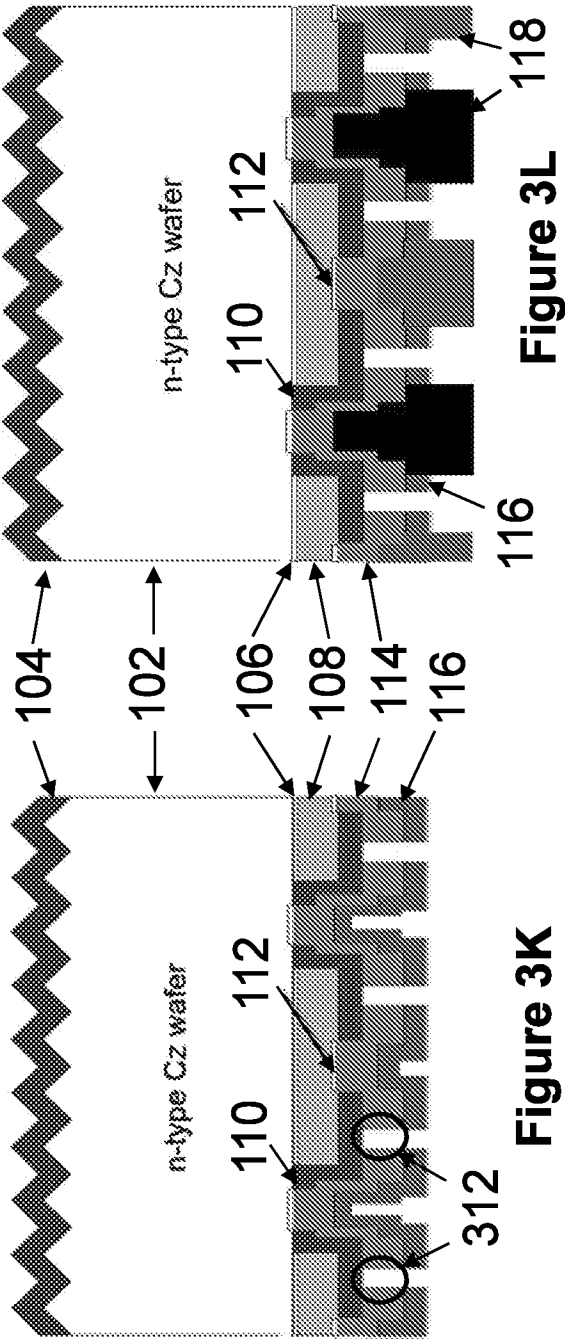


Figure 3J



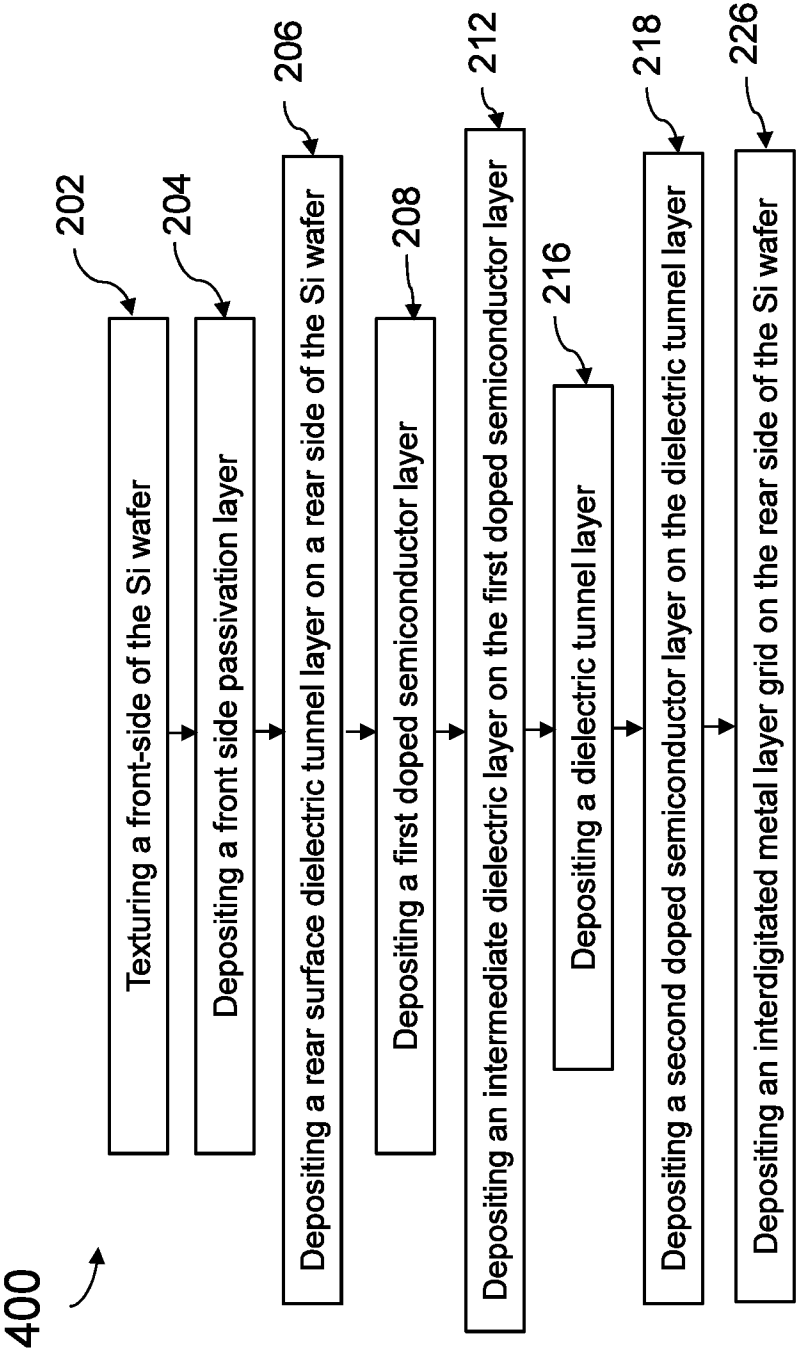
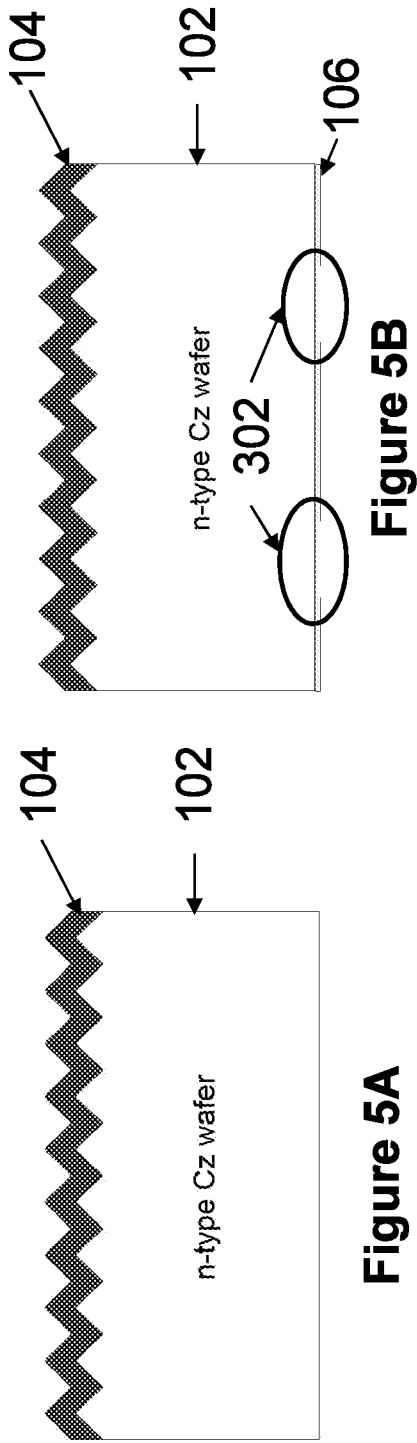
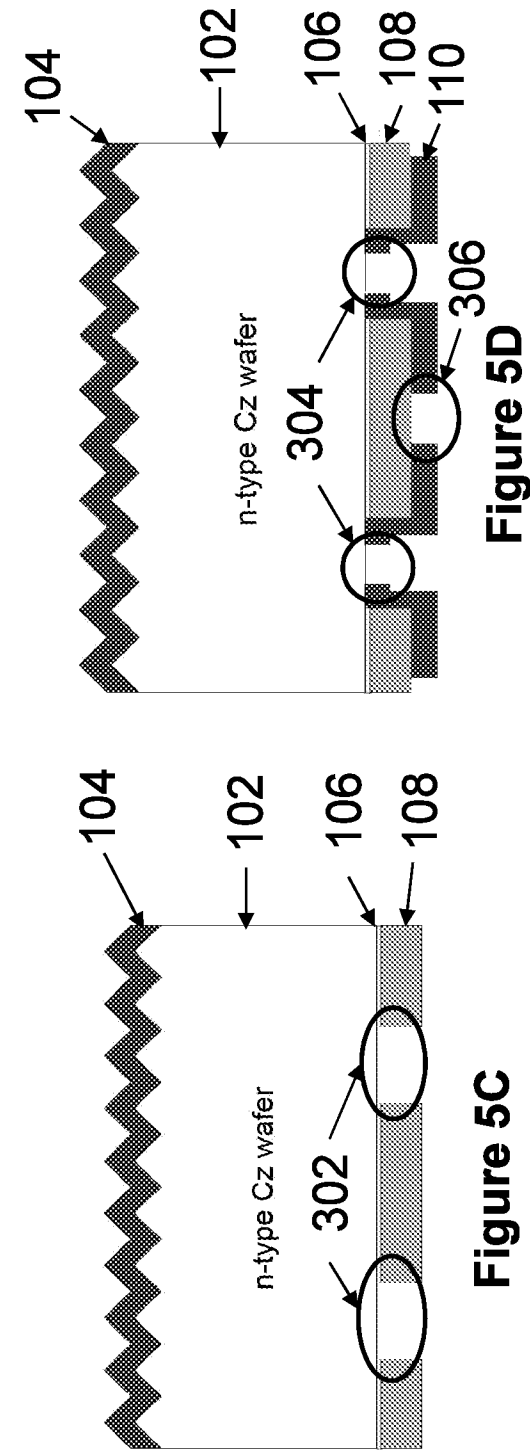
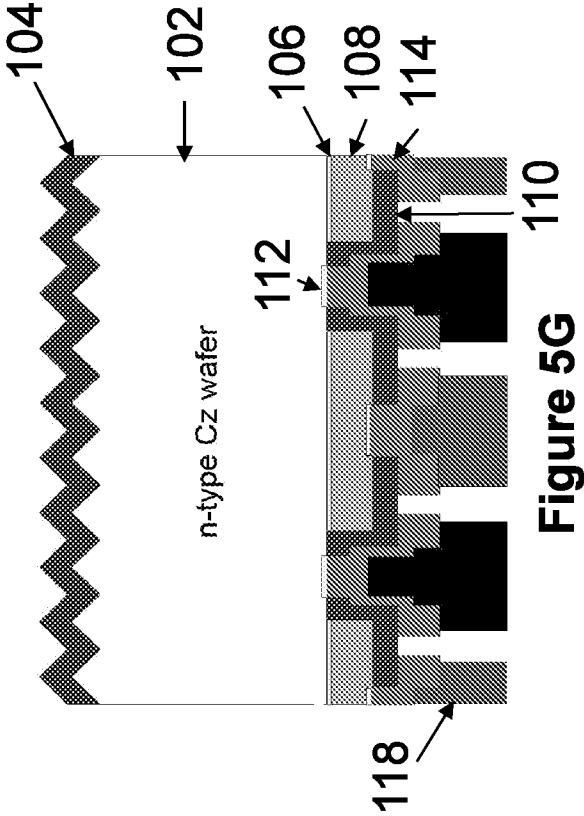
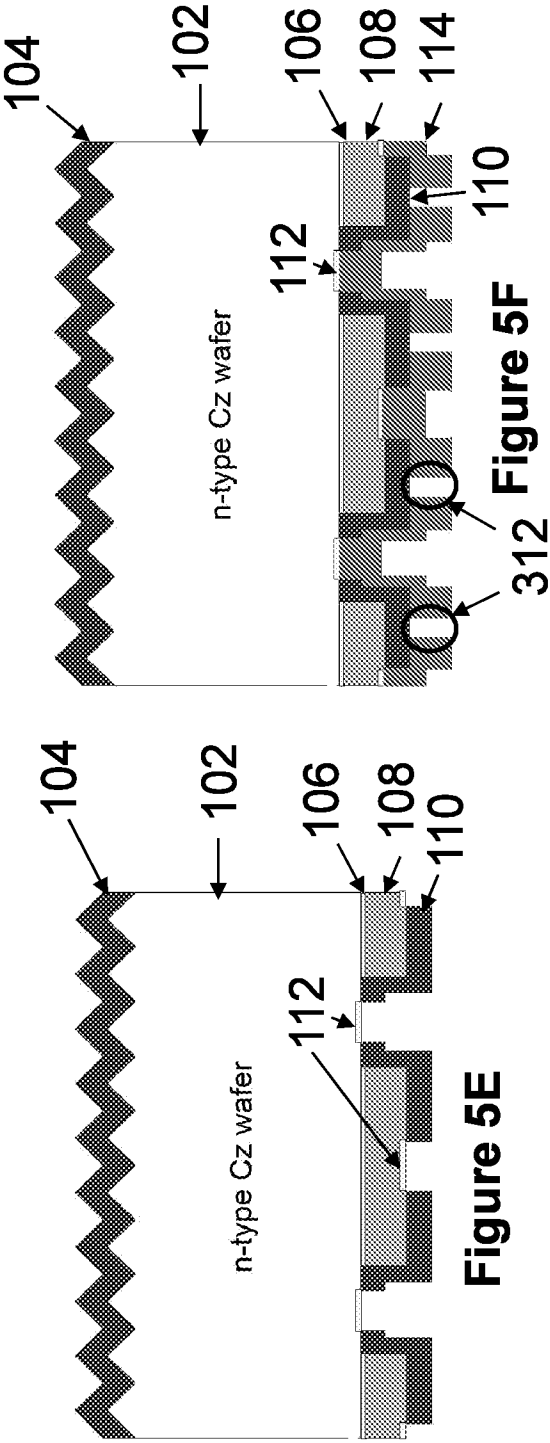


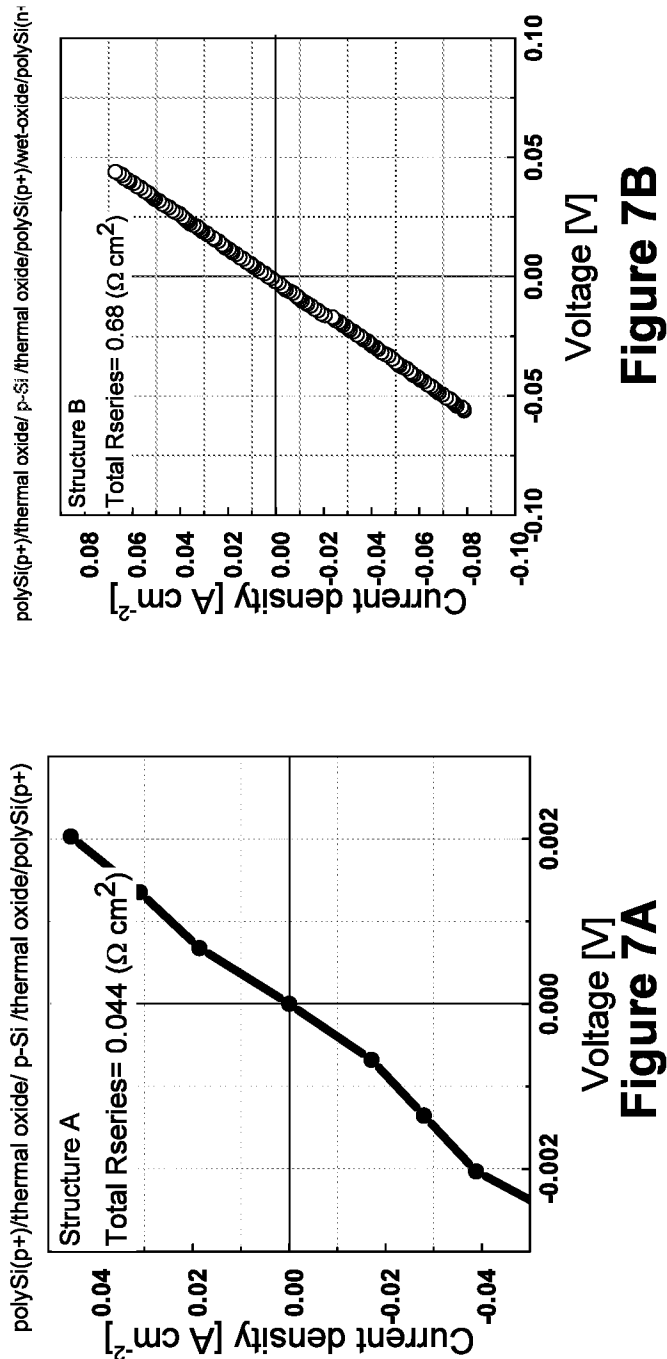
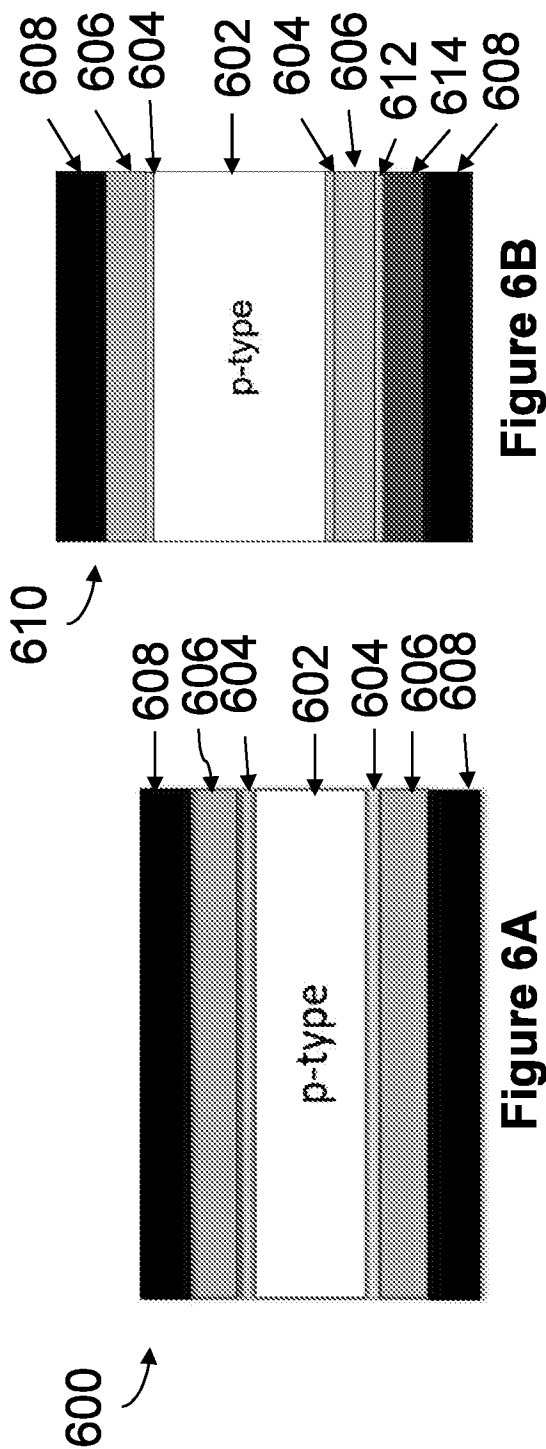
Figure 4



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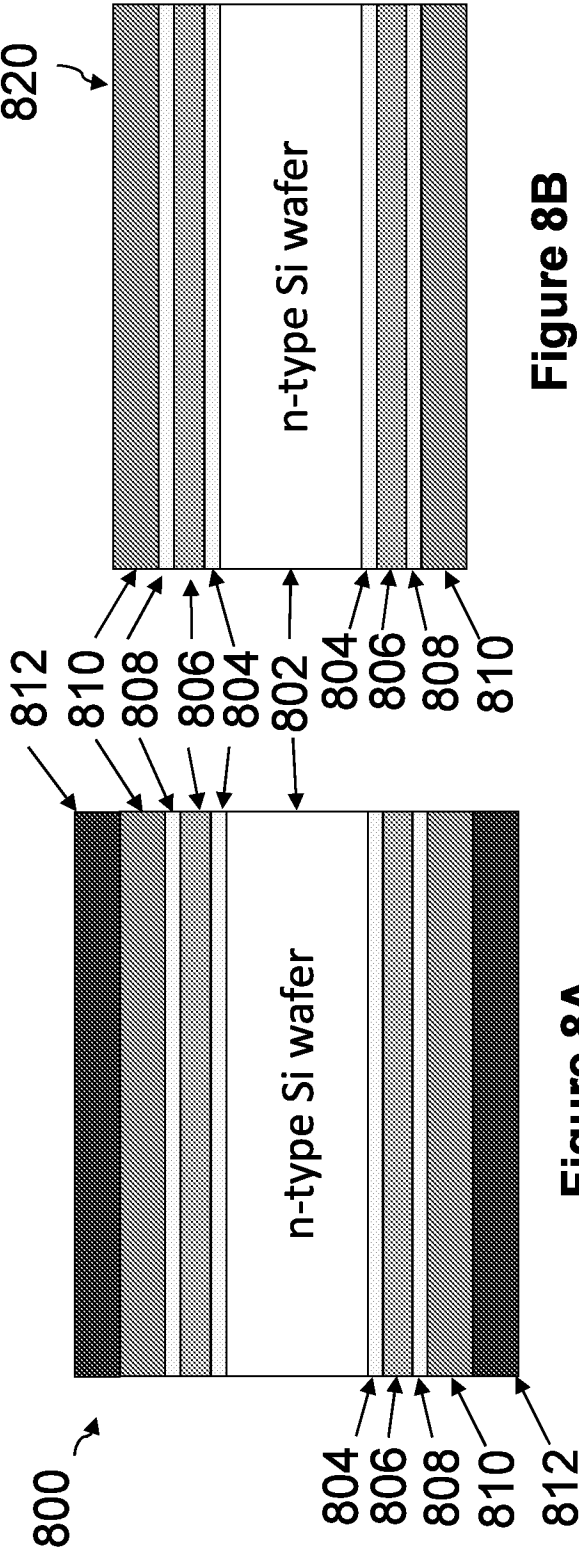


Figure 8B

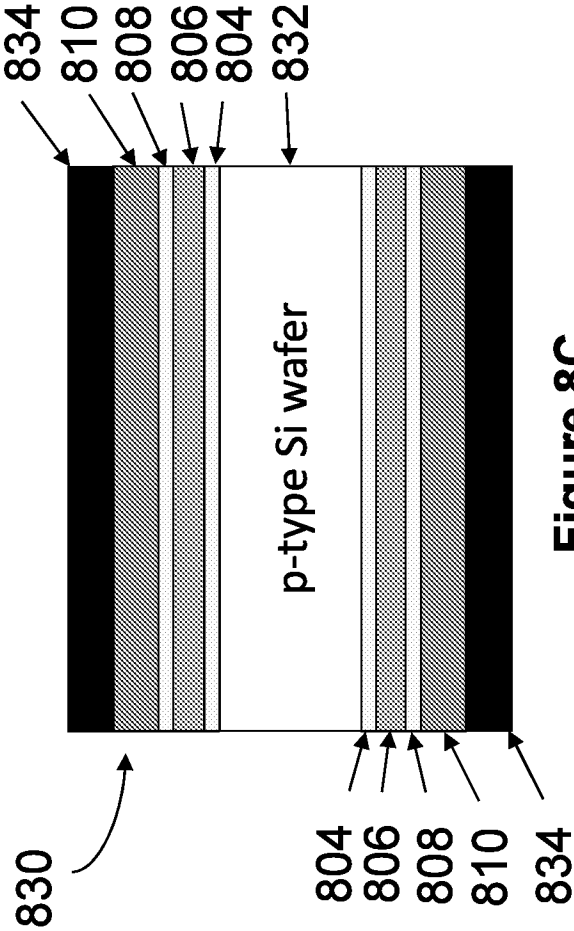


Figure 8C

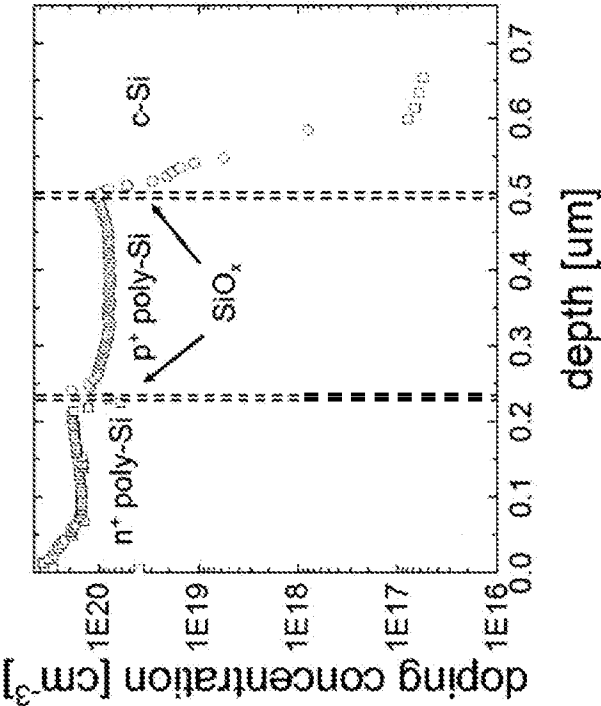


Figure 9A

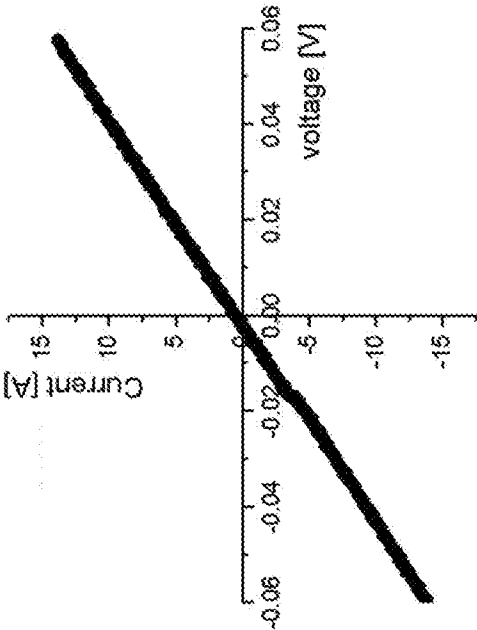


Figure 9B

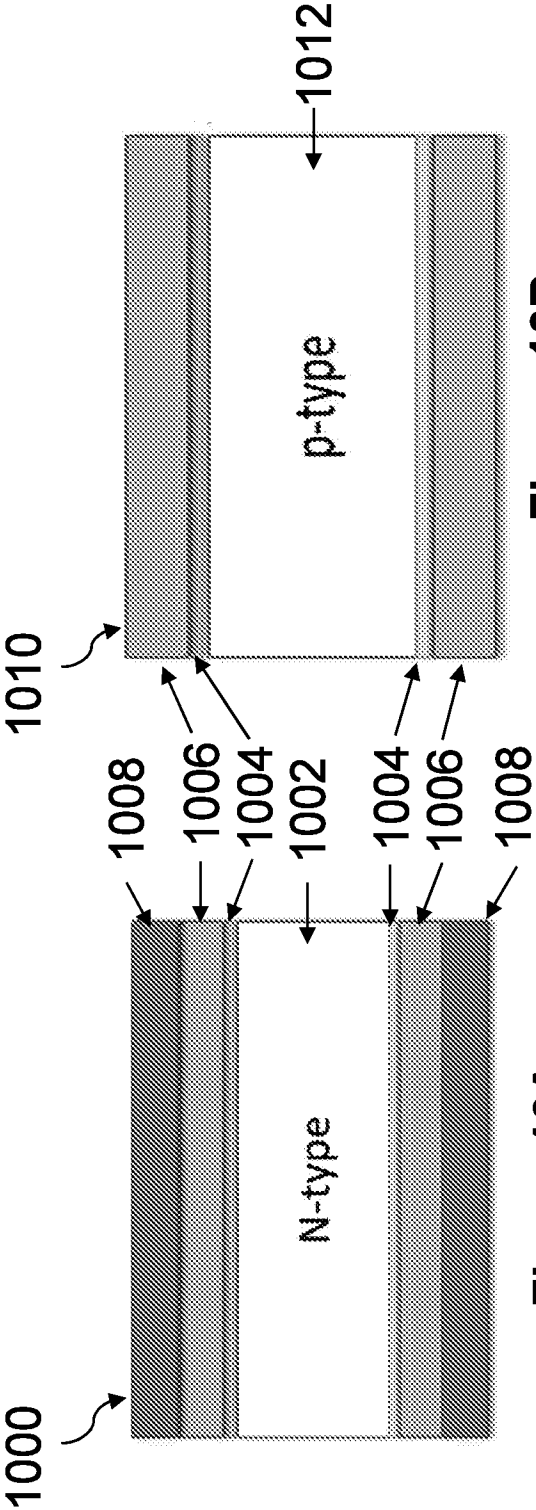


Figure 10A

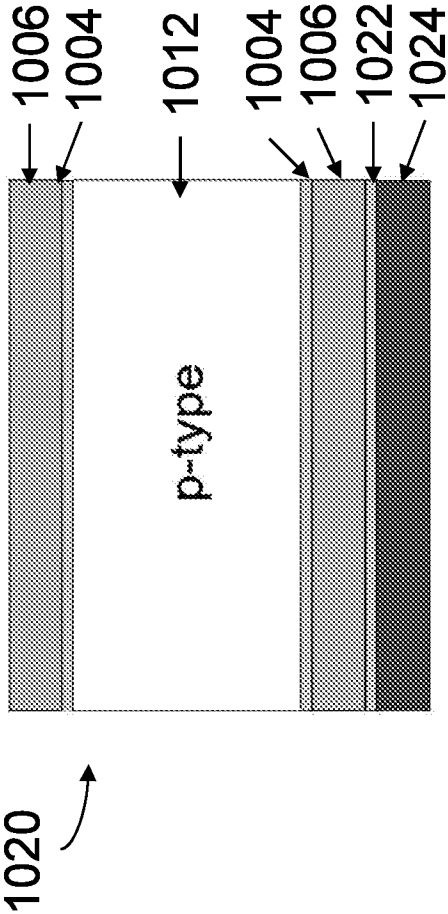


Figure 10C

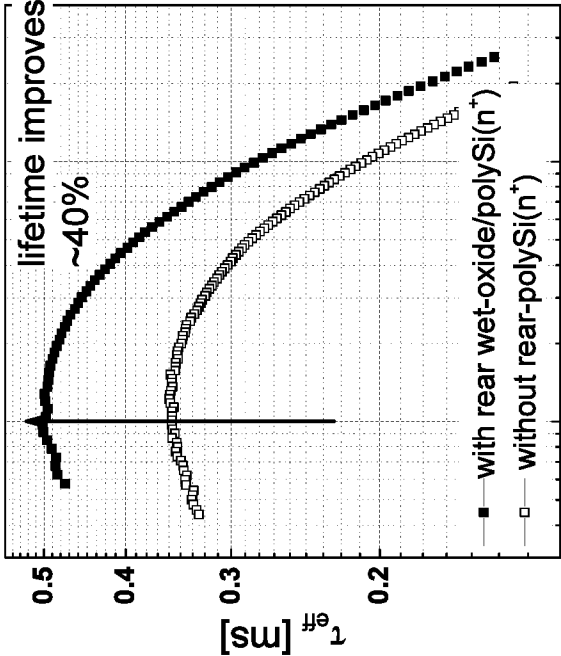


Figure 11B

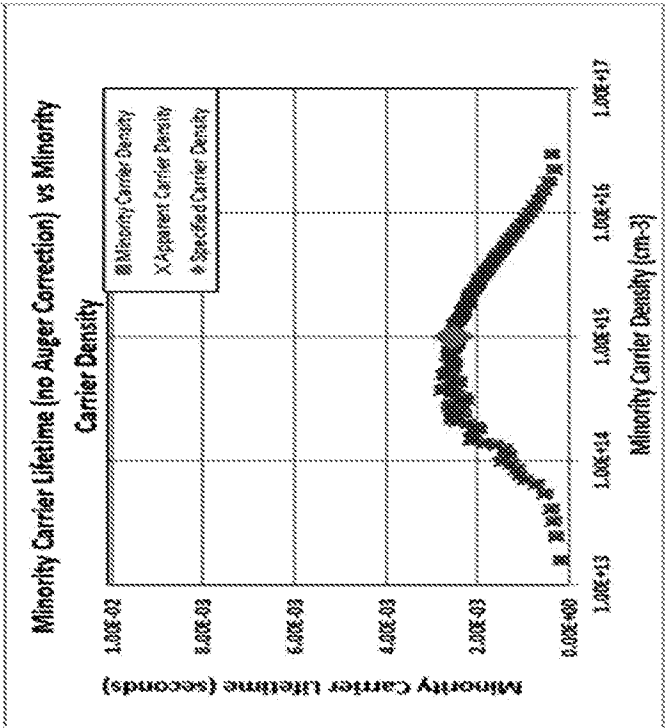


Figure 11A

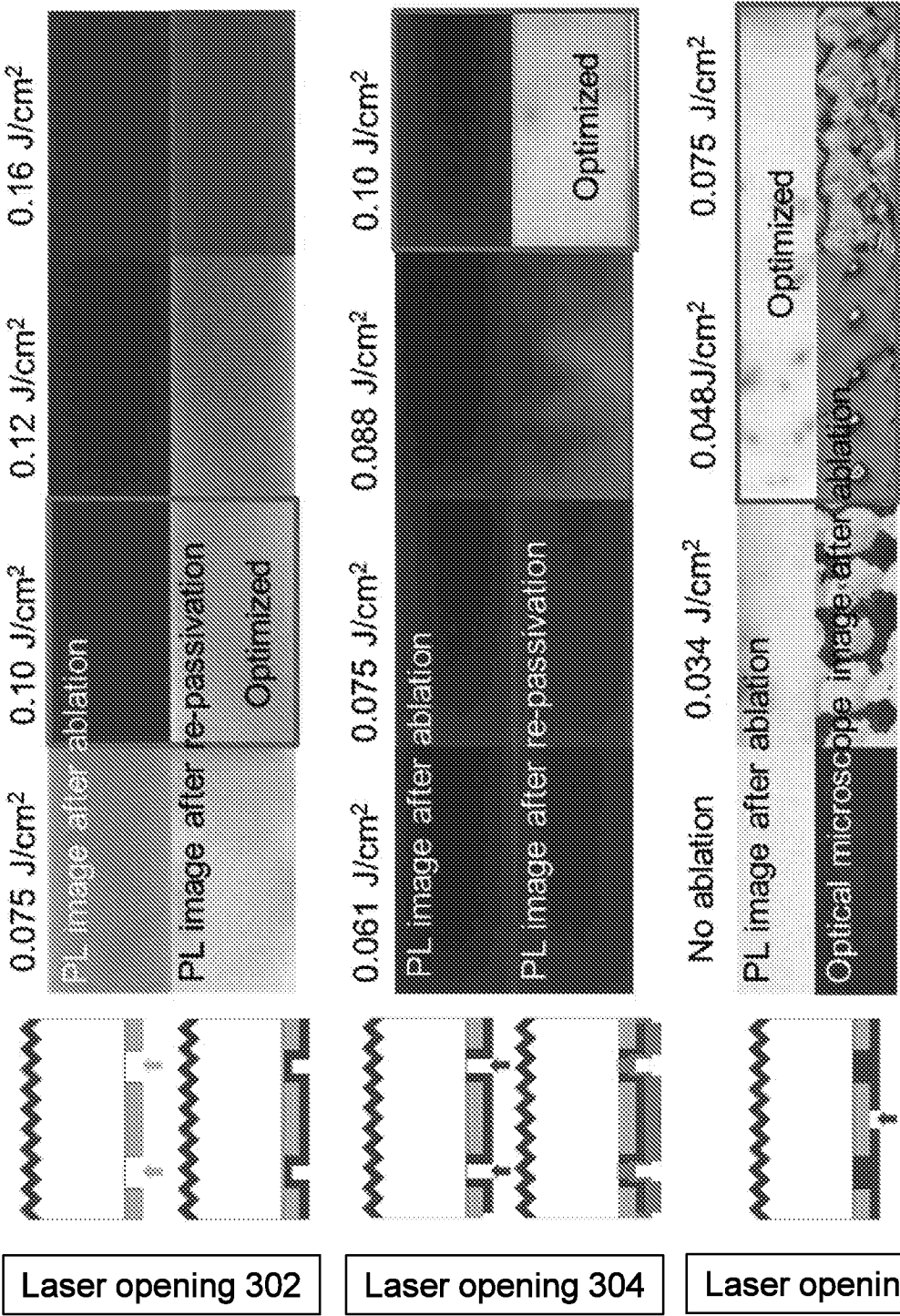
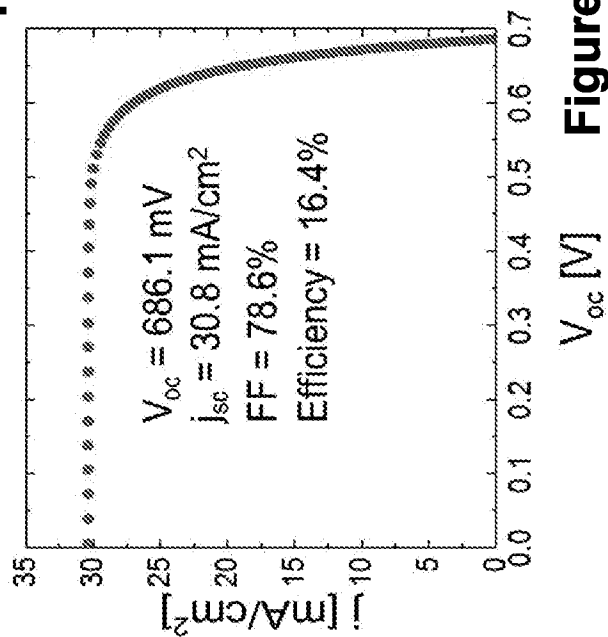
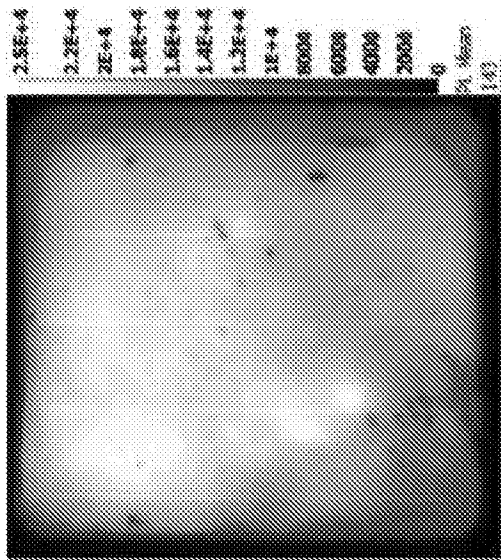
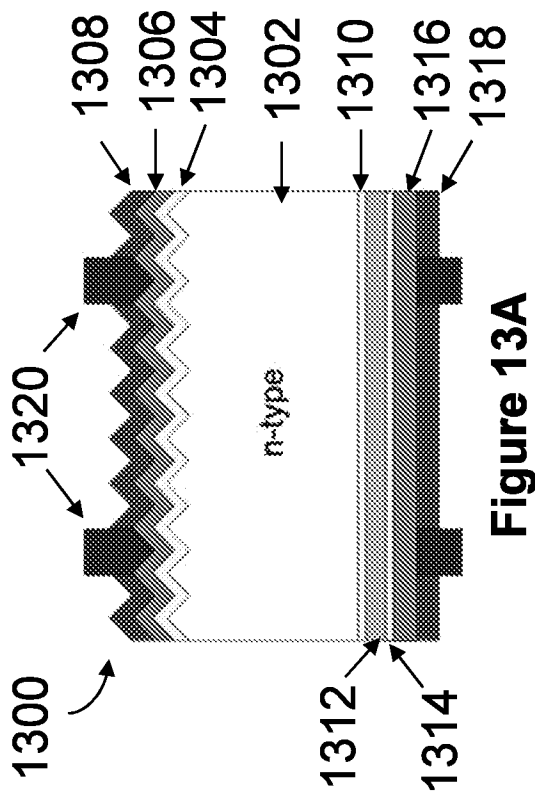


Figure 12



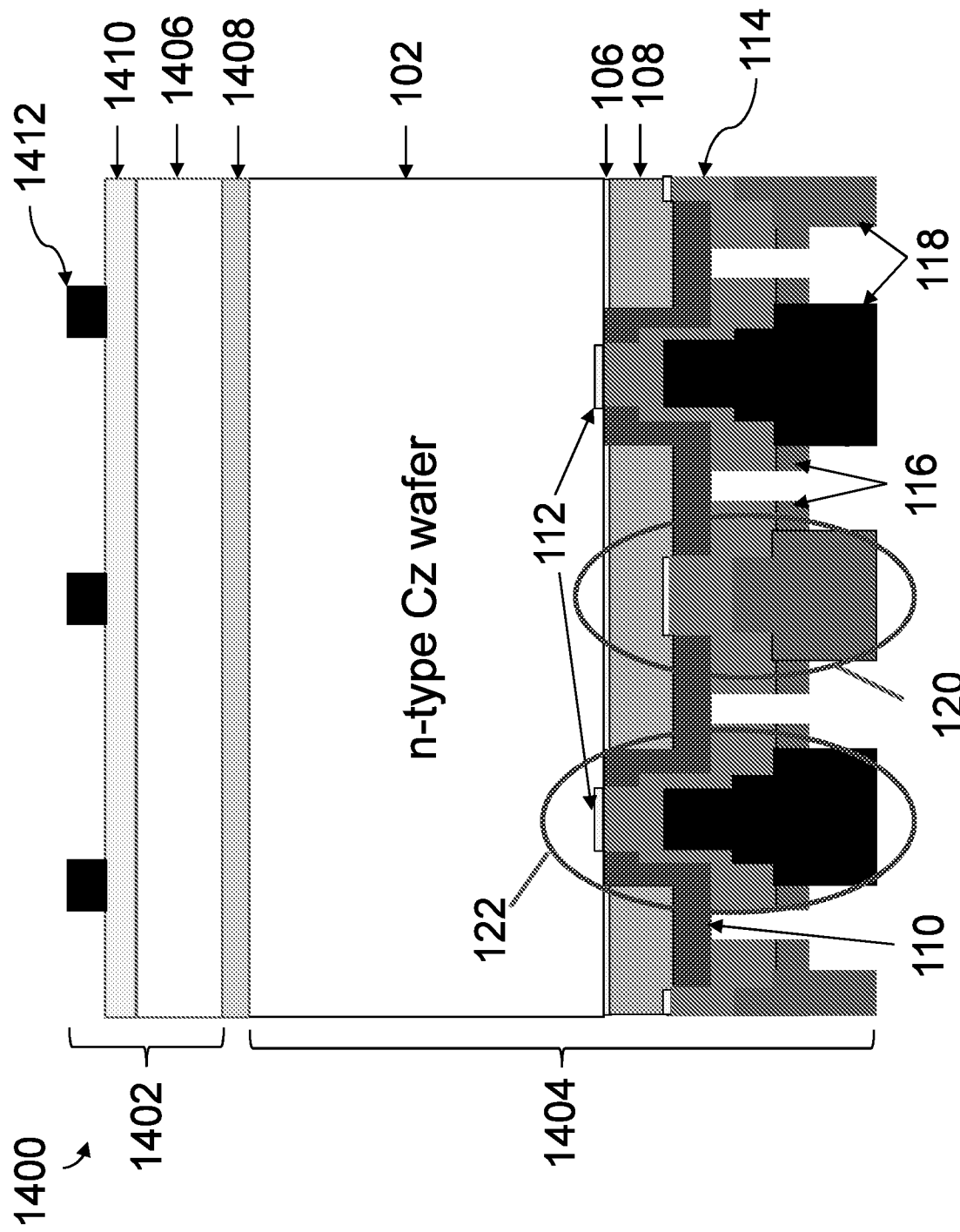


Figure 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2020/050096

A. CLASSIFICATION OF SUBJECT MATTER

H01L 31/18 (2006.01) H01L 21/00 (2006.01) H01L 31/04 (2014.01)

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT:

solar cell, tunnel, dielectric, deposit, coat, laser, ablation, pattern, back contact, interdigitate contact, heterojunction, 太阳能电池, 隧穿, 沉积, 镀膜, 激光, 开槽, 背结, 叉指电极, 异质结 and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 3319132 A1 (IMEC VZW ET AL.) 19 May 2018 Whole document, especially figs. 10, 17, para. [0081]	1-22
A	US 9627558 B2 (TRACY C. J. ET AL.) 18 April 2017 Whole document	
A	US 2017/0288070 A1 (TRACY K. M. ET AL.) 5 October 2017 Whole document	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

*Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

24/06/2020

(day/month/year)

Date of mailing of the international search report

25/06/2020

(day/month/year)

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2020/050096

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	TOMASI A. ET AL., Simple processing of back-contacted silicon heterojunction solar cells using selective-area crystalline growth. <i>Nature Energy</i> , 24 April 2017, Vol. 2, No. 5, pages 17062 [Retrieved on 2020-06-24] <DOI: HTTPS://10.1038/NENERGY.2017.62 > Whole document	
A	YAMAMOTO K. ET AL., High-efficiency heterojunction crystalline Si solar cells. <i>Japanese Journal of Applied Physics</i> , 18 July 2018, Vol. 57, No. 8S3, pages 08RB20 [Retrieved on 2020-06-24] <DOI: HTTPS://DOI.ORG/10.7567/JJAP.57.08RB20 > Whole document	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2020/050096

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 3319132 A1	09/05/2018	JP 2018-093180 A US 2018/0122963 A1	14/06/2018 03/05/2018
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US 2017/0288070 A1	05/10/2017	US 2019/0189813 A1 KR 20180122745 A WO 2017/173383 A1 DE 112017001811 T5 CN 109716535 A US 2020/0119220 A1	20/06/2019 13/11/2018 05/10/2017 20/12/2018 03/05/2019 16/04/2020