



(51) International Patent Classification:
H01L 23/525 (2006.01)

(21) International Application Number:
PCT/US2016/040063

(22) International Filing Date:
29 June 2016 (29.06.2016)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: SYSTEMS, METHODS AND DEVICE FOR A FUSE ARRAY

(1) Post Liner Deposition

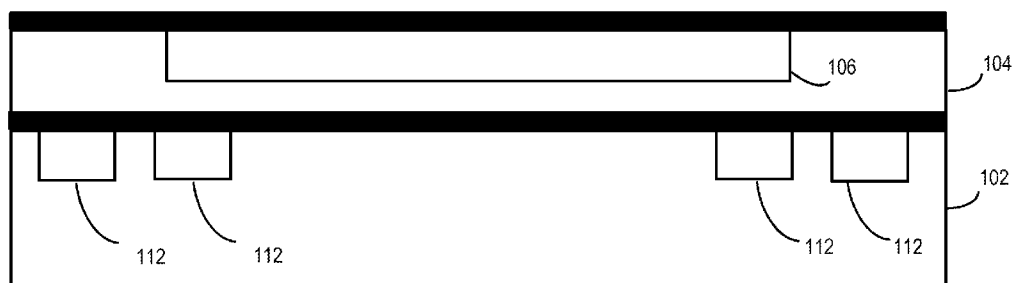


FIG. 1

(57) **Abstract:** A resistivity of a fuse element can be increased by using a local implant constructed with an implant mask and fuse array as an embedded heater. The fuse array can be used as an embedded heater to anneal and "activate" implants in a localized and customized manner. The implants and annealing can be used to (1) change the chemical composition into high resistive elements, (2) create voids within fuse elements via hydrogen embrittlement, and (3) create stress induced voiding with customized annealing. These chemical reactions can further increase the resistance of the fuse elements, without impacting or minimally impacting surrounding active elements.



Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

- *with international search report (Art. 21(3))*

SYSTEMS, METHODS AND DEVICES FOR A FUSE ARRAY

Technical Field

[0001] The present disclosure relates to formation of integrated chips and more specifically to fuse array construction.

Background

[0002] Semiconductor integrated chips can be fabricated in a process that includes imaging, deposition and etching. Additional steps can include doping and cleaning. Wafers (such as mono-crystal silicon wafers, silicon on sapphire wafers or gallium arsenide wafers) can be used as a substrate. Photolithography can be used to mark areas of the wafer for enhancement through doping or deposition. An integrated circuit (or chip) is composed of a plurality of layers, which can include diffusion layers (which can include dopants), implant layers (which can include additional ions), metal layers (defining conduction) and/or via or contact layers (which can define conduction between layers).

Brief Description of the Drawings

[0003] FIG. 1 is a diagram of a post liner deposition operation consistent with embodiments disclosed herein.

[0004] FIG. 2 is a diagram of an implanting operation consistent with embodiments disclosed herein.

[0005] FIG. 3 is a diagram of an implant removal operation consistent with embodiments disclosed herein.

[0006] FIG. 4 is a diagram of a local annealing operation consistent with embodiments disclosed herein.

[0007] FIG. 5 is a diagram illustrating an interposer consistent with embodiments disclosed herein.

[0008] FIG. 6 is a box diagram illustrating a computing device consistent with embodiments disclosed herein.

[0009] FIG. 7 is a flow chart illustrating an implant and annealing method consistent with embodiments disclosed herein.

Detailed Description

[0010] Described herein are systems and methods of increasing a resistivity of a fuse element with a local implant by using an implant mask and fuse array as an embedded heater. The fuse array can be used as an embedded heater to anneal and “activate” implants in a localized and customized manner. The implants and annealing can be used to (1) change the chemical composition into high resistive elements, such as CuO, (2) create voids within fuse elements via hydrogen embrittlement ($CuO + H_2 \rightarrow Cu + H_2O$), and (3) create stress induced voiding with customized annealing. These chemical reactions can further increase the resistance of the fuse elements, without impacting or minimally impacting surrounding active elements.

[0011] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0012] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention. However, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0013] The terms “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0014] Implementations of the invention may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternative materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

[0015] A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the invention, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the invention may also be carried out using nonplanar transistors.

[0016] Each MOS transistor includes a gate stack formed of at least two layers: a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0017] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal

layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0018] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0019] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the invention, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0020] In some implementations of the invention, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternative implementation, a plurality of spacer pairs may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0021] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing

process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternative semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0022] One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0023] With an increasing emphasis in robust metallization, a side effect has arisen in fuse array structures. The fuse array becomes robust and hard to break. As the fuse array is part of an active die, it goes through the same processing steps as other structures. However, additional operations can be performed to aid in creating an effective fuse array, such as to make the fuse array easy to break with a reasonable amount of current. These additional operations can be performed without impacting yield and/or reliability of surrounding active components and with minimal process change.

[0024] This implant and annealing process can provide a robust solution for a fuse array. In contrast, some processes fabricate the fuse array in the same steps used to fabricate active elements, resulting in a more difficult to break fuse array. By using an implant and annealing process, the proposed operations can enable the fuse array to move up to mid and/or upper back end (BE) layers with bigger critical dimension (CD) and/or pitch, as resistance change may create heat sufficient to break fuses with a larger CD. Moving the fuse array can enable saving previous space in lower BE layers for signals, and to avoid any detrimental effect to neighboring ferroelectric (FE) structures.

[0025] This implant and annealing process can create an effective fuse array that can be easily broken (i.e., blown away) with a reasonable amount of current shock. The fuse array can be processed differently from a remaining part of the die. This process can increase a resistivity of the fuse array and decrease an effective cross-sectional area where current passes through the fuse array.

[0026] Based on Ohm's law, these changes can increase the resistance of the fuse array.

$R = \rho \frac{l}{A}$. This higher resistance increases heat generation. $Q = I^2 R$. A larger heat generation accelerates a breakage of a fuse element in a fuse array. Achieving high resistivity and small effective cross-sectional area can be accomplished with local implanting and annealing.

[0027] While implant masks can be used for FE structures for doping, the implant mask can be used for a BE layer to locally implant foreign elements for use in the implant and annealing process. Some elements are summarized in a table below along with a description of potential purpose.

Element(s)	Chemical Reaction	Estimated Purpose
Ar, Xe or other inert species	Physical sputtering	Damage etch stop, create crystalline defects for void nucleation
Oxygen, or any species that creates resistive film	$Cu + O = CuO$	Oxidation of copper, structurally weakens interface between liner and copper. The activation energy of copper migration on weak interface is smaller than bulk copper, which accelerates the failures of the line, under high electric field. Further cures low-k dielectric film (shrinks the film) to further promote stress induced voids (SIV). The low-k dielectric film that is used as the insulation layer between Cu interconnect is porous dielectric material. This low-k dielectric films will be "cured" further in the presence of oxygen; during this process, the film becomes denser than original state, or shrinks.
Hydrogen	$CuO + H_2 = Cu + H_2O + voids$	Creates voids, aka, hydrogen embrittlement by reacting with metal oxides

[0028] FIGS. 1-4 show diagrams of operations performed in the implant and annealing process for fuse arrays. A current carrying liner 106 (such as metal) is deposited on a layer 104. The liner 106 is implanted with species 214 (e.g., dopants) to increase the resistivity of the liner 106 (such as Argon (Ar), Xenon (Xe), Oxygen and/or Hydrogen). An implant mask 202 is removed and electrodes 402 and 404 are used to provide current to the liner 414 to diffuse dopants (i.e., implants), initiate chemical reactions and/or speed up chemical reactions. FIG. 1 is a diagram of a post liner deposition operation. FIG. 2 is a diagram of a implanting operation. FIG. 3 is a diagram of an implant removal operation. FIG. 4 is a diagram of a local annealing operation.

[0029] In one embodiment, a current carrying liner 106 (such as a copper interconnect) is deposited on a layer 104 on a substrate 102 that can include other structures 112 (as shown in FIG. 1). An implant mask 202 is added and used to add species 214 to the current carrying liner 106 within the layer 104 (as shown in FIG. 2). The implant mask 202 is removed from the layer 104, leaving the species 214 within the current carrying liner 106 (as shown in FIG. 3). Electrodes 404 and 402 are used to provide current to the current carrying liner 106 to diffuse the species 214 (e.g., dopant), initiate chemical reactions and/or speed up chemical reactions to form a fuse element 414 (as shown in FIG. 4).

[0030] In some embodiments, the fuse array is used as an embedded heater to supply the local heat to the fuse array. While BE processing steps can use annealing operations (such as whole chip heating), these operations are mainly tailored for the yielding structures. The fuse array with local implants can customize the annealing temperature in order to enable the diffusion of the dopants and initiate the chemical reactions for copper oxidation and for hydrogen embrittlement.

[0031] In one embodiment, customized heating and subsequent cooling to a low temperature can initiate stress induced voiding (SIV). This can be enhanced when the fuse array has initial damage from Ar/Xe (or any other inert gas) bombardment or voids from the hydrogen embrittlement. Temperature cycle for maximizing SIV can be optimized with local heating elements.

[0032] FIG. 5 illustrates an interposer 500 that includes one or more embodiments of the invention. The interposer 500 is an intervening substrate used to bridge a first substrate 502 to a second substrate 504. The first substrate 502 may be, for instance, an integrated circuit die. The second substrate 504 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of the interposer 500 is to spread a connection to a wider pitch or to reroute a connection to a different connection.

For example, the interposer 500 may couple an integrated circuit die to a ball grid array (BGA) 506 that can subsequently be coupled to the second substrate 504. In some embodiments, the first and second substrates 502/504 are attached to opposing sides of the interposer 500. In other embodiments, the first and second substrates 502/504 are attached to the same side of the interposer 500. And in further embodiments, three or more substrates are interconnected by way of the interposer 500.

[0033] The interposer 500 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer 500 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0034] The interposer 500 may include metal interconnects 508 and vias 510, including but not limited to through-silicon vias (TSVs) 512. The interposer 500 may further include embedded devices 514, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 500.

[0035] In accordance with embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of the interposer 500.

[0036] FIG. 6 illustrates a computing device 600 in accordance with one embodiment of the invention. The computing device 600 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die, such as an SoC used for mobile devices. The components in the computing device 600 include, but are not limited to, an integrated circuit die 602 and at least one communications logic unit 608. In some implementations the communications logic unit 608 is fabricated within the integrated circuit die 602, while in other implementations the communications logic unit 608 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 602. The integrated circuit die 602 may include a CPU 604 as well as on-die memory 606, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM), SRAM, or spin-transfer torque memory (STT-MRAM).

[0037] The computing device 600 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components may include, but are not limited to, volatile memory 610 (e.g., DRAM), non-volatile memory 612 (e.g., ROM or flash memory), a graphics processing unit (GPU) 614, a digital signal processor (DSP) 616, a crypto processor 642 (e.g., a specialized processor that executes cryptographic algorithms within hardware), a chipset 620, at least one antenna 622 (in some implementations two or more antennas may be used), a display or a touchscreen display 624, a touchscreen controller 626, a battery 629 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 628, a compass (not shown), a motion coprocessor or sensors 632 (that may include an accelerometer, a gyroscope, and a compass), a microphone (not shown), a speaker 634, a camera 636, user input devices 638 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 640 (such as a hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). The computing device 600 may incorporate further transmission, telecommunication, or radio functionality not already described herein. In some implementations, the computing device 600 includes a radio that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space. In further implementations, the computing device 600 includes a transmitter and a receiver (or a transceiver) that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space.

[0038] The communications logic unit 608 enables wireless communications for the transfer of data to and from the computing device 600. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 608 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Infrared (IR), Near Field Communication (NFC), Bluetooth, and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 600 may include a plurality of communications logic units 608. For instance, a first communications logic unit 608 may be dedicated to shorter range wireless communications such as Wi-Fi, NFC, and Bluetooth, and

a second communications logic unit 608 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0039] The processor 604 of the computing device 600 includes one or more devices, such as transistors or metal interconnects, that are formed in accordance with embodiments of the invention to form fuse arrays. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0040] The communications logic unit 608 may also include one or more devices, such as transistors or metal interconnects, that are formed in accordance with embodiments of the invention to form fuse arrays.

[0041] In further embodiments, another component housed within the computing device 600 may contain one or more devices, such as transistors or metal interconnects, that are formed in accordance with implementations of the invention to form fuse arrays.

[0042] FIG. 7 is a flow chart illustrating an implant and annealing method 700. The method 700 can be accomplished using structures as seen in FIGS. 1-4, among others. In block 702, an integrated chip (IC) construction system deposits a metal layer in an integrated chip to form a fuse element. In block 704, the IC construction system implants a portion of the metal layer including the fuse element with a dopant using an implant mask. In block 706, the IC construction system provides a current to the fuse element to activate the dopant, perform a localized anneal and increase resistance of the fuse element.

Examples

[0043] The following examples pertain to further embodiments.

[0044] Example 1 is a fuse element of an integrated chip (IC). The fuse element of an IC includes a metal body placed within a layer of the IC, one or more dopants implanted within the fuse element, and one or more voids within the metal body. The dopants diffuse and promote voids within the metal body when annealed.

[0045] Example 2 is the subject matter of Example 1 or any of the Examples described herein where one or more dopants are an inert species that causes crystalline defects for void nucleation.

[0046] Example 3 is the subject matter of Example 2 or any of the Examples described herein where the inert species is Argon or Xenon.

[0047] Example 4 is the subject matter of Example 1 or any of the Examples described herein where one or more dopants are a species that causes a resistive film.

[0048] Example 5 is the subject matter of Example 4 or any of the Examples described herein where the resistive film shrinks while curing, promoting stress induced voids.

[0049] Example 6 is the subject matter of Example 4 or any of the Examples described herein where the resistive film structurally weakens an interface between a liner and the metal body.

[0050] Example 7 is the subject matter of Example 4 or any of the Examples described herein where the species is oxygen.

[0051] Example 8 is the subject matter of Example 1 or any of the Examples described herein where the one or more dopants include a first species that causes at least a portion of the metal body to form a metal oxide, and a second species that causes embrittlement of the metal body by reacting with the metal oxide.

[0052] Example 9 is the subject matter of Example 8 or any of the Examples described herein where the first species is oxygen and the second species is hydrogen.

[0053] Example 10 is the subject matter of Example 1 or any of the Examples described herein where the one or more dopants include a first species that causes at least a portion of the metal body to form a metal oxide, a second species that causes embrittlement of the metal body by reacting with the metal oxide, and a third species that causes crystalline defects.

[0054] Example 11 is the subject matter of Example 10 or any of the Examples described herein where the first species is Oxygen, the second species is Hydrogen, and the third species is Argon or Xenon.

[0055] Example 12 is the subject matter of Example 1 or any of the Examples described herein where the one or more dopants are a species that causes embrittlement of the metal body.

[0056] Example 13 is the subject matter of Example 12 or any of the Examples described herein where the species is hydrogen.

[0057] Example 14 is the subject matter of any of Examples 1-13 or any of the Examples described herein may further include an electrode attached to the metal body and designed to provide power to the metal body for use with annealing.

[0058] Example 15 is the subject matter of any of Examples 1-13 or any of the Examples described herein where the IC is a processor.

[0059] Example 16 is the subject matter of any of Examples 1-13 or any of the Examples described herein where the IC includes a memory unit.

[0060] Example 17 is the subject matter of any of Examples 1-13 or any of the Examples described herein where the IC includes a graphics processing unit.

[0061] Example 18 is a method which includes depositing a metal layer in an integrated chip to form a fuse element, implanting a portion of the metal layer including the fuse element with a dopant using an implant mask, and providing a current to the fuse element to activate the dopant, perform a localized anneal, and increase resistance of the fuse element.

[0062] Example 19 is the subject matter of Example 18 or any of the Examples described herein where providing the current to the fuse element further includes causing diffusion of the dopant in the metal layer.

[0063] Example 20 is the subject matter of Example 18 or any of the Examples described herein where providing the current to the fuse element further includes causing voids to form in the fuse element.

[0064] Example 21 is the subject matter of Example 20 or any of the Examples described herein where the voids increase resistance of the fuse element.

[0065] Example 22 is the subject matter of Example 18 or any of the Examples described herein where the dopant is Argon, Xenon, Oxygen or Hydrogen.

[0066] Example 23 is the subject matter of Example 18 or any of the Examples described herein where the dopant is Hydrogen, and where providing the current to the fuse element further includes causing hydrogen embrittlement by reacting Hydrogen with a metal oxide of the fuse element.

[0067] Example 24 is the subject matter of Example 18 or any of the Examples described herein where the dopant is Hydrogen and Oxygen, and where providing the current to the fuse element further includes causing oxidation of metal to form metal oxide within the fuse element, and causing hydrogen embrittlement by reacting Hydrogen with the metal oxide of the fuse element.

[0068] Example 25 is the subject matter of Example 18 or any of the Examples described herein where the dopant is Hydrogen, Oxygen, and Argon or Xenon, and where providing the current to the fuse element further includes causing crystalline defects for void nucleation, oxidation of metal to form metal oxide within the fuse element, and hydrogen embrittlement by reacting Hydrogen with the metal oxide of the fuse element.

[0069] Example 26 is an apparatus including a procedure to perform a method as identified in any of Examples 18-25.

[0070] Example 27 is a machine-readable storage including machine-readable instructions. When executed, the instructions employ a method or achieve an apparatus as identified in any of Examples 18-25.

[0071] Example 28 is a computing device. The computing device includes a processor mounted on a substrate, a memory unit capable of storing data, and a graphics processing unit. The computing device further includes an antenna within the computing device, a display, a battery, and a power amplifier and a voltage regulator within the processor. The processor further includes a metal body arranged within a layer of an integrated chip, one or more dopants implanted within the metal body, and one or more voids within the metal body where the dopants diffuse within the layer and promote voids within the metal body when annealed.

[0072] Example 29 is the subject matter of Example 28 or any of the Examples described herein where one or more dopants are Argon, Xenon, Oxygen or Hydrogen.

[0073] Example 30 is the subject matter of Example 28 or any of the Examples described herein where the processor further includes an electrode designed to provide power to the metal body and cause annealing.

[0074] Example 31 is an apparatus for etching which includes means for depositing a metal layer in an integrated chip to form a fuse element, means for implanting a portion of the metal layer including the fuse element with a dopant using an implant mask, and means for providing a current to the fuse element to activate the dopant, perform a localized anneal, and increase resistance of the fuse element.

[0075] Example 32 is machine-readable storage including machine-readable instructions. When executed, the instructions employ a method which includes depositing a metal layer in an integrated chip to form a fuse element, implanting a portion of the metal layer including the fuse element with a dopant using an implant mask, and providing a current to the fuse element to activate the dopant, perform a localized anneal, and increase resistance of the fuse element.

[0076] Reference throughout this specification to “an example” means that a particular feature, structure, or characteristic described in connection with the example is included in at least one embodiment of the present invention. Thus, appearances of the phrase “in an example” in various places throughout this specification are not necessarily all referring to the same embodiment.

[0077] As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on its presentation in a

common group without indications to the contrary. In addition, various embodiments and examples of the present invention may be referred to herein along with alternatives for the various components thereof. It is understood that such embodiments, examples, and alternatives are not to be construed as de facto equivalents of one another, but are to be considered as separate and autonomous representations of the present invention.

[0078] Furthermore, the described features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. In the description above, numerous specific details are provided, such as examples of materials, frequencies, sizes, lengths, widths, shapes, etc., to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention may be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

[0079] It should be recognized that the systems described herein include descriptions of specific embodiments. These embodiments can be combined into single systems, partially combined into other systems, split into multiple systems, or divided or combined in other ways. In addition, it is contemplated that parameters/attributes/aspects/etc. of one embodiment can be used in another embodiment. The parameters/attributes/aspects/etc. are merely described in one or more embodiments for clarity, and it is recognized that the parameters/attributes/aspects/etc. can be combined with or substituted for parameters/attributes/etc. of another embodiment unless specifically disclaimed herein.

[0080] Although the foregoing has been described in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatuses described herein. Accordingly, the present embodiments are to be considered illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

[0081] Those having skill in the art will appreciate that many changes may be made to the details of the above-described embodiments without departing from the underlying principles of the invention. The scope of the present invention should, therefore, be determined only by the following claims.

Claims:

1. A fuse element of an integrated chip (IC), comprising:
a metal body disposed within a layer of the IC;
one or more dopants implanted within the fuse element; and
one or more voids within the metal body,
wherein the dopants diffuse and promote voids within the metal body when annealed.
2. The fuse element of claim 1, wherein the one or more dopants are an inert species that causes crystalline defects for void nucleation.
3. The fuse element of claim 1, wherein the one or more dopants are a species that causes a resistive film.
4. The fuse element of claim 3, wherein the resistive film shrinks while curing, promoting stress induced voids.
5. The fuse element of claim 3, wherein the resistive film structurally weakens an interface between a liner and the metal body.
6. The fuse element of claim 1, wherein the one or more dopants comprise:
a first species that causes at least a portion of the metal body to form a metal oxide;
and
a second species that causes embrittlement of the metal body by reacting with the metal oxide.
7. The fuse element of claim 6, wherein the first species is oxygen and the second species is hydrogen.
8. The fuse element of claim 1, wherein the one or more dopants comprise:
a first species that causes at least a portion of the metal body to form a metal oxide;
a second species that causes embrittlement of the metal body by reacting with the metal oxide; and
a third species that causes crystalline defects.
9. The fuse element of claim 1, wherein the one or more dopants are a species that causes embrittlement of the metal body.
10. The fuse element of any of claims 1-9, further comprising an electrode coupled to the metal body and configured to provide power to the metal body for use with annealing.
11. The fuse element of any of claims 1-9, wherein the IC is a processor.
12. The fuse element of any of claims 1-9, wherein the IC comprises a memory unit.
13. A method comprising:
depositing a metal layer in an integrated chip to form a fuse element;

implanting a portion of the metal layer including the fuse element with a dopant using an implant mask; and

providing a current to the fuse element to activate the dopant, perform a localized anneal and increase resistance of the fuse element.

14. The method of claim 13, wherein providing the current to the fuse element further comprises causing diffusion of the dopant in the metal layer.

15. The method of claim 13, wherein providing the current to the fuse element further comprises causing voids to form in the fuse element.

16. The method of claim 15, wherein the voids increase resistance of the fuse element.

17. The method of claim 13, wherein the dopant is Argon, Xenon, Oxygen or Hydrogen.

18. The method of claim 13, wherein the dopant is Hydrogen, and wherein providing the current to the fuse element further comprises causing hydrogen embrittlement by reacting Hydrogen with a metal oxide of the fuse element.

19. The method of claim 13, wherein the dopant is Hydrogen and Oxygen, and wherein providing the current to the fuse element further comprises:

causing oxidation of metal to form metal oxide within the fuse element; and

causing hydrogen embrittlement by reacting Hydrogen with the metal oxide of the fuse element.

20. The method of claim 13, wherein the dopant is Hydrogen, Oxygen, and Argon or Xenon, wherein providing the current to the fuse element further comprises:

causing crystalline defects for void nucleation;

causing oxidation of metal to form metal oxide within the fuse element; and

causing hydrogen embrittlement by reacting Hydrogen with the metal oxide of the fuse element.

21. An apparatus comprising means to perform a method as claimed in any of claims 13-20.

22. Machine-readable storage including machine-readable instructions to, when executed, implement a method or realize an apparatus as claimed in any of claims 13-20.

23. A computing device comprising:

a processor mounted on a substrate;

a memory unit capable of storing data;

a graphics processing unit;

an antenna within the computing device;
a display on the computing device;
a battery within the computing device;
a power amplifier within the processor; and
a voltage regulator within the processor,
wherein the processor comprises:

a metal body disposed within a layer of an integrated chip;
one or more dopants implanted within the metal body; and
one or more voids within the metal body,

wherein the dopants diffuse within the layer and promote voids within the metal body when annealed.

24. The computing device of claim 23, wherein the one or more dopants are Argon, Xenon, Oxygen or Hydrogen.

25. The computing device of claim 23, wherein the processor further comprises an electrode configured to provide power to the metal body and cause annealing.

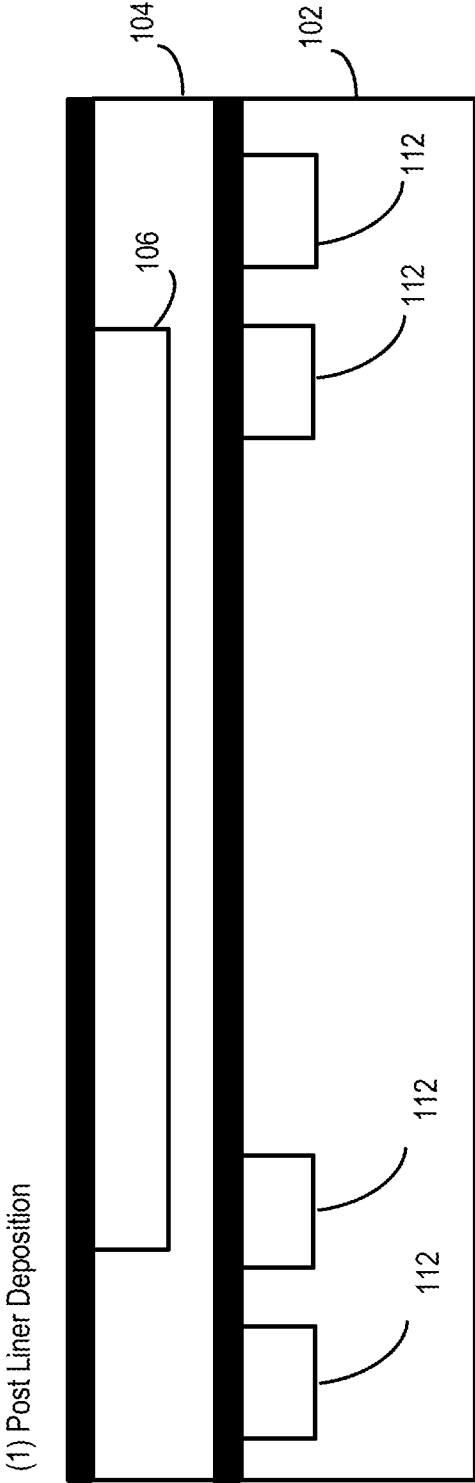


FIG. 1

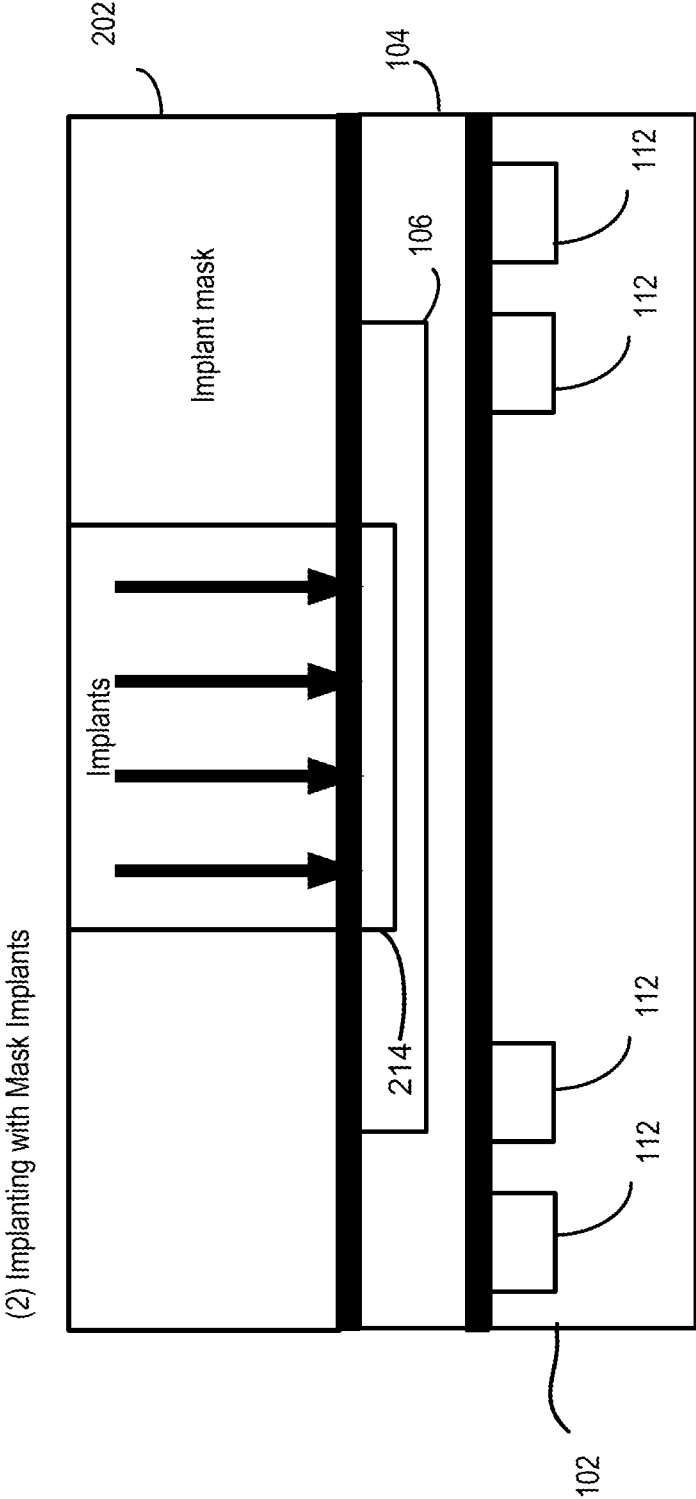


FIG. 2

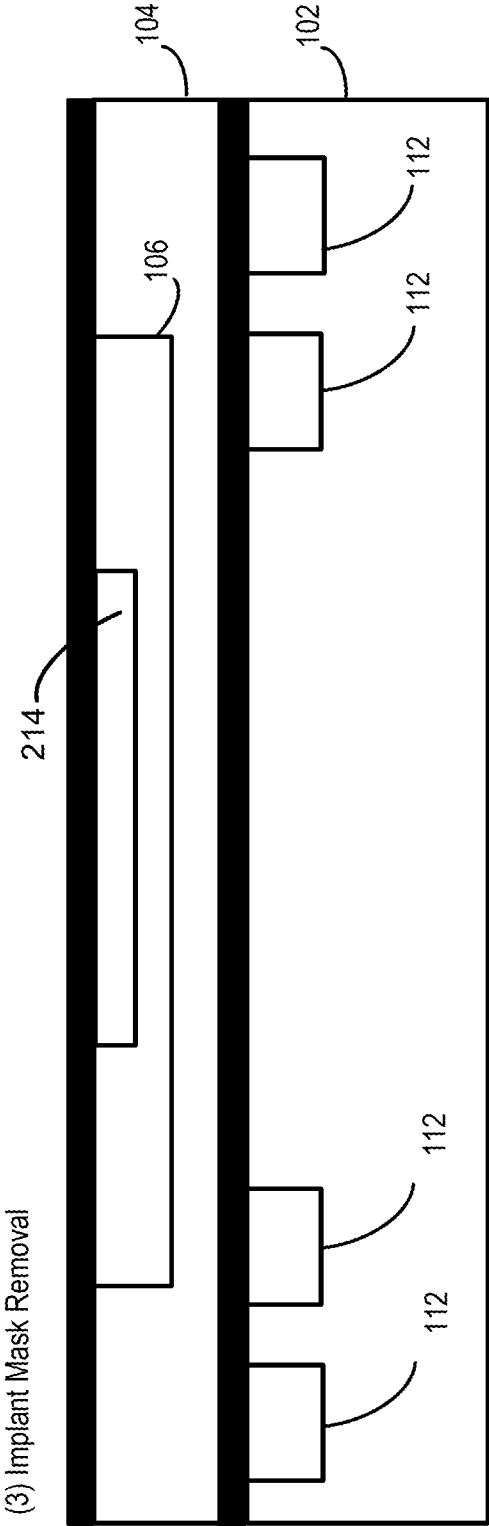


FIG. 3

(4) Local Anneal by Supplying Current to the Fuse Elements to Activate the Implants

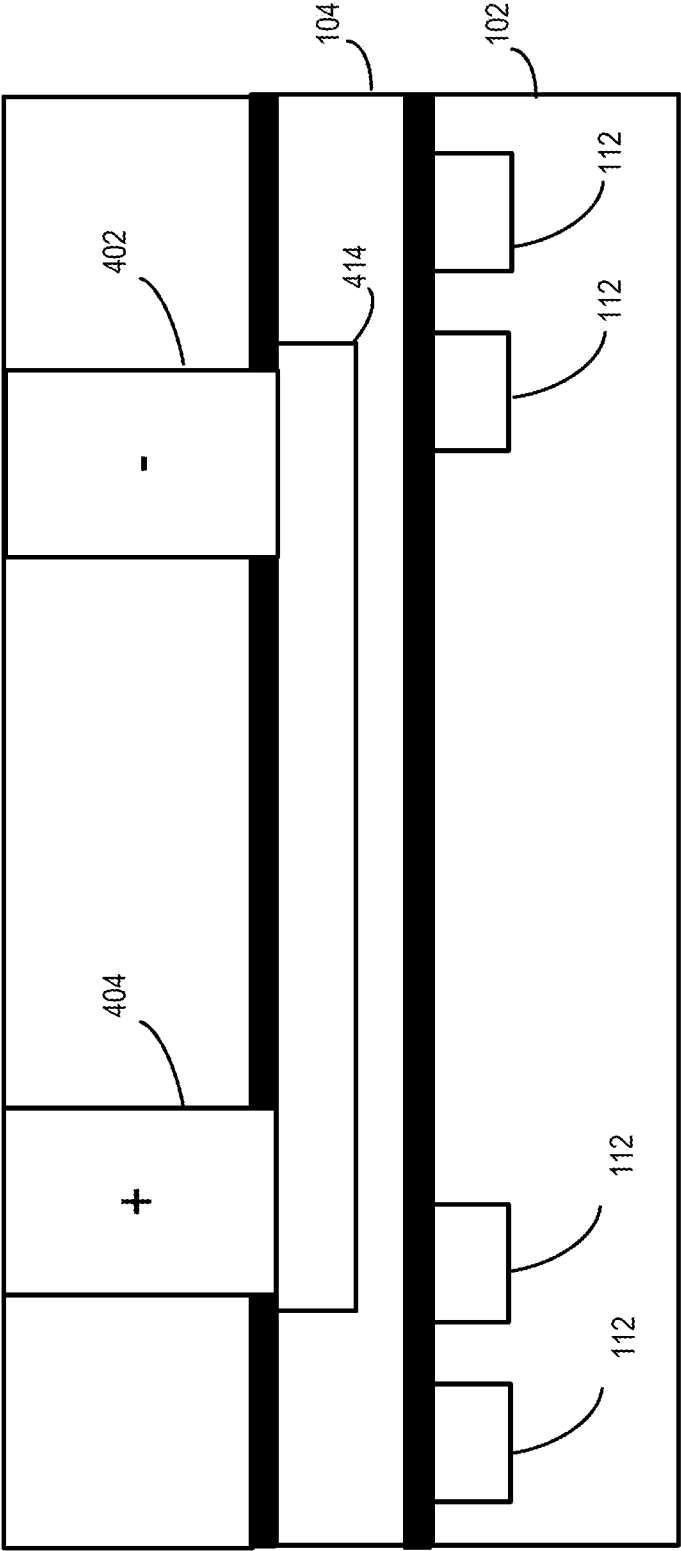


FIG. 4

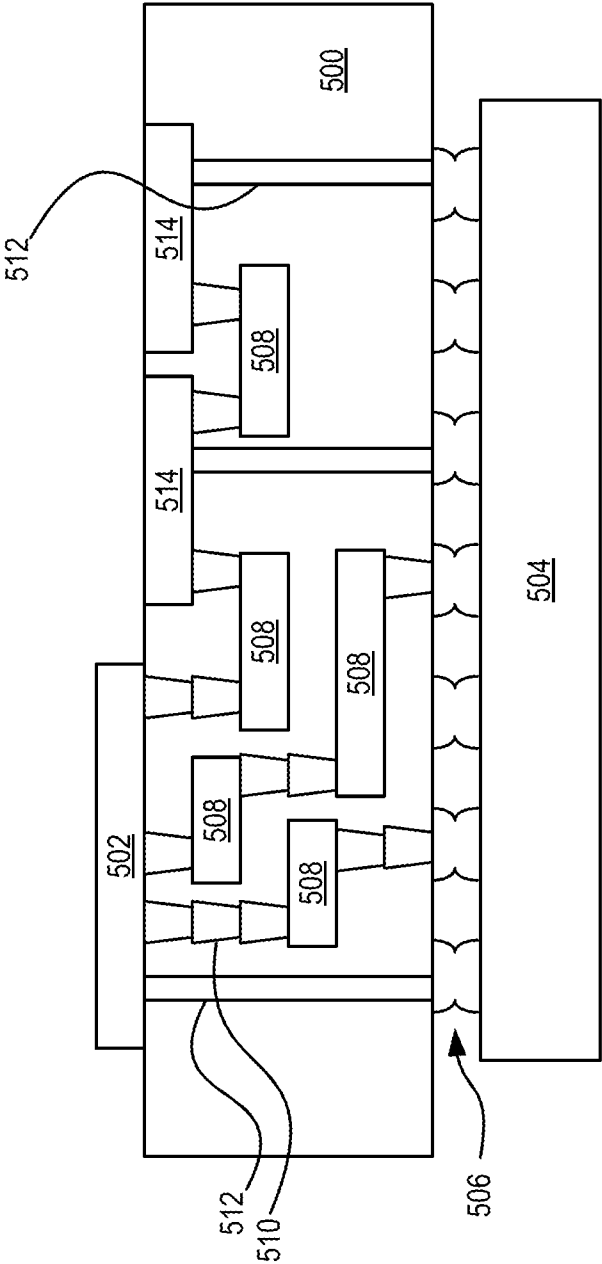


FIG. 5

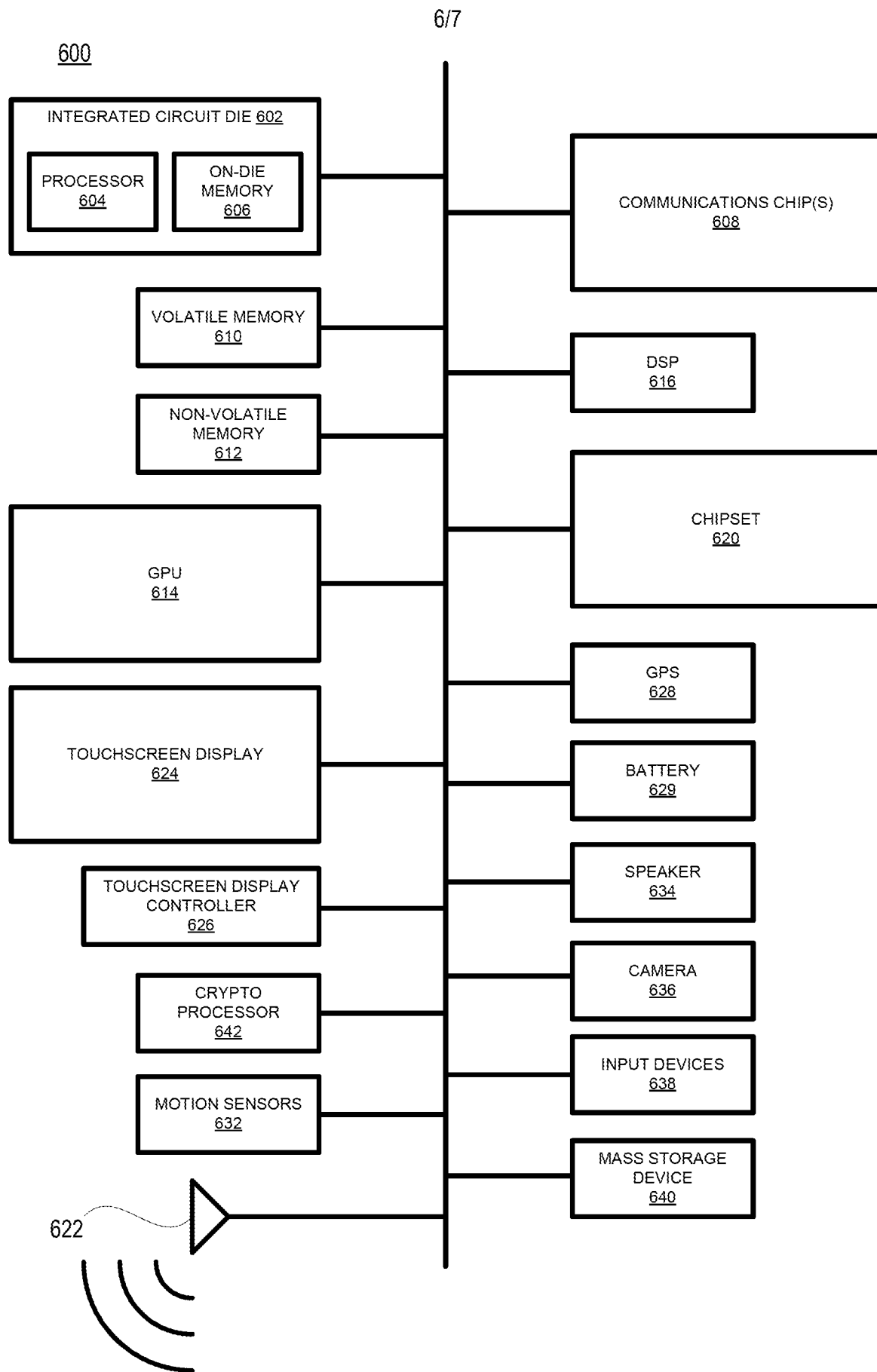


FIG. 6

7/7

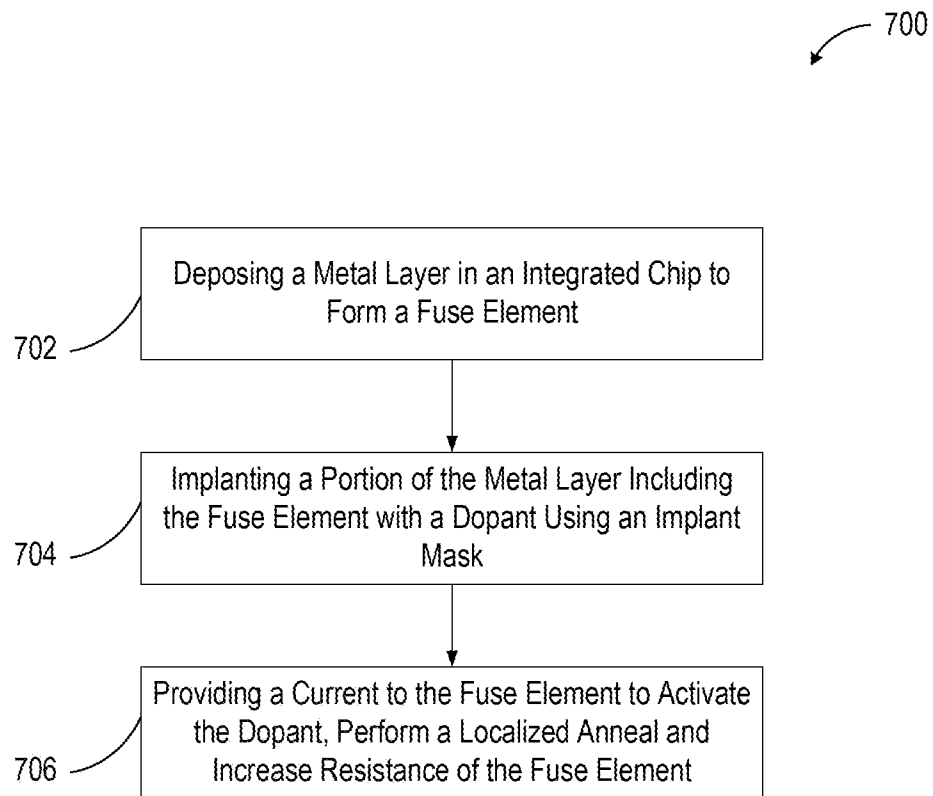


FIG. 7

A. CLASSIFICATION OF SUBJECT MATTER**H01L 23/525(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/525; H01L 29/00; H01L 21/02; H01L 21/822; H01L 21/82

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: fuse, easy, break, implant, anneal, void

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0273002 A1 (MIN-WK HWANG) 29 November 2007 See paragraphs [0024]-[0062] and figures 3A-4, 17.	1-25
Y	US 2011-0291230 A1 (MIN GU KO) 01 December 2011 See paragraphs [0029]-[0052], claim 1 and figures 2b-2c.	1-25
A	US 2007-0007621 A1 (MASAYOSHI OMURA et al.) 11 January 2007 See paragraphs [0162]-[0167] and figure 7.	1-25
A	US 2013-0234284 A1 (GRISELDA BONILLA et al.) 12 September 2013 See paragraphs [0040]-[0072] and figures 2A-4D.	1-25
A	JP 2010-267803 A (TOSHIBA CORP.) 25 November 2010 See paragraphs [0017]-[0019] and figure 1.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 March 2017 (28.03.2017)

Date of mailing of the international search report

28 March 2017 (28.03.2017)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040063

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