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(54) DISPLAY DEVICE

ANZEIGEVORRICHTUNG

DISPOSITIF D'AFFICHAGE

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(73) Proprietor: **Xianyang Caihong Optoelectronics Technology Co., Ltd**
Xianyang, Shaanxi 712000 (CN)

(72) Inventors:
- **WU, Yuan-liang**
  Xianyang, Shaanxi 712000 (CN)
- **CHEN, Yuyeh**
  Xianyang, Shaanxi 712000 (CN)
- **SUN, Lei**
  Xianyang, Shaanxi 712000 (CN)
- **LIU, Zihan**
  Xianyang, Shaanxi 712000 (CN)
- **SHI, Jun**
  Xianyang, Shaanxi 712000 (CN)

(74) Representative: **Herrero & Asociados, S.L.**
Edificio Aqua - Agustín de Foxá, 4-10
28036 Madrid (ES)

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Description

TECHNICAL FIELD

[0001] The invention relates to the field of display technologies, in particular to a display device. The invention is set out in the appended set of claims.

BACKGROUND

[0002] A conventional display device mainly includes a system-on-chip (SOC) disposed on a system board (also referred to as mainboard or motherboard), a timing controller (TCON) board, a horizontal direction circuit board (X-board, XB), a source driving circuit and a gate driving circuit. The SOC receives and outputs an image data signal to be transmitted, subsequently processes an input signal through a row expansion module and a column expansion module to obtain a processed data, and transmits the processed data to the TCON board, the TCON board transmits the processed data (also referred to as received data) to the source driving circuit and the gate driving circuit through the X-board, so as to drive a thin film transistor liquid crystal display for display.

[0003] At present, a flexible flat cable (FFC) is usually used to connect the system board and the horizontal direction circuit board for signal transmission between them. However, since the functions of TCON IC is integrated in the SOC on the system board, cooperation of the SOC is required when debugging and changing a panel. Since the operation of TCON needs to depend on the SOC, the TCON cannot be developed independently.

[0004] WO 2015/100786 A1 discloses a driving circuit of a liquid crystal panel, including a source driving board electrically connected directly to an array substrate of the liquid crystal panel. The driving circuit also includes a time-sequence control module, a voltage conversion module, and a gamma module. The time-sequence control module, the voltage conversion module and the gamma module are integrated on the source driving board.

[0005] CN 107241562 A discloses a circuit system of an ultra-high definition liquid crystal television. The circuit system includes a TCON driving module and a universal core panel, where the TCON driving module integrates a TCON driving portion, an upper screen interface and a U-P interface; and the universal core panel includes a master control SOC chip of the core, and integrates the U-P interface and a corresponding interface peripheral circuit. The U-P interface is used for connecting the universal core panel and the TCON driving module.

[0006] US 2009/0284455 A1 discloses a liquid crystal display in which a system board and a timing control board can be used in common in a 60 Hz driving mode and a 120 Hz driving mode without being modified. The liquid crystal display includes a system board for identifying a driving frequency of video data and supplying the video data and control signals at a first driving frequency or second driving frequency as a result of the identification, a timing control board equipped with a timing controller for processing the video data and control signals from the system board, the timing control board supplying the processed video data and control signals at the first or second driving frequency, and a liquid crystal panel for displaying an image based on the video data and control signals supplied from the timing control board.

[0007] CN 107396022 A discloses a data transmission device and a liquid crystal display device. The data transmission device is used for transmitting signals for a liquid crystal display panel in the liquid crystal display device, the data transmission device includes a video processing board and a time series control board, the video processing board converts original configuration data into first configuration data according to a preset protocol, converts original video data into first video data according to a preset protocol and outputs the first configuration data and the first video data, the time series control board converts the first configuration data into the original configuration data according to the preset protocol, converts the first video data into the original video data according to the preset protocol, outputs the original configuration data after power-on and outputs a first signal when the original configuration data is not output, and the first signal is used for enabling the liquid crystal display panel to display black pictures, where the original configuration data is used for configuring data when the liquid crystal display panel displays normally.

SUMMARY

[0008] In order to solve the above problems existing in the prior art, the invention provides a display device. The invention is set out in the appended set of claims.

[0009] Compared with the prior art, the above embodiments have one or more of the following advantages or beneficial effects:

[0010] 1. The display device of the embodiment disposes the driving circuit board assembly on the X-board, so that the X-board has some of TCON functions. When debugging and changing Panel Timing, it does not depend on the SOC and can be developed independently. Through the architecture adjustment of the embodiment, the system board (also referred to as mainboard, shorted as MB) and the horizontal direction circuit board (XB) can be manufactured and sold separately, the panel manufacturer can debug and change the panel independently without relying on changing the SOC.

[0011] 2. The display device of the embodiment adds the signal conversion circuit (for example, in the form of a chip) in the display control circuit of the driving circuit board assembly. On the one hand, it converts the P2P interface signal into the mini-LVDS interface signal, so that the interface between a COF type source driver of the source driving circuit and the driving circuit board assembly is changed into the mini-LVDS interface, which greatly reduces the cost; on the other hand, the signal conver-

sion circuit can generate the timing control signals required by the display panel, the debugging and revision of the panel can be completed by the panel manufacturer, and the whole machine manufacturer can reduce the development cost without any change; on the other hand, new panel technology can be completed by the signal conversion circuit, and the system board does not need any change.

[0012] 3. The display device of the embodiment stores the optical performance adjustment parameters in the nonvolatile memory of the X-board in the form of the parameter table, and debugging of each parameter in the optical performance adjustment parameter table is changed from the whole machine manufacturer to the panel manufacturer; because the optical performance adjustment parameters are strongly related to the panel, the optical performance adjustment parameter tables required for different panels are different, and the panel manufacturers know more about the optical characteristics of their own panels. Therefore, they can flexibly adjust the panel optical characteristics according to their own panel characteristics, which can liberate the whole machine manufacturers from the tedious work of adjusting optical characteristics, so as to accelerate the development speed of the whole machine.

[0013] The invention will be further described in detail below in combination with the accompanying drawings and embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

FIG. 1 is a schematic structural view of a display device according to an embodiment of the invention.
FIG. 2 is a schematic structural view of the display control circuit of the display device shown in FIG. 1.
FIG. 3 is another schematic structural view of the display control circuit of the display device shown in FIG. 1.
FIG. 4 is a schematic view of internal modules of the system-on-chip (SOC) and the nonvolatile memory disposed on the X-board in the display device shown in FIG. 1.
FIG. 5 is a schematic view of specific configurations of the optical performance adjustment parameter table and the optical performance adjustment IP core shown in FIG. 4.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0015] The invention is described in further detail below in combination with exemplary embodiments.

[0016] As shown in FIG.1, a display device 10 provided by an embodiment of the invention includes: a display panel 111, a X-board 113, a system board 13 and a connecting part (also referred to as connecting member) CL1. The display panel 111 is disposed with a gate driving circuit and a source driving circuit. The X-board 113 is disposed with a driving circuit board assembly 1130. The display device 10 is an active-matrix display device in the illustrated embodiment, for example, a TCONLESS liquid crystal television (LCD TV). A system-on-chip (SOC) disposed on the system board 13 integrates at least part of functions of traditional TCON chip, and the X-board integrates at least another part of the functions of the traditional TCON chip, but the embodiment of the invention is not limited to this.

[0017] The display panel 111 includes a display area 1111, a gate driving circuit electrically connected to the display area 1111 and a source driving circuit electrically connected to the display area 1111. The display area 1111 is disposed with a plurality of data lines DL, a plurality of gate lines GL and a plurality of pixels P respectively electrically connected to corresponding one of plurality of data lines DL and corresponding one of the plurality of gate lines GL. Each of the plurality of pixels P is located at the intersection of the corresponding gate line GL and the corresponding data line DL. The gate driving circuit includes, for example, two GOA (gate on array, gate driving circuit integrated on the array substrate) circuits 1113, which are located on the peripheral area of the display area 1111 and are divided on opposite sides of the display area 1111, that is, the gate driving circuit of the display panel 111 is a bilateral GOA circuit. The GOA circuit 1113 is electrically connected to the gate lines GL in the display area 1111 to provide gate driving signals to each of the plurality of gate lines GL in the display area 1111. The source driving circuit includes, for example, a plurality of chip-on-flex (COF) type source drivers 1115, such as twelve COF type source drivers 1115 shown in FIG. 1. The COF type source driver 1115 is electrically connected to the corresponding data line DL in the display area 1111 and configured to provide an image data signal to each of the plurality of data lines DL. More specifically, one of the plurality of COF type source drivers 1115 includes, for example, a flexible circuit board and a source driver IC disposed on the flexible circuit board.

[0018] The X-board 113 can be a whole independent circuit board or a plurality of circuit sub-boards juxtaposed with each other. If it is the plurality of circuit sub-boards juxtaposed with each other, the driving circuit board assembly 1130 can be disposed on one of the plurality of circuit sub-boards, and adjacent two circuit sub-boards of the plurality of circuit sub-boards form an electrical connection through another connecting part connected between connectors respectively disposed on the adjacent two circuit sub-boards.

[0019] The embodiment is described with two circuit sub-boards. The X-board 113 includes two circuit sub-boards 113a and 113b, which are arranged on one side of the display panel 111 along the horizontal direction of FIG. 1, that is, as a driving circuit board in the row direction; one side of each of the circuit sub-boards 113a and 113b adjacent to the display area 1111 is provided with a connection interface of the COF type

source driver 1115, such as a mini-LVDS interface. As described above, the driving circuit board assembly 1130 is disposed on the circuit sub-board 113a, specifically, the circuit sub-board 113a is provided with a display control circuit 1131, a connector CN1, a nonvolatile memory 1133 and a connector CN3. The circuit sub-board 113a is electrically connected to the display area 1111 through a plurality of COF type source drivers 1115, for example, seven COF type source drivers 1115, and electrically connected to the GOA circuit 1113 on the right side of the display panel 111 using the rightmost COF type source driver 1115. The circuit sub-board 113b is provided with a connector CN4. The circuit sub-board 113b is electrically connected to the display area 1111 through a plurality of COF type source drivers 1115, for example, five COF type source drivers 1115, and electrically connected to the GOA circuit 1113 on the left side of the display panel 111 using the leftmost COF type source driver 1115. An electrical connection is formed between the connector CN3 of the circuit sub-board 113a and the connector CN4 of the circuit sub-board 113b through the connecting part CL2, the connecting part CL2 is, for example, a flexible circuit board or flexible flat cable (FFC), so that the signal generated from the circuit sub-board 113a is transmitted to the circuit sub-board 113b through the connecting part CL2.

[0020] Further, the display control circuit 1131 is electrically connected to the first connector CN1, the connector CN3 and a plurality of COF type source drivers 1115, for example, seven COF type source drivers 1115. In this way, the display control circuit 1131 is not only electrically connected to the seven COF type source drivers 1115 on the right through a printed circuit board (PCB) of the circuit sub-board 113a, but also connected to the five COF type source drivers 1115 on the left through the connector CN3, the connecting part CL2, the connector CN4 and the PCB of the circuit sub-board 113b. The X-board 113 is also provided with a plurality of mini low voltage differential signaling (Mini-LVDS) interfaces, which are arranged between the COF type source drivers 1115 and the display control circuit 1131, and the first connector includes a point-to-point (P2P) interface. Referring to FIG. 2, the display control circuit 1131 includes a signal conversion circuit 11312, which is electrically connected with the first connector CN1 and the Mini-LVDS interface, and is configured to receive a P2P interface signal containing image data through the first connector, generate source control signals and second interface type image data signals according to the P2P interface signal, and output the source control signals and the second interface type image data signals to the source driving circuit through the plurality of Mini-LVDS interfaces; the second interface type image data signals are Mini-LVDS interface signals.

[0021] It should be noted that in the prior art, in order to match the signal sent by the SOC, the interface of the source driver needs to be adjusted accordingly. For example, if the signal sent by the SOC is transmitted through the P2P interface, the corresponding source driver interface can only use the P2P interface, resulting in an increase in the overall manufacturing cost and test cost. In this embodiment, if the connector CL1 transmits the signal from the SOC to the signal conversion circuit 11312 of the display control circuit 1131 through the P2P interface, the signal conversion circuit 11312 can convert the P2P interface signal into an interface signal corresponding to the panel source driver. For example, the interface of the COF type source driver 1115 is the Mini-LVDS interface, the P2P interface signal is correspondingly converted into the Mini-LVDS signal by the signal conversion circuit, and the Mini-LVDS signal is sent to the interface of the COF type source driver 1115 of the panel, that is, the conversion of the interface signal is completed through the signal conversion circuit 11312, so as to complete the data transmission without changing the original Mini-LVDS interface on the panel, by adding the signal conversion circuit (for example, in the form of a chip) in the display control circuit of the driving circuit board assembly. On the one hand, it converts the P2P interface signal into the mini-LVDS interface signal, so that the interface between the COF type source driver 1115 of the source driving circuit and the interface of the X-board is changed into the Mini-LVDS interface, which greatly reduces the cost; on the other hand, the signal conversion circuit 11312 can generate the timing control signals required by the display panel, the debugging and revision of the panel can be completed by the panel manufacturer, and the whole machine manufacturer can reduce the development cost without any change; on the other hand, new panel technology can be completed by the signal conversion circuit 11312, and the system board 13 does not need any change.

[0022] On the other hand, the display control circuit 1131 further includes a direct-current (DC) voltage conversion circuit 11314, a level conversion circuit 11316 and a Gamma correction circuit 11318. The signal conversion circuit 11312 is electrically connected to the connector CN1, the level conversion circuit 11316 and the source driving circuit, and configured to receive reference timing signals such as STV and CKV and a P2P interface signal containing image data (the image data such as RGB data) through the first connector, generate source control signals such as TP and POL and second interface type image data signals such as Mini-LVDS according to the P2P interface signal, and output them to the source driving circuit, and generate initial gate control signals such as ST_in, CKx_in, LC_in and Reset_in according to the reference timing signals such as STV and CKV to the level conversion circuit 11316. The DC voltage conversion circuit 11314 is electrically connected to the connector CN1 and configured to receive an input DC voltage such as Vin, and generate gate switching voltages such as VGH and VGL and a reference voltage such as VAA according to the input DC voltage such as Vin, and output the gate switching voltages and the reference voltage to the level conversion circuit 11316 and the Gamma cor-

rection circuit 11318 respectively. The level conversion circuit 11316 is configured to generate gate control signals such as ST, CKx, LCx and Reset according to the gate switching voltages such as VGH and VGL and the initial gate control signal such as ST_in, CKx_in, LC_in, Reset_in to the gate driving circuit. The Gamma correction circuit 11318 is configured to generate a plurality of Gamma voltages such as GMAx according to the reference voltage such as VAA to the source driving circuit. In an illustrated example, CKx_in is, for example, four high-frequency clock signals CK1 ~ CK4, CKx is, for example, eight high-frequency clock signals CK1 ~ CK8, and LCx is two low-frequency clock signals LC1 ~ LC2 relative to CKx, GMAx is, for example, fourteen channel Gamma voltages such as GMA1 ~ GMA14, VGH is, for example, + 20V ~ + 30V as the gate on voltage, and VGL is, for example, about - 5V as the gate off voltage, but this invention is not limited thereto. In addition, it is worth noting that the P2P interface signal includes multiple pairs of differential signals, which is another interface type different from the Mini-LVDS interface, and is very suitable for short-distance signal transmission from the system board 13 to the circuit sub-board 113a, which can be known mature USI-T, EPI, CMPI and ISP interface, etc. In addition, it should be noted that the DC voltage conversion circuit 11314 is not limited to generating the above VGH, VGL and VAA, but is also used to provide power supply voltages such as digital voltage VDD and analog voltage HVAA (not shown in the figure) to the signal conversion circuit 11312, the level conversion circuit 11316, the Gamma correction circuit 11318, the gate driving circuit and the source driving circuit.

[0023] As described above, the signal conversion circuit 11312, the DC voltage conversion circuit 11314, the level conversion circuit 11316 and the Gamma correction circuit 11318 in the embodiment shown in FIG. 2 are integrated into four different chips, for example. For example, the DC voltage conversion circuit 11314 adopts a PMIC chip of known mature technology, the level conversion circuit 11316 adopts a level shift chip of known mature technology, and the Gamma correction circuit 11318 adopts a P-Gamma chip of known mature technology. In addition, in order to further improve the integration of the circuit, in other embodiments, the DC voltage conversion circuit 11314 and the level conversion circuit 11316 can be integrated on the same chip and the Gamma correction circuit 11318 can be integrated on another chip; or the DC voltage conversion circuit 11314 and the Gamma correction circuit 11318 can be integrated on the same chip and the level conversion circuit 11316 can be integrated on another chip; or the level conversion circuit 11316 and the Gamma correction circuit 11318 can be integrated on the same chip, and the DC voltage conversion circuit 11314 can be integrated on the same chip; or even the DC voltage conversion circuit 11314, the level conversion circuit 11316 and the Gamma correction circuit 11318 can be integrated on the same chip.

[0024] In the prior art, since the functions of TCON IC are integrated in the SOC on the system board, SOC cooperation is required when debugging and changing Panel Timing. However, some functions of TCON IC in the embodiment are set on the X-board. When debugging and changing Panel Timing, it does not depend on the SOC at all and can be developed independently. Through the architecture adjustment of this embodiment, the system board and the X-board can be manufactured and sold separately, and the panel manufacturer can complete the panel debugging and change independently without relying on the change of SOC.

[0025] When the display control circuit 1131 includes the Gamma correction circuit 11318, since the Gamma correction circuit 11318 is disposed on the X-board, the gamma curve can be adjusted piece by piece. In addition, a power management circuit 135 can also be disposed on the X-board, and the power management circuit 135 is connected to the display control circuit 1131, so that panel manufacturers can adjust and revise the power supply part by themselves during panel manufacturing.

[0026] Of course, the display control circuit 1131 cannot include one or more selected from the group consisting of the DC voltage conversion circuit 11314, the level conversion circuit 11316 and the Gamma correction circuit 11318. For example, when the Gamma correction circuit 11318 is not included, the DC voltage conversion circuit 11314, the level conversion circuit 11316 and the signal conversion circuit 11312 can be integrated into the same chip; alternatively, the DC voltage conversion circuit 11314 and the level conversion circuit 11316 can be integrated on the same chip, and the signal conversion circuit 11312 can be integrated on another chip; alternatively, the DC voltage conversion circuit 11314 and the signal conversion circuit 11312 can be integrated on the same chip, and the level conversion circuit 11316 can be integrated on another chip; alternatively, the level conversion circuit 11316 and the signal conversion circuit 11312 can be integrated on the same chip, and the DC voltage conversion circuit 11314 can be integrated on another chip; alternatively, the DC voltage conversion circuit 11314, the level conversion circuit 11316 and the signal conversion circuit 11312 can be integrated on the same chip.

[0027] As shown in FIG. 3, in another embodiment, the display control circuit 1131 includes a signal conversion circuit 11312, a DC voltage conversion circuit 11314, a level conversion circuit 11316 and a Gamma correction circuit 11318. The signal conversion circuit 11312 is electrically connected to the connector CN1 and the source driving circuit and configured to receive the P2P interface signal containing image data through the connector CN1, generate source control signals such as TP and POL and second interface type image data signals such as Mini-LVDS according to the P2P interface signal, and output them to the source driving circuit. The DC voltage conversion circuit 11314 is electrically connected to the connector CN1 and configured to receive an

input DC voltage such as Vin through the connector CN1, and generate gate switching voltages such as VGH and VGL and a reference voltage such as VAA according to the input DC voltage such as Vin, and output the gate switching voltages and the reference voltage to the level conversion circuit 11316 and the Gamma correction circuit 11318 respectively. The level conversion circuit 11316 is electrically connected to the connector CN1 and configured to receive the reference timing signals such as STV and CKV, generate gate control signals such as ST, CKx, LCx and Reset according to the reference timing signals such as STV and CKV and the gate switching voltages such as VGH and VGL to the gate driving circuit. The Gamma correction circuit 11318 is configured to generate a plurality of Gamma voltages such as GMAx according to the reference voltage such as VAA to the source driving circuit. In short, the main difference between the embodiment shown in FIG.3 and the embodiment shown in FIG. 2 is that the reference timing signals such as STV and CKV in the embodiment shown in FIG. 3 are directly sent to the level conversion circuit 11316, rather than initially converted through the signal conversion circuit 11312 and then sent to the level conversion circuit 11316 as shown in FIG. 2. Alternatively, in other embodiments, the reference timing signals such as STV and CKV can also be generated locally by the signal conversion circuit 11312 rather than directly provided by the system board 13.

[0028] In addition, the display control circuit 1131 can be further electrically connected (not shown in FIG. 1) to the nonvolatile memory 1133, for example, connected to the same serial bus as the nonvolatile memory, such as SPI (serial peripheral interface) bus; SPI bus has the advantage of fast data reading and writing speed.

[0029] In addition, the nonvolatile memory 1133 is electrically connected to the connector CN1. As shown in FIG. 4, the nonvolatile memory 1133 stores an optical performance adjustment parameter table 11330. Parameters contained in the optical performance adjustment parameter table 11330 are parameters strongly related to the optical performance (also referred to as optical characteristics) of the display panel 111. In this embodiment, the nonvolatile memory 1133 is a SPI interface flash, and accordingly, the connector CN1 includes SPI bus interface.

[0030] The system board 13 is provided with a connector CN2, a system-on-chip 133 and a power management circuit 135. The connector CN2 of the system board 13 is connected to the connector CN1 of the circuit sub-board 113a through the connecting part CL1. Further, the system-on-chip 133 is electrically connected to the connector CN2 and has an optical performance adjustment intellectual property (IP) core 1330 as shown in FIG. 4, so that the system-on-chip 133 read the optical performance adjustment parameter table 11330 stored in the nonvolatile memory of the circuit sub-board 113a by serial communication through the connector CN2, the connecting part CL1 and the connector CN1, and load it into the optical performance adjustment IP core 1330 to adjust the optical performance of the display panel 111. In addition, the connecting part CL1 is, for example, a single flexible cable (FFC). In addition, it is worth mentioning that the system board 13 of the embodiment is typically provided with a plurality of audio and video input interfaces, such as a CVBS interface, a HDMI interface, etc; The system board 13, also known as the mainboard, is used to decode video and audio signals input through the audio and video input interface, and then output the video signal to the X-board in digital signal format.

[0031] As shown in FIG.5, the optical performance adjustment IP core 1330 includes: a Demura IP core 1331, a white balance adjustment (also referred to as white tracking adjustment) IP core 1332, a color shift compensation IP core 1333, an OverDrive IP core 1334 and a dithering processing IP core 1335; correspondingly, the optical performance adjustment parameter table 11330 includes a Demura parameter table 11331, a white balance adjustment parameter table 11331, a color shift compensation parameter table 11333, an OverDrive parameter table 11334 and a dithering processing parameter table 11335. More specifically, the Demura IP core 1331 is configured for performing Mura (i.e., a phenomenon of various traces caused by uneven display brightness) elimination (also referred to as Demura) operation according to the Demura parameter table 11331. The white balance adjustment IP core 1332 is configured for performing white balance adjustment operation according to the white balance adjustment parameter table 11332. The color shift compensation IP core 1333 is configured for performing color shift compensation operation according to the color shift compensation parameter table 11333 to make the display panel 111 achieve low color shift display quality. The OverDrive IP core 1334 is configured for performing overvoltage driving (also referred to as OverDrive) operation according to the OverDrive parameter table 11334. The dithering processing IP core 1335 is configured for performing dithering processing operation such as temporal dithering and/or spatial dithering according to the dithering processing parameter table 11335. The parameters required for the Mura elimination operation, the white balance adjustment operation, the color shift compensation operation, the overvoltage driving operation and the dithering processing operation are known mature technologies, so they will not be repeated here. As for the power management circuit 135, it is electrically connected to the connector CN2 to provide the input DC voltage, such as 12V, to the circuit sub-board 113a; Further, the power management circuit 135 uses, for example, a mature PMIC (Power Management IC).

[0032] It is worth mentioning that according to the experimental verification of the applicant, the system-on-chip 133 is configured to sequentially control the Demura IP core 1331, the white balance adjustment IP core 1332, the color shift compensation IP core 1333, the OverDrive IP core 1334 and the dithering processing IP

core 1335 to perform Demura operation, white balance adjustment, color shift compensation operation, OverDrive operation and dithering processing operation according to the Mura elimination parameter table 11331, the white balance adjustment parameter table 11332, the color shift compensation parameter table 11333, the OverDrive parameter table 11334 and the dithering processing parameter table 11335 respectively. This specific optical performance adjustment sequence makes it easier for the display panel 111 to achieve better display quality and optical taste.

[0033] In addition, the optical performance adjustment IP core 1330 also includes one or more selected from the group consisting of the Demura IP core 1331, the white balance adjustment IP core 1332, the color shift compensation IP core 1333, the OverDrive IP core 1334 and the dithering processing IP core 1335; Similarly, the optical performance adjustment parameter table 11330 includes one or more selected from the group consisting of the Mura elimination parameter table 11331, the white balance adjustment parameter table 11332, the color shift compensation parameter table 11333, the OverDrive parameter table 11334 and the dithering processing parameter table 11335 respectively.

[0034] The optical performance adjustment parameters (also referred to as optical codes) of the embodiment stored in the nonvolatile memory 1133 of the circuit sub-board 113a in the form of the parameter table, and debugging of each parameter in the optical performance adjustment parameter table is changed from the whole machine manufacturer to the panel manufacturer; because the optical performance adjustment parameters are strongly related to the panel, the optical performance adjustment parameter tables required for different panels are different, and the panel manufacturers know more about the optical characteristics of their own panels. Therefore, they can flexibly adjust the panel optical characteristics according to their own panel characteristics, which can liberate the whole machine manufacturers from the tedious work of adjusting optical characteristics, so as to accelerate the development speed of the whole machine.

[0035] Further, it can be understood that the signal conversion circuit 11312, the DC voltage conversion circuit 11314, the level conversion circuit 11316 and the Gamma correction circuit 11318 of the display control circuit 1131 in the foregoing embodiments are not limited to being distributed on a single circuit sub-board 113a, but can also be distributed on a plurality of driving circuit boards, such as circuit sub-boards 113a and 113b in FIG. 1.

[0036] The above display devices can be: LTPO (Low Temperature Polycrystalline Oxide) display device, Micro LED display device, liquid crystal panel, electronic paper, OLED (Organic Light-Emitting Diode) panel, AMOLED (Active-Matrix Organic Light Emitting Diode) panel, mobile phone, tablet computer, TV, display, notebook computer, digital photo frame and other products or components with display function.

[0037] In the several embodiments provided by the invention, it should be understood that the illustrated system, device, and method may be implemented in other manners. For example, the embodiments of device described above are merely illustrative, for example, the division of units is only a logical function division, and in actual implementations there may be another division manner, for example, multiple units or components may be combined or integrated into another system, or some features can be ignored or not executed. In addition, the coupling or direct coupling or communication connection as illustrated may be an indirect coupling or communication connection through some interfaces, devices or units, and further may be in an electrical, mechanical or other form.

[0038] The units described as separate components may be or may not be physically separated, and the components illustrated as units may be or may not be physical units, that is, may be located in one place, or may be distributed to multiple network units. Some or all of the units may be selected according to actual needs to achieve the purposes of the solutions of the embodiments.

[0039] In addition, each functional unit in each embodiment of the invention may be integrated into one processing unit, or each unit may be physically separated, or two or more units may be integrated into one unit. The above integrated unit can be implemented in a form of hardware or in a form of hardware with a software functional unit(s).

[0040] The above integrated unit implemented in the form of the software functional unit(s) can be stored in a computer readable storage medium. The above software functional unit(s) is/are stored in a storage medium and include(s) several instructions for causing a computer device (which may be a personal computer, a server, or a network device, etc.) to perform some of the steps of various embodiments of the invention. The foregoing storage medium may be a U-disk, a mobile hard disk, a read-only memory (ROM), a random-access memory (RAM), a magnetic disk, or an optical disk, which can store program codes.

Claims

1. A display device (10), comprising:

a display panel (111), comprising a gate driving circuit and a source driving circuit;

a horizontal direction circuit board, X-board, (113), wherein a driving circuit board assembly (1130) is disposed on the X-board (113); wherein the driving circuit board assembly (1130) comprises a display control circuit (1131) and a first connector (CN1), and the display control circuit (1131) is connected to the gate driving circuit, the source driving circuit and the first connector

(CN1), and a nonvolatile memory (1133) is disposed on the X-board (113) and is electrically connected to the first connector (CN1);
a system board (13), wherein a second connector (CN2) and a system-on-chip (133) are disposed on the system board (13), and the system-on-chip (133) is connected to the second connector (CN2); and
a connecting part (CL1), connected between the first connector (CN1) and the second connector (CN2);
wherein the display device (10) is **characterized in that**
the display control circuit (1131) comprises a signal conversion circuit (11312), a direct-current (DC) voltage conversion circuit (11314) and a level conversion circuit (11316); the signal conversion circuit (11312) is electrically connected to the first connector (CN1) and the source driving circuit, and the level conversion circuit (11316) is electrically connected to the DC voltage conversion circuit (11314) and the gate driving circuit;
the signal conversion circuit (11312) is configured to receive a point-to-point, P2P, interface signal containing image data through the first connector (CN1) and generate source control signals and mini low voltage differential signaling, Mini-LVDS, interface signals according to the P2P interface signal, and output the source control signals and the Mini-LVDS interface signals to the source driving circuit;
the level conversion circuit (11316) is configured to generate gate control signals according to gate switching voltages generated from the DC voltage conversion circuit (11314) and reference timing signals, and output the gate control signals to the gate driving circuit;
the nonvolatile memory (1133) stores an optical performance adjustment parameter table (11330); and the system board (13) comprises an optical performance adjustment intellectual property, IP, core (1330);
the system-on-chip (133) is configured to read the optical performance adjustment parameter table (11330) stored in the nonvolatile memory (1133) through the second connector (CN2), the connecting part (CL1) and the first connector (CN1) and load the optical performance adjustment parameter table (11330) into the optical performance adjustment IP core (1330); and
the optical performance adjustment IP core (1330) comprises one or more selected from the group consisting of a Demura IP core (1331), a white balance adjustment IP core (1332), a color shift compensation IP core (1333), an OverDrive IP core (1334) and a dithering processing IP core (1335); and the optical performance adjustment parameter table (11330) correspondingly comprises one or more selected from the group consisting of a Demura parameter table (11331), a white balance adjustment parameter table (11332), a color shift compensation parameter table (11333), an OverDrive parameter table (11334) and a dithering processing parameter table (11335).

2. The display device (10) according to claim 1, wherein the X-board (113) comprises at least two circuit sub-boards juxtaposed with each other, the driving circuit board assembly (1130) is disposed on one of the at least two circuit sub-boards, and adjacent two circuit sub-boards (113a, 113b) of the at least two circuit sub-boards form an electrical connection through another connecting part (CL2) connected between connectors (CN3, CN4) respectively disposed on the adjacent two circuit sub-boards (113a, 113b).

3. The display device (10) according to claim 1, wherein a plurality of Mini-LVDS interfaces are disposed on the X-board (113), and the first connector (CN1) comprises a P2P interface.

4. The display device (10) according to claim 3, wherein the DC voltage conversion circuit (11314) is electrically connected to the first connector (CN1), and configured to receive an input DC voltage through the first connector (CN1), generate the gate switching voltages according to the input DC voltage, and output the gate switching voltages to the level conversion circuit (11316).

5. The display device (10) according to claim 4, wherein an integration manner of the DC voltage conversion circuit (11314), the level conversion circuit (11316) and the signal conversion circuit (11312) is one selected from the group consisting of:

the DC voltage conversion circuit (11314), the level conversion circuit (11316) and the signal conversion circuit (11312) are integrated into a same chip;
the DC voltage conversion circuit (11314) and the level conversion circuit (11316) are integrated into a same chip, and the signal conversion circuit (11312) is integrated into another chip;
the DC voltage conversion circuit (11314) and the signal conversion circuit (11312) are integrated into a same chip, and the level conversion circuit (11316) is integrated into another chip;
the level conversion circuit (11316) and the signal conversion circuit (11312) are integrated into a same chip, and the DC voltage conversion

circuit (11314) is integrated into another chip; and
the DC voltage conversion circuit (11314), the level conversion circuit (11316) and the signal conversion circuit (11312) are respectively integrated into different chips.

6. The display device (10) according to claim 3, wherein the display control circuit (1131) further comprises a Gamma correction circuit (11318);

wherein the DC voltage conversion circuit (11314) is electrically connected to the first connector (CN1), and configured to receive an input DC voltage through the first connector (CN1), generate the gate switching voltages and a reference voltage according to the input DC voltage, and output the gate switching voltages and the reference voltage to the level conversion circuit (11316) and the Gamma correction circuit (11318) respectively;
wherein the Gamma correction circuit (11318) is configured to generate a plurality of Gamma voltages according to the reference voltage and output the plurality of Gamma voltages to the source driving circuit.

7. The display device (10) according to claim 1, wherein the signal conversion circuit (11312) is further configured to receive the reference timing signals through the first connector (CN1), generate initial gate control signals according to the reference timing signals and output the initial gate control signals to the level conversion circuit (11316); and the level conversion circuit (11316) is specifically configured to generate the gate control signals according to the gate switching voltages and the initial gate control signal, and output the gate control signals to the gate driving circuit.

8. The display device according to claim 1, wherein the optical performance adjustment IP core (1330) comprises the Demura IP core (1331), the white balance adjustment IP core (1332), the color shift compensation IP core (1333), the OverDrive IP core (1334) and the dithering processing IP core (1335); and
the system-on-chip (133) is configured to sequentially control the Demura IP core (1331), the white balance adjustment IP core (1332), the color shift compensation IP core (1333), the OverDrive IP core (1334) and the dithering processing IP core (1335) to perform a Demura operation, a white balance adjustment, a color shift compensation operation, an OverDrive operation and a dithering processing operation according to the Demura parameter table (11331), the white balance adjustment parameter table (11332), the color shift compensation parameter table (11333), the OverDrive parameter table (11334) and the dithering processing parameter table (11335) respectively.

Patentansprüche

1. Ein Anzeigegerät (10), umfassend:

ein Anzeigefeld (111), das eine Gatter-Treiberschaltung und eine Quelle-Treiberschaltung umfasst;
eine waagerechte Leiterplatte (X-Platte) (113), wobei eine Treiberschaltungsbaukomponente (1130) auf der X-Platte (113) angeordnet ist; wobei der Treiberschaltungsbaukomponente (1130) eine Anzeigesteuerschaltung (1131) und einen ersten Stecker (CN1) umfasst und der Anzeigesteuerschaltung (1131) mit der Gatter-Treiberschaltung, der Quelle-Treiberschaltung und dem ersten Stecker (CN1) verbunden ist, und ein nicht-flüchtiges Speichermedium (1133) auf der X-Platte (113) angeordnet ist und elektrisch mit dem ersten Stecker (CN1) verbunden ist;
eine Systemplatte (13), wobei ein zweiter Stecker (CN2) und ein System-on-Chip (133) auf der Systemplatte (13) angeordnet sind und der System-on-Chip (133) mit dem zweiten Stecker (CN2) verbunden ist; und
ein Verbindungsteil (CL1), das zwischen dem ersten Stecker (CN1) und dem zweiten Stecker (CN2) verbunden ist;
wobei das Anzeigegerät (10) **dadurch gekennzeichnet ist, dass**

der Anzeigesteuerschaltung (1131) eine Signalumwandlungsschaltung (11312), eine Gleichspannungs-Umsetzungsschaltung (11314) und eine Pegelumwandlungsschaltung (11316) umfasst; der Signalumwandlungsschaltung (11312) ist elektrisch mit dem ersten Stecker (CN1) und der Quelle-Treiberschaltung verbunden und der Pegelumwandlungsschaltung (11316) ist elektrisch mit der Gleichspannungs-Umsetzungsschaltung (11314) und der Gatter-Treiberschaltung verbunden;
der Signalumwandlungsschaltung (11312) dazu bestimmt ist, ein Punkt-zu-Punkt (P2P)-Schnittstellen-Signal, das Bildinformationen enthält, über den ersten Stecker (CN1) zu empfangen und Quelle-Steuerungssignale und Mini-Low-Voltage-Differential-Signaling (Mini-LVDS)-Schnittstellen-Signale gemäß dem P2P-Schnittstellen-Signal zu erzeugen und der Quelle-Steuerungssignale und der Mini-LVDS-Schnittstellen-Signale an der Quelle-Trei-

berschaltung auszugeben;
der Pegelumwandlungsschaltung (11316) dazu bestimmt ist, Gatter-Steuerungssignale gemäß Gatter-Schaltspannungen, der von der Gleichspannungs-Umsetzungsschaltung (11314) erzeugt werden, und Referenztakt-Signale zu erzeugen und der Gatter-Steuerungssignale an der Gatter-Treiberschaltung auszugeben;
der nicht-flüchtiges Speichermedium (1133) eine Optik-Leistungs-Anpassungs-Parameter-Tabelle (11330) speichert; und der Systemplatte (13) einen Optik-Leistungs-Anpassungs-IP-Kern (1330) umfasst;
der System-on-Chip (133) dazu bestimmt ist, der Optik-Leistungs-Anpassungs-Parameter-Tabelle (11330), der im nicht-flüchtiges Speichermedium (1133) gespeichert ist, über den zweiten Stecker (CN2), das Verbindungsteil (CL1) und den ersten Stecker (CN1) zu lesen und der Optik-Leistungs-Anpassungs-Parameter-Tabelle (11330) in den Optik-Leistungs-Anpassungs-IP-Kern (1330) zu laden; und
der Optik-Leistungs-Anpassungs-IP-Kern (1330) einen oder mehrere aus der Gruppe bestehend aus einem Demura-IP-Kern (1331), einem Weißabgleich-Anpassungs-IP-Kern (1332), einem Farbversatz-Kompensations-IP-Kern (1333), einem Over-Drive-IP-Kern (1334) und einem Rundung-Bearbeitungs-IP-Kern (1335) umfasst; und der Optik-Leistungs-Anpassungs-Parameter-Tabelle (11330) entsprechend einen oder mehrere aus der Gruppe bestehend aus einer Demura-Parameter-Tabelle (11331), einer Weißabgleich-Anpassungs-Parameter-Tabelle (11332), einer Farbversatz-Kompensations-Parameter-Tabelle (11333), einer OverDrive-Parameter-Tabelle (11334) und einer Rundung-Bearbeitungs-Parameter-Tabelle (11335) umfasst.

2. Der Anzeigegerät (10) nach Anspruch 1, wobei der X-Platte (113) mindestens zwei nebeneinander angeordnete Schaltkreis-Teilplatten umfasst, der Treiberschaltungsbaukomponente (1130) auf einer der mindestens zwei Schaltkreis-Teilplatten angeordnet ist und angrenzende zwei Schaltkreis-Teilplatten (113a, 113b) der mindestens zwei Schaltkreis-Teilplatten eine elektrische Verbindung durch ein weiteres Verbindungsteil (CL2) bilden, das zwischen den jeweils auf den angrenzenden zwei Schaltkreis-Teilplatten (113a, 113b) angeordneten Steckern (CN3, CN4) verbunden ist.

3. Der Anzeigegerät (10) nach Anspruch 1, wobei eine Vielzahl von Mini-LVDS-Schnittstellen auf der X-Platte (113) angeordnet sind und der erste Stecker (CN1) ein P2P-Schnittstellen enthält.

4. Der Anzeigegerät (10) nach Anspruch 3, wobei der Gleichspannungs-Umsetzungsschaltung (11314) elektrisch mit dem ersten Stecker (CN1) verbunden ist und dazu bestimmt ist, eine Eingangs-Gleichspannung über den ersten Stecker (CN1) zu empfangen, der Gatter-Schaltspannungen gemäß der Eingangs-Gleichspannung zu erzeugen und der Gatter-Schaltspannungen an der Pegelumwandlungsschaltung (11316) auszugeben.

5. Der Anzeigegerät (10) nach Anspruch 4, wobei der Art der Integration der Gleichspannungs-Umsetzungsschaltung (11314), der Pegelumwandlungsschaltung (11316) und der Signalumwandlungsschaltung (11312) eine der folgenden ist:

der Gleichspannungs-Umsetzungsschaltung (11314), der Pegelumwandlungsschaltung (11316) und der Signalumwandlungsschaltung (11312) werden in dieselbe Chip integriert;
der Gleichspannungs-Umsetzungsschaltung (11314) und der Pegelumwandlungsschaltung (11316) werden in dieselbe Chip integriert und der Signalumwandlungsschaltung (11312) wird in einen anderen Chip integriert;
der Gleichspannungs-Umsetzungsschaltung (11314) und der Signalumwandlungsschaltung (11312) werden in dieselbe Chip integriert und der Pegelumwandlungsschaltung (11316) wird in einen anderen Chip integriert;
der Pegelumwandlungsschaltung (11316) und der Signalumwandlungsschaltung (11312) werden in dieselbe Chip integriert und der Gleichspannungs-Umsetzungsschaltung (11314) wird in einen anderen Chip integriert; und
der Gleichspannungs-Umsetzungsschaltung (11314), der Pegelumwandlungsschaltung (11316) und der Signalumwandlungsschaltung (11312) werden jeweils in unterschiedliche Chips integriert.

6. Der Anzeigegerät (10) nach Anspruch 3, wobei der Anzeigesteuerschaltung (1131) ferner eine Gamma-Korrekturschaltung (11318) umfasst; wobei der Gleichspannungs-Umsetzungsschaltung (11314) elektrisch mit dem ersten Stecker (CN1) verbunden ist und dazu bestimmt ist, eine Eingangs-Gleichspannung über den ersten Stecker (CN1) zu empfangen, der Gatter-Schaltspannungen und eine Referenzspannung gemäß der Eingangs-Gleichspannung zu erzeugen und derGatter-Schaltspannungen und der Referenzspannung jeweils an der Pegelumwandlungsschaltung (11316) und der Gam-

ma-Korrekturschaltung (11318) auszugeben;
wobei der Gamma-Korrekturschaltung (11318) dazu bestimmt ist, eine Vielzahl von Gamma-Spannungen gemäß der Referenzspannung zu erzeugen und der Vielzahl von Gamma-Spannungen an der Quelle-Treiberschaltung auszugeben.

7. Der Anzeigegerät (10) nach Anspruch 1, wobei der Signalumwandlungsschaltung (11312) ferner dazu bestimmt ist, der Referenztakt-Signale über den ersten Stecker (CN1) zu empfangen, anfängliche Gatter-Steuerungssignale gemäß der Referenztakt-Signale zu erzeugen und der anfänglichen Gatter-Steuerungssignale an der Pegelumwandlungsschaltung (11316) auszugeben; und der Pegelumwandlungsschaltung (11316) speziell dazu bestimmt ist, der Gatter-Steuerungssignale gemäß der Gatter-Schaltspannungen und dem anfänglichen Gatter-Steuerungssignal zu erzeugen und der Gatter-Steuerungssignale an der Gatter-Treiberschaltung auszugeben.

8. Der Anzeigegerät (10) nach Anspruch 1, wobei der Optik-Leistungs-Anpassungs-IP-Kern (1330) den Demura-IP-Kern (1331), den Weißabgleich-Anpassungs-IP-Kern (1332), den Farbversatz-Kompensations-IP-Kern (1333), den OverDrive-IP-Kern (1334) und den Rundung-Bearbeitungs-IP-Kern (1335) umfasst; und
der System-on-Chip (133) dazu bestimmt ist, den Demura-IP-Kern (1331), den Weißabgleich-Anpassungs-IP-Kern (1332), den Farbversatz-Kompensations-IP-Kern (1333), den OverDrive-IP-Kern (1334) und den Rundung-Bearbeitungs-IP-Kern (1335) nacheinander zu steuern, um eine Demura-Operation, einen Weißabgleich, eine Farbversatz-Kompensation, eine OverDrive-Operation und eine Rundung-Bearbeitung gemäß der Demura-Parameter-Tabelle (11331), der Weißabgleich-Anpassungs-Parameter-Tabelle (11332), der Farbversatz-Kompensations-Parameter-Tabelle (11333), der OverDrive-Parameter-Tabelle (11334) und der Rundung-Bearbeitungs-Parameter-Tabelle (11335) jeweils durchzuführen.

Revendications

1. Un dispositif d'affichage (10), comprenant:

un panneau d'affichage (111), comprenant un circuit de commande de grille et un circuit de commande de source;
une carte mère en direction horizontale (X-board) (113), sur laquelle est disposé un assemblage de carte de circuit de commande (1130);
où l'assemblage de carte de circuit de commande (1130) comprend un circuit de contrôle d'affichage (1131) et un premier connecteur (CN1), et le circuit de contrôle d'affichage (1131) est connecté au circuit de commande de grille, au circuit de commande de source et au premier connecteur (CN1), et une mémoire non volatile (1133) est disposée sur la X-board (113) et est connectée électriquement au premier connecteur (CN1);
une carte système (13), sur laquelle sont disposés un deuxième connecteur (CN2) et un système sur puce (133), et le système sur puce (133) est connecté au deuxième connecteur (CN2); et
une partie de connexion (CL1), connectée entre le premier connecteur (CN1) et le deuxième connecteur (CN2);

où le dispositif d'affichage (10) est **caractérisé par le fait que**
le circuit de contrôle d'affichage (1131) comprend un circuit de conversion de signal (11312), un circuit de conversion de tension en courant continu (DC) (11314) et un circuit de conversion de niveau (11316); le circuit de conversion de signal (11312) est connecté électriquement au premier connecteur (CN1) et au circuit de commande de source, et le circuit de conversion de niveau (11316) est connecté électriquement au circuit de conversion de tension en courant continu (DC) (11314) et au circuit de commande de grille;
le circuit de conversion de signal (11312) est configuré pour recevoir un signal d'interface point à point (P2P) contenant des données d'image par le premier connecteur (CN1) et générer des signaux de commande de source et des signaux d'interface Mini-LVDS (Mini-LVDS) en fonction du signal d'interface P2P, et transmettre les signaux de commande de source et les signaux d'interface Mini-LVDS au circuit de commande de source;
le circuit de conversion de niveau (11316) est configuré pour générer des signaux de commande de grille en fonction des tensions d'interrupteur de grille générées par le circuit de conversion de tension en courant continu (DC) (11314) et des signaux de référence de synchronisation, et transmettre les signaux de commande de grille au circuit de commande de grille;
le mémoire non volatile (1133) stocke un tableau de paramètres d'ajustement des performances optiques (11330); et la carte système (13) comprend un cœur de propriété intellectuelle (IP) d'ajustement des performances optiques (1330);

le système sur puce (133) est configuré pour lire le tableau de paramètres d'ajustement des performances optiques (11330) stocké dans la mémoire non volatile (1133) par le deuxième connecteur (CN2), la partie de connexion (CL1) et le premier connecteur (CN1) et charger le tableau de paramètres d'ajustement des performances optiques (11330) dans le cœur de propriété intellectuelle (IP) d'ajustement des performances optiques (1330); et
le cœur de propriété intellectuelle (IP) d'ajustement des performances optiques (1330) comprend un ou plusieurs éléments choisis parmi le groupe comprenant un cœur de propriété intellectuelle (IP) de correction de la mosaïque (Demura IP core) (1331), un cœur de propriété intellectuelle (IP) d'ajustement du blanc (1332), un cœur de propriété intellectuelle (IP) de compensation du décalage de couleur (1333), un cœur de propriété intellectuelle (IP) de surtension (OverDrive IP core) (1334) et un cœur de propriété intellectuelle (IP) de traitement de diffusion (1335); et le tableau de paramètres d'ajustement des performances optiques (11330) comprend respectivement un ou plusieurs éléments choisis parmi le groupe comprenant un tableau de paramètres de correction de la mosaïque (11331), un tableau de paramètres d'ajustement du blanc (11332), un tableau de paramètres de compensation du décalage de couleur (11333), un tableau de paramètres de surtension (11334) et un tableau de paramètres de traitement de diffusion (11335).

2. Le dispositif d'affichage (10) selon la revendication 1, où la X-board (113) comprend au moins deux sous-cartes de circuit juxtaposées les unes aux autres, l'assemblage de carte de circuit de commande (1130) est disposé sur l'une des au moins deux sous-cartes de circuit, et deux sous-cartes de circuit adjacentes (113a, 113b) des au moins deux sous-cartes de circuit forment une connexion électrique par une autre partie de connexion (CL2) connectée entre des connecteurs (CN3, CN4) respectivement disposés sur les deux sous-cartes de circuit adjacentes (113a, 113b).

3. Le dispositif d'affichage (10) selon la revendication 1, où une pluralité d'interfaces Mini-LVDS sont disposées sur la X-board (113), et le premier connecteur (CN1) comprend une interface P2P.

4. Le dispositif d'affichage (10) selon la revendication 3, où le circuit de conversion de tension en courant continu (DC) (11314) est connecté électriquement au premier connecteur (CN1), et configuré pour recevoir une tension en courant continu (DC) d'entrée par le premier connecteur (CN1), générer les tensions d'interrupteur de grille en fonction de la tension en courant continu (DC) d'entrée, et transmettre les tensions d'interrupteur de grille au circuit de conversion de niveau (11316).

5. Le dispositif d'affichage (10) selon la revendication 4, où une manière d'intégration du circuit de conversion de tension en courant continu (DC) (11314), du circuit de conversion de niveau (11316) et du circuit de conversion de signal (11312) est une parmi les suivantes:

le circuit de conversion de tension en courant continu (DC) (11314), le circuit de conversion de niveau (11316) et le circuit de conversion de signal (11312) sont intégrés dans le même puce;
le circuit de conversion de tension en courant continu (DC) (11314) et le circuit de conversion de niveau (11316) sont intégrés dans le même puce, et le circuit de conversion de signal (11312) est intégrée dans une autre puce;
le circuit de conversion de tension en courant continu (DC) (11314) et le circuit de conversion de signal (11312) sont intégrés dans le même puce, et le circuit de conversion de niveau (11316) est intégrée dans une autre puce;
le circuit de conversion de niveau (11316) et le circuit de conversion de signal (11312) sont intégrés dans le même puce, et le circuit de conversion de tension en courant continu (DC) (11314) est intégrée dans une autre puce; et
le circuit de conversion de tension en courant continu (DC) (11314), le circuit de conversion de niveau (11316) et le circuit de conversion de signal (11312) sont respectivement intégrés dans des puces différentes.

6. Le dispositif d'affichage (10) selon la revendication 3, où le circuit de contrôle d'affichage (1131) comprend en outre un circuit de correction Gamma (11318);

où le circuit de conversion de tension en courant continu (DC) (11314) est connecté électriquement au premier connecteur (CN1), et configuré pour recevoir une tension en courant continu (DC) d'entrée par le premier connecteur (CN1), générer les tensions d'interrupteur de grille et une tension de référence en fonction de la tension en courant continu (DC) d'entrée, et transmettre les tensions d'interrupteur de grille et la tension de référence respectivement au circuit de conversion de niveau (11316) et au circuit de

correction Gamma (11318);
où le circuit de correction Gamma (11318) est configuré pour générer une pluralité de tensions Gamma en fonction de la tension de référence et transmettre les tensions Gamma au circuit de commande de source.

7. Le dispositif d'affichage (10) selon la revendication 1, où le circuit de conversion de signal (11312) est en outre configuré pour recevoir les signaux de référence de synchronisation par le premier connecteur (CN1), générer des signaux de commande de grille initiaux en fonction des signaux de référence de synchronisation et transmettre les signaux de commande de grille initiaux au circuit de conversion de niveau (11316); et le circuit de conversion de niveau (11316) est spécifiquement configuré pour générer les signaux de commande de grille en fonction des tensions d'interrupteur de grille et du signal de commande de grille initial, et transmettre les signaux de commande de grille au circuit de commande de grille.

8. Le dispositif d'affichage (10) selon la revendication 1, où le cœur de propriété intellectuelle (IP) d'ajustement des performances optiques (1330) comprend le cœur de propriété intellectuelle (IP) de correction de la mosaïque (1331), le cœur de propriété intellectuelle (IP) d'ajustement du blanc (1332), le cœur de propriété intellectuelle (IP) de compensation du décalage de couleur (1333), le cœur de propriété intellectuelle (IP) de surtension (1334) et le cœur de propriété intellectuelle (IP) de traitement de diffusion (1335); et
le système sur puce (133) est configuré pour contrôler séquentiellement le cœur de propriété intellectuelle (IP) de correction de la mosaïque (1331), le cœur de propriété intellectuelle (IP) d'ajustement du blanc (1332), le cœur de propriété intellectuelle (IP) de compensation du décalage de couleur (1333), le cœur de propriété intellectuelle (IP) de surtension (1334) et le cœur de propriété intellectuelle (IP) de traitement de diffusion (1335) pour effectuer une opération de correction de la mosaïque, une opération d'ajustement du blanc, une opération de compensation du décalage de couleur, une opération de surtension et une opération de traitement de diffusion respectivement en fonction du tableau de paramètres de correction de la mosaïque (11331), du tableau de paramètres d'ajustement du blanc (11332), du tableau de paramètres de compensation du décalage de couleur (11333), du tableau de paramètres de surtension (11334) et du tableau de paramètres de traitement de diffusion (11335).

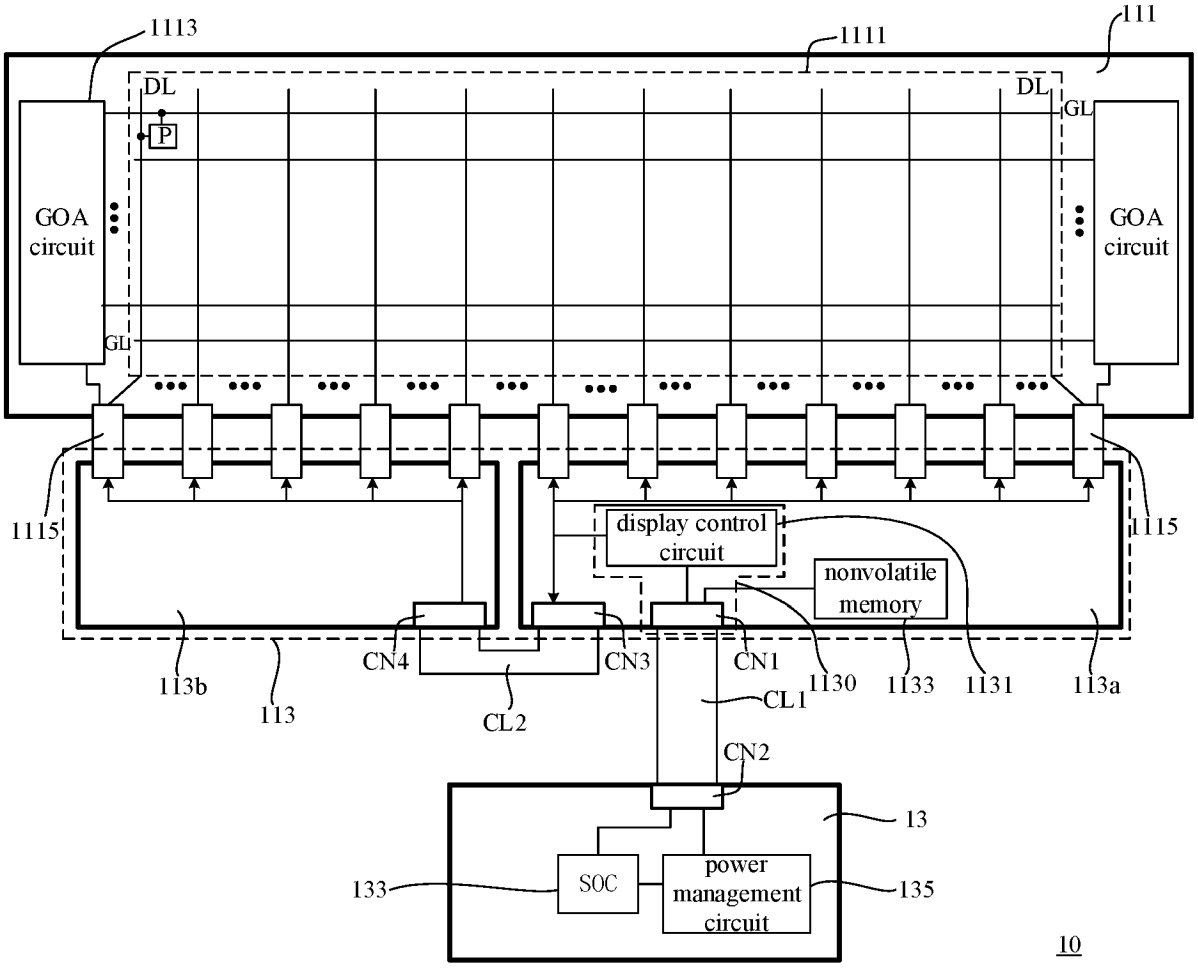
1113
1111
111
DL
DL
GL
P
GOA circuit
GOA circuit
GL
1115
1115
display control circuit
nonvolatile memory
CN4
CN3
CN1
1130
1133
1131
113a
113b
113
CL2
CL1
CN2
13
SOC
power management circuit
133
135
10

FIG. 1

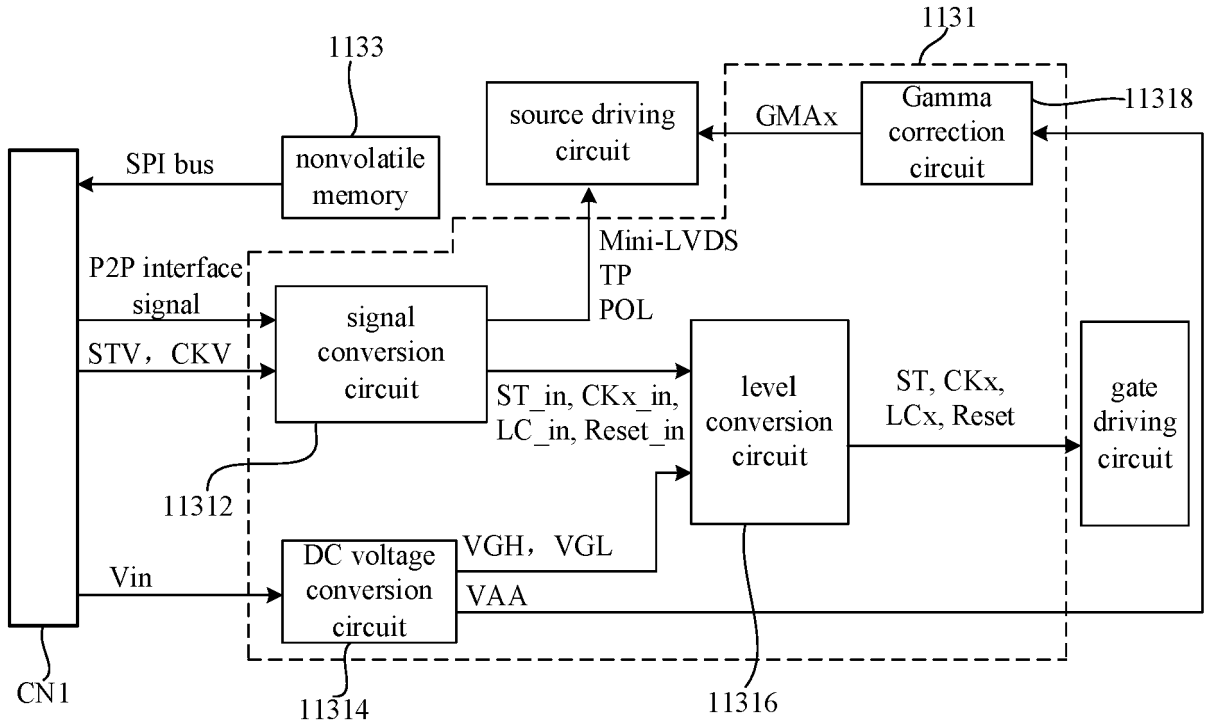
1131
1133
source driving circuit
GMAx
Gamma correction circuit
11318
SPI bus
nonvolatile memory
Mini-LVDS
TP
POL
P2P interface signal
signal conversion circuit
STV，CKV
ST_in, CKx_in, LC_in, Reset_in
level conversion circuit
ST, CKx, LCx, Reset
gate driving circuit
11312
VGH，VGL
Vin
DC voltage conversion circuit
VAA
CN1
11314
11316

FIG. 2

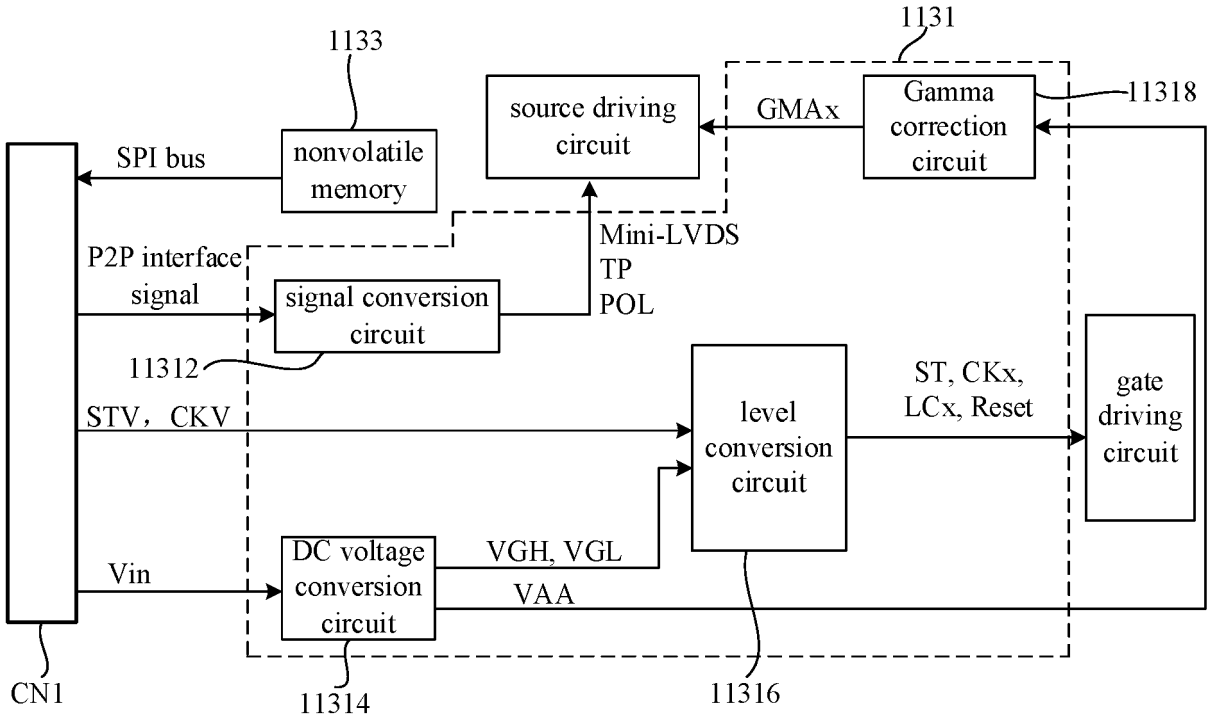
1131
1133
source driving circuit
GMAx
Gamma correction circuit
11318
SPI bus
nonvolatile memory
Mini-LVDS
TP
POL
P2P interface signal
signal conversion circuit
11312
ST, CKx, LCx, Reset
STV，CKV
level conversion circuit
gate driving circuit
VGH, VGL
Vin
DC voltage conversion circuit
VAA
CN1
11314
11316

FIG. 3

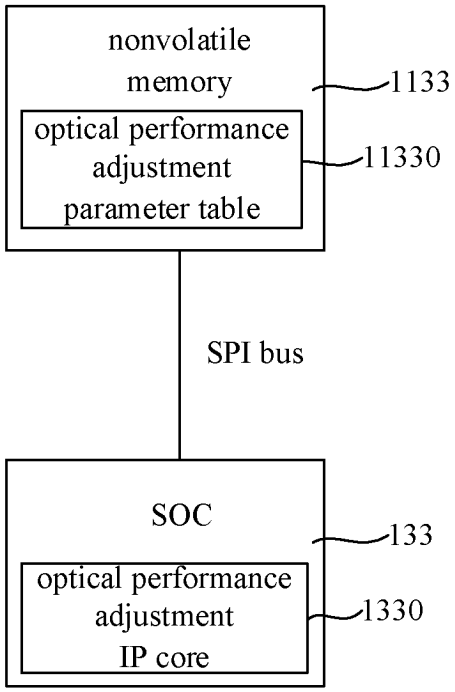
nonvolatile memory
1133
optical performance adjustment parameter table
11330
SPI bus
SOC
133
optical performance adjustment IP core
1330

FIG. 4

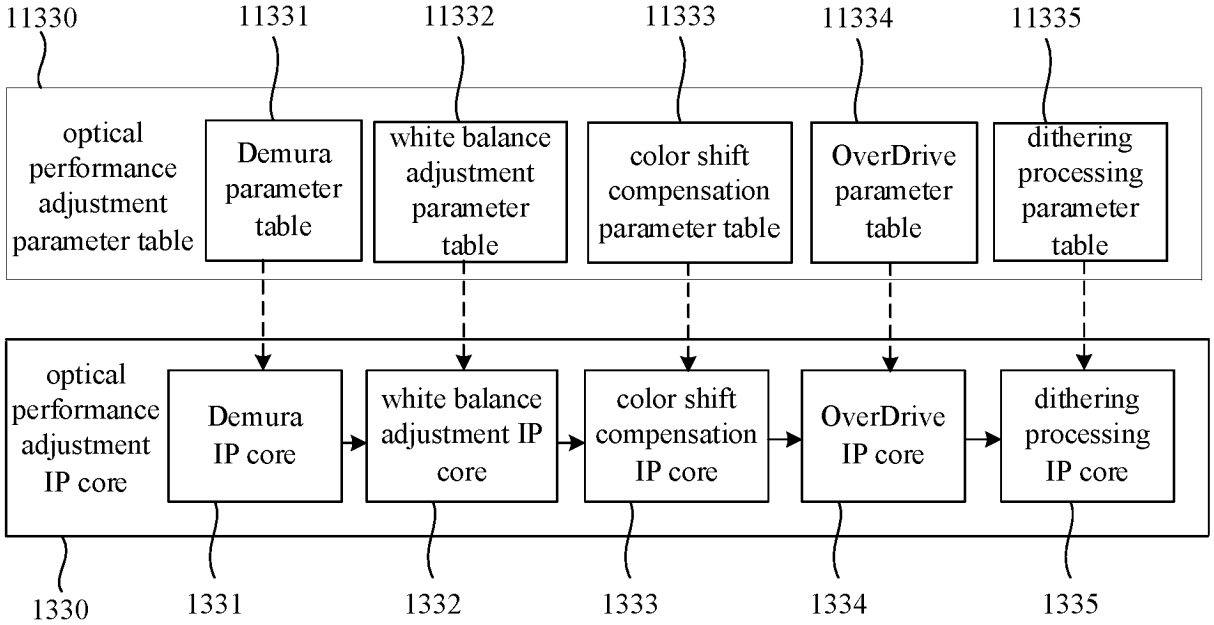
11330
11331
11332
11333
11334
11335
optical performance adjustment parameter table
Demura parameter table
white balance adjustment parameter table
color shift compensation parameter table
OverDrive parameter table
dithering processing parameter table
optical performance adjustment IP core
Demura IP core
white balance adjustment IP core
color shift compensation IP core
OverDrive IP core
dithering processing IP core
1330
1331
1332
1333
1334
1335

FIG.5

REFERENCES CITED IN THE DESCRIPTION

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