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(54) **Title**: CONDUCTIVE THROUGH-POLYMER VIAS FOR CAPACITIVE STRUCTURES

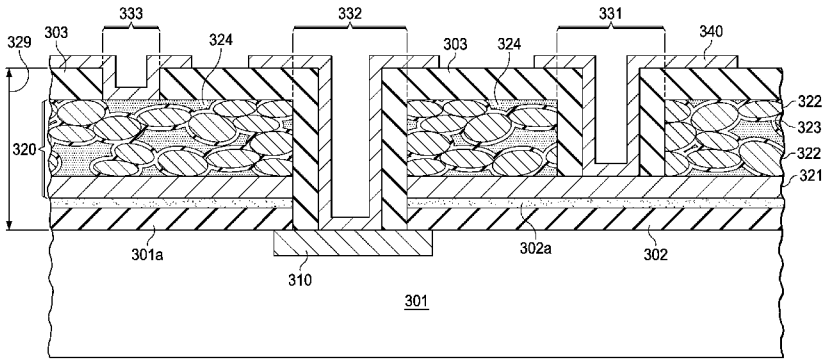

FIG. 3

(57) **Abstract**: In described examples, an electronic system includes an electronic body (301) with terminal pads (310) and at least one capacitor embedded in the electronic body. The capacitor includes: an insulating and adhesive first polymeric film (302) covering the body surface except the terminal pads; a sheet (320) of high-density capacitive elements, the first capacitor terminal being a metal foil (321) attached to the first polymeric film (302), the second terminal being a conductive polymeric compound (324), and the insulator being a dielectric skin (323). Sheet (320) has sets of via-holes, including: a first set of holes reaching the metal foil (321), a second set of holes reaching the terminals (310), and a third set of holes reaching the conductive polymeric compound (324). An insulating second polymeric film (303) lines the sidewalls of the holes and planarizes the sheet surface. Metal fills the via-holes between the polymeric sidewalls and forms conductive traces and attachment pads on the system surface.

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CONDUCTIVE THROUGH-POLYMER VIAS FOR CAPACITIVE STRUCTURES

[0001] This relates generally to semiconductor devices and processes, and more particularly to a structure and fabrication method of electronic systems encapsulated in a package with embedded nanometer-sized three-dimensional capacitors.

BACKGROUND

[0002] Popular families of power supply circuits include DC/DC converters, which are power switching devices for converting one DC voltage to another DC voltage. For emerging power delivery requirements, a particularly suitable assembly (also called a half bridge) is a power block with two power MOS field effect transistors (FETs) connected in series and coupled together by a common switch node. When a regulating driver and controller are added, the assembly is referred to as power stage, or more commonly as synchronous buck converter or voltage regulator. In the synchronous buck converter, the control FET chip (also called the high-side switch) is connected between the supply voltage V_{IN} and the LC_{OUT} output filter, and the synchronous (sync) FET chip (also called the low side switch) is connected between the LC_{OUT} output filter and ground potential. The gates of the control FET chip and the sync FET chip are connected to a semiconductor chip, including the circuitry for the driver of the converter and the controller.

[0003] For many of today's power switching devices, the chips of the power MOSFETs and the driver and controller IC are assembled as individual components. The chips are typically attached to a rectangular or square-shaped pad of a metallic leadframe. The pad is surrounded by leads as output terminals. This approach consumes area and increases the footprint of the module. In another technique, the control FET chip and the sync FET chip are assembled vertically on top of the other as a stack. In this assembly, at least one MOSFET chip is configured for vertical current flow. The source electrode of the control FET chip is facing the drain electrode of the sync FET chip.

[0004] Typically, capacitors of various sizes are among the components of electronic systems assembled on printed circuit boards. To save board space and reduce parasitics, these capacitors

are often placed as piece parts in tight proximity to other board components, such as transistors and inductors. Driven by the relentless trend to conserve board real estate and minimize parasitic electrical effects, these capacitors are sometimes placed under or on top of other components.

[0005] In another example for conservation, stacked chip power MOSFETs have been proposed, which integrate a capacitor into the package of the device. To increase the obtainable value of capacitance per area by at least one order of magnitude, capacitors have been demonstrated based on the concept of folding the third dimension into the area of two dimensions. Cavities are etched into metal boards, such as boards made of aluminum. The aluminum surface in the cavities is then oxidized, and the cavities are filled with a conductive material, such as a polymeric compound. After applying contacts to the metal board and the conductive compound, the three-dimensional structure can be operated as a capacitor offering high capacitance values.

SUMMARY

[0006] In described examples, an electronic system includes an electronic body with terminal pads and at least one capacitor embedded in the electronic body. The capacitor includes: an insulating and adhesive first polymeric film covering the body surface except the terminal pads; a sheet of high-density capacitive elements, the first capacitor terminal being a metal foil attached to the first polymeric film; the second terminal being a conductive polymeric compound; and the insulator being a dielectric skin. The sheet has sets of via-holes, including: a first set of holes reaching the metal foil, a second set of holes reaching the terminals, and a third set of holes reaching the conductive polymeric compound. An insulating second polymeric film lines the sidewalls of the holes and planarizes the sheet surface. Metal fills the via-holes between the polymeric sidewalls and forms conductive traces and attachment pads on the system surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 shows a circuit diagram of a power supply system including DC/DC converter, capacitors and inductor.

[0008] FIG. 2 illustrates a simplified cross section of a power supply system with capacitors integrated into a packaged semiconductor body according to example embodiments.

[0009] FIG. 3 shows a schematic cross section of a portion of a semiconductor wafer with attached high-density capacitive structures and conductive through-polymer vias reaching

conductors at three depth levels.

[0010] FIG. 4A illustrates a cross section of a portion of an example embodiment, a semiconductor body integral with high-density capacitive structures and conductive through-polymer vias connecting body terminal pads to surface contact pads having solder ball connectors.

[0011] FIG. 4B illustrates a cross section of a portion of an example embodiment, a semiconductor body integral with high-density capacitive structures and conductive through-polymer vias connecting body terminal pads to surface contact pads having wire ball bond connectors.

[0012] FIG. 5A depicts the process of providing a semiconductor wafer with embedded circuitry and circuitry contact pads on a wafer side.

[0013] FIG. 5B illustrates the process of laminating an insulating and adhesive first polymeric film across the wafer surface.

[0014] FIG. 5C shows the process of attaching a sheet of high density capacitive elements to the first polymeric film.

[0015] FIG. 5D depicts the process of attaching a metal foil carrying pre-defined high density capacitive elements to the first polymeric film.

[0016] FIG. 6A depicts the processes of opening sets of via-holes of a first diameter in the sheet of FIG. 5C.

[0017] FIG. 6B illustrates the process of laminating an insulating second polymeric film to fill the via-holes of first diameter and to planarize the surface of the sheet of FIG. 6A.

[0018] FIG. 6C shows the process of opening sets of through-polymer vias of a second diameter in the second polymeric film of FIG. 6B.

[0019] FIG. 6D depicts the process of laminating an insulating second polymeric film to fill the via-holes of first diameter and to planarize the surface of the sheet of FIG. 5D.

[0020] FIG. 6E illustrates the process of opening sets of through-polymer vias of a second diameter in the second polymeric film of FIG. 6D.

[0021] FIG. 7A depicts the process of depositing a metal seed layer across the surface.

[0022] FIG. 7B illustrates the process of patterning the metal seed layer.

[0023] FIG. 7C shows the process of plating metal on the patterned seed layer to fill the through-polymer vias and thicken to attachment pads and redistribution traces.

[0024] FIG. 8 illustrates the cross section of a portion of another embodiment.

[0025] FIG. 9 depicts the cross section of yet another embodiment.

[0026] FIG. 10 shows the cross section of a portion of yet another embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0027] For providing miniature capacitors with high capacitance values to semiconductor chips and electronic systems of ever shrinking geometrical dimensions, these capacitors are most effective when they are thin film capacitors, integrated into the conductive network interconnecting the circuit elements, and in close proximity to active circuitry. For devices needing a package for protecting bonding wires, the capacitors may be fully integrated into the package. For devices that can be solder-assembled without housing, the capacitors may be fully integrated into the semiconductor chip.

[0028] The integration into conductive networks requires conductive vias of controlled depth through insulating materials, so that the capacitors can be connected to each conductive level of a multi-level laminated network.

[0029] The problem of conductive vias through insulating polymers is solved by a methodology to create concurrently polymeric bonds to metals, refractory metals, conductive polymers, and inorganic insulators. The methodology accepts pre-fabricated sheets of high density nano-capacitors, attaches the sheets to semiconductor wafers, fabricates the interconnections between capacitors and chip circuitry at various levels of a multi-level laminate, and, if needed, forms the packages for the devices before singulating the devices from the wafer.

[0030] Example embodiments of conductive through-polymer-vias are distinguished by the absence of a problem of mismatched coefficients of thermal expansion (which otherwise is a problem with through-silicon-vias), avoiding device failures due to delamination and temperature cycling.

[0031] The methodology is flexible and applicable to diverse devices with a single semiconductor chip, and to devices such as power supply systems with multiple chips. Due to the capacitors combining high capacitance density, high operating frequency and miniscule size, the semiconductor devices may have small overall sizes in the low millimeter range. They further demonstrate stability of capacitance and frequency, and exhibit high reliability in high and low temperatures and in temperature swings.

[0032] For the preferred application to power supply systems, example embodiments reduce

electrical parasitics by placing the input capacitor in close proximity to the active circuitry. The reduced parasitic inductance allows an increase of switching frequency, which in turn allows a shrinkage of the bulky output inductor.

[0033] The preferred process flow enables concurrent lithography through multiple consecutively applied polymeric compounds and a concurrent curing process of the polymers.

[0034] In the circuit diagram of FIG. 1, the power supply indicated by dashed outline 101 includes DC/DC converter 102, input capacitor C_{IN} 103, output capacitor C_{OUT} 104 and inductor L 105. FIG. 2 illustrates an implementation of a power supply as an example silicon-in-package device 200 for board attachment with solder balls 260. Device 200 is based on an example embodiment. Device 200 includes semiconductor body 201 in a package 202, input capacitor C_{IN} 203, output capacitor C_{OUT} 204 and inductor L 205. Semiconductor body may be a single silicon chip, or an assembly of more than one chip. More generally, body 201 may be an electronic body, which may include an assembly of one or more semiconductor chips, or generally may include electronic circuitry.

[0035] As shown in the power supply of FIG. 2, both capacitors are embedded with semiconductor body 201, while the inductor 205 (serving as the energy storage of the power supply circuit) is a large enough discrete component (such as 300 to 400 nH) to reliably function as the maintainer of a constant output voltage V_{OUT}. In other embodiments, the capacitors may be embedded, so that the output capacitor 204a is on the backside of body 201, or the input capacitor is positioned in a gap between the inductor and the package.

[0036] By embedding the capacitors with the semiconductor body, the physical dimensions of the power supply device can be reduced significantly. For example, while a device with conventional discrete capacitors and inductor may require device dimensions of length 2.9 mm, width 2.3 mm, and height 1 mm (including the discrete components), the same device with embedded capacitors achieves dimensions of length 2.0 mm, width < 1.5 mm (such as 1.0 mm), and height 1 mm (including a discrete inductor).

[0037] FIG. 3 summarizes the composition and the methodology of integrating the capacitors with the semiconductor body, or generally with the electronic body. In FIG. 3, semiconductor body 301 has a surface 301a with conductive terminal pads 310 of the circuitry inside the semiconductor body. For the example of a DC/DC converter, pads 310 include the terminals displayed in the diagram in FIG. 1 (V_{IN}, V_{OUT}, Enable, Ground, Mode Selection).

[0038] Multiple features tie one or more capacitors to the electronic body and physically embed the capacitors into body 301. FIG. 3 shows an insulating first polymeric film 302, which covers the body surface 301a except the terminal pads 310. First film 302 is adhesive, and its adhesive character is indicated in FIG. 3 by tacky extra film 302a.

[0039] Adhering to first film 302 is a sheet 320 of high-density capacitive elements, which have with first and second capacitor terminals. The first terminal is a metal foil 321 attached to the first polymeric film 302, and the second terminal is formed by a conductive polymeric compound 324. The thickness 329 of sheet 320, together with first insulating film 302 and second insulating film 303, is approximately 50 μm.

[0040] The sheet of capacitive elements includes a metal foil 321, which is the first terminal of the capacitor (sometimes referred as the anode). A porous conglomerate of sintered metal particles 322 is in touch with foil 321. The particle surfaces are covered with a dielectric skin 323, which can be created by oxidation of the particle metal or by coating the particles with an insulating material. As FIG. 3 shows, the voids and pores between the dielectric skin-covered sintered metal particles are filled by a conductive polymeric material 324. Conductive polymer 324 forms the sheet side opposite the metal film 321 and serves as second terminal of the capacitor (sometimes referred to as the cathode). Due to a density of approximately 200 $\mu F/cm^2$ or less and a capacitor stability up to 125 °C, the sheet is operable as a high-density capacitor with metal film 321 as first terminal, conductive polymer 324 as second terminal, and dielectric skin 323 of the metal particles as insulator.

[0041] In the example of FIG. 3, the capacitor sheet 320 has sets of conductive through-hole vias. The first set of holes, generally designated 331, reaches the metal foil 321. The second set of holes, generally designated 332, reaches the body terminals pads 310. The third set of holes, generally designated 333, reaches the conductive polymeric compound 324, and potentially partially contacts the sintered metal particles 322. The conductive through-hole vias of the three sets share some common features.

[0042] As FIG. 3 shows, an insulating second polymeric film 303 lines the sidewalls of the holes. Polymeric film 303 also planarizes the sheet surface between the holes. The processes for applying film 303 and opening of the through-hole vias are described below. After the process of opening the through-polymer vias in the polymeric film 303, the vias are made conductive by filling the through-polymer vias between the polymeric sidewalls with metal. FIG. 3 includes

the process of depositing a layer of seed metal 340 over the sidewalls of the opened holes. In FIG. 3, seed layer 340 is patterned, so that it covers only narrow areas surrounding each hole. The shape of actual through-polymer vias may deviate from the cylindrical shape with vertical sidewalls depicted in FIG. 3. For example, the hole sidewalls may have conical shape.

[0043] In the embodiments of FIGS. 4A and 4B, seed layer 340 has been patterned, so that the patterning allows the formation of redistribution traces 341 and attachment pads 342 on the surface of first insulator film 303. FIGS. 4A and 4B include conductive through-polymer vias (of set 332) reaching terminals pads 310 of body 301. For these vias, metal 432 has been plated (about 3 μm thick) onto the patterned seed layer to fill the through-polymer vias and thicken the attachment pads 342. The preferred plated metal 432 is copper. In FIG. 4A, solder balls 460 are attached to the thickened pads. In FIG. 4B, wire ball bonds 461 are attached to the thickened pads.

[0044] As FIGS. 4A and 4B show, some redistribution traces 341 connect from a through-polymer via reaching a body terminal to a conductive through-polymer via reaching metal foil 321, which is the first terminal (anode) of the capacitor. Other redistribution traces 341 connect from a through-polymer via reaching another body terminal to a conductive through-polymer via reaching the conductive polymeric compound 324, which is the second terminal (cathode) of the capacitor.

[0045] Another embodiment is a method for batch fabricating electronic systems, such as power supply systems, which are integrated with embedded capacitors. As depicted in FIG. 5A, the method starts by providing a semiconductor wafer 501 with embedded electronic bodies, such as integrated circuits, power blocks or power stages. Conductive contact pads of the electronic bodies are integrated in the wafer surface.

[0046] In the next process, depicted in FIG. 5B, an insulating first polymeric film 502 is laminated across the wafer surface 501a. A preferred material is an epoxy-based polymer with a filler and high modulus. First polymeric film 502 is adhesive; the adhesive property is indicated in FIG. 5B by tacky extra film 502a.

[0047] FIGS. 5C illustrates the next processes. A sheet 520 of high density capacitive elements is provided. One side of sheet 520 is formed as a foil 521 of a metal, such as tantalum or a metal readily forming uniform and stable oxides. Foil 521 is in touch with a porous conglomerate of sintered particles 522 of the same metal. For example, the sintered particles

may be tantalum particles. The particle surfaces are covered with a dielectric skin 523, which may be formed as an oxide of the metal, such as tantalum. Alternatively, the skin may be a thin layer of a temperature-stable insulating material. The opposite side of sheet 520 is formed by a conductive polymeric material 524, which is dispensed to fill the pores and voids between the particles. Sheet 520 is operable as a capacitor, which has metal 521 as its first terminal, the conductive polymer 524 as its second terminal, and the dielectric skin 523 of the metal particles as the insulator between the terminals. More detail of the methods for high-density capacitor sheet 520 is described in: Patent No. US 8,084,841 B2, issued Dec. 27, 2011 (Pulugurtha et al, "Systems and Methods for Providing High-Density Capacitors"); and Patent No. US 8,174,017 B2, issued May 8, 2012 (Pulugurtha et al., "Integrating Three-Dimensional High Capacitance Density Structures").

[0048] As shown in FIG. 5C, sheet 520 is attached by its metal foil 521 onto the adhesive first polymeric film 502.

[0049] FIG. 5D depicts an alternative process for providing high density capacitive elements. In FIG. 5D, the metallic foil 521a carries the attached porous conglomerates of sintered particles as discrete pre-etched elements, rather than as continuous layer as in FIG. 5C. The discrete elements are separated by via-holes of a first diameter 601 (the same diameter as produced by the process of FIG. 6A), while the foil surrounding the elements remains as supportive carrier (indicated by dashed line 521b) outside the via-holes. As shown in FIG. 5D, sheet 520 is attached by its metal foil 521 onto the adhesive first polymeric film 502a.

[0050] FIG. 6A illustrates the process of opening a set of via-holes of a first diameter 601 into sheet 520. Holes 631 of the first set are reaching the metal foil 521, and holes 632 of the second set are reaching the wafer contact pads 510. A preferred method for drilling the openings is a UV laser.

[0051] In the next process, shown in FIG. 6B, an insulating second polymeric film 503 is laminated across the wafer, so that the polymeric material fills the via-holes of the first diameter 601 and planarizes the sheet surface.

[0052] After curing the polymeric material, the next process, shown in FIG. 6C, opens sets of through-polymer via-holes of a second diameter 602 into the second polymeric film 503. The second diameter 602 is smaller than the first diameter 601, and the sidewalls of these via-holes are composed of the insulating second polymeric material. The third set includes the holes 651,

which are nested inside the first set of holes 631; holes 651 reach the metal foil 521. The fourth set includes the holes 652, which are nested inside the second set of holes 632; holes 652 reach a contact pad 510. The fifth set includes holes 653, which reach the conductive polymeric surface 524. A preferred method for drilling the holes is a UV laser.

[0053] In FIG. 6D, the above processes are modified for adapting them to the discrete pre-etched elements of porous conglomerates of sintered particles. As illustrated in FIG. 6D, in a process analogous to the process of FIG. 6B, an insulating second polymeric film 503 is laminated across the wafer, so that the polymeric material fills the via-holes of the first diameter 601 and planarizes the sheet surface. After curing the polymeric material, the process of FIG. 6E (analogous to the process of FIG. 6C) opens sets of through-polymer via-holes of a second diameter 602 into the second polymeric film 503, and into the first polymeric film 502. The second diameter 602 is smaller than the first diameter 601, and the sidewalls of these via-holes are composed mostly of the insulating second polymeric material, and partially also of the first polymeric material. The third set includes the holes 651, which are nested inside the first set of holes 631; holes 651 reach the metal foil 521. The fourth set includes the holes 652, which are nested inside the second set of holes 632; holes 652 reach a contact pad 510. The fifth set includes holes 653, which reach the conductive polymeric surface 524. A preferred method for drilling the holes is a UV laser.

[0054] In the next processes, the through-polymer vias are metallized. FIG. 7A shows the preferred process of depositing a metal seed layer 540 onto the sidewalls and bottoms of the through-polymer vias and the surface of the second polymeric film 503; the preferred technology is electroless plating. An alternative technology involves sputtering. The preferred metal is a refractory metal, such as titanium or tungsten, which adheres well to polymeric compounds. FIG. 7B illustrates the process of patterning seed metal layer 540 to create redistribution traces 541 and attachment pads on the surface of the second polymeric film 503.

[0055] In the process depicted in FIG. 7C, a relatively thick layer 532 of metal (such as copper) is plated onto the patterned seed layer to fill the through-polymer vias and thicken the attachment pads and redistribution traces. A preferred thickness of the redistribution traces is about 3 μm.

[0056] In yet another process, the deposition of the relatively thick metal layer occurs immediately after the deposition of the seed metal layer, while the process of patterning is

applied concurrently to the thick metal layer and the seed metal layer.

[0057] In an alternative process, the deposition of the metallic seed layer may be replaced by activating the sidewall surfaces of the polymeric materials before the 3 μm thick copper layer is deposited by electroless plating.

[0058] Additional processes involve the attachment of solder balls or wire ball bonds, such as shown in FIGS. 4A and 4B, and further the step of singulating the semiconductor wafer into discrete units. Each unit includes a system of one or more active semiconductor chips embedded with one or more capacitors composed of high density capacitive elements, and multiple attachment pads for external components.

[0059] After the processes in the sequence described above for implementing high-density capacitive structures with conductive through-polymer vias into semiconductor chips, and simplifying in the drawings the capacitor structure into uniform layers for the first and second terminals and the intermediate insulator, a portion of an example embodiment with solder balls can be represented as shown in FIG. 8. In the embodiment 800 of FIG. 8, the high-density capacitive structures are embedded in the redistribution layers on the surface of the semiconductor chip. The designations of device 800 correspond to analogous designations in FIG. 4. Semiconductor chip 801 has a surface with conductive terminal pads 810. The levels of parallel first insulating polymeric film 802 and second insulating polymeric film 803 are interconnected by metallic vias 804 and allow an extension into a redistribution layer 841 to a terminal 832 with metallization for attaching a solder ball 860. The length of the redistribution layer between two adjacent terminals 832 is used for accommodating the high-density capacitive structure indicated by first terminal (anode, metal) 821, second terminal (cathode, conductive polymer) 824, and insulator layer 823.

[0060] The process flow for fabricating device 800 follows the sequence described above. However, in another embodiment 900 (FIG. 9), when the high-density capacity structure (first terminal 921, second terminal 924, insulator layer 923) can occupy the place of a depopulated solder ball, the second insulating polymeric film 903 is preferably laminated immediately after the lamination of the first insulating polymeric film 902, and before the attachment of the sheet of high-density capacitive elements.

[0061] In yet another embodiment, such as device 1000 (FIG. 10), semiconductor chip 1001 may have conductive through-silicon vias (TSVs) 1080, which enable contacts to structures on

the active chip side 1001a from the opposite and generally passive chip side 1001b. In these cases, for the assembly of systems on boards, it may be helpful to place the one or more capacitors on chip side 1001b and connect the capacitor to the structures on chip side 1001a with the help of the TSVs 1080. FIG. 10 shows an elongated capacitor with first terminal 1021, second terminal 1024 and insulator 1023 extended between adjacent TSVs. For the fabrication flow of device 100, the second insulating polymeric film 1003 is preferably laminated immediately after the lamination of the first insulating polymeric film 1002, and before the attachment of the sheet of high-density capacitive elements.

[0062] As FIG. 4B indicates, high density capacitors can be embedded in semiconductor chips, which use wire ball bonding on top of the embedded capacitor to connect the chip terminals to substrates, such as metallic leadframes. Due to the bonding wires, such electronic bodies need to be encapsulated in protective packages.

[0063] In addition to the example power systems with DC/DC converters as the electronic bodies described above, the embedding of high density capacitors can be applied to flyback converters, DC/DC boost converters and isolated converters, charge pumps, fuel gauges, power stages with drivers and load switches, voltage references, current references, current sensors, and generally any electronic systems using capacitors.

[0064] The conductive through-polymer vias, which enable the embedding of the capacitive structures in semiconductor chips, are free of thermomechanical stresses due to differences in CTE (coefficients of thermal expansion). This absence of stress sensitivity is a technical advantage compared to the conventional TSVs (through-silicon vias) 1080 of FIG. 10, which are plagued by thermomechanical stress problems.

[0065] Example embodiments are applicable to a chip with integrated circuits, and to devices with any type of semiconductor chip. For example, the capacitor sheet may be attached to the surface of a chip, which is assembled on a leadframe pad, wire bonded to leads, and encapsulated in a protective packaging compound.

[0066] As another example, the method can be extended to capacitors embedded in an arbitrary number of semiconductor chips integrated into a system. The capacitors may be embedded inside the system or on either surface of the system.

[0067] As another example, the capacitance value of capacitors may be modified by varying the process of creating the porous structure, thus allowing use of the same geometrical capacitor

values yet with different capacitance values, which is an inexpensive way of using available package structures with different electrical values.

[0068] In yet another example, the metals, insulators, geometries and thicknesses of the capacitors can be selected as a function of the size of the chip, so that specific product goals of the assembled package can be achieved, such as final thickness, mechanical strength, minimum warpage, prevention of cracking, compatibility with pick-and-place machines, and minimum electrical parasitics.

[0069] In yet another example, the high-density capacitive elements can be adjusted and positioned, so that electrical characteristics (such as operational frequency and frequency stability) can be optimized.

[0070] In yet another example, the properties of the capacitive structures may have unique sensitivity to physical parameters (such as stress, moisture, pressure, irradiation, chemical exposure, or others that may be discovered), so that the electrical properties of the capacitive structures can be measured, and the structures can be used as a sensor.

[0071] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An electronic system comprising:

an electronic body having a surface with conductive terminal pads;

at least one capacitor embedded in the electronic body, the capacitor including:

an insulating first polymeric film covering the body surface except the terminal pads, the first film being adhesive;

a sheet of high-density capacitive elements with first and second capacitor terminals, the first terminal being a metal foil attached to the first polymeric film and the second terminal being a conductive polymeric compound;

the sheet having sets of via-holes, the first set of holes reaching the metal foil, the second set of holes reaching the body terminals pads, and the third set of holes reaching the conductive polymeric compound;

an insulating second polymeric film lining the sidewalls of the holes and planarizing the sheet surface; and

metal filling the via-holes between the polymeric sidewalls, and forming conductive traces and attachment pads on the system surface.

2. The system of claim 1 wherein the sheet of capacitive elements includes a metal foil in touch with a porous conglomerate of sintered metal particles, the particle surfaces covered with a dielectric skin, and the opposite sheet side formed by a conductive polymeric material filling the pores between the metal particles, the sheet operable as a high-density capacitor having the metal as first terminal, the conductive polymer as second terminal, and the dielectric skin of the metal particles as insulator.

3. The system of claim 1 wherein the electronic body includes embedded circuitry.

4. The system of claim 1 wherein the electronic body includes an assembly of one or more active semiconductor chips.

5. The system of claim 1 wherein the electronic system is selected from a group including power supply systems having a DC/DC converter, including a synchronous Buck converter, flyback converters, DC/DC boost converters, isolated converters, charge pumps, fuel gauges, power stages with drivers and load switches, voltage references, current references, and current sensors.

6. The system of claim 5 wherein the embedded at least one capacitor has, on its surface, redistribution traces and attachment pads for externals parts.

7. The system of claim 6 wherein the attachment pads have attached connectors selected from a group including solder balls and wire ball bonds.

8. The system of claim 6 wherein the external parts include an inductor.

9. The system of claim 1 wherein the electronic body and the embedded at least one capacitor are encapsulated in a package.

10. A method for fabricating an electronic system comprising:

providing a semiconductor wafer having embedded electronic bodies, the wafer surface having conductive contact pads of the electronic bodies;

laminating an insulating first polymeric film across the wafer surface, the first film being adhesive;

providing a sheet of high density capacitive elements, one sheet side formed as a metal foil in touch with a porous conglomerate of sintered metal particles, the particle surfaces covered with a dielectric skin, and the opposite sheet side formed by a conductive polymeric material filling the pores between the particles, the sheet operable as a capacitor having the metal as first terminal, the conductive polymer as second terminal, and the dielectric skin of the metal particles as insulator;

attaching the sheet by its metal foil onto the first polymeric film;

opening sets of via-holes of a first diameter into the sheet, including a first set of holes reaching the metal foil, and a second set of holes reaching the wafer contact pads;

laminating an insulating second polymeric film across the wafer, filling the via-holes of the first diameter and planarizing the sheet surface;

opening sets of through-polymer vias of a second diameter into the second polymeric film, the second diameter being smaller than the first diameter; a third set of holes, nested inside the first set of holes, reaching the metal foil; a fourth set of holes, nested inside the second set of holes, reaching a contact pad; and a fifth set of holes reaching the conductive polymeric surface;

depositing and patterning a metal seed layer onto the sidewalls and bottoms of the through-polymer vias and the surface of the second polymeric film, creating redistribution traces and attachment pads on the surface; and

plating metal onto the patterned seed layer to fill the through-polymer vias and thicken

the attachment pads and redistribution traces.

11. The method of claim 10 further including the process of concurrently curing the first and second polymeric materials.

12. The method of claim 10 further including the process of singulating the wafer into discrete units, each unit including a system of one or more active semiconductor chips embedded with one or more capacitors composed of high density capacitive elements, and a plurality of attachment pads for external components.

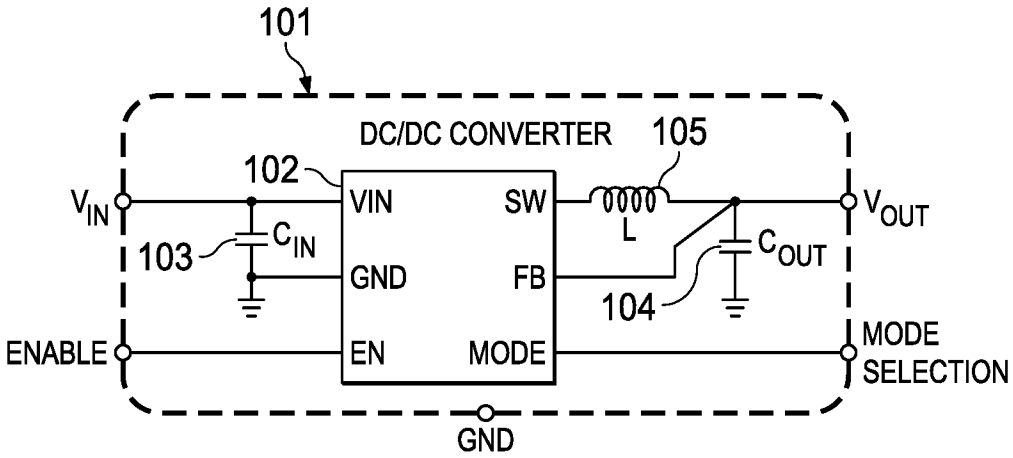
13. The method of claim 10 wherein the electronic bodies are selected from a group including power supply systems having a DC/DC converter, including a synchronous Buck converter, flyback converters, DC/DC boost converters, isolated converters, charge pumps, fuel gauges, power stages with drivers and load switches, voltage references, current references, and current sensors.

14. The method of claim 10 wherein the dielectric skin is coherent and free of voids.

15. The method of claim 14 wherein the dielectric skin is an insulating metal oxide layer.

16. The method of claim 12 wherein the external components include an inductor.

17. The method of claim 10 wherein the metal foil is suitable to oxidize uniformly and adhere to polymeric compounds.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DC/DC CONVERTER
105
102
VIN
SW
V_{IN}
C_{IN}
L
V_{OUT}
103
GND
FB
C_{OUT}
104
ENABLE
EN
MODE
MODE SELECTION
GND

FIG. 1

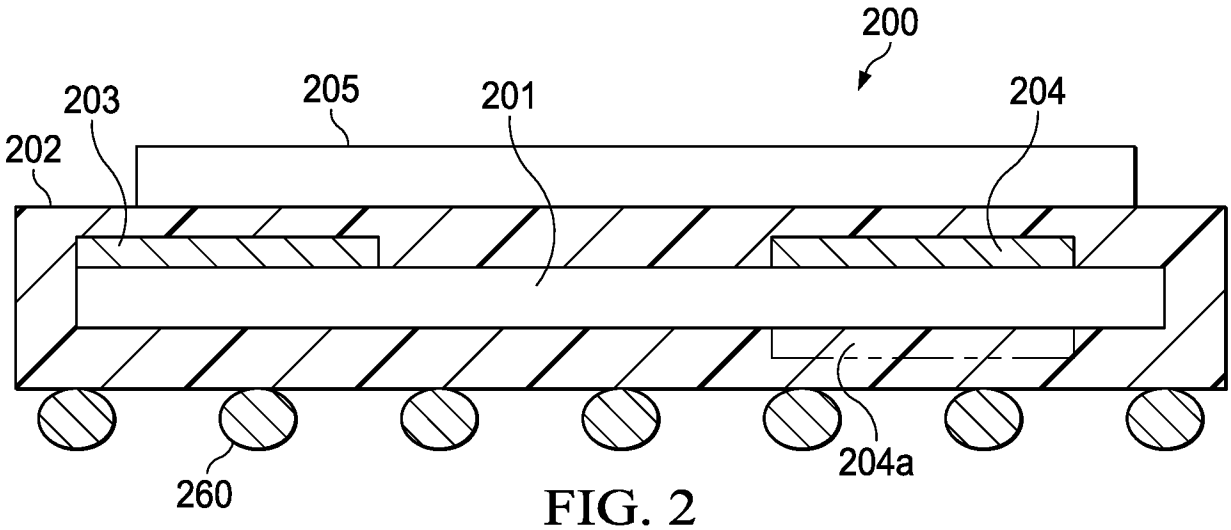
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FIG. 2

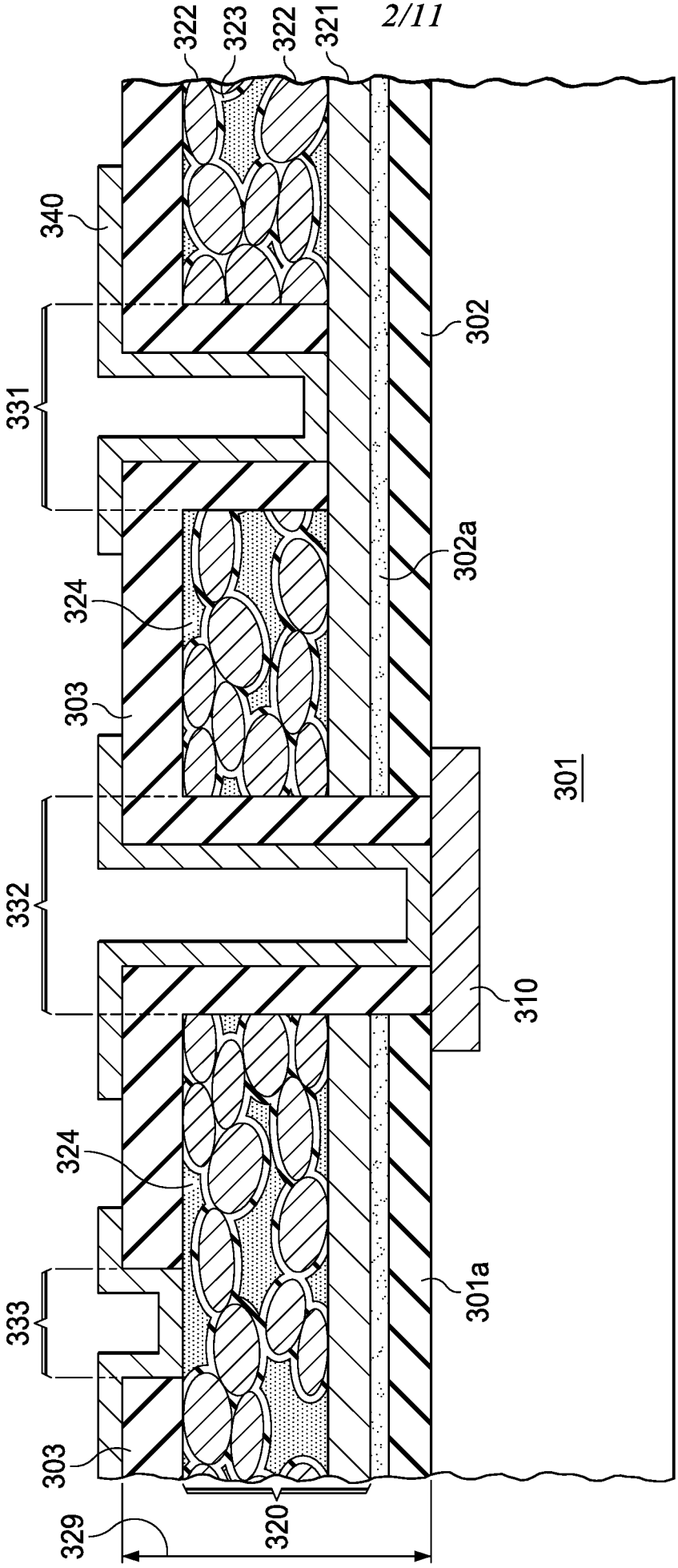
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FIG. 3

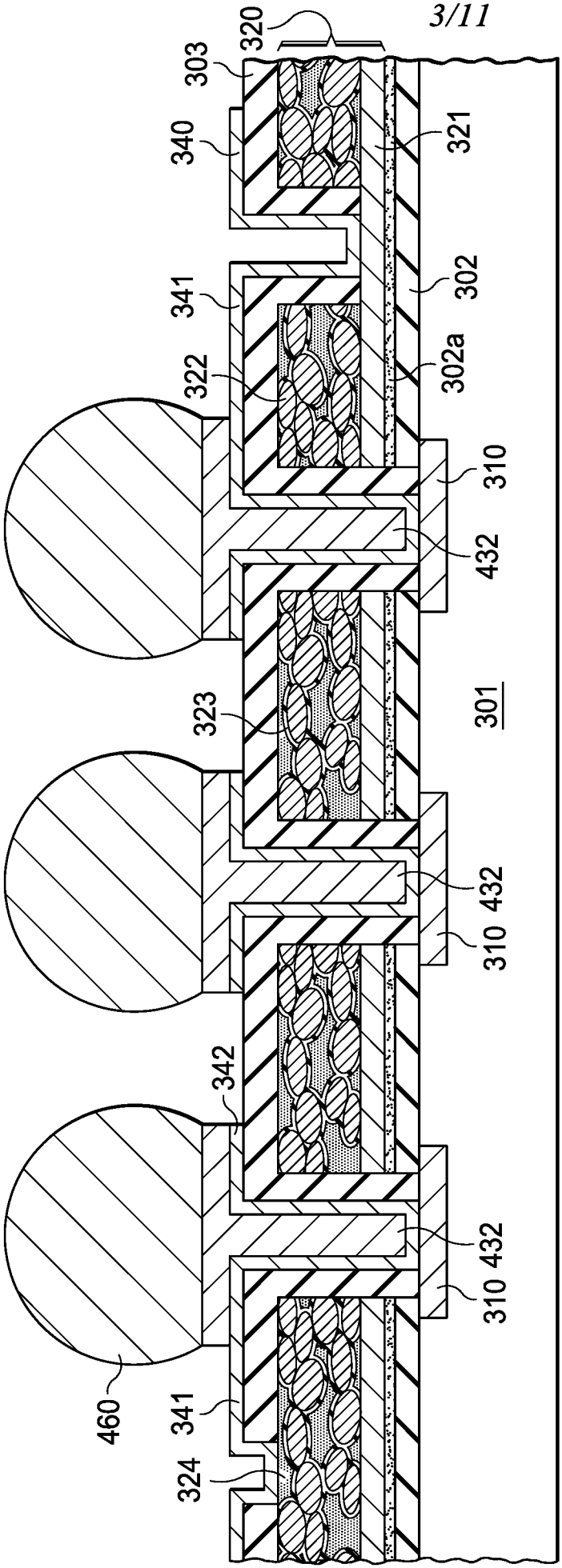
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FIG. 4A

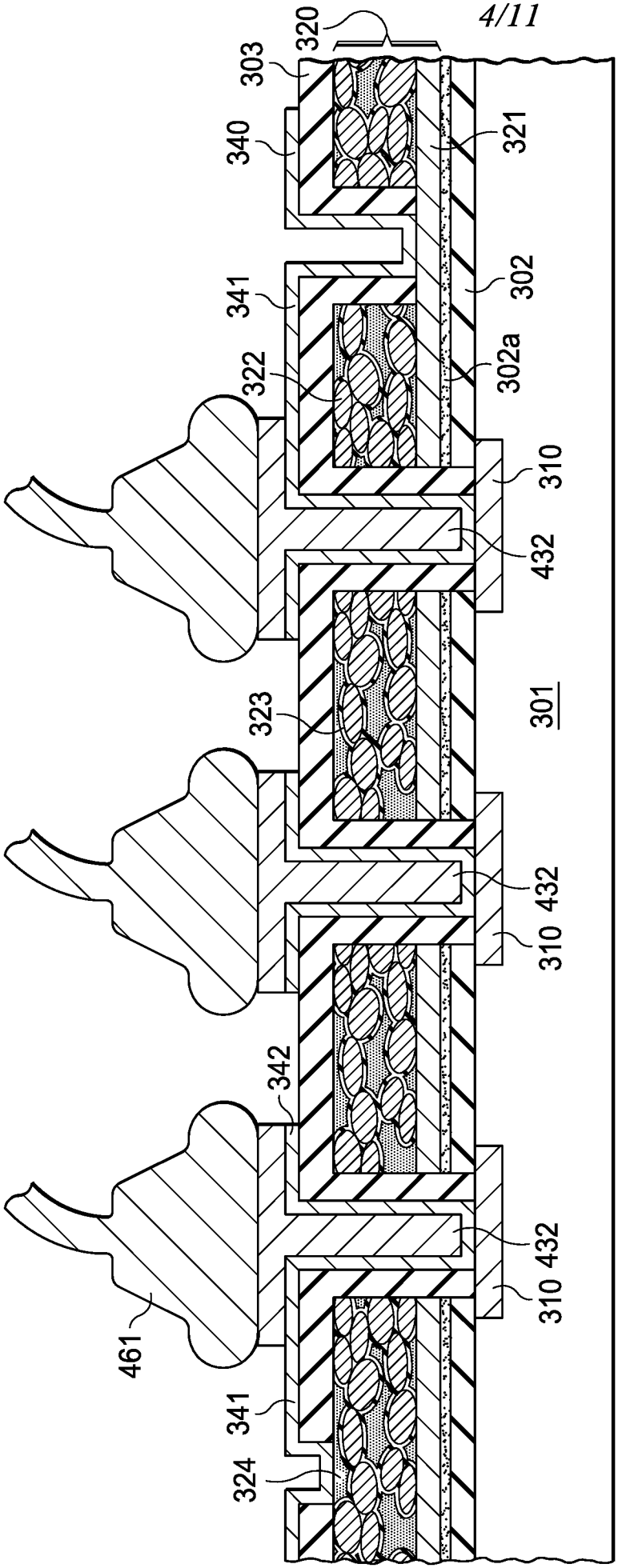
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FIG. 4B

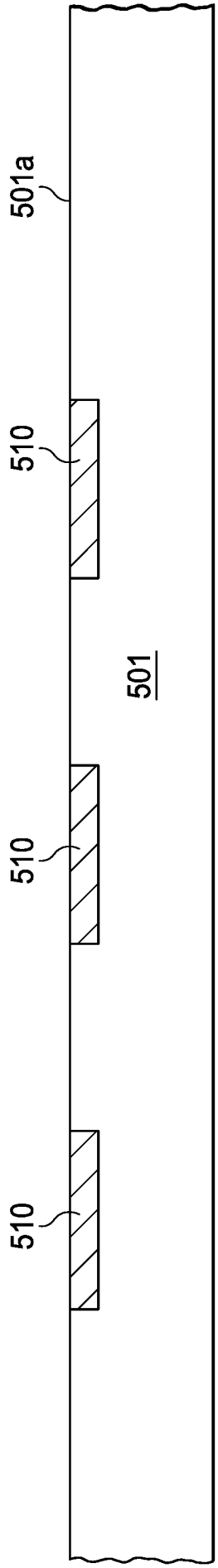
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FIG. 5A

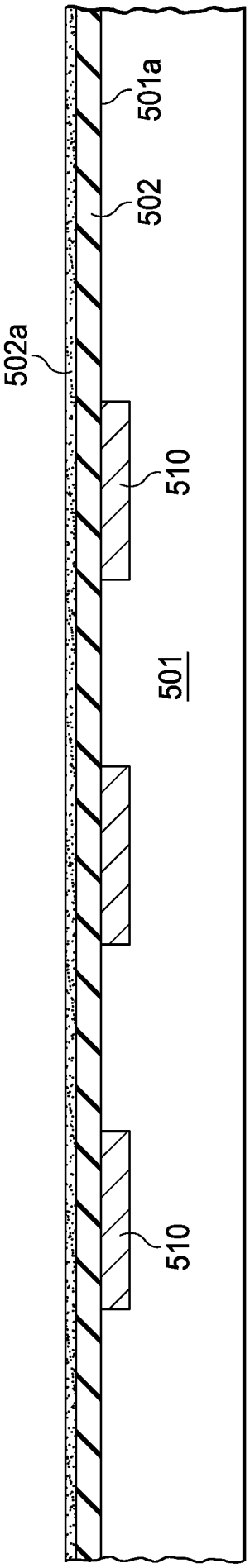
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FIG. 5B

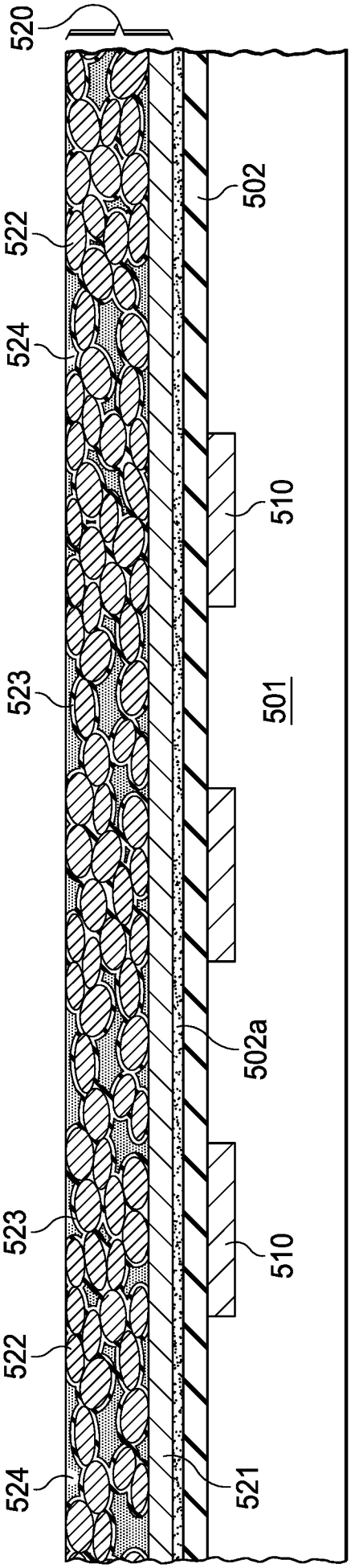
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FIG. 5C

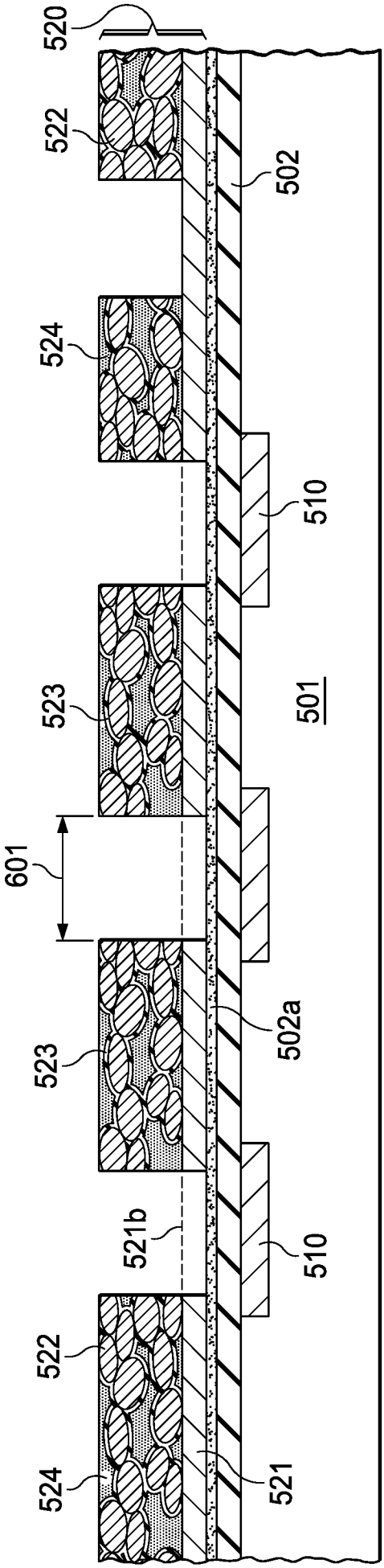
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FIG. 5D

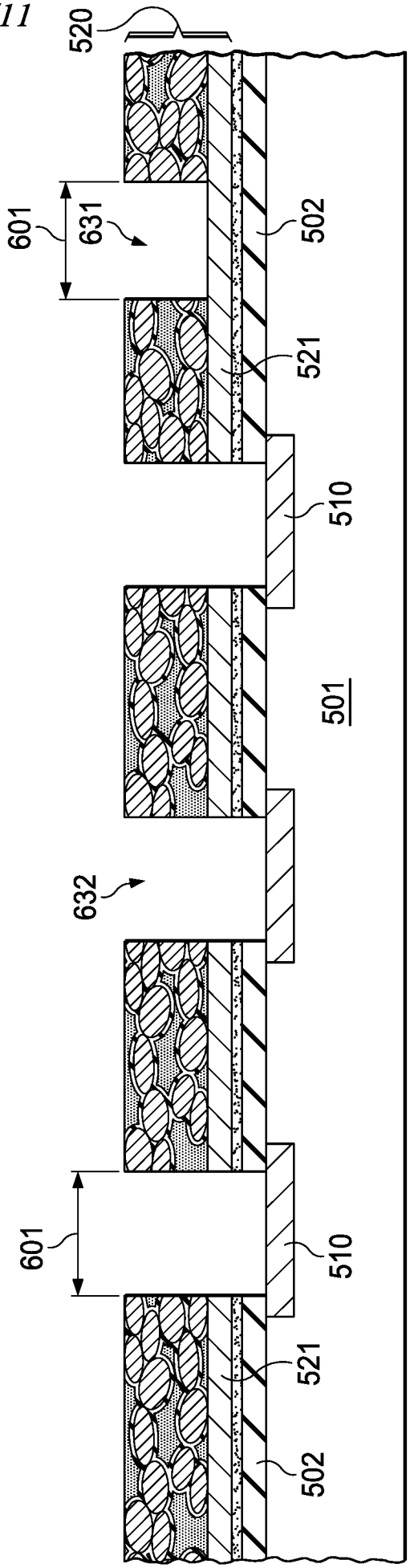
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FIG. 6A

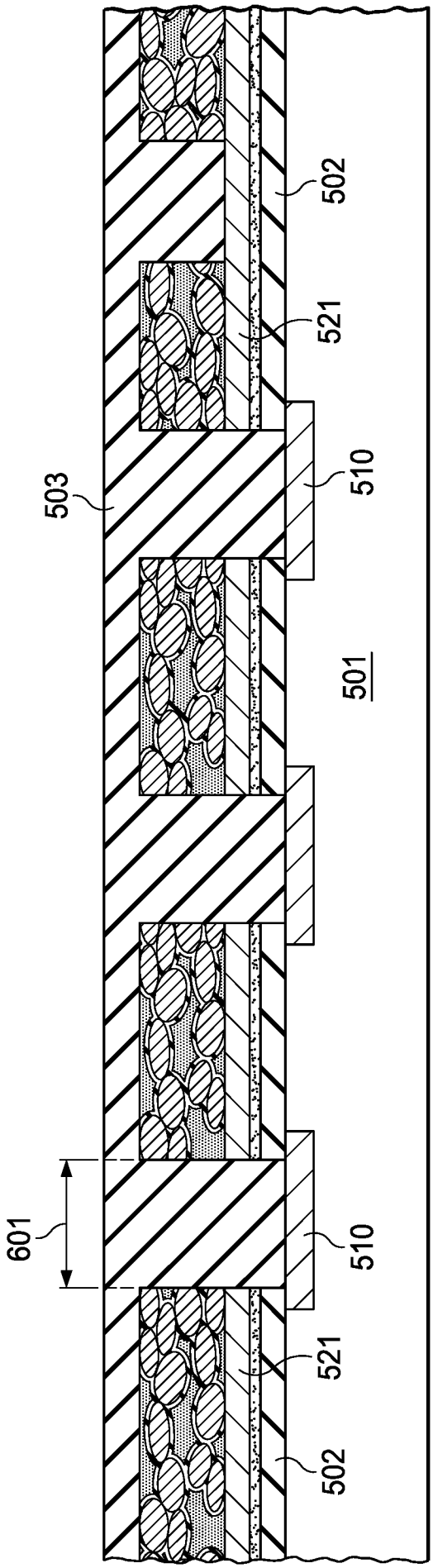
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FIG. 6B

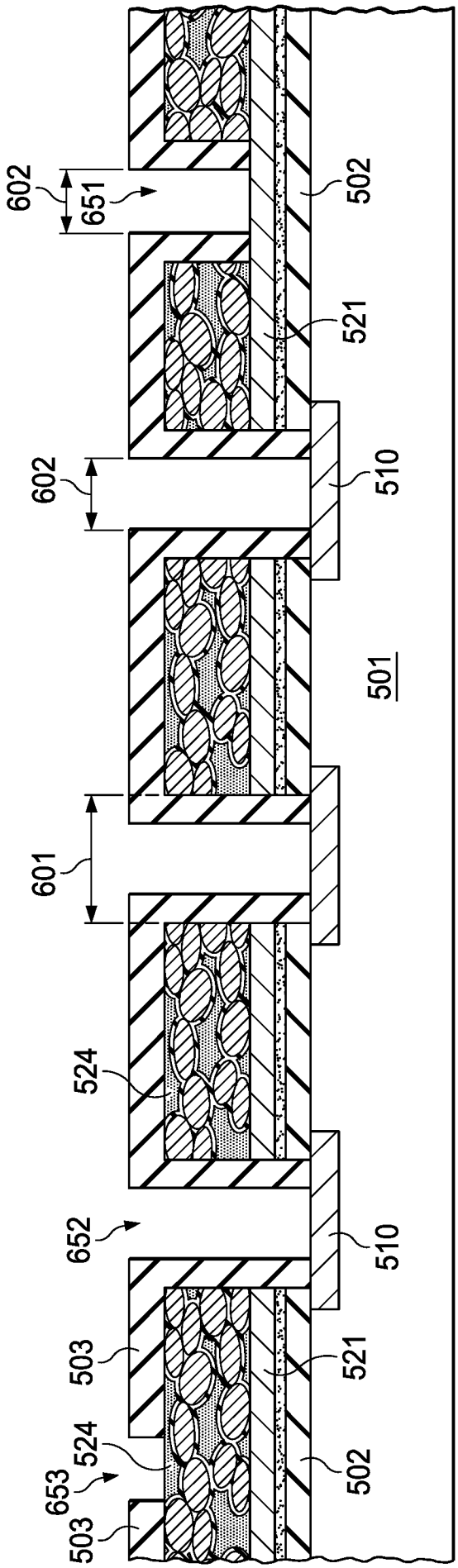
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FIG. 6C

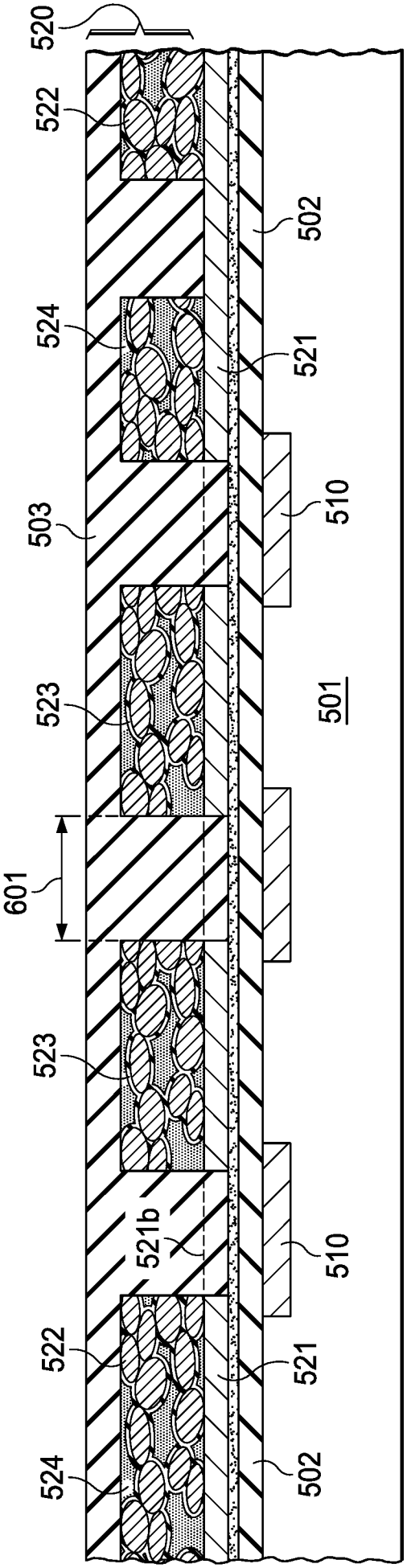
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FIG. 6D

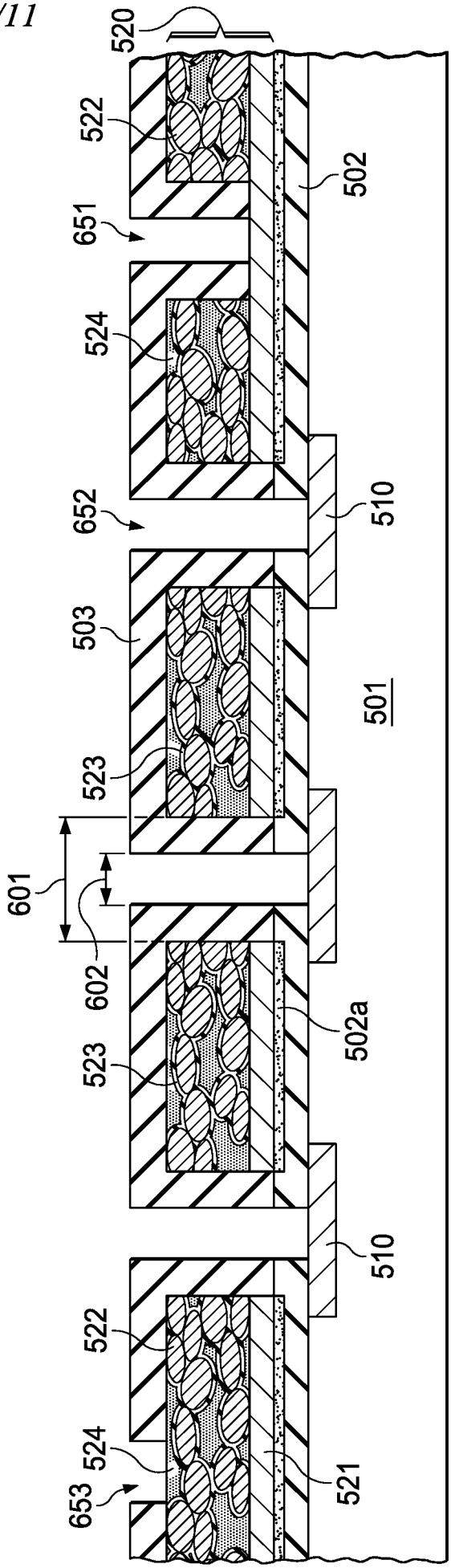
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FIG. 6E

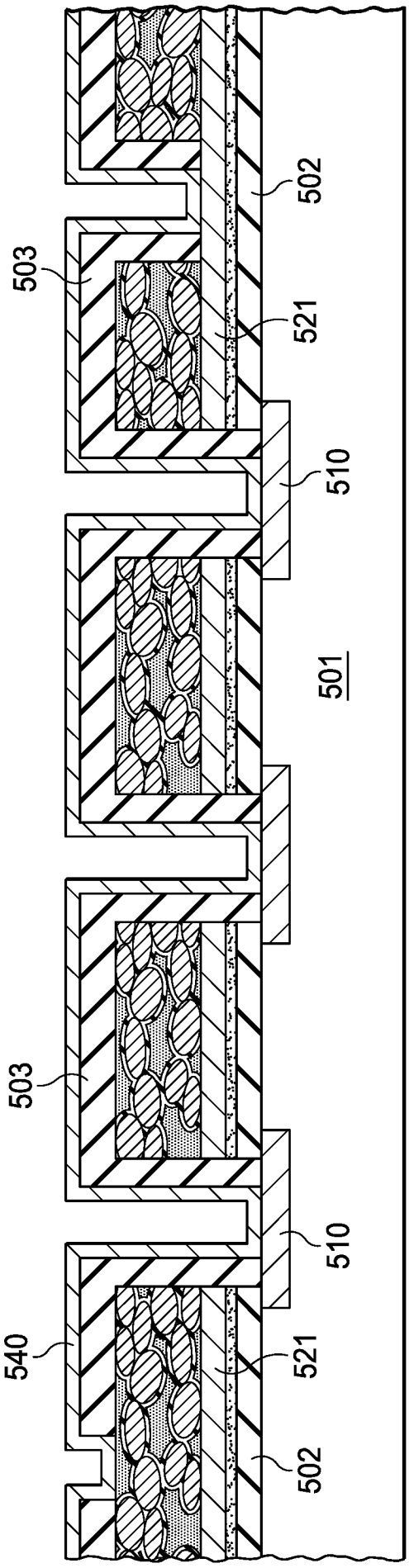
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FIG. 7A

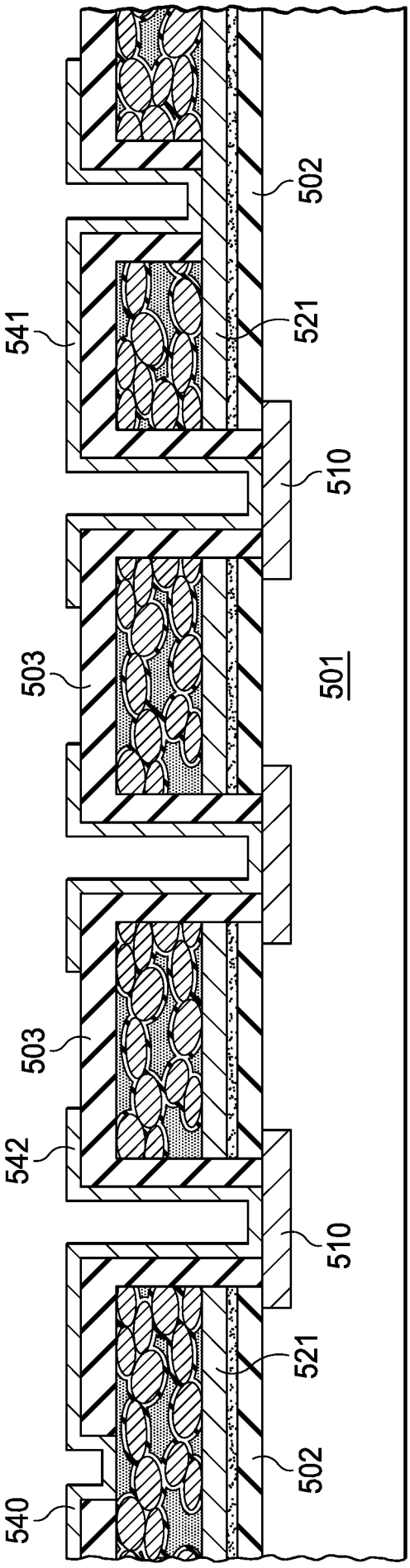
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FIG. 7B

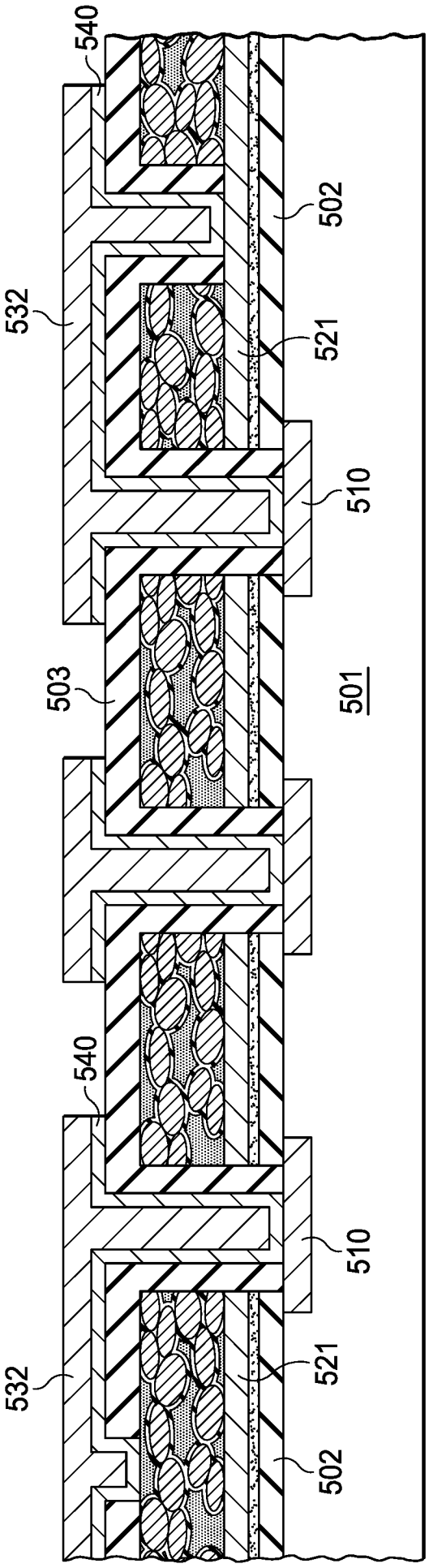
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FIG. 7C

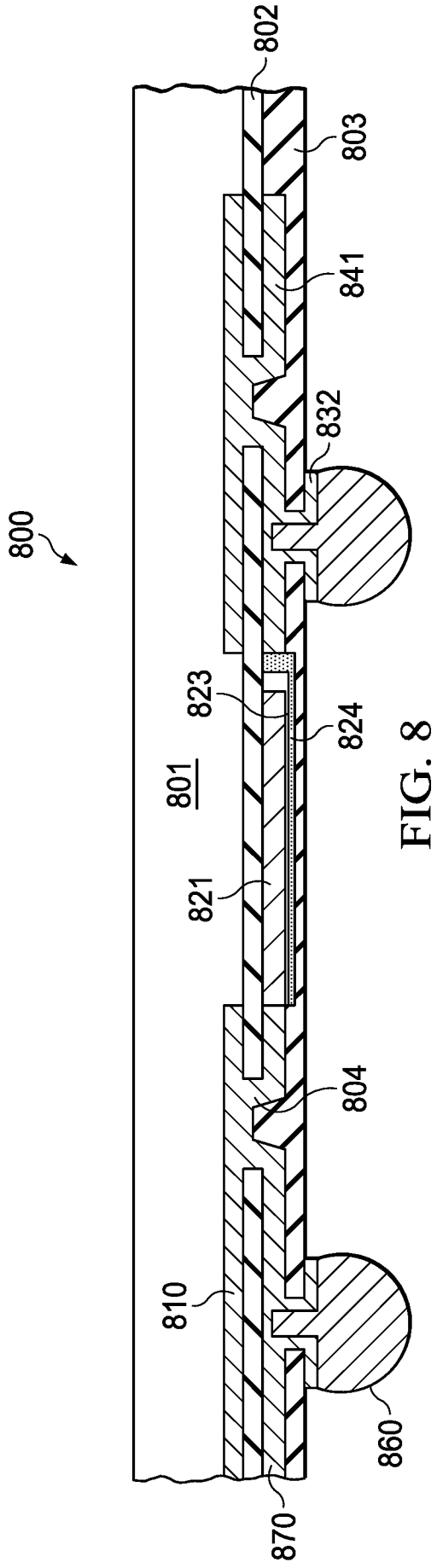
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FIG. 8

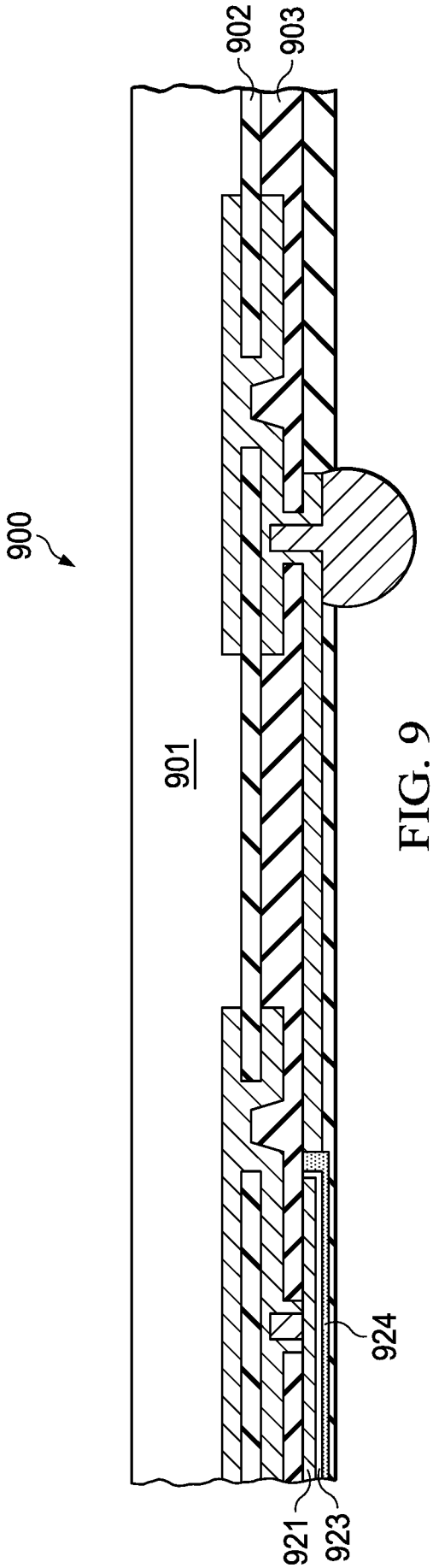
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FIG. 9

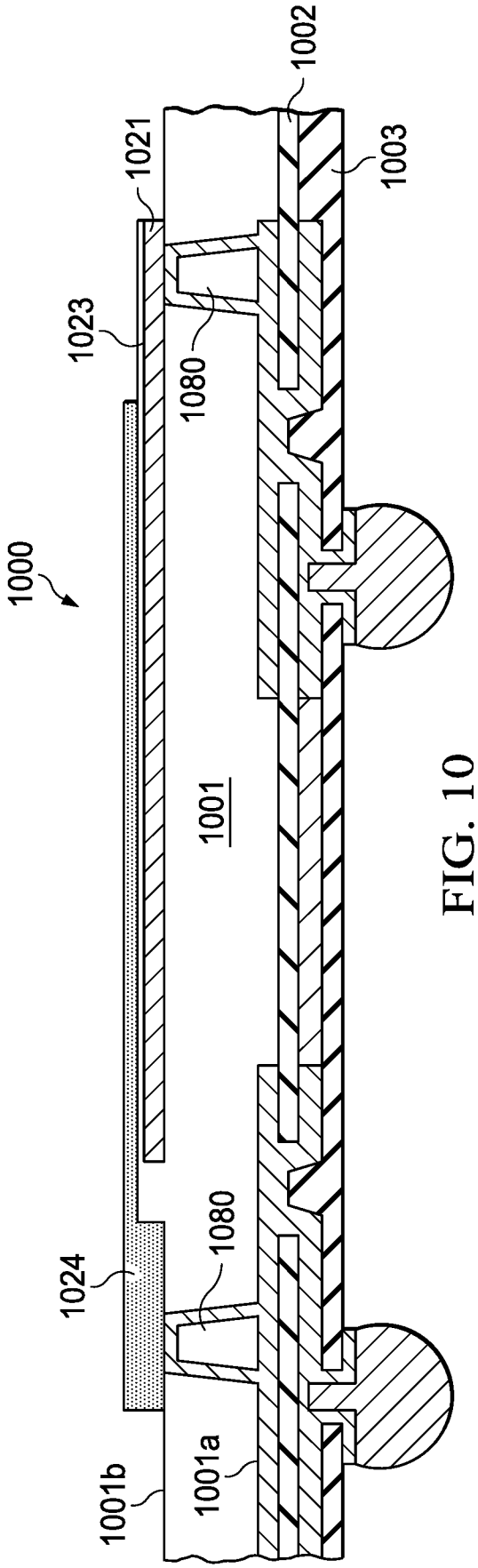
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FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2016/023817

A. CLASSIFICATION OF SUBJECT MATTER

H01L 51/00 *(2006.01)*
H01G 9/04 *(2006.01)*
H01L 29/94 *(2006.01)*
B82Y 40/00 *(2011.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01G 9/00, 9/004, 9/04, H01L 29/00, 29/66, 29/76, 29/86, 29/92, 29/94, H02M 3/00, 3/02, 3/04, 3/06, 3/07, H05K 1/00, 1/18, H01L 25/00, 27/00, 51/00, 21/47, 21/469, B82Y 40/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAPATIS, Espace, Espacenet, Google, KIPRIS, PAJ, PatSearch (RUPTO internal), RUABRU, RAUBU1, RUPAT, RUPAT-OLD, RUPTO, USPTO, Patentscope, Elibrary

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2009188219 A (FUJITSU LTD) 20.08.2009	1-17
A	WO 2008/139392 A2 (NXP B.V. et al.) 20.11.2008	1-17
A	US 6388207 B1 (INTEL CORPORATION) 14.05.2002	1-17
A	US 5825628 A (INTERNATIONAL BUSINESS MACHINES CORPORATION) 20.10.1998	1-17
A	US 6211542 B1 (RAMTRON INTERNATIONAL CORPORATION) 03.04.2001	1-17

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 May 2016 (30.05.2016)	07 July 2016 (07.07.2016)

Name and mailing address of the ISA/RU:	Authorized officer
Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	M. Adireeva Telephone No. (495)531-64-81