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(54) **Title**: MULTI-PATH ANALOG FRONT END AND ANALOG-TO-DIGITAL CONVERTER FOR A SIGNAL PROCESSING SYSTEM WITH LOW-PASS FILTER BETWEEN PATHS

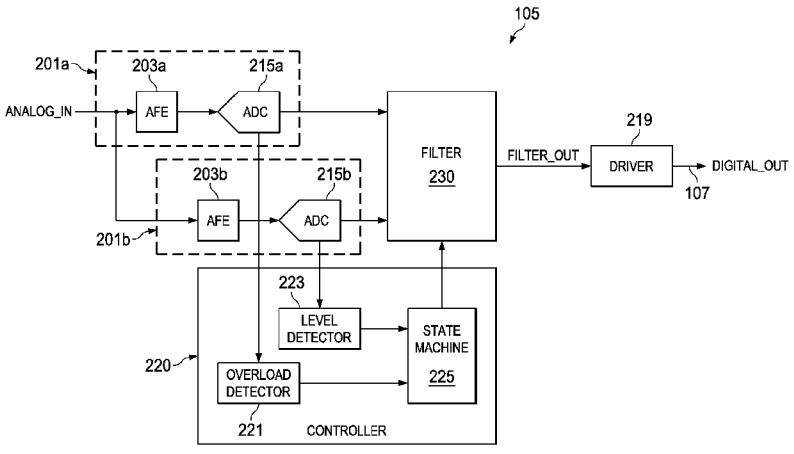

FIG. 2

(57) **Abstract**: In accordance with embodiments of the present disclosure, a processing system comprising may include a plurality of processing paths and a filter. The plurality of processing paths may include a first processing path and a second processing path, wherein the first processing path is configured to generate a first digital signal based on an analog input signal and the second processing path is configured to generate a second digital signal based on the analog input signal. The filter may have a corner frequency and may be configured to generate a filtered digital output signal combining spectral components of the first digital signal lower than the corner frequency and spectral components of the second digital signal higher than the corner frequency to generate a filtered digital signal.

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MULTI-PATH ANALOG FRONT END AND ANALOG-TO-DIGITAL CONVERTER FOR A SIGNAL PROCESSING SYSTEM WITH LOW-PASS FILTER BETWEEN PATHS

FIELD OF DISCLOSURE

The present disclosure relates in general to signal processing systems, and more particularly, to multiple path signal processing systems.

BACKGROUND

The use of multipath analog-to-digital converters (ADCs) and analog front ends (AFEs) (e.g., two or more path ADCs/AFEs) in electrical circuits is known. Example multipath ADCs and AFEs and use of them in multiple electrical circuit paths are disclosed in U.S. Patent No. 5,714,956 entitled "Process and System for the Analog-to-Digital Conversion of Signals" to Jahne et al. ("Jahne patent"), U.S. Patent No. 5,600,317 entitled "Apparatus for the Conversion of Analog Audio Signals to a Digital Data Stream" to Knoth et al. ("Knoth patent") and U.S. Patent No. 6,271,780 entitled "Gain Ranging Analog-to-Digital Converter with Error Correction" to Gong et al. ("Gong patent"). The use of multipath circuits may reduce noise as one path may be optimized for processing small amplitude signals (e.g., for processing low noise signals) while another circuit path with another set of ADC and AFE is optimized for large amplitude signals (e.g., allowing for higher dynamic range).

An example application for multipath ADCs/AFEs is use of it in a circuit for an audio system application, such as an audio mixing board or in a digital microphone system. Such an example application is disclosed in the Jahne patent. In designing a circuit with multipath ADCs/AFEs that are used in respective multiple circuit paths, a tradeoff may exist between allowing larger signal swing (e.g., to allow swing of a signal between larger scale amplitudes) and low noise. Furthermore, the multipath ADCs/AFEs may provide high dynamic range signal digitization, with higher dynamic range for a given input power, and lower overall area than would be possible with conventional means. In other words, by allowing a separate optimization for each type of signal (e.g., large and small signals) that is provided each respective path, multipath ADCs/AFEs

allow the overall circuit to burn less power, consume less area, and save on other such design costs.

Despite their advantages, existing multipath ADC/AFE approaches have disadvantages and problems. For example, many existing approaches have disadvantages related to transitioning and switching between the multiple paths, as such switching may not be smooth, leading to undesirable signal artifacts, especially in audio applications in which such artifacts may be perceptible to a listener of an audio device. As another example, a trend in electric circuits is to scale circuitry to the integrated circuit level. However, existing approaches to multipath AFEs/ADCs do not scale well to the integrated circuit level.

SUMMARY

In accordance with the teachings of the present disclosure, certain disadvantages and problems associated with implementation of multiple AFE/ADC paths may be reduced or eliminated.

In accordance with embodiments of the present disclosure, a processing system comprising may include a plurality of processing paths and a filter. The plurality of processing paths may include a first processing path and a second processing path, wherein the first processing path is configured to generate a first digital signal based on an analog input signal and the second processing path is configured to generate a second digital signal based on the analog input signal. The filter may have a corner frequency and may be configured to generate a filtered digital output signal combining spectral components of the first digital signal lower than the corner frequency and spectral components of the second digital signal higher than the corner frequency to generate a filtered digital signal.

In accordance with these and other embodiments of the present disclosure, a method may include processing an analog input signal with a first processing path to generate a first digital signal based on the analog input signal, processing the analog input signal with a second processing path to generate a second digital signal based on the analog input signal, and generating, with a filter having a corner frequency, a filtered digital output signal combining spectral components of the first digital signal lower than

the corner frequency and spectral components of the second digital signal higher than the corner frequency to generate a filtered digital signal.

Technical advantages of the present disclosure may be readily apparent to one having ordinary skill in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are explanatory examples and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 illustrates a block diagram of selected components of an example signal processing system, in accordance with embodiments of the present disclosure;

FIGURE 2 illustrates a block diagram of selected components of an integrated circuit for processing an analog signal to generate a digital signal, in accordance with embodiments of the present disclosure;

FIGURE 3 illustrates a block diagram of selected components of the integrated circuit of FIGURE 2 depicting selected components of example embodiments of analog front ends, analog-to-digital converters, and a filter, in accordance with embodiments of the present disclosure; and

FIGURE 4 illustrates a block diagram of selected components of the integrated circuit of FIGURE 2 depicting selected components of example embodiments of analog front ends, analog-to-digital converters, and another filter, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 illustrates a block diagram of selected components of an example signal processing system 100, in accordance with embodiments of the present disclosure. As shown in FIGURE 1, signal processing system 100 may include an analog signal source 101, an integrated circuit (IC) 105, and a digital processor 109. Analog signal source 101 may comprise any system, device, or apparatus configured to generate an analog electrical signal, for example an analog input signal ANALOG_IN. For example, in embodiments in which signal processing system 100 is a processing system, analog signal source 101 may comprise a microphone transducer.

Integrated circuit 105 may comprise any suitable system, device, or apparatus configured to process analog input signal ANALOG_IN to generate a digital output signal DIGITAL_OUT and condition digital output signal DIGITAL_OUT for transmission over a bus to digital processor 109. Once converted to digital output signal DIGITAL_OUT, the signal may be transmitted over significantly longer distances without being susceptible to noise as compared to an analog transmission over the same distance. In some embodiments, integrated circuit 105 may be disposed in close proximity with analog signal source 101 to ensure that the length of the analog line between analog signal source 101 and integrated circuit 105 is relatively short to minimize the amount of noise that can be picked up on an analog output line carrying analog input signal ANALOG_IN. For example, in some embodiments, analog signal source 101 and integrated circuit 105 may be formed on the same substrate. In other embodiments, analog signal source 101 and integrated circuit 105 may be formed on different substrates packaged within the same integrated circuit package.

Digital processor 109 may comprise any suitable system, device, or apparatus configured to process a digital output signal for use in a digital system. For example, digital processor 109 may comprise a microprocessor, microcontroller, digital signal processor (DSP), application specific integrated circuit (ASIC), or any other device configured to interpret and/or execute program instructions and/or process data, such as digital output signal DIGITAL_OUT.

Signal processing system 100 may be used in any application in which it is desired to process an analog signal to generate a digital signal. Thus, in some embodiments, signal processing system 100 may be integral to an audio device that

converts analog signals (e.g., from a microphone) to digital signals representing the sound incident on a microphone. As another example, signal processing system 100 may be integral to a radio-frequency device (e.g., a mobile telephone) to convert radio-frequency analog signals into digital signals.

FIGURE 2 illustrates a block diagram of selected components of integrated circuit 105, in accordance with embodiments of the present disclosure. As shown in FIGURE 2, integrated circuit 105 may include two or more processing paths 201a and 201b (which may be referred to herein individually as a processing path 201 and collectively as processing paths 201), each processing path 201 including a respective AFE 203 (e.g., AFE 203a, AFE 203b) and a respective ADC 215 (e.g., ADC 215a, ADC 215b). An AFE 203 may receive analog input signal ANALOG_IN via one or more input lines which may allow for receipt of a single-ended signal, differential signal, or any other suitable analog signal format and may comprise any suitable system, device, or apparatus configured to condition analog input signal ANALOG_IN for processing by ADC 215. Selected components for example embodiments of AFEs 203a and 203b are discussed in greater detail below with respect to FIGURE 3. The output of each AFE 203 may be communicated to a respective ADC 215 on one or more output lines.

An ADC 215 may comprise any suitable system, device, or apparatus configured to convert an analog signal received at its input, to a digital signal representative of analog input signal ANALOG_IN. ADC 215 may itself include one or more components (e.g., delta-sigma modulator, decimator, etc.) for carrying out the functionality of ADC 215. Selected components for the example embodiments of ADCs 215a and 215b are discussed in greater detail below with respect to FIGURE 3.

Filter 230 may comprise any suitable system, device, or apparatus configured to, based on a corner frequency of filter 230 control the relative contributions of the digital signals output by processing paths 201a and 201b to a digital output signal FILTER_OUT generated by filter 230. For example, as such corner frequency increases, the contribution of the digital signal output by processing path 201a may become less dominant in digital output signal FILTER_OUT while the contribution of the digital signal output by processing path 201b may become more dominant in digital output signal FILTER_OUT. Conversely, as such corner frequency decreases, the contribution of the digital signal output by processing path 201a may become more dominant in digital output signal

FILTER_OUT while the contribution of the digital signal output by processing path 201b may become less dominant in digital output signal FILTER_OUT. Thus, filter 230 may effectively serve as a combined filter which low-pass filters the digital signal output by processing path 201b and high-pass filters the digital signal output by processing path 201a and combines the filtered digital signals to generate digital output signal FILTER_OUT such that digital output signal FILTER_OUT includes the spectral components of digital signal output by processing path 201b lower than the corner frequency and includes the spectral components of digital signal output by processing path 201a higher than the corner frequency. Example embodiments of filter 230 are described in greater detail below with respect to FIGURES 3 and 4.

Controller 220 may comprise any suitable system, device, or apparatus for controlling a corner frequency of filter 230. In some embodiments, controller 220 may perform such control based on a magnitude of analog input signal ANALOG_IN or a signal derivative thereof. For example, controller 220 may include an overload detector 221 that may determine whether or not a signal derivative of analog input signal ANALOG_IN (e.g., a signal generated within ADC 215a) is likely to cause clipping or other distortion of digital output signal DIGITAL_OUT if a particular processing path (e.g., processing path 201a) is the dominant component of digital output signal DIGITAL_OUT. If clipping or other distortion of digital output signal DIGITAL_OUT is likely if the particular processing path (e.g., processing path 201a) is dominant, state machine 225 of controller 220 may generate a control signal to increase a corner frequency of filter 230 such that such processing path 201a becomes less dominant. To further illustrate, in some embodiments, processing path 201a may be a path adapted for low amplitudes of analog input signal ANALOG_IN and may thus have a high signal gain, while processing path 201b may be a path adapted for higher amplitudes of analog input signal ANALOG_IN and may thus have a lower signal gain. Thus, if analog input signal ANALOG_IN or a derivative thereof is greater than a threshold value indicative of a condition whereby digital output signal DIGITAL_OUT may experience clipping or other distortion if processing path 201a is dominant, overload detector 221 may detect such condition, and cause state machine 225 to generate a control signal to increase the corner frequency of filter 230 in order to make processing path 201a less dominant in digital output signal DIGITAL_OUT.

As another example, controller 220 may include a level detector 223 that may detect an amplitude of analog input signal ANALOG_IN or a signal derivative thereof (e.g., a signal generated within ADC 215b) and communicate a signal indicative of such amplitude to state machine 225. Responsive to the signal received from level detector 223, state machine 225 may generate a control signal communicated to filter 230. To illustrate, as analog input signal ANALOG_IN decreases from a relatively high amplitude to a lower amplitude, it may cross a threshold amplitude level whereby controller 220 may decrease the corner frequency of filter 230, in order to make the output of processing path 201a more dominant in digital output signal DIGITAL_OUT and the output of processing path 201b less dominant in digital output signal DIGITAL_OUT. In some embodiments, state machine 225 may wait for passage of a predetermined time after crossing of the threshold level before beginning to decrease the corner frequency. When decreasing the corner frequency, state machine 225 may do so continuously or in steps as the magnitude of the analog input signal decreases. Similarly, when below the threshold amplitude level, state machine 225 may cause the corner frequency to increase in response to increasing magnitude of the analog input signal.

Driver 219 may receive the filtered digital output signal FILTER_OUT generated by filter 230. Driver 219 may comprise any suitable system, device, or apparatus configured to condition such digital signal (e.g., encoding into Audio Engineering Society/European Broadcasting Union (AES/EBU), Sony/Philips Digital Interface Format (S/PDIF)), in the process generating conditioned digital output signal DIGITAL_OUT for transmission over a bus to digital processor 109. In FIGURE 2, the bus receiving conditioned digital output signal DIGITAL_OUT is shown as single-ended. In some embodiments, driver 219 may generate a differential conditioned digital output signal 107.

FIGURE 3 illustrates a block diagram of selected components of integrated circuit 105 depicting selected components of example embodiments of AFEs 203, ADCs 215, and filter 230, in accordance with embodiments of the present disclosure. As shown in FIGURE 3, analog front end 203a of processing path 201a may include a high-pass filter 302 configured to high-pass filter analog input signal ANALOG_IN to remove direct current offsets or biases, which are often particularly troublesome for high-gain amplifiers, and output such filtered signal to a non-inverting amplifier 304. Non-

inverting amplifier 304 may amplify analog input signal ANALOG_IN by a non-inverting gain and communicate such amplified analog signal to ADC 215a. In some embodiments, high-pass filter 302 may be formed on the same integrated circuit as one or more of AFE 203a, AFE 203b, ADC 215a, and ADC 215b. Because of the presence of high-pass filter 302 in processing path 201a, but not processing path 201b, processing paths 201 may each have a different frequency response to analog input signal ANALOG_IN.

Also as shown in FIGURE 3, analog front end 203b of processing path 201b may include an inverting amplifier 306 which may amplify analog input signal ANALOG_IN by an inverting gain and communicate such amplified analog signal to ADC 215b. In some embodiments, inverting amplifier 306 may be configured to apply a multiplicative gain of less than unity to analog input signal ANALOG_IN. By attenuating higher-amplitude signals, a greater dynamic range for analog input signal ANALOG_IN may be achieved, in spite of conventional wisdom that would generally dictate that signal loss should be avoided in a low-noise system. In these and other embodiments, although not depicted in FIGURE 3, inverting amplifier 306 may receive the output of high-pass filter 302 instead of the unfiltered analog input signal ANALOG_IN.

Although AFEs 203a and 203b are described above having a non-inverting gain and an inverting gain, respectively, each of processing paths 201 may have approximately the same cumulative gain. Those of skill in the art may appreciate that simply applying a digital gain with a negative sign in either of ADC 215a or ADC 215b will negate the opposite polarities of the gains of AFEs 203.

As depicted in FIGURE 3, each ADC 215 may include a respective delta-sigma modulator 308 (e.g., delta-sigma modulators 308a and 308b), a respective digital gain element 310 (e.g., digital gain elements 310a and 310b), and respective high-pass filters 312 (e.g., high-pass filters 312a and 312b). Each delta-sigma modulator 308 may be configured to modulate an analog signal into a corresponding digital signal. As known in the art, each delta-sigma modulator 308 may include a respective modulator 316 (e.g., modulators 316a, 316b) and a decimator 318 (e.g., decimators 318a, 318b). Each digital gain element 310 may apply a gain to a digital signal generated by its associated delta-sigma modulator 308. Each high-pass filter 312 may high-pass filter a digital signal generated by its associated digital gain element, to filter out any direct-current offsets

present in the digital signal. High-pass filter 312b may also compensate for high-pass filter 302 present in AFE 203a.

In addition, ADC 215a may comprise a latency matching element 314 to match any signal latencies between processing path 201a and processing path 201b, while ADC 215b may comprise a phase matching element 320 to account for any phase offset between processing path 201a and processing path 201b. For example, phase matching element 320 may dynamically compensate for any phase mismatch between processing paths 201a and 201b by varying a delay of at least one of processing path 201a and processing path 201b. In some embodiments, phase matching element 320 may comprise a high-pass filter.

In some embodiments, a magnitude of a gain of non-inverting amplifier 304 may be substantially larger than (e.g., significantly more than manufacturing tolerances, one or more orders of magnitude) a magnitude of a gain of inverting amplifier 306. In addition, in these and other embodiments, a magnitude of digital gain element 310b may be substantially larger than (e.g., significantly more than manufacturing tolerances, one or more orders of magnitude) a magnitude of a gain of digital gain element 310a. Consequently, in such embodiments, a first path gain equal to the product of the magnitude of the gain of inverting amplifier 306 and the magnitude of a gain of digital gain element 310b may be substantially equal (e.g., within manufacturing tolerances) to a second path gain equal to the product of the magnitude of gain of non-inverting amplifier 304 and the gain of digital gain element 310a. As a specific example, in some embodiments, the inverting gain of inverting amplifier 306 may be approximately -6 decibels, the non-inverting gain of non-inverting amplifier 304 may be approximately 20 decibels, the gain of digital gain element 310a may be approximately -26 decibels, and the gain of digital gain element 310b may be approximately 0 decibels.

Accordingly, each processing path 201 may be adapted to process a particular amplitude of analog input signal ANALOG_IN. For example, AFE 203a may be suited to process lower signal amplitudes, as non-inverting amplifier 304 may have a practically infinite input resistance, may have a relatively low level of input-referred noise as compared to inverting amplifier 306, and its larger gain may permit effective processing of smaller signals, but characteristics of AFE 203a may not be amenable to higher amplitudes. The high input resistance of non-inverting amplifier 304 may facilitate the

use of a smaller capacitor area for high-pass filter 302 (as compared to traditional approaches for implementing high-pass filters) and thus may permit integration of circuitry of high-pass filter 302 into the same integrated circuit as non-inverting amplifier 304, inverting amplifier 306, ADC 215a, and/or ADC 215b. In addition, the ability to integrate circuitry into a single integrated circuit may allow for centralized control of the stimuli for switching between processing paths 201 by controller 220, and may allow for more direct timing control of the actual switching and transitioning between processing paths 201. For example, because circuitry is integrated into a single integrated circuitry, level detector 223 may receive an output of delta-sigma modulator 308b as an input signal, rather than receiving an output of ADC 215b.

On the other hand, AFE 203b may be suited to process higher signal amplitudes, as its lower gain will reduce the likelihood of signal clipping, and may provide for greater dynamic range for analog input signal ANALOG_IN as compared to traditional approaches.

As described above with respect to FIGURE 2, controller 220 may comprise any suitable system, device, or apparatus for controlling a corner frequency of filter 230. For example, overload detector 221 that may determine whether or not a signal derivative of analog input signal ANALOG_IN (e.g., an output of a modulator 316a of delta-sigma modulator 308a, as shown in greater detail in FIGURE 3) is likely to cause clipping or other distortion of digital output signal DIGITAL_OUT if a particular processing path (e.g., processing path 201a) is the dominant component of digital output signal DIGITAL_OUT, and communicate a resulting signal to state machine 225, as described above with respect to FIGURE 2. As another example, controller 220 may include a level detector 223 that may detect an amplitude of analog input signal ANALOG_IN or a signal derivative thereof (e.g., an output of a decimator 316b of delta-sigma modulator 308b, as shown in greater detail in FIGURE 3) and communicate a signal indicative of such amplitude to state machine 225, as described above with respect to FIGURE 2.

Despite a designer's best efforts to match the first path gain and the second path gain, process variations, temperature variations, manufacturing tolerances, and/or other variations may lead to the first path gain and the second path gain being unequal. If switching between paths occurs when such path gains are unequal, signal artifacts may occur due to an instantaneous, discontinuous change in magnitude of the digital output

signal between two gain levels. For example, in audio signals, such artifacts may include human-perceptible "pops" or "clicks" in acoustic sounds generated from audio signals.

In some embodiments, in order to reduce or eliminate the occurrence of such artifacts when switching selection between the digital output signal of ADC 215a and the digital output signal of ADC 215b, and vice versa, controller 220 may program an additional gain into one or both of processing paths 201 to compensate for differences in the first path gain and second path gain. This additional gain factor may equalize the first path gain and the second path gain To illustrate, controller 220 may determine a scale factor indicative of the magnitude of difference (e.g., whether an intentional difference or unintentional mismatch) between the first path gain of processing path 201a and the second path gain of processing path 201b. The controller may determine the first path gain and the second path gain by comparing the digital output signals of each processing path to analog input signal ANALOG_IN or a derivative thereof. If such digital output signals have been filtered by a high-pass filter (e.g., high-pass filters 312), a direct-current offset between the signals may be effectively filtered out, which may be necessary to accurately compute the relative path gains. Controller 220 may determine the scale factor by calculating one of a root mean square average of the first path gain and the second path gain and a least mean squares estimate of the difference between the first path gain and the second path gain. Prior to switching selection between the first digital signal generated by ADC 215a and the second digital signal generated by ADC 215b (or vice versa), controller 220 may program an additional gain into one of processing paths 201 to compensate for the gain difference indicated by the scale factor. For example, controller 220 may calibrate one or both of the first path gain and the second path gain by applying a gain equal to the scale factor or the reciprocal of the gain factor (e.g., 1/gain factor), as appropriate. Such scaling may be performed by modifying one or both of digital gains 310. In some embodiments, controller 220 may apply the additional gain to the processing path 201 of the digital signal not selected as digital output signal DIGITAL_OUT. For example, controller 220 may apply the additional gain to processing path 201a when the digital signal of ADC 215b is selected as digital output signal DIGITAL_OUT and apply the additional gain to processing path 201b when the digital signal of ADC 215a is selected as digital output signal DIGITAL_OUT.

In some embodiments, the additional gain, once applied to a path gain of a processing path 201, may be allowed over a period of time to approach or "leak" to a factor of 1, in order to constrain the additional gain and compensate for any cumulative (e.g., over multiple switching events between digital signals of ADCs 215) bias in the calculation of the additional gain. Without undertaking this step to allow the additional gain to leak to unity, multiple switching events between paths may cause the gain factor to increase or decrease in an unconstrained manner as such additional gain, if different than unity, affects the outputs of the multiple paths and thus affects the calculation of the scaling factor.

As shown in FIGURE 3, an example filter 230 may include a combiner 331, a low-pass filter 333, a combiner 335, and a cross-fader 327. Combiner 331 may receive a respective digital signal from each of processing paths 201 and determine a difference between the two digital signals. The difference may be filtered by a low-pass filter 333 to generate a filtered difference. In some embodiments, low-pass filter 333 may have a variable corner frequency, wherein the variable corner frequency is controlled based on a control signal generated by and communicated from a controller 220, as described above. The filtered difference output by low-pass filter 333 may be summed by combiner 335 with the digital signal output by one of the processing paths (e.g., processing path 201a) to generate a digital output signal.

A crossfader 327 may receive the digital output signal received from combiner 335 and the digital signal output by one of the processing paths (e.g., processing path 201b) and output filtered digital output signal FILTER_OUT comprising a weighted average of the digital output signal and the digital signal output by processing path 201b based on a control signal generated by and communicated from a controller 220. In some embodiments, crossfader 327 may not be present, in which case the digital output signal generated by combiner 335 may be communicated to driver 219 as filtered digital output signal FILTER_OUT.

In some embodiments, to reduce or eliminate artifacts from occurring when varying a corner frequency to adjust the relative dominance of processing paths 201 in digital output signal DIGITAL_OUT, controller 220 and crossfader 327 may be configured to transition, continuously or in steps, filtered digital output signal FILTER_OUT from a first digital signal (e.g., output of processing path 201b) to the

digital output signal generated by combiner 335, or vice versa, such that during such transition, digital output signal DIGITAL_OUT is a weighted average of the first digital signal and the digital output signal. For example, for decreases in the magnitude of the analog input signal, crossfader 327 may transition from the first digital signal to the digital output signal generated by combiner 335 such that a weight of the digital output signal relative to the weight of the first digital signal increases during the transition. Similarly, for increases in the magnitude of the analog input signal, crossfader 327 may transition from the digital output signal generated by combiner 335 to the first digital signal such that a weight of the first digital signal relative to the weight of the digital output signal increases during the transition.

FIGURE 4 illustrates a block diagram of selected components of integrated circuit 105A depicting a different example filter 230A, in accordance with embodiments of the present disclosure. Integrated circuit 105A depicted in FIGURE 4 may be similar to that of integrated circuit 105 of FIGURE 3, and thus only the differences between integrated circuit 105A depicted in FIGURE 4 and integrated circuit 105 of FIGURE 3 are discussed below. In particular, in integrated circuit 105A, filter 230 of FIGURE 3 is replaced with example filter 230A. As shown in FIGURE 4, example filter 230A may include a low-pass filter 433, combiners 431, 435, and 437, and delay blocks 441 and 443. As shown in FIGURE 4, low-pass filter 433 may generate a filtered difference signal by low-pass filtering a difference (e.g., generated by combiner 431) between the digital output signal generated by processing path 201b and a filtered digital signal based on the digital output signal generated by processing path 201a, as delayed by delay block 441. A corner frequency of low-pass filter 433 may be controlled by controller 220, as described elsewhere in this disclosure. Such filtered difference signal may be integrated by combiner 435 and delay block 443, which as depicted in FIGURE 4, may operate as a signal integrator to generate an integrated filtered difference signal. The integrated filtered difference signal may then be combined with the digital output signal generated by processing path 201a to generate the filtered digital signal. Crossfader 327 may receive the filtered digital signal received from combiner 437 and the digital signal output by processing path 201b and output filtered digital output signal FILTER_OUT comprising a weighted average of the filtered digital signal and the digital signal output

by processing path 201b based on a control signal generated by and communicated from a controller 220.

The presence of filter 230 (or 230A) may be advantageous so as to decrease a minimum time needed to switch between selection of processing paths 201 as the dominant processing path contributing to filtered digital output signal FILTER_OUT. For example, high-pass filters in each of processing paths 201 (e.g., high-pass filter 302 and phase matching element 320) may contribute to differences between processing paths 201, particularly in response to impulsive sound events in analog input signal ANALOG_IN. Due to such differences, and in the absence of filter 230 to frequency modulate between the paths, switching between processing paths 201 may lead to audio artifacts unless switching between paths is delayed. By including filter 230 in integrated circuit 105, such delay may be decreased over embodiments not having filter 230.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the disclosure and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present disclosure have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

WHAT IS CLAIMED IS:

1. A processing system comprising:

a plurality of processing paths including a first processing path and a second processing path, wherein:

the first processing path is configured to generate a first digital signal based on an analog input signal; and

the second processing path is configured to generate a second digital signal based on the analog input signal; and

a filter having a corner frequency and configured to generate a filtered digital output signal combining spectral components of the first digital signal lower than the corner frequency and spectral components of the second digital signal higher than the corner frequency to generate a filtered digital signal.

2. The processing system of Claim 1, wherein the filter comprises:

a low-pass filter configured to low-pass filter a difference between the second digital signal and the first digital signal to generate a filtered difference in accordance with a corner frequency of the low-pass filter; and

a combiner configured to sum the second digital signal and the filtered difference to generate a filtered digital signal, wherein the filtered digital output signal is based on the digital output signal.

3. The processing system of Claim 2, further comprising a controller configured to:

set the corner frequency based on a magnitude of the analog input signal; and

in response to an increase in the magnitude of the analog input signal, transition continuously or in steps the filtered digital output signal between the digital output signal and the second digital signal during a duration of time, and such that during such transition, the filtered digital output signal is a weighted average of the second digital signal and the filtered digital signal wherein a weight of the second digital signal relative to a weight of the filtered digital signal increases during the transition.

4. The processing system of Claim 2, further comprising a controller configured to:

set the corner frequency based on a magnitude of the analog input signal; and

in response to a decrease in the magnitude of the analog input signal, transition continuously or in steps the filtered digital output signal between the second digital signal and the filtered digital signal during a duration of time, and such that during such transition, the filtered digital output signal is a weighted average of the second digital signal and the filtered digital signal wherein a weight of the filtered digital signal relative to a weight of the second digital signal increases during the transition.

5. The processing system of Claim 1, further comprising a controller configured to set the corner frequency based on a magnitude of the analog input signal.

6. The processing system of Claim 5, wherein the controller is configured to increase the corner frequency in response to an increase in the magnitude of the analog input signal.

7. The processing system of Claim 5, wherein the controller is configured to decrease the corner frequency in response to a decrease in the magnitude of the analog input signal.

8. The processing system of Claim 5, wherein the controller is configured to decrease the corner frequency in response to:

a decrease in the magnitude of the analog input signal below a predetermined threshold; and

passage of a predetermined duration of time after the decrease in the magnitude below the predetermined threshold.

9. The processing system of Claim 8, wherein the controller is configured to decrease the corner frequency continuously or in steps as the magnitude of the analog input signal decreases.

10. The processing system of Claim 1, wherein:

the first processing path comprises a first analog front end and a first digital processing subsystem having a first analog-to-digital converter, wherein the first analog front end is configured to amplify the analog input signal in order to generate a first amplified analog signal and the first analog-to-digital converter is configured to convert the first amplified analog signal into the first digital signal; and

the second processing path comprises a second analog front end and a second digital processing subsystem having a second analog-to-digital converter, wherein the second analog front end is configured to amplify the analog input signal to generate a second amplified analog signal and the second analog-to-digital converter is configured to convert the second amplified analog signal into the second digital signal, and further wherein a magnitude of the gain of the second analog front end is substantially larger than a magnitude of a gain of the first analog front end.

11. The processing system of Claim 10, wherein:

the first analog front end includes an inverting amplifier configured to amplify an analog input signal to generate the first amplified analog signal; and

the second analog front end includes a non-inverting amplifier configured to amplify the analog input signal to generate a second amplified analog signal.

12. The processing system of Claim 11, wherein a magnitude of gain of the inverting amplifier is substantially less than a unity gain.

13. The processing system of Claim 11, wherein the second analog front end includes a high-pass filter configured to filter the analog input signal prior to the analog input signal being amplified by the non-inverting amplifier.

14. The processing system of Claim 11, wherein a magnitude of a gain of the non-inverting amplifier is substantially larger than a magnitude of a gain of the inverting amplifier.

15. The processing system of Claim 1, wherein the processing system is an audio processing system, and the analog input signal and the digital output signal are each an audio signal.

16. The processing system of Claim 1, wherein the filter comprises:

a low-pass filter configured to low-pass filter a difference between the second digital signal and a filtered digital signal based on the first digital signal to generate a filtered difference in accordance with a corner frequency of the low-pass filter;

an integrator configured to integrate the filtered difference to generate an integrated filtered difference; and

a combiner configured to sum the first digital signal and the integrated filtered difference to generate the filtered digital signal;

wherein the filtered digital output signal is a weighted average of the second digital signal and the filtered digital signal.

17. A method comprising:

processing an analog input signal with a first processing path to generate a first digital signal based on the analog input signal;

processing the analog input signal with a second processing path to generate a second digital signal based on the analog input signal; and

generating, with a filter having a corner frequency, a filtered digital output signal combining spectral components of the first digital signal lower than the corner frequency and spectral components of the second digital signal higher than the corner frequency to generate a filtered digital signal.

18. The method of Claim 17, wherein generating the filtered digital output signal comprises:

a low-pass filtering a difference between the second digital signal and the first digital signal to generate a filtered difference in accordance with a corner frequency of the low-pass filter; and

summing the second digital signal and the filtered difference to generate a filtered digital signal, wherein the filtered digital output signal is based on the digital output signal.

19. The method of Claim 18, further comprising:

setting the corner frequency based on a magnitude of the analog input signal; and

in response to an increase in the magnitude of the analog input signal, transitioning continuously or in steps the filtered digital output signal between the digital output signal and the second digital signal during a duration of time, and such that during such transition, the filtered digital output signal is a weighted average of the second digital signal and the filtered digital signal wherein a weight of the second digital signal relative to a weight of the filtered digital signal increases during the transition.

20. The method of Claim 18, further comprising:

setting the corner frequency based on a magnitude of the analog input signal; and

in response to a decrease in the magnitude of the analog input signal, transitioning continuously or in steps the filtered digital output signal between the second digital signal and the filtered digital signal during a duration of time, and such that during such transition, the filtered digital output signal is a weighted average of the second digital signal and the filtered digital signal wherein a weight of the filtered digital signal relative to a weight of the second digital signal increases during the transition.

21. The method of Claim 17, further comprising setting the corner frequency based on a magnitude of the analog input signal.

22. The method of Claim 21, further comprising increasing the corner frequency in response to an increase in the magnitude of the analog input signal.

23. The method of Claim 21, further comprising decreasing the corner frequency in response to a decrease in the magnitude of the analog input signal.

24. The method of Claim 21, further comprising decreasing the corner frequency in response to:

a decrease in the magnitude of the analog input signal below a predetermined threshold; and

passage of a predetermined duration of time after the decrease in the magnitude below the predetermined threshold.

25. The method of Claim 24, further comprising decreasing the corner frequency continuously or in steps as the magnitude of the analog input signal decreases.

26. The method of Claim 17, wherein:

the first processing path comprises a first analog front end and a first digital processing subsystem having a first analog-to-digital converter, wherein the first analog front end is configured to amplify the analog input signal in order to generate a first amplified analog signal and the first analog-to-digital converter is configured to convert the first amplified analog signal into the first digital signal; and

the second processing path comprises a second analog front end and a second digital processing subsystem having a second analog-to-digital converter, wherein the second analog front end is configured to amplify the analog input signal to generate a second amplified analog signal and the second analog-to-digital converter is configured to convert the second amplified analog signal into the second digital signal, and further wherein a magnitude of the gain of the second analog front end is substantially larger than a magnitude of a gain of the first analog front end.

27. The method of Claim 26, wherein:

the first analog front end includes an inverting amplifier configured to amplify an analog input signal to generate the first amplified analog signal; and

the second analog front end includes a non-inverting amplifier configured to amplify the analog input signal to generate a second amplified analog signal.

28. The method of Claim 27, wherein a magnitude of gain of the inverting amplifier is substantially less than a unity gain.

29. The method of Claim 27, wherein the second analog front end includes a high-pass filter configured to filter the analog input signal prior to the analog input signal being amplified by the non-inverting amplifier.

30. The method of Claim 27, wherein a magnitude of a gain of the non-inverting amplifier is substantially larger than a magnitude of a gain of the inverting amplifier.

31. The method of Claim 17, wherein the processing system is an audio processing system, and the analog input signal and the digital output signal are each an audio signal.

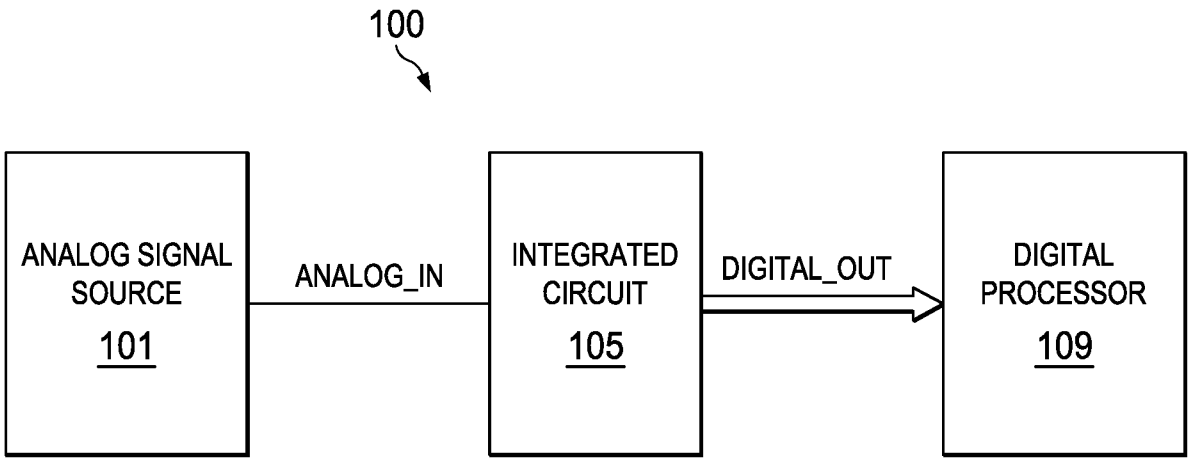
32. The method of Claim 17, wherein generating the filtered digital output signal comprises:

low-pass filtering a difference between the second digital signal and a filtered digital signal based on the first digital signal to generate a filtered difference in accordance with a corner frequency of the low-pass filter;

integrating the filtered difference to generate an integrated filtered difference; and

summing the first digital signal and the integrated filtered difference to generate the filtered digital signal;

wherein the filtered digital output signal is a weighted average of the second digital signal and the filtered digital signal.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DIGITAL_OUT
DIGITAL PROCESSOR
109

FIG. 1

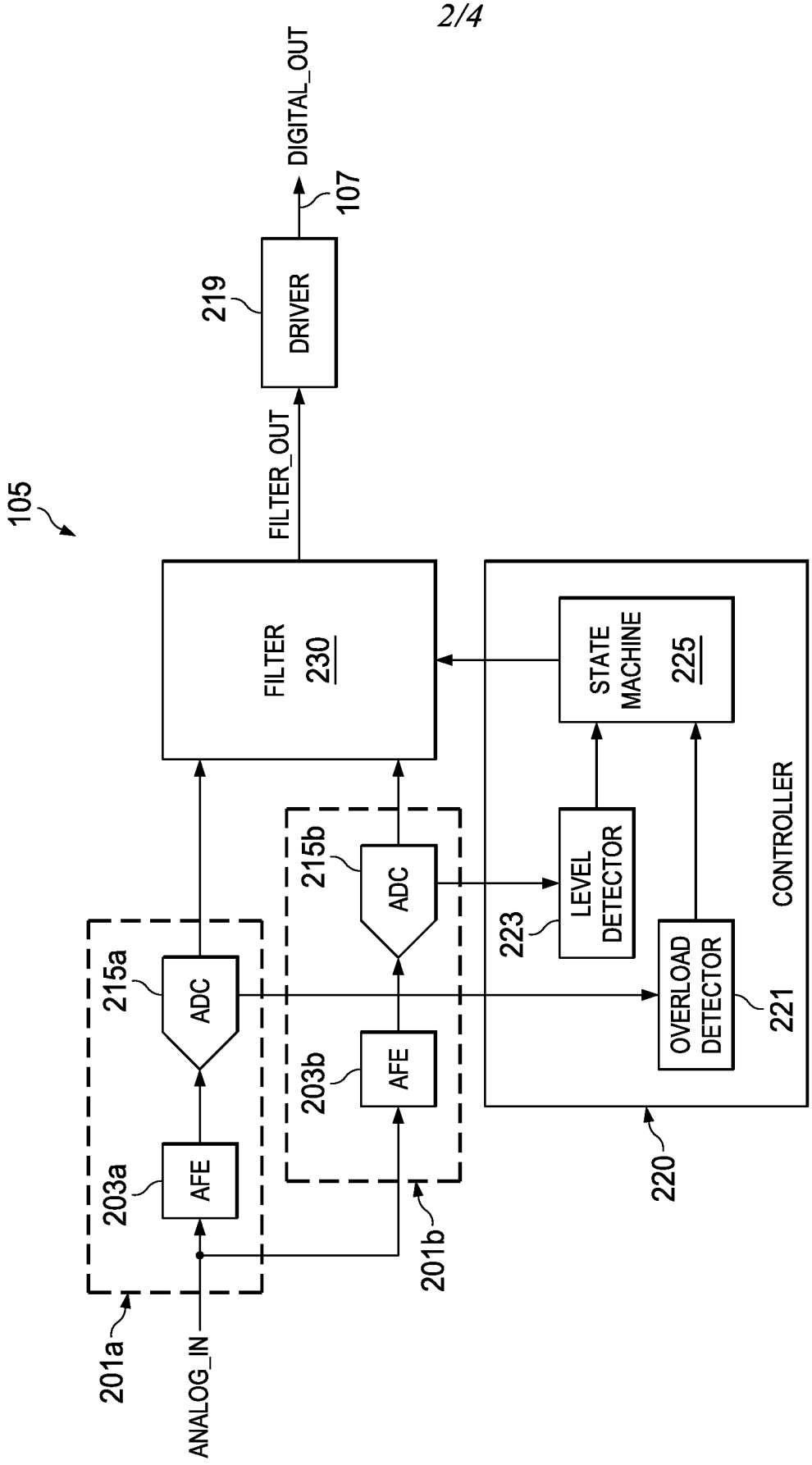
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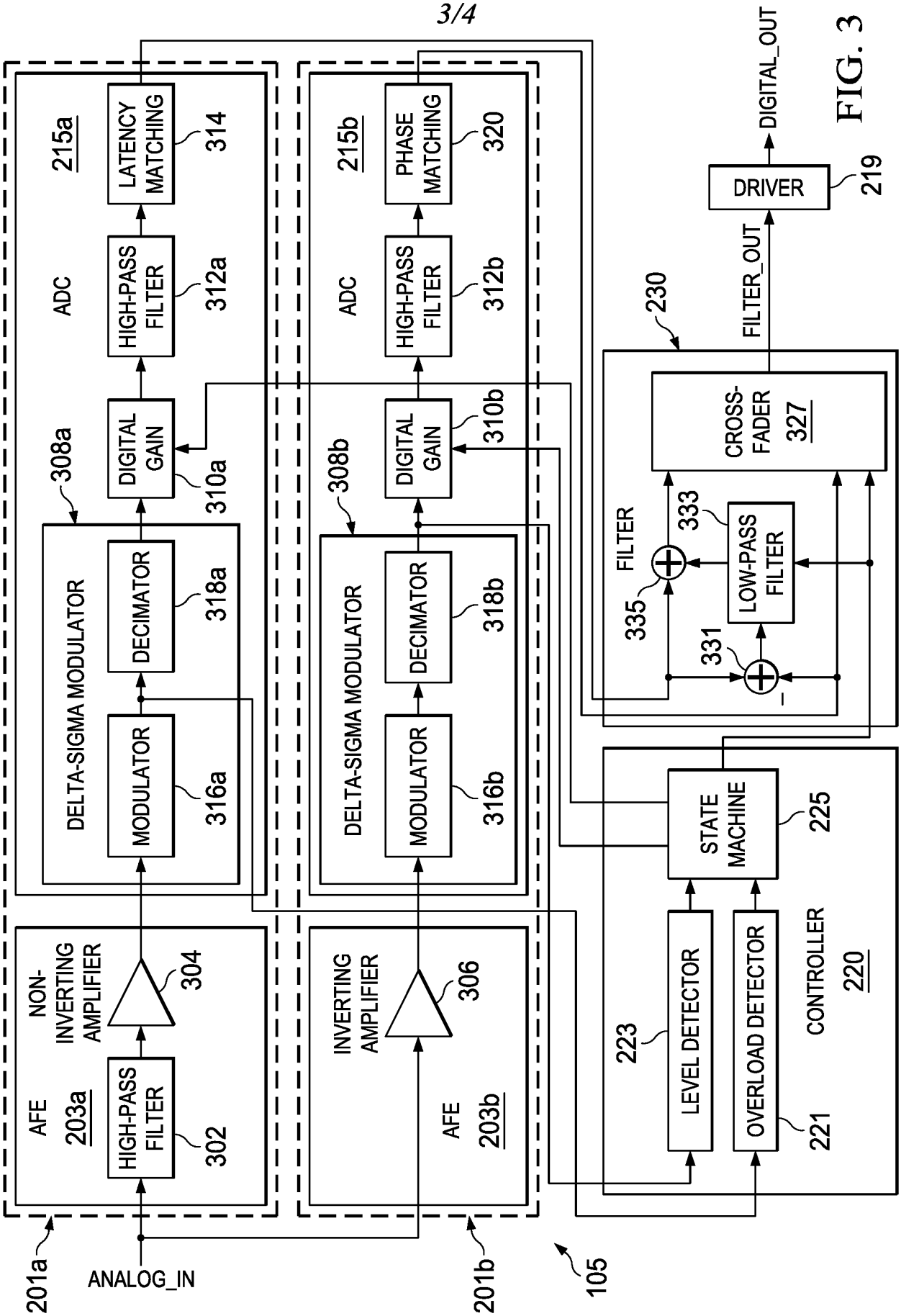
FIG. 2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MODULATOR
316a
DECIMATOR
318a
DIGITAL GAIN
310a
HIGH-PASS FILTER
312a
LATENCY MATCHING
314
ADC
215b
DELTA-SIGMA MODULATOR
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310b
HIGH-PASS FILTER
312b
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230
CROSS-FADER
327
FILTER
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LOW-PASS FILTER
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331
FILTER_OUT
DRIVER
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DIGITAL_OUT
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LEVEL DETECTOR
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OVERLOAD DETECTOR
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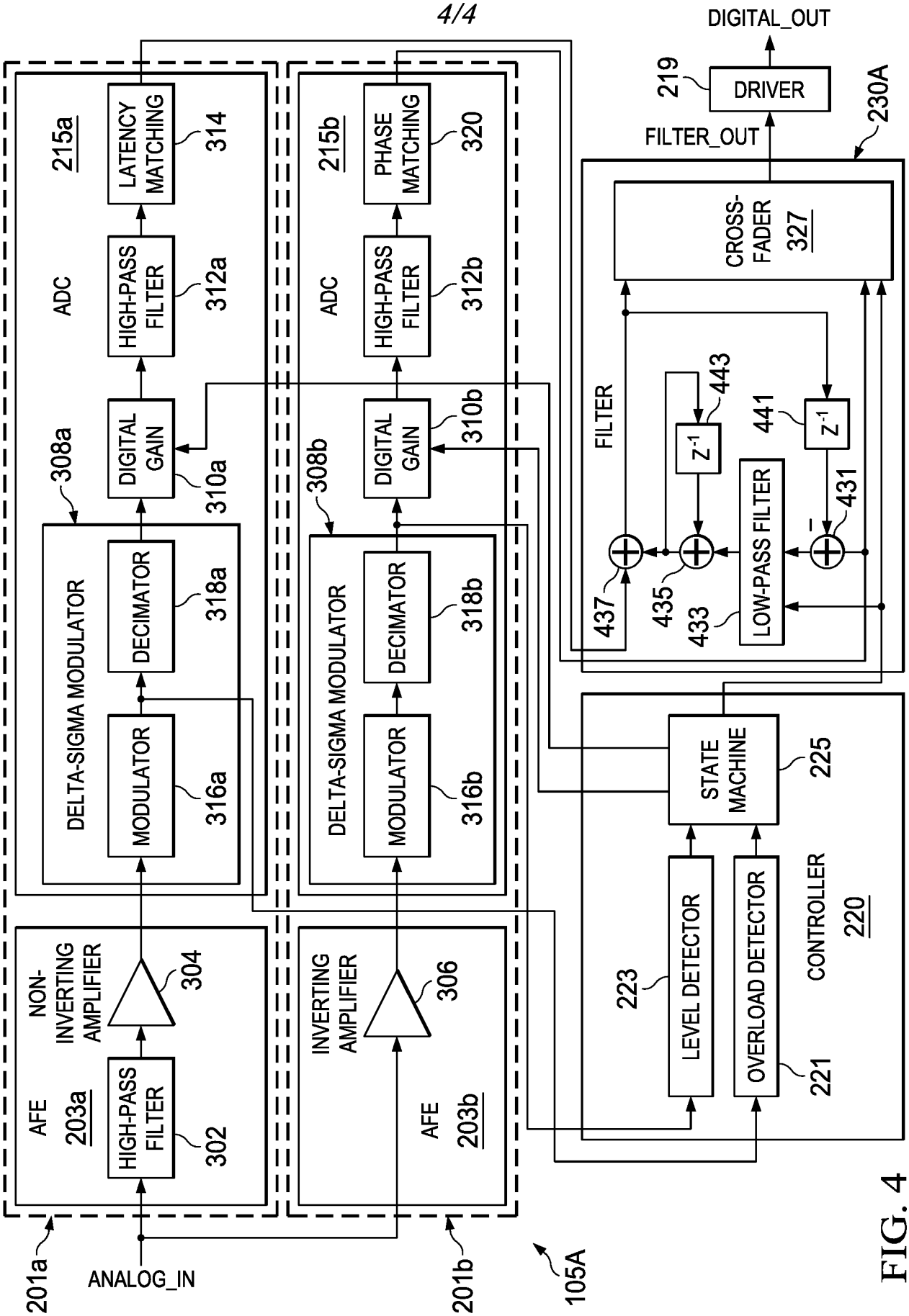
201a
ANALOG_IN
201b
105

FIG. 3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CONTROLLER 220
LEVEL DETECTOR 223
OVERLOAD DETECTOR 221
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LATENCY MATCHING 314
HIGH-PASS FILTER 312a
DIGITAL GAIN 310a
308a
DELTA-SIGMA MODULATOR
DECIMATOR 318a
MODULATOR 316a
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HIGH-PASS FILTER 302
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308b
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DECIMATOR 318b
MODULATOR 316b
AFE 203b
INVERTING AMPLIFIER 306
201a
ANALOG_IN
201b
105A

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/065134

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/12 H03M1/18 H03M3/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 207 264 A1 (AKG ACOUSTICS GMBH [AT]) 14 July 2010 (2010-07-14) paragraph [0014] paragraphs [0016] - [0025] figures 1,2 -----	1-32
X	US 9 071 267 B1 (SCHNEIDER EDMUND MARK [US] ET AL) 30 June 2015 (2015-06-30) column 6 - column 12 column 6, lines 45-50 column 11, lines 12-20 figures 2,3 -----	1,10-15, 17, 26-29,31

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 March 2017	15/03/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Rocha, Daniel

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/065134

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2010176980 A1	15-07-2010
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		US 9071268 B1	30-06-2015
		US 9148164 B1	29-09-2015
		US 9525940 B1	20-12-2016