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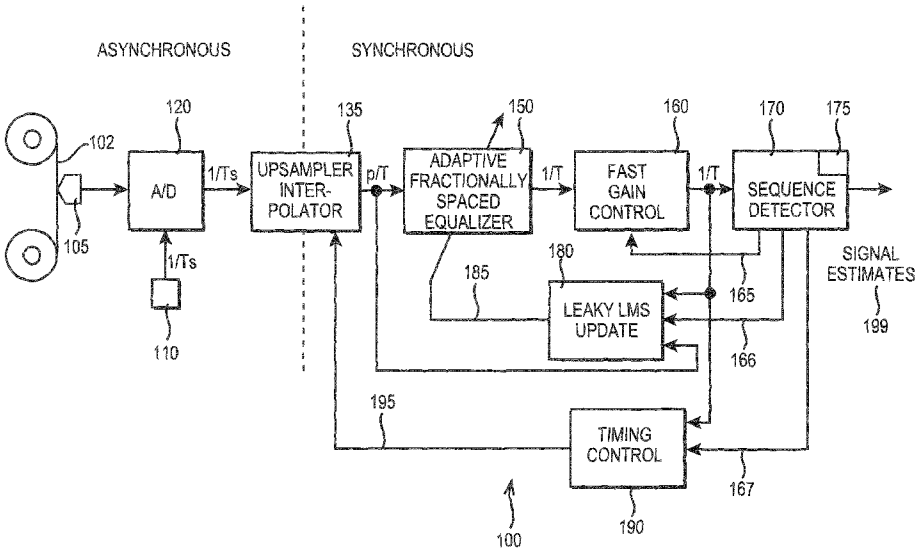
(54) Title: READ CHANNEL APPARATUS FOR ASYNCHRONOUS OVERSAMPLING, SYNCHRONOUS FRACTIONALLY SPACED EQUALIZATION AND DIGITAL GAIN CONTROL



(57) Abstract: A read channel receiver apparatus and a method are disclosed. The read channel receiver chain comprises an analog to digital converter which asynchronously samples at a fixed rate an analog signal formed by reading a data track, where that data track was written to a data storage medium at a symbol rate, and an upsampler and interpolator interconnected with the analog to digital converter. The receiver further comprises a fractionally-spaced equalizer, where the interpolator provides a signal to the fractionally-spaced equalizer at an interpolation rate greater than the symbol rate. The fractionally-spaced equalizer forms a synchronous equalized signal. The receiver further comprises a digital gain control module interconnected with the fractionally-spaced equalizer, and a sequence detector outputing a maximum likelihood signal sequence.

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READ CHANNEL APPARATUS FOR ASYNCHRONOUS OVERSAMPLING, SYNCHRONOUS FRACTIONALLY SPACED EQUALIZATION AND DIGITAL GAIN CONTROL

Field Of The Invention

The invention relates to an apparatus and method to read information encoded to a data storage medium using asynchronous sampling and synchronous equalization.

Background Of The Invention

Automated media storage libraries are known for providing cost effective access to large quantities of stored media. Generally, media storage libraries include a large number data storage media. In certain implementations, such an information storage and retrieval system comprises a plurality of storage slots on which are stored portable data storage media. The typical data storage media comprises one or more magnetic tapes, one or more optical disks, one or more magnetic hard disks, electronic storage media, and the like.

As the amount of information written to a data storage medium increases, it becomes more difficult to read that information, and to distinguish valid data signals from noise. What is needed is an apparatus and method to reliably read information encoded to a data storage medium.

Summary of the Invention

This invention provides a read channel and method using that read channel. The read channel comprises an analog to digital converter which asynchronously samples an analog signal formed by reading a data track, where that data track was written to a data storage medium at a symbol rate, or a rate specified by the write equalization process, and an interpolator interconnected with the analog to digital converter.

The read channel further comprises a fractionally-spaced equalizer, where the interpolator provides an interpolated signal to the fractionally-spaced equalizer at an interpolation rate, where that interpolation rate is greater than the symbol rate. The fractionally-spaced equalizer forms a synchronous symbol-spaced equalized signal. The read channel further comprises a gain control module interconnected with the fractionally-spaced equalizer, and a sequence detector interconnected with the gain control module.

Brief Description of the Drawings

The invention will be better understood from a reading of the following detailed description taken in conjunction with the drawings in which like reference designators are used to designate like elements, and in which:

FIG. 1A is a block diagram showing a first embodiment of Applicants' read channel;

FIG. 1B is a block diagram showing a second embodiment of Applicants' read channel

FIG. 2 is a block diagram showing Applicants' fractionally-spaced equalizer;

FIG. 3 is a block diagram showing a third embodiment of Applicants' read channel;

FIG. 4 is a block diagram showing a fourth embodiment of Applicants' read channel;

FIG. 5 is a block diagram showing a fifth embodiment of Applicants' read channel;

FIG. 6 is a block diagram showing a sixth embodiment of Applicants' read channel;

FIG. 7 is a flow chart summarizing certain steps in Applicants' method; and

FIG. 8 is a flow chart summarizing additional steps in Applicants' method.

Detailed Description Of The Preferred Embodiments

eferring to the illustrations, like numerals correspond to like parts depicted in the figures. An example of the invention will be described as embodied in a read channel assembly used to read information from a magnetic tape. The following description of a method to adjust the amplitudes of a plurality of digital signals is not meant, however, to limit the invention to either reading information from a magnetic tape, or to data processing applications, as the invention herein can be applied to reading information from an information storage medium in general.

An example of the invention comprises an apparatus, i.e. a read channel, and a method using that apparatus, to read information from an information storage medium by asynchronously sampling an analog signal comprising information encoded to the storage medium, and then synchronously equalizing those samples. Applicants' method is summarized in FIGs. 7 and 8.

Referring now to FIGs. 1A and 7, in step 710 the method supplies a read channel comprising an analog to digital converter, an interpolator interconnected with the analog to digital converter, a fractionally-spaced equalizer interconnected with the interpolator, a gain control module interconnected with the fractionally-spaced equalizer, and a sequence detector interconnected with the gain control module.

In step 720, read head 105 generates an analog signal from reading data encoded on magnetic tape 102 as tape 102 moves past read head 105. In certain embodiments, the data written to tape 102 was encoded at a first rate, i.e. the symbol rate. In certain embodiments, the first rate was specified by the write equalization process. Read head 105 provides that analog signal to analog to digital converter 120. Fixed frequency clock 110 provides timing signals to A/D converter 120.

In step 730, the analog signal is sampled asynchronously with respect to the clock used to write the data symbols. It is found that asynchronous sampling channels allow reduced implementation complexity because a digital phase-locked loop replaces the analog phase locked oscillator used in synchronous sampling. As a result, many problems caused by the variations in analog components are eliminated. Where (N) data tracks are being read using synchronous sampling, (N) analog PLOs are needed, i.e. one analog PLO per channel.

In contrast, where (N) data tracks are being read using an apparatus and method embodying the invention, one system-wide, free running clock 110 controls the sampling of the (N) analog signals to obtain the asynchronous samples for the (N) channels. In this case, the need for (N) analog PLOs is avoided and (N) digital phase-lock loops are used. Increasing the sampling rate with respect to the data rate reduces errors due to aliasing.

In step 740, the asynchronously sampled signals are provided to upsampler / interpolator 135 which computes synchronous samples by interpolation at a designated upsampling rate. In step 750, upsampler / interpolator 135 provides synchronous samples to fractionally-spaced equalizer 150. Thus, the apparatus and method employ asynchronous signal sampling in combination with synchronous fractionally-spaced equalization.

Referring now to FIGs. 1A, 2, and 7, in step 750 fractionally-spaced equalizer 150 receives at a rate p/T samples from sampler / interpolator 135. The value of p is an integer greater than or equal to 2. The

equalizer weights w1, w2, w3..wL tap the equalizer delay line every q * T/p delay elements starting before the first delay element.

In step 760, fractionally-spaced equalizer 150 accepts p input samples per data symbol interval T and produces one sample every T. The equalizer weights w1, w2, w3 . . . wL are also updated every symbol interval T. Thus, the output sample rate is 1/T, while the input sample rate is p/T. The weight-updating occurs at the output rate 1/T. The output from equalizer 150 comprises the ideal distortion-free channel-output signal, and distortion due to residual intersymbol interference from misequalization, and colored noise.

Fractionally-spaced equalizer 150 provides synchronous, equalized samples to gain control module 160 at a rate of 1/T. In step 770, the gain control module 160 adjusts the gain of the equalized samples.

In step 780, the gain-adjusted, synchronous, equalized samples are processed by sequence detector 170, wherein detector 170 is configured to produce signal estimates based on detector decisions, e.g., signal estimates from data decisions along a survivor sequence of the maximum likelihood sequence detector. As those skilled in the art will appreciate, the sequence detector provides those detected data symbols to a decoder which decodes those data symbols.

Referring now to FIGs. 1A and 8, read channel 100 comprises a first feedback loop comprising communication link 165. In step 810 the method generates signal estimates 199 by sequence detector 170. In step 820, those signal estimates 199 are provided to gain control module 160.

The read channel 100 further comprises a second feedback loop comprising communication link 166, least mean square ("LMS") algorithm 180, and communication link 185. Traditional LMS algorithms can show significant stability and performance deficiencies caused by (1) nonstationary, impulsive environmental noise, (2) finite precision arithmetic, and (3) measurement noise associated with quantization and electronic amplifiers. In certain embodiments, LMS algorithm 180 comprises a "leaky" LMS algorithm wherein the leakage parameter addresses stability deficiencies that arise from nonstationary inputs, low signal-to-noise ratios, and finite-precision arithmetic.

In step 830, the signal estimates 199 are provided to LMS algorithm 180. In step 840, LMS algorithm 180 provides an updated set of equalizer coefficients to fractionally-spaced equalizer 150.

The read channel 100 further comprises a third feedback loop comprising communication link 167, timing control module 190, and communication link 195. In step 850, the signal estimates 199 are provided to timing control module 190, and timing control module 190 generates a timing signal. In step 860, that timing signal is provided to upsampler / interpolator 135.

In certain embodiments, the method transitions from step 860 to step 740 and continues as described herein. Although FIG. 8 shows steps 810 through 860 being performed seriatim, in certain embodiments of the apparatus and method steps 810 through 860 are performed substantially synchronously.

Referring now to FIG. 1B, FIG. 1B is a block diagram showing the read channel 101. Read channel 101 comprises a separate upsampler 130 and interpolator 140.

In certain embodiments of the read channel 100 / 101, the equalizer adaptation feedback loop is decoupled from the gain adaptation feedback loop. Without decoupling, the interaction of these two feedback loops could potentially result in gain and/or equalizer coefficient drift that could decrease the overall performance of the read channel, and/or could lead to divergence of the adaptive loops in case the equalizer and gain control adaptations are not properly constrained.

Referring now to FIG. 3, read channel 300 comprises gain adaptation loop 310 wherein a gain control error signal comprising the difference between a delayed output signal from gain control module 160 provided by communication link 330 and the signal estimates 199 formed by sequence detector 170 decisions provided by communication link 320 is provided to gain control module 160 using communication link 340.

Read channel 300 further comprises equalizer adaptation loop 350 wherein an equalizer error signal comprising the difference between a delayed equalized signal, provided by communication link 370, and the signal estimates 199 formed by sequence detector 170 decisions, provided by communication link 360, is provided by communication link 380 to LMS algorithm 180.

In certain embodiments, the apparatus and method employ equalization to a partial response class-4 (PR4) target and maximum-likelihood sequence detection using a Euclidean distance metric, a combination known in the art as PRML. In these PRML detector embodiments, sequence detector 170 comprises a PRML detector, and target polynomial 175 (FIG. 1A) comprises integer coefficients, i.e., , where D denotes a delay operator.

At higher linear recording densities, a linear PR4 equalizer leads to substantial noise enhancement. In certain embodiments the apparatus and method, detector 170 comprises an Extended PRML detector ("EPRML"). Such an EPRML detector 170, with a target polynomial of , is also a fixed structure wherein the target polynomial 175 cannot be adapted to changing channel operating points.

At even higher linear recording densities, an EPR4 target might lead to further noise enhancement. In certain embodiments Applicants' apparatus and method, detector 170 comprises an Extended EPRML detector ("E2PRML"). Such an E2PRML detector 170, with a target polynomial of , is also a fixed structure wherein the target polynomial 175 cannot be adapted to changing channel operating points.

In certain embodiments, it is found that equalizing to a short target does not allow mitigating the mismatch of the channel and target, and the subsequent equalization required to alter the overall response leads to noise coloration, noise enhancement, and a resulting performance degradation. Alternatively, overly increasing the length of the target leads to an undesirable increase in the complexity of the maximum likelihood sequence detector.

In certain embodiments, the apparatus and method employ a Noise Predictive Maximum Likelihood ("NPML") detector. The NPML detector provides enhanced reliability by adding a noise whitening filter at the input to the sequence detector and performing sequence detection based upon a longer effective target. In certain of the NPML embodiments, the target polynomial comprises non-integer coefficients. By allowing the PR target polynomial to take noninteger coefficients, a better match to the channel is possible.

In certain embodiments, target polynomial 175 (FIGs. 1A, 1B) is set during initialization of the information storage and retrieval system comprising read channel 100. In other embodiments, target polynomial 175 is provided

by a host computer interconnected with the information storage and retrieval system comprising read channel 100.

In certain embodiments of the apparatus and method, both a partial-response target and the fractionally-spaced equalizer are updated jointly. Referring now to FIG. 4, Applicants' read channel 400 comprises NPML detector 410, target adaptation loop 440 wherein circuit 430 provides an updated target 420 to NPML detector 410. At the same time, the equalizer output signal 450 is utilized to generate an equalizer error signal which is provided to fractionally-spaced equalizer 150. In this embodiment, the equalizer combines the functions of signal shaping and noise prediction.

Read channel 400 further comprises fixed clock 110, analog to digital converter 120, upsampler/interpolator 135 (FIG. 1A) or upsampler 130 (FIG. 1B) and interpolator 140 (FIG. 1B). In certain embodiments, read channel 400 further comprises gain adaptation loop 310 (FIG. 3), wherein the equalizer/target adaptations as well as the timing and gain adjustments are decoupled, as described above.

Referring now to FIGs. 4 and 8, in target adaptation embodiments the method includes step 870 wherein the apparatus and method generate an adjusted target. In step 880, the apparatus and method provide that adjusted target to the NPML detector 410.

In certain embodiments, the read channel comprises separate implementations of the fractionally-spaced equalizer and noise prediction filters. For example referring to FIG. 5, read channel 500 comprises fractionally-spaced equalizer 150 in combination with noise prediction filter 510 comprising a noise prediction filter update loop 520, wherein both filters are adaptively adjusted. Read channel 500 further comprises fixed clock 110, analog to digital converter 120, upsampler/interpolator 135 (FIG. 1A) or upsampler 130 (FIG. 1B) and interpolator 140 (FIG. 1B). In certain embodiments, read channel 500 further comprises gain adaptation loop 310 (FIG. 3), wherein the equalizer adaptation as well as the timing and gain adjustments are decoupled, as described above.

In certain embodiments, the apparatus comprises a state-dependent NPML detector. Referring now to FIG. 6, read channel 600 comprises NPML detector 610 which comprises metric computation unit 620, wherein the Pk(D), k=0, 1, ... 2xNstates-1 denote the set of predictor coefficients corresponding to the (k)th transition on the NPML trellis. Read channel

600 further comprises fixed clock 110, analog to digital converter 120, upsampler/interpolator 135 (FIG. 1A) or upsampler 130 (FIG. 1B) and interpolator 140 (FIG. 1B). In certain embodiments, read channel 600 further comprises gain adaptation loop 310 (FIG. 3), wherein the equalizer adaptation as well as the timing and gain adjustments are decoupled, as described above.

Storage services providers may provide enhanced information storage services to storage services customers using the apparatus and method. More specifically, a storage services provider may enhance the services provided to a storage services customer by encoding, at a symbol rate, data received from the storage services customer to an information storage medium, and later reading that data from said information storage medium to form an analog signal. The storage services provider may, using the apparatus and method, asynchronously sample at a fixed sampling rate the analog signal to form sampled signals, form interpolated samples, and provide those interpolated samples to a fractionally-spaced equalizer at an interpolation rate, where that interpolation rate is greater than the symbol rate. The storage services provider may, using the apparatus and method, form synchronous, equalized samples at an equalization rate, where that equalization rate is less than or equal to the interpolation rate, adjust the gain of those equalized samples, and detect data symbols representing a maximum likelihood sequence estimate using said gain-adjusted, synchronous, equalized samples.

The embodiments of the method shown in FIGs7 and 8 may be implemented separately. Moreover, in certain embodiments, individual steps recited in FIGs. 7 and/or 8 may be combined, eliminated, or reordered.

In certain embodiments, the invention includes instructions residing in memory disposed in the data storage device comprising the read channel, where those instructions are executed by a processor disposed in the data storage device comprising the read channel to performs steps 720, 730, 740, 750, 760, 770, and/or 780, recited in FIG. 7, and/or steps 810, 820, 830, 840, 850, 860, 870, and/or 880, recited in FIG. 8.

In other embodiments, the invention includes instructions residing in any other computer program product, where those instructions are executed by a computer external to, or internal to, the information storage and retrieval system comprising the read channel, to perform steps 720, 730, 740, 750, 760, 770, and/or 780, recited in FIG. 7, and/or steps 810, 820, 830, 840, 850, 860, 870, and/or 880, recited in FIG. 8. In either case,

the instructions may be encoded in an information storage medium comprising, for example, a magnetic information storage medium, an optical information storage medium, an electronic information storage medium, and the like. By "electronic storage media," what is meant, for example, is a device such as a PROM, EPROM, EEPROM, Flash PROM, compactflash, smartmedia, and the like.

While the preferred embodiments of the present invention have been illustrated in detail, it should be apparent that modifications and adaptations to those embodiments may occur to one skilled in the art without departing from the scope of the present invention as set forth in the following claims.

CLAIMS

1. A read channel, comprising:

an asynchronous analog to digital converter to asynchronously sample an analog signal formed by reading a data track at a rate larger than the first rate, wherein said data track was written to a data storage medium at a first rate;

an interpolator interconnected with said analog to digital converter;

a fractionally-spaced equalizer interconnected with said interpolator, wherein said interpolator provides interpolated samples to said fractionally-spaced equalizer at an interpolation rate, and wherein said fractionally-spaced equalizer forms synchronous equalized samples at an equalization rate, wherein said interpolation rate is greater than or equal to said equalization rate, and wherein said interpolation rate is greater than said first rate;

a gain control module interconnected with said fractionally-spaced equalizer; and

a sequence detector interconnected with said gain control module.

2. The read channel of claim 1, further comprising an upsampler to oversample in the asynchronous domain said analog signal at a rate greater than said first rate.

3. The read channel of claim 2, further comprising a first feedback circuit comprising a timing control circuit interconnected with said sequence detector and with said interpolator.

4. The read channel of claim 3, further comprising a second feedback circuit comprising a least mean square update circuit interconnected with said sequence detector and said fractionally-spaced equalizer.

5. The read channel of claim 4, further comprising a third feedback circuit interconnecting said sequence detector and said gain control module.

6. The read channel of claim 5, wherein said second feedback circuit is decoupled from said third feedback circuit.

7. The read channel of claim 6, wherein said sequence detector comprises a Partial Response Maximum Likelihood sequence detector.

8. The read channel of claim 6, wherein said sequence detector comprises a Noise Predictive Maximum Likelihood sequence detector.

9. The read channel of claim 8, wherein said Noise Predictive Maximum Likelihood sequence detector comprises a branch metric computation algorithm and a plurality of predictor filters, wherein said predictor filters are embedded into said branch metric computation algorithm, wherein each transition of said algorithm is associated with a different one of said plurality of predictor filters.

10. A method to read information encoded in a data storage medium, comprising the steps of:

supplying a read channel comprising an analog to digital converter, an interpolator interconnected with said analog to digital converter, a fractionally-spaced equalizer interconnected with said interpolator, a gain control module interconnected with said fractionally-spaced equalizer, and a sequence detector interconnected with said gain control module;

reading a data track written to a data storage medium to form an analog signal, wherein said data track comprises information encoded at a first rate;

asynchronously sampling at a fixed sampling rate said analog signal to form sampled signals;

forming interpolated samples;

providing said interpolated samples to said fractionally-spaced equalizer at an interpolation rate, wherein said interpolation rate is greater than said first rate;

forming synchronous, equalized samples at an equalization rate, wherein said equalization rate is less than said interpolation rate;

adjusting the gain of said equalized samples;

detecting data symbols representing a maximum likelihood sequence estimate using said gain-adjusted, synchronous, equalized samples.

11. The method of claim 10, wherein said supplying step further comprises supplying an upsampler, said method further comprising the step of upsampling in the asynchronous domain at an upsampling rate, wherein said upsampling rate is greater than said first rate.

12. The method of claim 10, further comprising the steps of:

supplying a timing control circuit interconnected with said sequence detector and with said interpolator;

generating a timing signal;

providing said timing signal to said interpolator.

13. The method of claim 12, further comprising the steps of:
generating an equalizer error signal;
providing said equalizer error signal to said fractionally-spaced equalizer.

14. The method of claim 13, further comprising the steps of:
generating signal estimates formed by decisions from said sequence detector;
wherein said generating an equalizer error signal step further comprises generating an equalizer error signal comprising the difference between said signal estimates and a delayed equalized signal, before gain control.

15. The method of claim 14, further comprising the steps of:
generating a gain control error signal comprising the difference between a delayed gain-adjusted signal and said signal estimates;
providing said gain control error signal to said gain control module;
wherein said generating an equalizer error signal step and said generating a gain control error signal steps are decoupled.

16. The method of claim 15, wherein said supplying a sequence detector step further comprises supplying a sequence detector comprising a target, said method further comprising the steps of:
generating an adjusted target;
providing said adjusted target to said sequence detector;
setting said target to said adjusted target.

17. The method of claim 15, wherein said supplying a sequence detector step further comprises supplying a Partial Response Maximum Likelihood sequence detector, and wherein said detecting step further comprises detecting data symbols representing a maximum likelihood sequence estimate using said Partial Response Maximum Likelihood sequence detector.

18. The method of claim 15, wherein said supplying a sequence detector step further comprises supplying a Noise Predictive Maximum Likelihood sequence detector, and wherein said detecting step further comprises detecting data symbols representing a maximum likelihood sequence estimate using said Noise Predictive Maximum Likelihood sequence detector.

19. The method of claim 18, wherein said Noise Predictive Maximum Likelihood sequence detector comprises a branch metric computation algorithm and a plurality of predictor filters, wherein said predictor filters are embedded into said branch metric computation algorithm, wherein each transition of said algorithm is associated with a different one of said plurality of predictor filters.

20. A computer program product usable with a programmable computer processor to read information encoded in a data storage medium using a read channel comprising an analog to digital converter, an interpolator interconnected with said analog to digital converter, a fractionally-spaced equalizer interconnected with said interpolator, a gain control module interconnected with said fractionally-spaced equalizer, and a sequence detector interconnected with said gain control module, comprising:

computer readable program code which causes said programmable computer processor to read a data track written to a data storage medium to form an analog signal, wherein said data track comprises information encoded at a first rate;

computer readable program code which causes said programmable computer processor to asynchronously sample at a fixed sampling rate said analog signal to form sampled signals;

computer readable program code which causes said programmable computer processor to form interpolated samples;

computer readable program code which causes said programmable computer processor to provide said interpolated samples to said fractionally-spaced equalizer at an interpolation rate, wherein said interpolation rate is greater than said first rate;

computer readable program code which causes said programmable computer processor to form synchronous, equalized samples at an equalization rate, wherein said equalization rate is less than said interpolation rate;

computer readable program code which causes said programmable computer processor to adjust the gain of said equalized samples;

computer readable program code which causes said programmable computer processor to detect data symbols representing a maximum likelihood sequence estimate using said gain-adjusted, synchronous, equalized samples.

21. The computer program product of claim 20, wherein said read channel further comprises an upsampler, further comprising computer readable

program code which causes said programmable computer processor to upsample in the asynchronous domain at a rate greater than said first rate.

22. The computer program product of claim 21, wherein said read channel further comprises a timing control circuit interconnected with said sequence detector and with said interpolator, further comprising:

computer readable program code which causes said programmable computer processor to generate a timing signal;

computer readable program code which causes said programmable computer processor to provide said timing signal to said interpolator.

23. The computer program product of claim 22, further comprising:

computer readable program code which causes said programmable computer processor to generate an equalizer error signal;

computer readable program code which causes said programmable computer processor to provide said equalizer error signal to said fractionally-spaced equalizer.

24. The computer program product of claim 23, further comprising:

computer readable program code which causes said programmable computer processor to receive signal estimates from said sequence detector decisions;

computer readable program code which causes said programmable computer processor to generate an equalizer error signal comprising the difference between said signal estimates and a delayed equalized signal, before gain control.

computer readable program code which causes said programmable computer processor to provide said equalizer error signal to said fractionally-spaced equalizer.

25. The computer program product of claim 24, further comprising:

computer readable program code which causes said programmable computer processor to generate a gain control error signal comprising the difference between a delayed gain-adjusted signal and said signal estimates;

computer readable program code which causes said programmable computer processor to provide said gain control error signal to said gain control module;

wherein generating said equalizer error signal is decoupled from generating said gain control error signal.

26. The computer program product of claim 24, wherein said sequence detector comprises a target, further comprising:

computer readable program code which causes said programmable computer processor to generate an adjusted target;

computer readable program code which causes said programmable computer processor to provide said adjusted target to said sequence detector;

computer readable program code which causes said programmable computer processor to set said target to said adjusted target.

27. The computer program product of claim 26, wherein said sequence detector comprises a Partial Response Maximum Likelihood sequence detector, further comprising computer readable program code which causes said programmable computer processor to detect said data symbols representing a maximum likelihood sequence estimate using said Partial Response Maximum Likelihood sequence detector.

28. The computer program product of claim 26, wherein said sequence detector comprises a Noise Predictive Maximum Likelihood sequence detector, further comprising computer readable program code which causes said programmable computer processor to detect said data symbols representing a maximum likelihood sequence estimate using said Noise Predictive Maximum Likelihood sequence detector.

29. A method to enhance the services provided by a storage services provider to a storage services customer, comprising the steps of:

encoding, at a first rate, data received from a storage services customer to an information storage medium;

reading said data from said information storage medium to form an analog signal;

asynchronously sampling at a fixed sampling rate said analog signal to form sampled signals;

forming interpolated samples;

providing said interpolated samples to a fractionally-spaced equalizer at an interpolation rate, wherein said interpolation rate is greater than said first rate;

forming synchronous, equalized samples at an equalization rate, wherein said equalization rate is less than said interpolation rate;

adjusting the gain of said equalized samples;

detecting data symbols representing a maximum likelihood sequence estimate using said gain-adjusted, synchronous, equalized samples.

FIG. 1A

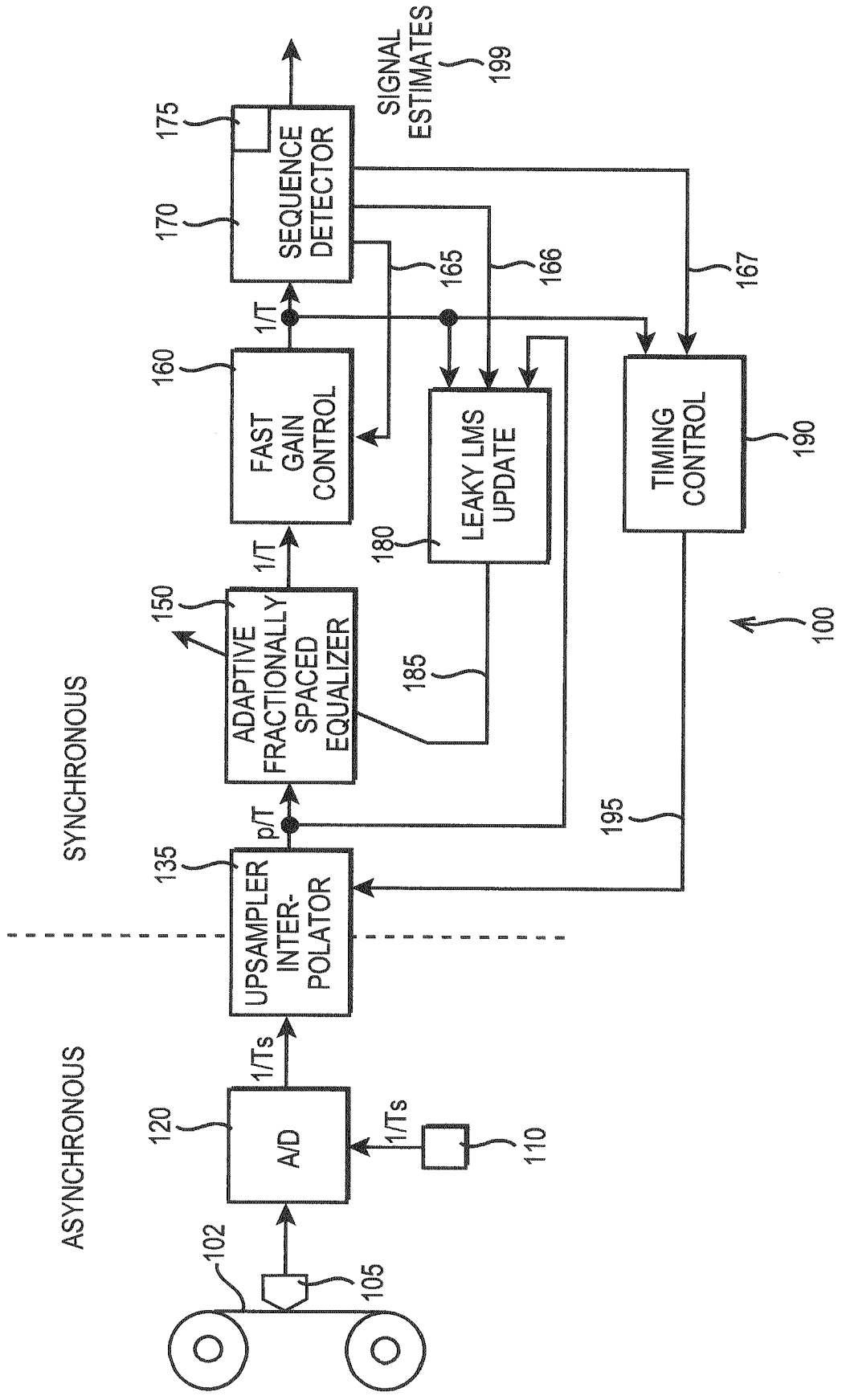

ASYNCHRONOUS
SYNCHRONOUS
102
105
120
A/D
1/Ts
110
1/Ts
135
UPSAMPLER INTER-POLATOR
p/T
150
ADAPTIVE FRACTIONALLY SPACED EQUALIZER
1/T
160
FAST GAIN CONTROL
1/T
170
SEQUENCE DETECTOR
175
SIGNAL ESTIMATES
199
165
166
167
180
LEAKY LMS UPDATE
185
TIMING CONTROL
190
195
100

FIG. 1B

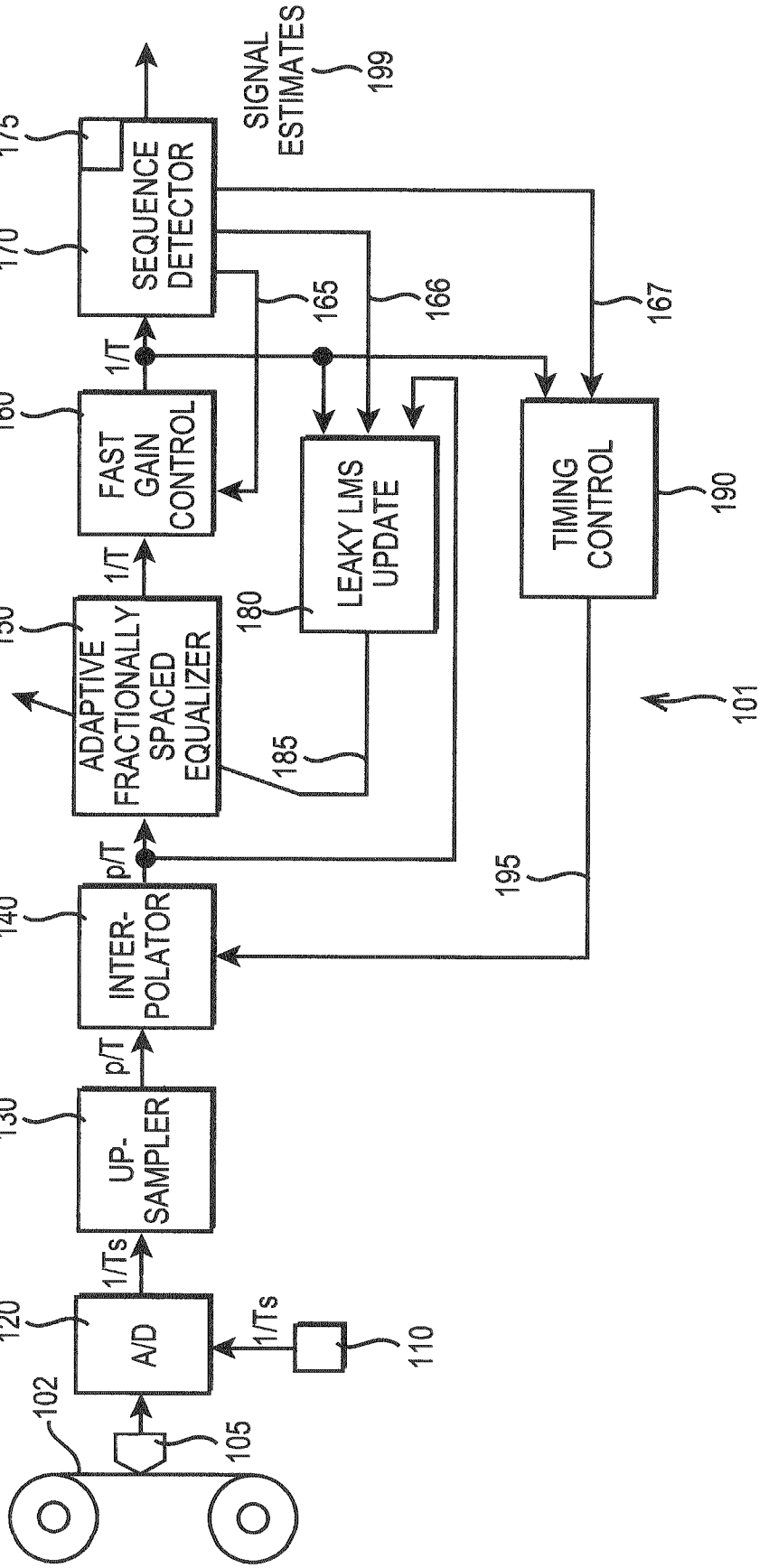

SIGNAL ESTIMATES
199
175
SEQUENCE DETECTOR
170
165
166
167
1/T
160
FAST GAIN CONTROL
LEAKY LMS UPDATE
TIMING CONTROL
190
150
ADAPTIVE FRACTIONALLY SPACED EQUALIZER
180
185
101
p/T
140
INTER-POLATOR
195
130
UP-SAMPLER
1/Ts
120
A/D
110
102
105

FIG. 2

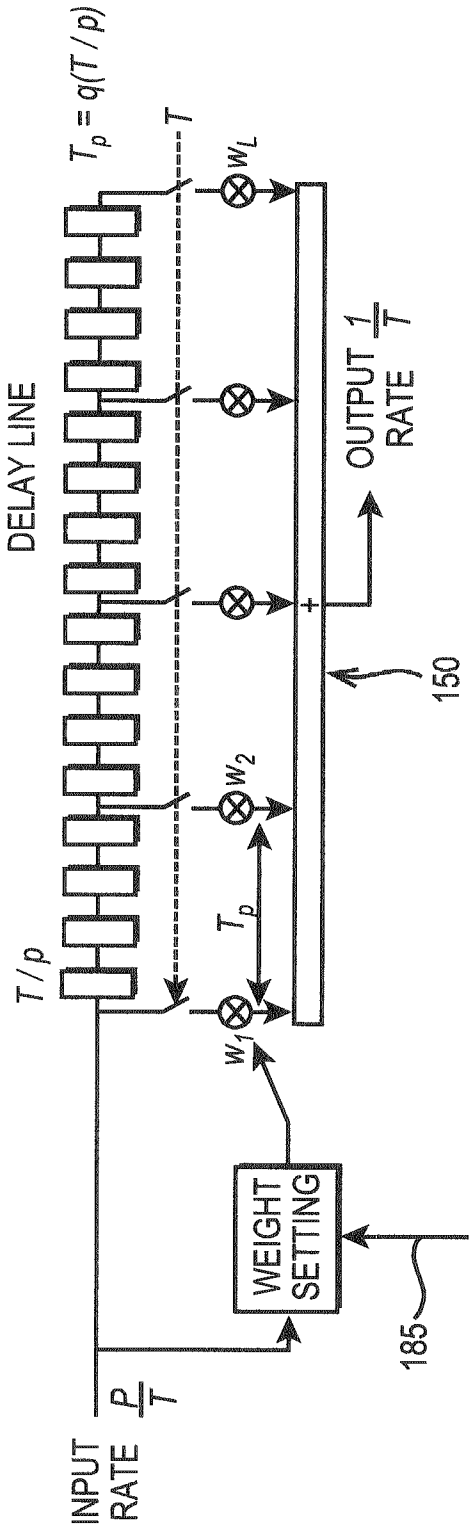

$T_p = q(T/p)$
T
w_L
DELAY LINE
OUTPUT $\frac{1}{T}$ RATE
150
w_2
T_p
T/p
w_1
WEIGHT SETTING
185
INPUT RATE $\frac{P}{T}$

FIG. 3

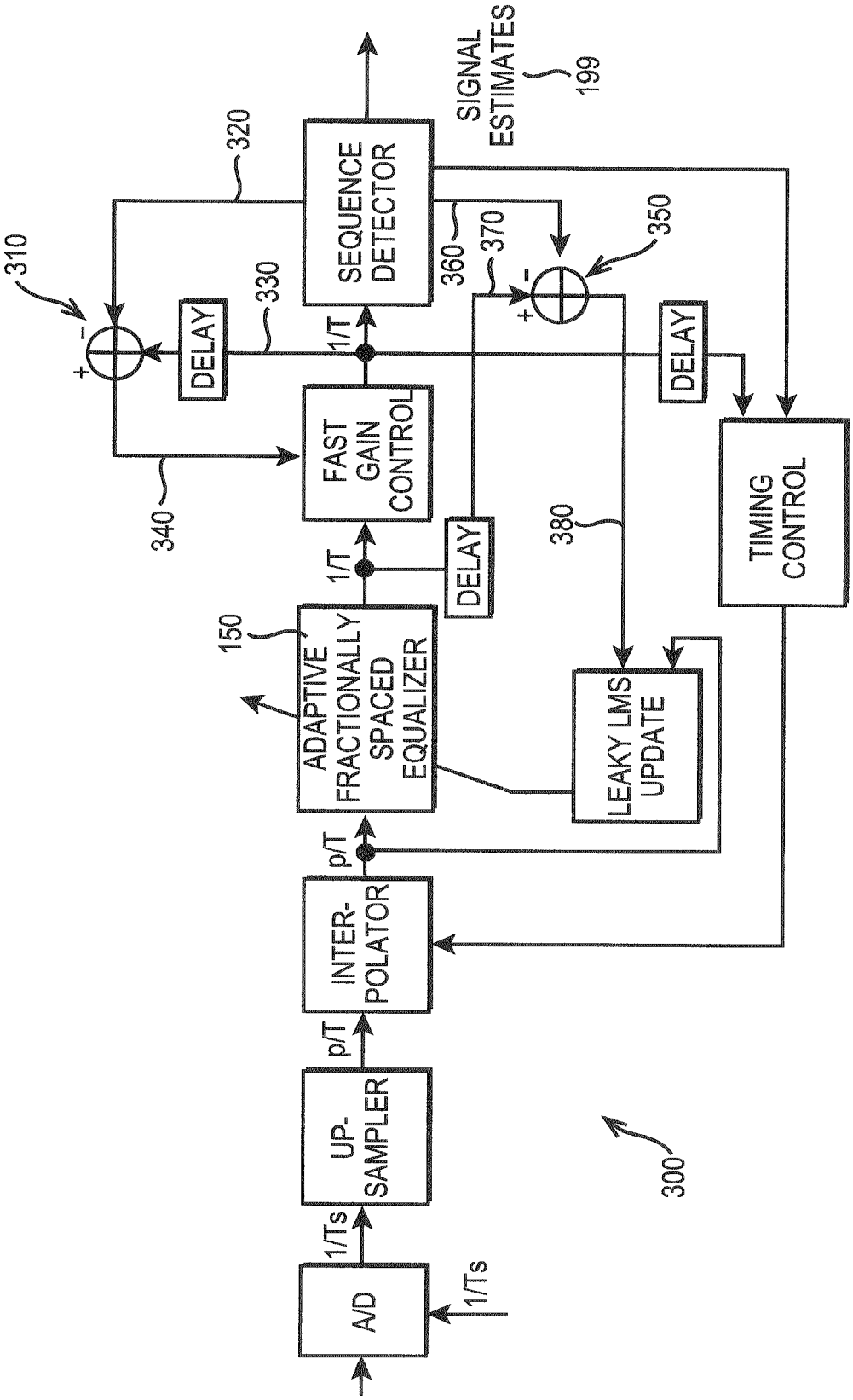

A/D
1/Ts
1/Ts
UP-SAMPLER
p/T
INTER-POLATOR
p/T
ADAPTIVE FRACTIONALLY SPACED EQUALIZER
150
1/T
DELAY
FAST GAIN CONTROL
340
1/T
SEQUENCE DETECTOR
320
SIGNAL ESTIMATES
199
310
DELAY
330
360
370
350
DELAY
380
LEAKY LMS UPDATE
TIMING CONTROL
300

FIG. 4

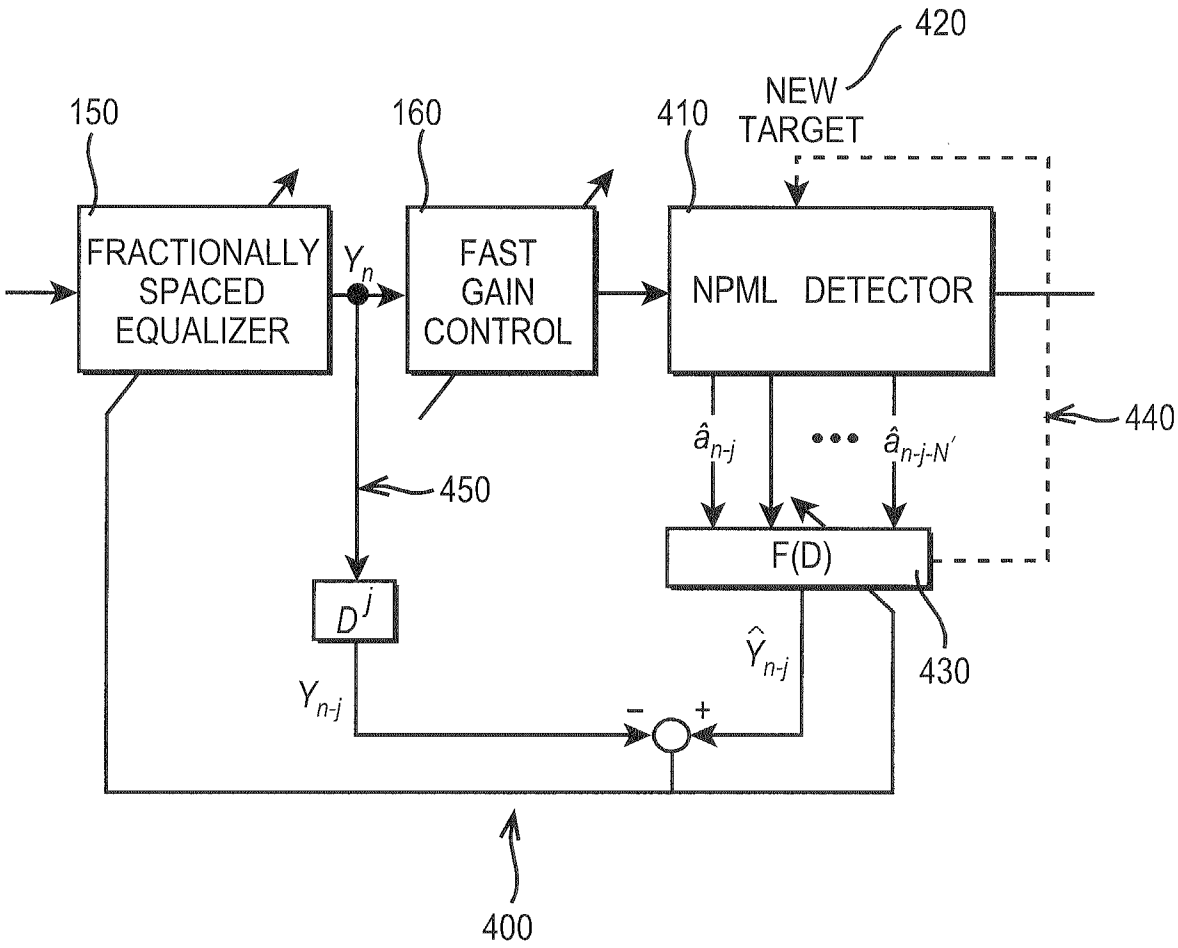

420
NEW
TARGET
150
160
410
FRACTIONALLY
SPACED
EQUALIZER
Y_n
FAST
GAIN
CONTROL
NPML DETECTOR
440
$\hat{a}_{n-j}$
$\hat{a}_{n-j-N'}$
450
F(D)
D^j
$\hat{Y}_{n-j}$
430
Y_{n-j}
−
+
400

FIG. 5

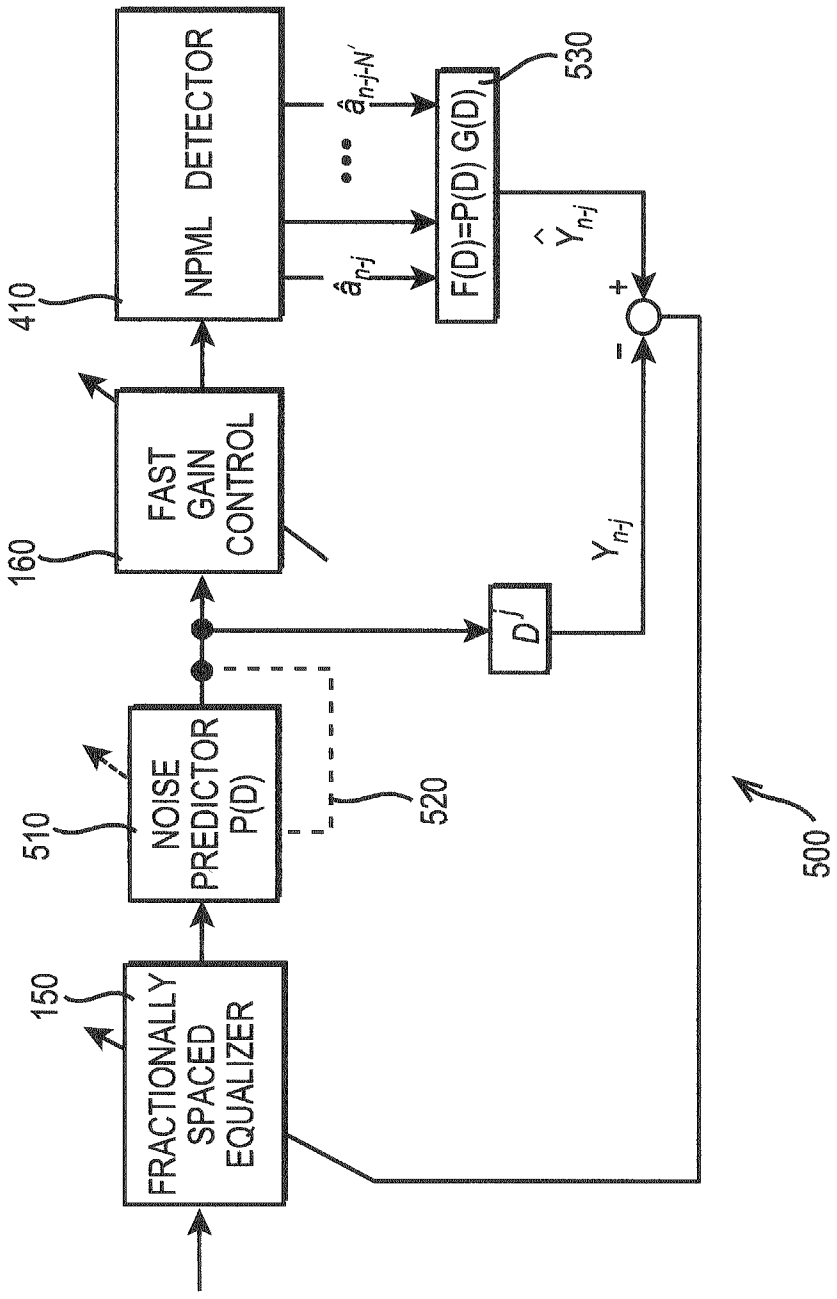

FRACTIONALLY SPACED EQUALIZER
150
NOISE PREDICTOR P(D)
510
520
FAST GAIN CONTROL
160
NPML DETECTOR
410
F(D)=P(D) G(D)
530
D^j
Y_{n-j}
$\hat{Y}_{n-j}$
$\hat{a}_{n-j}$
$\hat{a}_{n-j-N'}$
+
-
500

FIG. 6

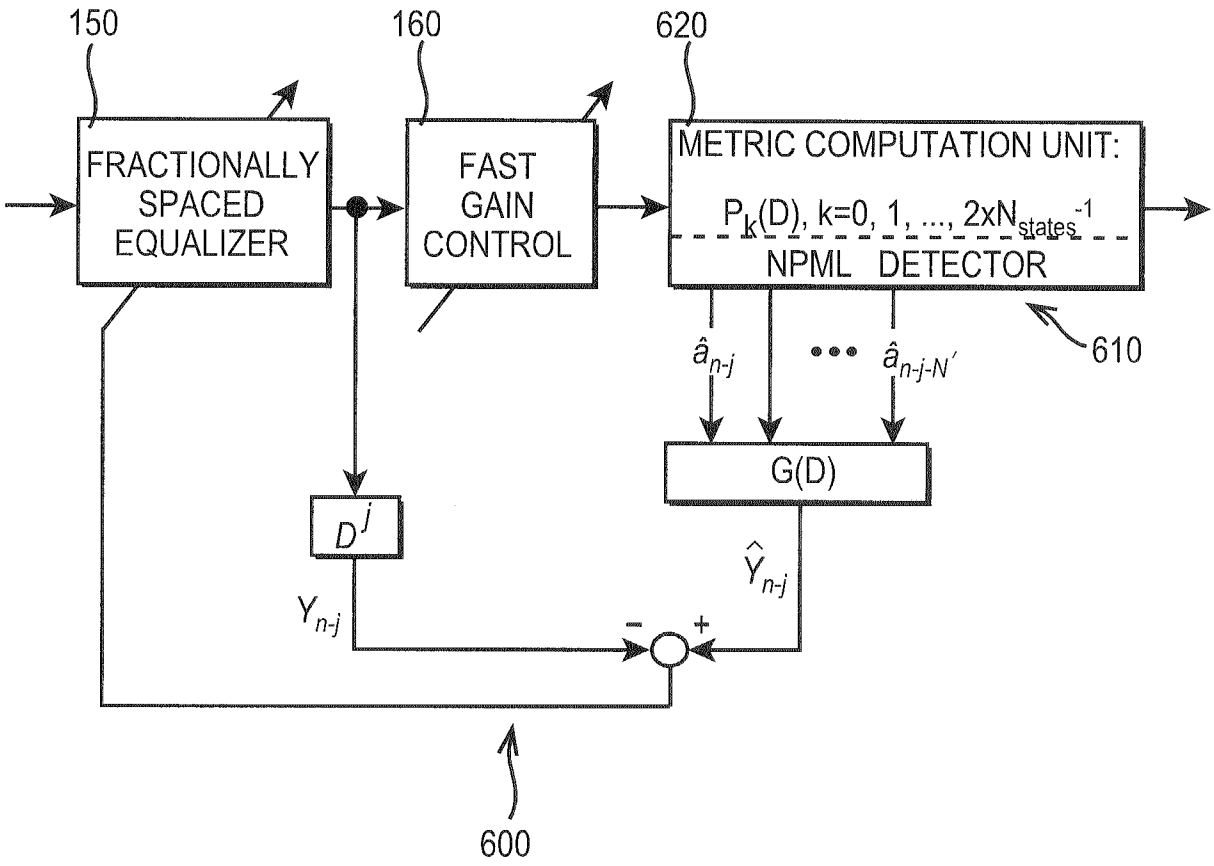

150
160
620
FRACTIONALLY SPACED EQUALIZER
FAST GAIN CONTROL
METRIC COMPUTATION UNIT:
$P_k(D)$, k=0, 1, ..., $2xN_{states}^{-1}$
NPML DETECTOR
610
$\hat{a}_{n-j}$
$\hat{a}_{n-j-N'}$
G(D)
D^j
$\hat{Y}_{n-j}$
Y_{n-j}
-
+
600

FIG. 7

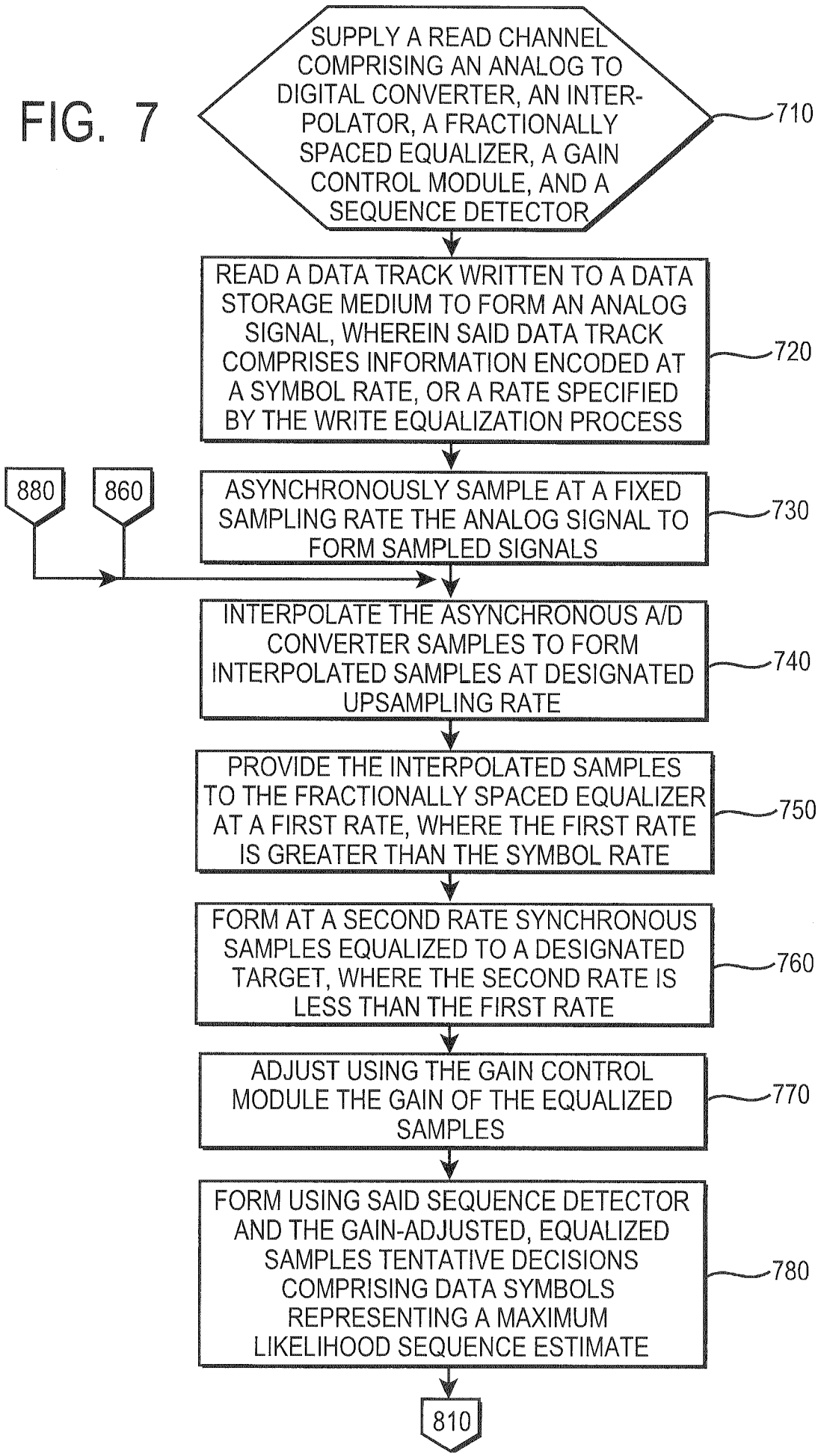
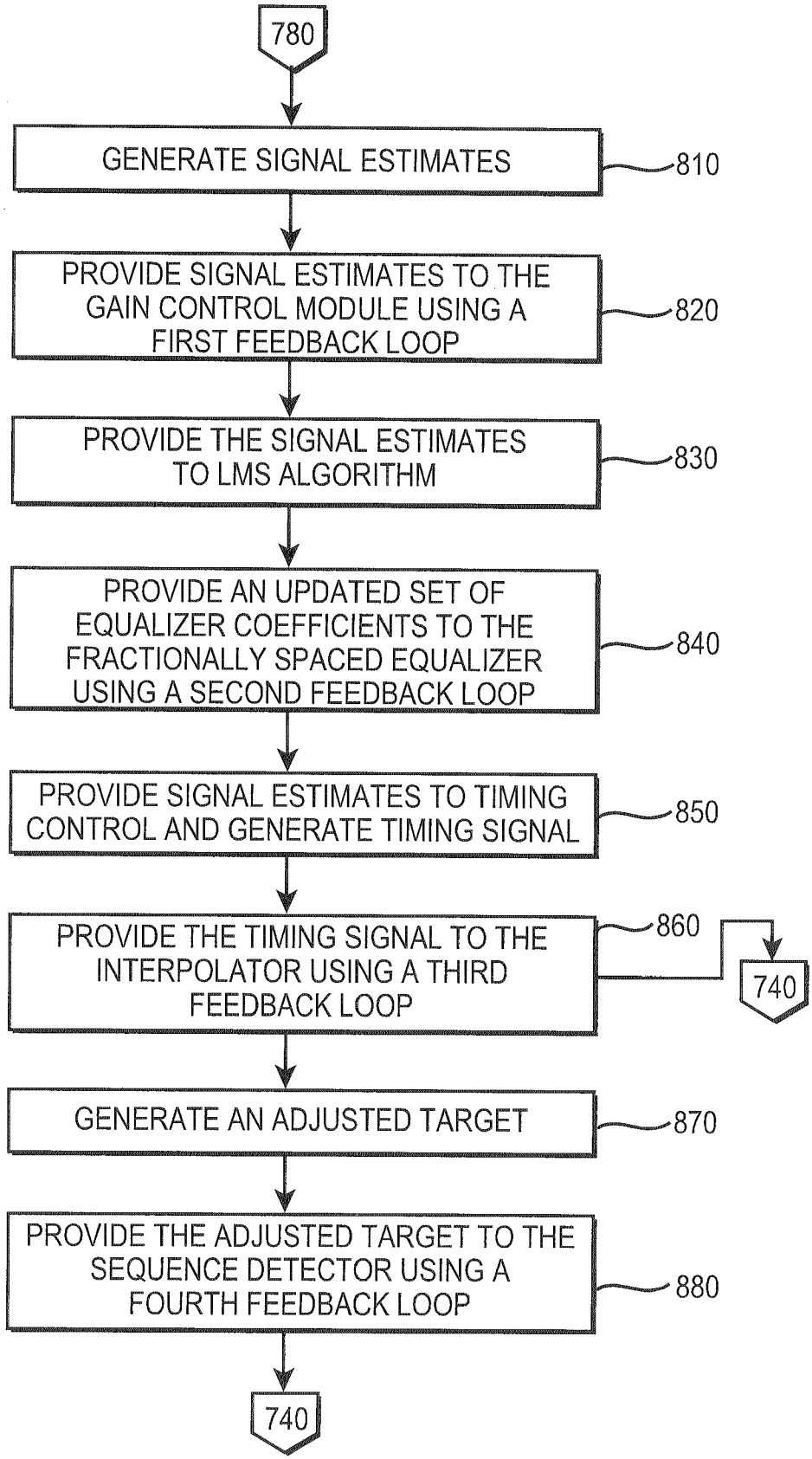

SUPPLY A READ CHANNEL COMPRISING AN ANALOG TO DIGITAL CONVERTER, AN INTER-POLATOR, A FRACTIONALLY SPACED EQUALIZER, A GAIN CONTROL MODULE, AND A SEQUENCE DETECTOR
710
READ A DATA TRACK WRITTEN TO A DATA STORAGE MEDIUM TO FORM AN ANALOG SIGNAL, WHEREIN SAID DATA TRACK COMPRISES INFORMATION ENCODED AT A SYMBOL RATE, OR A RATE SPECIFIED BY THE WRITE EQUALIZATION PROCESS
720
880
860
ASYNCHRONOUSLY SAMPLE AT A FIXED SAMPLING RATE THE ANALOG SIGNAL TO FORM SAMPLED SIGNALS
730
INTERPOLATE THE ASYNCHRONOUS A/D CONVERTER SAMPLES TO FORM INTERPOLATED SAMPLES AT DESIGNATED UPSAMPLING RATE
740
PROVIDE THE INTERPOLATED SAMPLES TO THE FRACTIONALLY SPACED EQUALIZER AT A FIRST RATE, WHERE THE FIRST RATE IS GREATER THAN THE SYMBOL RATE
750
FORM AT A SECOND RATE SYNCHRONOUS SAMPLES EQUALIZED TO A DESIGNATED TARGET, WHERE THE SECOND RATE IS LESS THAN THE FIRST RATE
760
ADJUST USING THE GAIN CONTROL MODULE THE GAIN OF THE EQUALIZED SAMPLES
770
FORM USING SAID SEQUENCE DETECTOR AND THE GAIN-ADJUSTED, EQUALIZED SAMPLES TENTATIVE DECISIONS COMPRISING DATA SYMBOLS REPRESENTING A MAXIMUM LIKELIHOOD SEQUENCE ESTIMATE
780
810

FIG. 8


780
GENERATE SIGNAL ESTIMATES
810
PROVIDE SIGNAL ESTIMATES TO THE GAIN CONTROL MODULE USING A FIRST FEEDBACK LOOP
820
PROVIDE THE SIGNAL ESTIMATES TO LMS ALGORITHM
830
PROVIDE AN UPDATED SET OF EQUALIZER COEFFICIENTS TO THE FRACTIONALLY SPACED EQUALIZER USING A SECOND FEEDBACK LOOP
840
PROVIDE SIGNAL ESTIMATES TO TIMING CONTROL AND GENERATE TIMING SIGNAL
850
PROVIDE THE TIMING SIGNAL TO THE INTERPOLATOR USING A THIRD FEEDBACK LOOP
860
740
GENERATE AN ADJUSTED TARGET
870
PROVIDE THE ADJUSTED TARGET TO THE SEQUENCE DETECTOR USING A FOURTH FEEDBACK LOOP
880
740

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/063793

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11B20/10 H04N5/52

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11B H04L H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/250197 A1 (TAKEHARA SHINTARO [JP]) 9 December 2004 (2004-12-09) abstract; figure 4 paragraphs [0038], [0048], [0055]	1-29
Y	US 2003/081670 A1 (BOLOGNA FRANK PATRICK [US] ET AL) 1 May 2003 (2003-05-01) abstract paragraph [0019]; figure 1	1-29
Y	JP 04 183016 A (NIPPON ELECTRIC CO) 30 June 1992 (1992-06-30) abstract	1-29
Y	US 2003/043898 A1 (HUANG KE-CHIANG [TW] ET AL) 6 March 2003 (2003-03-06) abstract; figure 1	1-29

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 November 2006	09/01/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Glasser, Jean-Marc

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2006/063793

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004250197 A1	09-12-2004	CN 1571057 A	26-01-2005
		JP 3813931 B2	23-08-2006
		JP 2004234785 A	19-08-2004
US 2003081670 A1	01-05-2003	NONE	
JP 4183016 A	30-06-1992	NONE	
US 2003043898 A1	06-03-2003	TW 236229 B	11-07-2005
		US 2005220184 A1	06-10-2005