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(71) Applicant *(for all designated States except US)*: **APPLIED MATERIALS, INC.** [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **WEIDMAN, Timothy W.** [US/US]; 776 Henderson Avenue, Sunnyvale, CA 94086 (US). **WIJEKOON, Kapila P.** [US/US]; 438 East Charleston Road, Palo Alto, CA 94306 (US). **ZHU, Zhize** [CN/US]; 10282 Terry Way, Apt. #3, Cupertino, CA 95014 (US). **GELATOS, Avgerinos V. (Jerry)** [US/US]; 2651 Eaton Avenue, Redwood City, CA 94062 (US). **KHANDELWAL, Amit** [IN/US]; 3770 Flora Vista Ave., #2102, Santa Clara, CA 95051 (US). **SHANMUGASUNDRAM, Arulkumar** [IN/US]; 428 Madera Avenue #10, Sunnyvale, CA 94086 (US). **YANG, Michael X.** [US/US]; 793 Cereza Drive, Palo Alto, CA 94306 (US). **WANG, Yaxin** [US/US]; 44224 Ibero Way, Fremont, CA 94539 (US). **MEI, Fang** [CN/US]; 975 Laguna Circle, Foster City, CA 94404 (US). **MOGHADAM, Farhad K.** [US/US]; 276 Old Adobe Road, Los Gatos, CA 95030 (US). **STEWART, Michael P.** [US/US]; 392 N. Rengstorff Ave., Apt. 2, Mountain View, CA 94043 (US). **KRISHNA, Nety M.** [IN/US]; 1345 Floyd Avenue, Sunnyvale, CA 94087 (US). **KONECNI, Anthony** [US/US]; 12891 Andys Gulch Road, Boise, ID 83714 (US). **GANDIKOTA, Srinivas** [US/US]; 2727 Monroe Street, Santa Clara, CA 95054 (US).

(74) Agents: **PATTERSON, B. Todd** et al.; PATTERSON & SHERIDAN, L.L.P., 3040 Post Oak Blvd., Suite 1500, Houston, Texas 77056-6582 (US).

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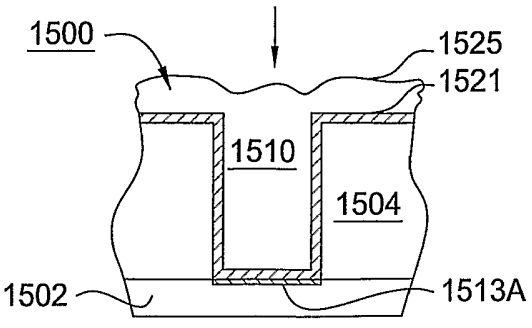
(54) Title: CONTACT METALLIZATION METHODS AND PROCESSES



(57) Abstract: Embodiments of the invention generally provide methods of filling contact level features formed in a semiconductor device by depositing a barrier layer over the contact and then filing the contact using an PVD, CVD, ALD, electrochemical plating and/or electroless deposition processes. In one embodiment, the barrier layer contains catalytically active surface that allows the electroless deposition of a metal on the surface. In one aspect, the electrolessly deposited metal is copper or a copper alloy. In one embodiment, a method for depositing a material on a substrate includes positioning a substrate within a process chamber, exposing the substrate to at least one pretreatment step and filling the contact by an electroless deposition process. Embodiments of the invention provide a simplified method of filling contact level features formed in a semiconductor device, which include novel methods of forming a contact level feature that contains a silicide interface and a tungsten CVD deposited layer.

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CONTACT METALLIZATION METHODS AND PROCESSES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention generally relate to methods for depositing materials on a substrate, and more specifically to methods for filling apertures within a contact formed on a substrate.

Description of the Related Art

[0002] Multilevel, 45 nm node metallization is one of the key technologies for the next generation of very large scale integration (VLSI). The multilevel interconnects that lie at the heart of this technology possess features with small CD's and high aspect ratios including contacts, vias, lines and other apertures. Reliable formation of these features is very important for the success of VLSI and the continued effort to increase quality and circuit density on individual substrates. Therefore, there is a great amount of ongoing effort being directed to the formation of void-free features with low contact resistance for the 45 nm node and nodes below.

[0003] Tungsten is a choice metal for filling VLSI features, such as sub-micron contact on a substrate. Conventional "contacts" are formed by depositing a conductive interconnect material, such as tungsten into an aperture (*e.g.,* via) on the surface of insulating material disposed between two spaced-apart conductive layers. The aspect ratio of such an opening may inhibit deposition of a conformal conductive interconnect material to fill an aperture. Although tungsten is a popular interconnect material, vapor deposition processes for depositing tungsten commonly suffer from void or a seam type defect creation within the contact plug, as illustrated in Figure 1C. Also, tungsten is has a relatively high resistivity, which will result in a high circuit resistance formed using the tungsten containing contact.

[0004] Figure 1A depicts a schematic cross-sectional view of an integrated circuit device on substrate 100 containing a via or aperture 105 formed in dielectric layer 104 to expose contact layer 102. During a vapor deposition process that may include chemical vapor deposition (CVD) or atomic layer deposition (ALD), a tungsten layer 106 is deposited on dielectric layer 104 and within aperture 105 including on contact layer 102 and the sidewalls of dielectric layer 104 to form plug

103, as illustrated in Figure 1B. Near the opening 107 of plug 103, tungsten layer 106 may pinch off, depicted in Figure 1C, so that plug 103 maintains a seam or a void 108 therein. During a subsequent chemical mechanical polishing (CMP) process that removes a portion of tungsten layer 106 and dielectric layer 104 from the surface of substrate 100, void 108 may be breached or exposed to form gap 110 within plug 103, as illustrated in Figure 1D. Figure 1E depicts conductive layer 112 (*e.g.,* copper) deposited on substrate 100 forming void 114 by enclosing gap 110. Substrate 100 may contain additional layers of material depending on the overall architecture of the electronic device. For example, dielectric layer 104 may be covered by a barrier layer (not shown) thereon prior to the deposition of conductive layer 112 and/or conductive layer 112 may also contain a barrier layer (not shown) thereon prior to the deposition of layer 120.

[0005] Defects, such as a seam or a void 114, may cause a series of problems during the fabrication of electronic devices depicted herein. The resistance to current flow through the plug 103 is impaired due to the lack of tungsten material in the void 114. However, a more serious obstacle during fabrication is the displacement of voids from one layer to the next. For example, subsequent fabrication processes of substrate 100 may include the deposition of layer 120 (*e.g.,* dielectric layer) on conductive layer 112. During subsequent thermal processing, such as an annealing process, the material 116 from conductive layer 112 may diffuse into void 114 and form a void 118 within conductive layer 112. As illustrated in Figure 1F, material 116 may not diffuse completely to the bottom of void 114. The defect formed in the conductive layer 112, such as void 118, will increase the resistance of the circuit containing the defect and thus affect device performance. Ultimately, the defects in the conductive layer 112 can affect the device yield of the fabricated substrate. Therefore, there is a need for a method of reliably forming a plug 103 that does not have a seam or void type defect.

[0006] Also, one limitation of device performance, or device speed, is related to the resistance of the circuit formed in the semiconductor device. If the geometry of the device(s) remain the same (*e.g.*, trace length, contact feature aspect ratio) the main factor that effects the resistance of a formed circuit is the resistivity of the materials used to form the device. The lower the resistivity, the better one material will perform versus another material. For example, the resistivity of pure tungsten is

about 3.3 times higher than the resistivity of pure copper and thus a copper containing device would be faster than a comparable circuit made using tungsten. This among other reasons is often why copper interconnects are formed on integration levels M1 and above. In general, the term metal layer 1, or M1 layer, is generally intended to describe an interconnect layer (*e.g.*, conductive layer 112) formed over the contact level layer, such as a tungsten plug (*e.g.*, plug 103) that is formed during the contact layer formation process. Tungsten is commonly used at the contact level features due to it ability to fill features using CVD processes and it will not rapidly diffuse into silicon and adjacent oxide layers.

[0007] Reliably producing nanometer-sized features is one of the key technologies for the next generation of very large scale integration (VLSI) and ultra large scale integration (ULSI) of semiconductor devices. However, as the fringes of circuit technology are pressed, the shrinking dimensions of interconnects in VLSI and ULSI technology have placed additional demands on the processing capabilities. The multilevel interconnects that lie at the heart of this technology require precise processing of the contact level features (*e.g.*, contacts, vias and other interconnects). Reliable formation of these interconnects is very important to VLSI and ULSI success and to the continued effort to increase circuit density and quality of individual substrates.

[0008] Copper has become the metals of choice for nanometer-sized interconnect technology used in the metal layers M1 and above because copper has a lower electrical resistivity than most commonly used metals (*e.g.*, aluminum) and a higher current carrying capacity. These characteristics are important for supporting the higher current densities experienced at high levels of integration and increased device speed. Further, copper has a good thermal conductivity and is available in a highly pure state. Unfortunately, the use of copper at the contact level of a device has a number of drawbacks which include that it rapidly diffuses through silicon and dielectric materials, it has a relatively low melting point which can limit the maximum allowable silicidation formation temperature.

[0009] Contact level metallization processes require the formation of a silicide at the doped silicon source or drain interface to reduce the contact resistance and thus improve the speed of the formed device(s). Typically, conventional contact level metallization process(es) require the time consuming and complex process steps of

depositing a metal layer that will form a silicide at the doped silicon interface (*e.g.*, source or drain interface), removing the excess metal layer from the "field" (*e.g.*, top surface of the substrate in which the features are formed) by use of a chemical mechanical polishing (CMP) type process, performing a high temperature anneal process to form a metal silicide layer, depositing a liner/barrier layer (*e.g.*, titanium nitride (TiN), titanium (Ti), tantalum (Ta), tantalum nitride (TaN)) over the formed metal/metal silicide layer, and then filling the contact feature formed in the dielectric layer with tungsten (W) using a tungsten hexafluoride (WF_6) chemical vapor deposition (CVD) process. Since the contact level metallization process is relatively complex and requires a number of process steps, the chance of misprocessing the substrate or the chance that contamination will affect the device yield is very high.

[0010] Therefore, there exists a need for an improved contact level device that is void free, that has a low electrical resistance, that has good electromigration performance, that is reliable, and that can be reliably formed. Also, there is a need for a less time consuming and less complex method of forming a contact level interconnect that has a silicide formed at the doped silicon interface.

SUMMARY OF THE INVENTION

[0011] The present invention generally provide a method for depositing a material on a contact level feature formed on a substrate, comprising providing a substrate that has one or more contact level features that have an exposed silicide layer formed on a silicon containing region, depositing a barrier layer over the surface of the exposed silicide layer, wherein the depositing the barrier layer comprises depositing a first metal layer on the exposed silicide layer, and depositing a second metal layer over the first metal layer, wherein the second metal layer contains a metal selected from a group consisting of ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) and platinum (Pt), and filling the contact level feature with a metal containing layer.

[0012] Embodiments of the invention further provide a material on a contact level feature formed on a substrate, comprising providing a substrate that has one or more contact level features that have an exposed silicide layer formed on a doped silicon containing region, depositing a barrier layer over the surface of the exposed silicide layer, wherein the depositing the barrier layer comprises depositing a first metal layer on the exposed silicide layer, and depositing a second metal layer over

the first metal layer, wherein the second metal layer contains a metal selected from a group consisting of ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) and platinum (Pt), electrolessly depositing a first copper containing layer on the barrier layer, and depositing a second copper containing layer on the first copper containing layer to fill the one or more contact level features.

[0013] Embodiments of the invention further provide a method for depositing a material on a contact level feature formed on a substrate, comprising depositing a barrier layer over the surfaces of one or more contact level features formed on the substrate, and electrolessly depositing a copper containing layer on the barrier layer using a metal layer electroless deposition solution, wherein the metal layer electroless deposition solution comprises EDTA and copper ions at a concentration ratio of less than about 6:1.

[0014] Embodiments of the invention further provide a method for depositing a material on a contact level feature formed on a substrate, comprising electrolessly depositing a first metal containing layer on a doped silicon region on a surface of a substrate, forming a contact level interconnect feature, wherein the process of forming the contact level interconnect comprises depositing a dielectric layer over a surface of the substrate and the first metal containing layer, and forming one or more contact level features in the dielectric layer using conventional semiconductor processing methods, wherein the first metal containing layer is exposed at the bottom of one or more of the contact level features, depositing a barrier layer over the surface of the first metal layer, wherein the depositing the barrier layer comprises depositing a second metal layer over the first metal layer, wherein the second metal layer contains a metal selected from a group consisting of ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) and platinum (Pt); and electrolessly depositing a copper containing layer on the barrier layer.

[0015] Embodiments of the invention further provide a method for depositing a material on a contact level feature formed on a substrate, comprising providing a substrate that has one or more contact level features that have an exposed doped silicon containing region, depositing a first metal layer on the doped silicon containing region, depositing a barrier layer over the surface of the first metal layer, wherein the depositing the barrier layer comprises depositing a second layer over

the first layer, wherein the second layer comprises ruthenium and tantalum, and filling the contact level feature with a metal containing layer.

[0016] Embodiments of the invention further provide a method of forming an electrical contact on a silicon substrate, comprising providing a substrate containing an exposed tungsten-containing contact plug exposed that has an exposed gap formed therein, exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten-containing contact plug, filling the exposed gap with a fill material.

[0017] Embodiments of the invention further provide a method of forming an electrical contact on a silicon substrate, comprising providing a silicon substrate having a first dielectric layer which is disposed on a surface of the silicon substrate and a first aperture formed in the first dielectric layer, wherein a doped silicon containing region of the silicon substrate is exposed at the bottom of the first aperture, filling the first aperture formed in the first dielectric layer with a tungsten containing layer, wherein the tungsten containing layer is in electrical communication with the doped silicon containing region, removing an amount of the tungsten containing layer disposed on the first dielectric layer, wherein a gap formed in the tungsten containing layer during the step of filling the first aperture is exposed, and depositing a material on the surface of the silicon substrate to substantially cover the gap formed in the tungsten containing layer.

[0018] Embodiments of the invention further provide a method of forming an electrical contact on a silicon substrate, comprising providing a substrate containing first dielectric layer that contains at least one tungsten-containing contact plug that has an exposed surface, forming a second dielectric layer over the first dielectric layer and the tungsten-containing contact plug, forming a second aperture in the second dielectric layer that is in communication with the exposed surface of the tungsten-containing contact plug, and selectively filling the second aperture with a fill material.

[0019] Embodiments of the invention further provide a method for depositing a material on a substrate, comprising positioning a silicon containing substrate that has one or more contact level features that have an exposed doped silicon containing region, pretreating the exposed doped silicon containing region, wherein the pretreating process is adapted to remove an oxide layer from the exposed doped

silicon containing region, depositing a metal containing layer over a surface of the exposed doped silicon containing regions, and depositing a tungsten layer over the metal containing layer at a temperature between about 300 °C and about 400 °C, wherein during the tungsten layer deposition process a metal silicide is formed.

[0020] Embodiments of the invention further provide a method for depositing a material on a substrate, comprising positioning a silicon containing substrate that has one or more contact level features that have an exposed doped silicon containing region, pretreating the exposed doped silicon containing region, wherein the pretreating process is adapted to remove an oxide layer from the exposed doped silicon containing region, depositing a nickel containing layer over the bottom surface of the one or more contact level features, forming a nickel silicide layer by exposing the deposited nickel containing layer and silicon containing substrate to temperatures greater the 250 °C, depositing a cobalt containing layer over the nickel silicide layer, and depositing a tungsten layer on the cobalt containing layer.

[0021] Embodiments of the invention further provide a method for depositing a material on a substrate, comprising providing a substrate that has one or more contact level features that have an exposed doped silicon containing region, selectively depositing a metal containing layer over a surface of the exposed doped silicon containing regions, and depositing a tungsten layer on the metal layer at a temperature between about 300 °C and about 400 °C, wherein during the process of depositing tungsten layer a metal silicide is formed at the surface of the exposed doped silicon containing region.

[0022] Embodiments of the invention further provide a method of forming an interconnect on a silicon substrate, comprising providing a substrate having an aperture formed in a dielectric layer disposed on a surface of the substrate, wherein the aperture is in communication with an exposed surface of a tungsten-containing contact plug, dispensing a clean solution on an the exposed surface of the tungsten-containing contact plug, wherein the clean solution comprises hydrogen fluoride, disposing a preparation solution on the exposed surface of the tungsten-containing contact plug, wherein the preparation solution comprises a tungstate source, depositing a initiation layer on the exposed surface of the tungsten-containing contact plug using an activation solution, activating the initiation layer using a rinse activation solution, and selectively filling the second aperture with a fill material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] So that the manner in which the above recited features of the invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0024] Figures 1A-1F illustrate schematic cross-sectional views of an integrated circuit formed by a process described in the art;

[0025] Figures 2A-2G illustrate schematic cross-sectional views of an contact level feature formed by a process described within an embodiment herein;

[0026] Figure 3 is a flow chart depicting an deposition process as described within an embodiment herein;

[0027] Figure 4 is a flow chart depicting a deposition process as described within an embodiment herein.

[0028] Figures 5A-5D illustrate schematic cross-sectional views of an contact level feature formed by a process described within an embodiment herein;

[0029] Figure 6 is a flow chart depicting a deposition process as described within an embodiment herein;

[0030] Figures 7A-7C illustrate schematic cross-sectional views of an integrated circuit formed by a process to cap a defect within a contact plug described within an embodiment herein;

[0031] Figures 8A-8K illustrate schematic cross-sectional views of an integrated circuits formed by processes to fill defects within contact plugs described within embodiments herein;

[0032] Figures 9A-9F illustrate schematic cross-sectional views of an integrated circuit formed by another process to fill a defect within a contact plug described within an embodiment herein;

[0033] Figures 10A-10G illustrate schematic cross-sectional views of a method of forming an interconnect layer on a contact plug that is described within an embodiment herein;

[0034] Figure 11 illustrate schematic cross-sectional view of a MOS type integrated circuit formed by a process described in the art;

[0035] Figure 12 illustrates a flow chart depicting an electroless deposition process as described within an embodiment herein;

[0036] Figure 13A-G illustrate schematic cross-sectional views of an integrated circuit formed by a process to cap a defect within a contact plug described within an embodiment herein;

[0037] Figure 14 illustrates a flow chart depicting an electroless deposition process as described within an embodiment herein;

[0038] Figure 15 is a flow chart depicting a pretreatment process as described within an embodiment herein.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0039] Embodiments of the invention generally provide methods of filling contact level features formed in a semiconductor device by depositing a barrier layer over the contact feature and then filing the layer using an PVD, CVD, ALD, electrochemical plating process (ECP) and/or electroless deposition processes. The term "barrier layer" as used herein is generally intended describe a single layer, or two or more layers, that act as an adhesion layer and a diffusion barrier for the subsequently deposited metal layer(s). In one embodiment, the barrier layer has a catalytically active surface that will allow the electroless deposition of a metal on the barrier layer. In one aspect, the electrolessly deposited metal is copper or a copper alloy. Copper alloys may be useful to improve the device speed and performance, help prevent electromigration or stress migration degradation during subsequent processing, improve the manufacturing device yield and device lifetime due to electromigration or stress migration limitations of copper or allow the deposited materials to diffuse to unwanted areas in the formed device. In one embodiment, a portion of the barrier layer is purposely allowed to react with traces of residual oxide at the silicon junction of the contact level feature to form a low resistance connection

(*e.g.*, silicide formation). One embodiment includes a method of filling a contact level feature with a copper alloy by use of an electroless deposition process. In another embodiment, a copper alloy is used to from a thin conductive copper layer that is used to subsequently fill features with a copper containing material by use of an electrochemical plating process (ECP), PVD, CVD, and/or ALD deposition process.

Electroless Fill Contact Formation Process

[0040] The first novel method, illustrated in Figure 3, is a series of method steps 1000 that are used to fill a contact level feature. Figure 2A illustrates a cross-sectional view of substrate 1500 having a contact level aperture 1510 formed into dielectric layer 1504. The dielectric layer 1504 contains an insulating material that includes silicon dioxide, silicon nitride, SOI, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, California. Contact level aperture 1510 may be formed in dielectric layer 1504 using conventional lithography and etching techniques to expose the silicon junction 1502, such as a MOS type source or drain interface. Silicon junction 1502 is generally a doped silicon region formed in a silicon substrate, such as a n+ or p+ doped silicon region.

[0041] An oxide surface 1512 is usually formed at the silicon junction 1502 during previous etching and ashing processes used to form contact level aperture 1510. Oxide surface 1512 may be a continuous layer or a discontinuous layer across the surface of silicon junction 1502 and include a surface terminated with oxygen, hydrogen, hydroxides, a metal or combinations thereof. In examples wherein silicon junction 1502 contains a single crystal or polycrystalline silicon substrate the oxide surface 1512 is usually a silicon oxide surface. Also, where the silicon junction 1502 contains a doped layer and/or metal silicide formed on the surface, the oxide surface 1512 will generally contain metal oxides and silicon oxides present at the surface.

[0042] The first step of the method steps 1000 includes an optional pretreatment process step 1002, to remove the oxide layer so subsequent processes can be preformed on the surface of the silicon junction 1502. In this process step the substrate 1500 is exposed to a pretreatment process to form a treated surface (not shown) on the silicon junction 1502, which is substantially free of oxide surface

1512. The various processes that may be used to perform the pretreatment process step 1002 on the surface of the silicon junction 1502 include, but are not limited to wet-clean processes and plasma cleaning processes. Examples of various wet-clean processes that may be used to remove oxide surface 1512 are further described in the US Provisional Applications Serial No. 60/709,564 [APPM 9916.L05], filed 8/19/2005, US Provisional Applications Serial No. 60/703,538 [APPM 9916.L03], filed 7/29/2005, and US Provisional Applications Serial No. 60/663,493 [APPM 9916L], filed 3/18/2005, which are all incorporated by reference herein in their entirety. A plasma cleaning processes may be performed using a vacuum preclean chamber, such as a Siconi Preclean chamber available from Applied Materials Inc. of Santa Clara, California.

[0043] The second step includes a silicide layer formation step 1003 that is used to form a metal layer 1513 over the silicon junction 1502. In general the metal layer 1513 contains a metal that forms a silicide (*e.g.*, element 1513A in Figures 2C-2G) with the silicon material contained in the silicon junction 1502 during subsequent thermal processing steps. In general the deposited metal layer 1513 may contain one or more of the following elements nickel (Ni), titanium (Ti), tantalum (Ta), cobalt (Co), molybdenum (Mo) or tungsten (W). The metal layer 1513 may be selectively or non-selectively deposited using a conventional ALD or CVD deposition process. Also, the metal layer 1513 may be non-selectively deposited using a conventional PVD deposition process. Preferably, the metal layer 1513 is deposited using an electroless deposition process, such as the processes described in United States Provisional Patent Application Serial number 60/703,538, filed 7/29/2005 [APPM 9916L03] and United States Provisional Patent Application Serial number 60/731,624, filed 10/28/2005 [APPM 10659L], which are herein incorporated by reference. In one embodiment, the metal layer 1513 is a nickel layer containing layer that has been deposited using an electroless deposition process. In one aspect, the metal layer 1513 when deposited is between about 5 and about 100 angstroms (Å) thick. Preferably, the metal layer 1513 is from about 10 Å to about 50 Å thick, and more preferably, from about 10 Å to about 30 Å. In one aspect, to achieve a contact resistance of 45 ohms at 50 nm plug with 5:1 aspect ratio a metal layer 1513 having a resistivity less than about 35 microohm-cm, and preferably less than about 10 microohm-cm, and more preferably less than about 5 microohm-cm.

[0044] In one aspect of the method steps 1000 (not shown in Figures 2A-2G or Figure 3), the metal silicide layer 1513A is formed at the silicon junction 1502 by use of a thermal process, such as a conventional anneal or RTP process, prior to performing the subsequent method steps. Generally, the silicide formation process step is performed in a vacuum or inert environment to prevent the oxidation or damage to the surface of the metal silicide layer 1513A and contact level aperture 1510 surfaces. Typically, the metal silicide layer 1513A formed at the silicon junction 1502 is a nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, tungsten silicide, tantalum silicide, or other common metal silicides. In one aspect, where a nickel silicide layer is to be formed at the silicon junction 1502 the substrate may be heated to a temperature between about 300 °C and about 450 °C for a period of time that allows a silicide layer of a desired thickness and resistance to be formed. The silicide formation process step is used to reduce the contact resistance between the metal layers deposited in the contact level aperture 1510 and the silicon junction 1502.

[0045] In one embodiment of the method steps 1000 (not shown in Figure 3), an optional cleaning process is performed on the surface of the formed metal silicide layer 1513A, or metal layer 1513, using a very dilute solution of hydrofluoric acid (HF) (*e.g.*, 100:1 ratio of DI Water:HF) prior to depositing barrier layer 1521. The optional cleaning process step may be used to remove any surface oxides formed on the exposed surfaces of the metal silicide layer 1513A or metal layer 1513. The removal of these oxides can help reduce the contact resistance of the formed structure.

[0046] In one embodiment, a thin layer cobalt containing layer (step 1004 in Figure 3) may be deposited over the metal silicide layer 1513A to inhibit the diffusion of the metal layer component(s) into the subsequently deposited layers or other contact level aperture 1510 elements. In one aspect, step 1004 is completed before the silicide layer formation step 1003 and thus is deposited directly on the metal layer 1513. In general the cobalt containing layer (not shown) is a binary alloy or ternary alloy, such as cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof. In

one aspect, the cobalt containing layer (not shown) is between about 5 and about 100 angstroms (Å) thick. Preferably, the cobalt containing layer is from about 5 Å to about 50 Å thick, and more preferably, from about 10 Å to about 30 Å. Preferably, the cobalt containing layer is deposited using an electroless deposition process, such as the processes described in United States Patent Application serial number 11/040,962, filed 1/22/2005 [APPM 8926] and United States Patent Application serial number 10/967,644, filed 10/18/2004 [APPM 8660.02], which are herein incorporated by reference..

[0047] The third step includes a barrier layer deposition step 1005 that is used to form a barrier layer 1521 over the metal silicide layer 1513A. While the discussion below describes the deposition of the barrier layer 1521 over the metal silicide layer 1513A, this is not intended to be limiting as to processing sequence described herein since the thermal processes used to form the metal silicide layer 1513A may be performed after the barrier layer 1521 or other subsequent layers are formed. In general the barrier layer 1521 contains one or more layers of material that act as an adhesion layer and a diffusion barrier for the subsequently deposited metal layer 1525. In one aspect, the barrier layer 1521 is between about 5 and about 100 angstroms (Å) thick. Preferably, the barrier layer 1521 is from about 10 Å to about 50 Å thick, and more preferably, from about 10 Å to about 30 Å. In one embodiment, a portion of the barrier layer 1521 is selected so that it will react with traces of residual oxide at the silicon junction 1502 to further provide a low resistance connection to the metal silicide layer 1513A.

[0048] In one aspect, the exposed surface of the barrier layer 1521 may have a catalytically active surface for the subsequently deposited metal layers (*e.g.*, metal layer 1525) using an electroless deposition process. For example, in some embodiments, it may be desirable to form a barrier layer 1521 that has an exposed surface layer that contains a group VIII metal, such as ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) or platinum (Pt) to serve as a catalytically active initiation and adhesion layer for the subsequently deposited metal layer 1525 (*e.g.*, copper (Cu)).

[0049] The barrier layer 1521 may also contain one or more layers that contain titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), molybdenum (Mo), tungsten nitride (WN), tungsten carbon nitride (WCN),

molybdenum carbon nitride (MoCN), tantalum carbon nitride (TaCN), titanium silicon nitride (TiSiN), or any other combinations thereof. The barrier layer deposition step 1005 may be performed by use of conventional PVD, CVD, plasma enhanced CVD (PECVD), ALD, plasma enhanced ALD (PEALD). In one aspect, a non-selective deposition process is used, such as a PVD, non-selective CVD, non-selective plasma enhanced CVD, non-selective ALD, and/or non-selective plasma enhanced ALD process(es). Examples of an exemplary CVD and ALD type deposition processes and hardware configuration are further described in the commonly assigned United States Patent Application number 6,951,804, the commonly assigned United States Patent Publication number 20030108674 [APPM 6043], the commonly assigned United States Patent Publication number 20050106865 [APPM 6303.P3], and the commonly assigned United States Patent Application publication number 20030049931 [APPM 5350], which are all herein incorporated by reference.

[0050] In one aspect, the barrier layer 1521 is deposited in the barrier deposition step 1005 by use of a PVD deposition process that is used to deposit a layer that contains two or more elements, such as a ruthenium and tantalum alloy. Ruthenium and Tantalum alloys are useful, since it they have the combined benefits of blocking copper diffusion as effectively as conventional tantalum barrier layers and providing a suitable surface for direct electroless and/or electrochemical plating of a copper seed layer thereon. In general Ru-Ta alloys do not suffer from the same adhesion problems as found with conventional Ta and TaN barrier layers. Therefore, in one aspect of the invention, the barrier layer 1521 contains a Ru-Ta alloy that contains between about 70 atomic % and about 95 atomic % ruthenium and the balance tantalum. In another aspect, the barrier layer 1521 preferably contains a Ru-Ta alloy that contains between about 70 atomic % and about 90 atomic % ruthenium and the balance tantalum. In yet another aspect, the barrier layer 1521 more preferably contains a Ru-Ta alloy that contains between about 80 atomic % and about 90 atomic % ruthenium and the balance tantalum. In one aspect, it may be desirable to select a Ru-Ta alloy that does not contain regions of pure tantalum on the surface. In one aspect, a PVD type deposition process is used to deposit a barrier layer 1521 that contains the Ru-Ta alloy containing about 90 atomic % ruthenium and the balance tantalum (*e.g.*, 0.9Ru:0.1Ta).

[0051] In one embodiment, a selective deposition process may be used, such as electroless, selective CVD, selective PECVD, selective ALD, and/or selective PEALD, to form a barrier layer 1521 that may only cover the exposed area(s) of the metal silicide layer 1513A. Also, one or more of the layers in the barrier layer 1521 may be selectively deposited by use of an electroless deposition process. The electroless deposition process may be used to form a layer that contains a binary alloy or ternary alloy, such as cobalt boride (CoB), cobalt phosphide (CoP), nickel boride (NiB), nickel phosphide (NiP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), nickel rhenium boride (NiReB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof. The film composition of the binary or ternary alloys can be preferably designed to have a resistivity in the range of about 1 to about 200 microohm-cm.

[0052] In one aspect, a nickel containing barrier layer 1521 is formed by performing two or more process steps which may include depositing a self-assembled-monolayer (SAM) material on to the surface of the substrate 1500 (*e.g.*, covers field region 1505 and in the contact level aperture 1510) and then electrolessly depositing a nickel layer onto the deposited SAM layer. Examples of a prototypical SAM materials include, but are not limited to aminopropyltriethoxy silane (APTES) that may be deposited using a vapor phase deposition process. In one aspect, it may be desirable to perform a hydrogen and/or water containing plasma treatment process to the metal silicide layer 1513A, field region 1505 and contact level aperture 1510 prior to depositing the SAM layer to form a silanol (*e.g.*, Si-OH) surface to promote the adhesion of the SAM layer. In one aspect, the hydrogen and/or water containing plasma treatment is used to perform the photoresist stripping process.

[0053] In another aspect, the barrier layer 1521 contains a multilayer stack of materials that are deposited on the field region 1505 and in the contact level aperture 1510. Examples of multilayer stacks that may be used to form a barrier layer 1521 that has desirable diffusion barrier and contact resistance properties

include, but are not limited to layers containing Ti/TiN/Ru, Ti/TiN/Co, Ti/TiN/Ni, Ti/Ru, Ta/Ru, TaN/Ru, Ni/Co, Ti/TiN/W/Ni, and Ti/TiN/W/Co. The nomenclature used herein to define a multilayer stack is intended to describe a barrier layer 1521 that contains discrete layers that may be arranged in a any desired order (*e.g.*, Ni/Co = Ni on Co or Co on Ni) as long as the final exposed surface of the barrier layer 1521 is catalytically active to enable a subsequent electroless deposition process or can be readily rendered catalytically active by performing a activation process (*e.g.*, palladium activation). For example, a Ti/TiN/Ru stack contains three layers, which are a titanium (Ti) containing layer, a titanium nitride (TiN) containing layer, and a ruthenium (Ru) containing layer (*e.g.*, pure Ru, 0.9Ru:0.1Ta, etc.), that may be arranged so that the Ti containing layer is deposited on the metal silicide layer 1513A and then the TiN containing layer is deposited on the Ti layer and then the Ru containing layer is deposited over both layers. The multilayer stacks that may be used to form a barrier layer 1521 may be deposited by use of one or more conventional deposition techniques, such as PVD, CVD, PECVD, ALD, PEALD, ECP, or electroless deposition processes.

[0054] In yet another aspect, the barrier layer 1521 may contain a multilayer stack of metals, such as, Ti, TiN, Ti/TiN/W, Ti/TiN, Ti/W, Ta/TaN/W, Ta/W, Ni/W, and Co/W that have an additional catalytic layer deposited on the top surface so that an electroless layer can be deposited thereon. A typical catalytic layer that is deposited on these multilayer stacks may be a ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) or platinum (Pt) containing layer. The multilayer stacks that may be used to form a barrier layer 1521 may be deposited by use of one or more conventional deposition techniques, such as PVD, CVD, PECVD, ALD, PEALD, ECP, or electroless deposition processes.

[0055] In one embodiment, it may be desirable to deposit a single layer type barrier layer 1521 that contains a material, such as titanium, palladium, platinum or ruthenium prior to electrolessly depositing the subsequent metal layer(s) (*e.g.*, metal layer 1525). In one example, the titanium (Ti) is deposited using a two step process that contains a preclean process step (*e.g.*, performed in a Siconi, Preclean II or Preclean XT chambers available from Applied Materials, Inc. of Santa Clara, California) and then PVD titanium deposition step using a Endura™ RTM PVD chamber, which are both available from Applied Materials, Inc. of Santa Clara,

California. In another example, a ruthenium (Ru) and tantalum (Ta) alloy layer (*e.g.*, 0.9Ru:0.1Ta) is deposited using a two step process that contains a preclean process step (*e.g.*, Siconi) and then PVD ruthenium and tantalum alloy deposition step using a Endura™ RTM PVD chamber. In another example, a ruthenium (Ru) layer is deposited using a CVD, ALD or PEALD processes. In another example, the ruthenium layer is deposited by use of an electroless displacement plating process using a ruthenium chloride solution. In another example, a palladium (Pd) layer is deposited using either an ALD, PEALD, CVD, or PECVD process or by use of an electroless displacement plating process. The thickness and the choice of the type of material that may be used depends on the types subsequent processes performed on the formed device (*e.g.*, thermal cycling) and the barrier properties of the material or the stack formed using the material.

[0056] In one embodiment, an optional metal removal step 1006 may be added to the method steps 1000 to remove any deposited barrier layer 1521 from the field region 1505 (Figures 2A-B) by use of a wet clean process, CMP process, electrochemical process or other comparable material removal processes. A CMP process may be performed using a Reflexion™ CMP system available from Applied Materials Inc. of Santa Clara, California.

[0057] In the deposit a metal alloy layer step 1008, a metal layer 1525 is deposited so that it fills the contact level aperture 1510. In one aspect, this process is performed using an electroless deposition process. In general the contact level aperture 1510 can be filled with a metal, such as copper (Cu), nickel (Ni), cobalt (Co), ruthenium (Ru), tungsten (W) or combinations thereof. In one embodiment, the metal layer 1525 is formed by use of a metal layer electroless deposition solution (discussed below) that contains only a copper ion source and a reducing agent that allows the deposition of copper.

[0058] In another embodiment, metal layer 1525 is formed by use of metal layer electroless deposition solution (discussed below) that contains two or more metal ion sources and a reducing agent that allows the co-deposition of two or more metals. In one aspect, one of the metals ions is a copper ion and the other metal ion(s) are a metal selected from a group consisting of aluminum (Al), indium (In), molybdenum (Mo), tungsten (W), manganese (Mn), cobalt (Co), tin (Sn), nickel (Ni), magnesium (Mg), rhenium (Rh), beryllium (Be), phosphorus (P), boron (B), gallium

(Ga), or ruthenium (Ru). In one aspect, a metal alloying element that is more electropositive than copper may be beneficial to improve the oxidation resistance and corrosion resistance of the deposited film. The addition of the alloying element will also generally improve the stability of the formed device by reducing the ability of some of the elements in deposited layer to rapidly diffuse into silicon or the silicon oxides. Examples of various chemistries that may be used to form the metal layer 1525 are further described below. In this configuration the electrical resistance of the electrical connection formed using method steps 1000 will be reduced, since a significant part, or volume, of the contact level aperture 1510 will contain predominantly copper, or a copper containing alloy, that has a resistivity lower than a conventional tungsten plug. The use of a metal layer 1525 is advantageous since by the selection of a desirable elements, such as a copper aluminum alloy, copper indium alloy, copper manganese alloy, a copper tungsten alloy, or a copper molybdenum alloy, to name just a few, the resistance of the formed connection will be reduced versus a conventional tungsten plug, and the metal alloy will have better electromigration performance than pure copper and/or diffusion resistance. It should be noted that the term "alloy" as used herein is not intended to be limited to the case of where one element forms a bond or compound with another element, and is intended to generally describe a film that contains a percentage of two or more elements. In one example, one of the elements may be positioned in an interstitial site or be deposited on the grain boundaries of a formed crystalline or amorphous structure containing a second element (*e.g.*, Cu), rather than form a compound containing two or more elements. Further, in one aspect of the invention, due to the addition of the alloying element to copper, the copper atoms in the formed copper containing layer become less mobile thus reducing, or possibly eliminating the need for the barrier layer 1521. Thus, in some cases by adding an alloying element to a metal, such as copper will tend prevent or inhibit the metal from diffusing into unwanted areas of the formed device. In one aspect, it may be desirable to have the second metal ion source (*i.e.*, metal ion other than copper ions) in the metal layer electroless deposition solution because the second ion is better suited to form an adhesion promoting interface between the barrier layer 1521 and the growing alloy layer (*i.e.*, element 1525 and 1526).

[0059] In another embodiment of the deposit a metal alloy layer step 1008, the metal layer 1525 is formed using a metal layer electroless deposition solution that contains one or more metal ion sources and a reducing agent that allows the co-deposition of two or more metals. In one aspect, one of the metals ions is a cobalt or nickel based alloy can be deposited on top of these materials by electroless process. For example, the cobalt or nickel based alloys may be a binary alloy or ternary alloy, such as cobalt boride (CoB), cobalt phosphide (CoP), nickel boride (NiB), nickel phosphide (NiP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), nickel molybdenum phosphide (NiMoP), nickel molybdenum boride (NiMoB), nickel rhenium phosphide (NiReP), nickel rhenium boride (NiReB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof. The selection of materials used to form the metal layer 1525 is influenced by the resistivity of the films deposited. In one aspect, all the deposited films are pure metals and thus their resistivity is less than about 10 microohms-cm, and more preferably less than about 5 microohms-cm. In another aspect, a stack of discrete metal layers having different thickness may be used to form a device that has good diffusion barrier properties as well as lower overall contact resistance of the device.

Second Contact Fill Formation Process

[0060] Another novel method of filling a contact level feature is illustrated in Figures 2A-2D, 2F-2G and 4. Figure 4 illustrates is a series of method steps 1001 that are used to fill a contact level feature. The steps 1002-1006 in the method steps 1001 are generally the same as the method steps 1000 and thus are not recited below. The method steps 1001 differ from the method steps 1000, described above, due to the variation of only depositing a thin metal layer 1526 (step 1009 in Figure 4) and then filling the contact level aperture 1510 with a second metal layer 1527 (step 1010 in Figure 4).

[0061] In one embodiment of the method steps 1001, after performing steps 1002-1006, the step 1009 is performed to deposit a thin metal layer 1526 on the field region 1505 and in the contact level aperture 1510. Step 1009 is similar to step 1008 described above in conjunction with Figure 3, except that the thin metal layer 1526 is formed rather than filling the contact level aperture 1510. Therefore, as

noted above the metal layer 1526 will contain one or more metal elements that are deposited using an electroless deposition process that utilizes the metal layer electroless deposition solution (discussed below). The use of an electroless deposition process may be especially useful due to the deposition of a conformal coating having a uniform thickness formed over the contact level aperture 1510. In one aspect, electrolessly deposited films are preferred, since they generally do not contain the amount of carbon that CVD and ALD deposited films contain from the incorporation of the CVD or ALD precursor materials in the deposited film. The incorporation of carbon in the deposited film will affect the resistivity and adhesion of the deposited layer to prior or subsequently deposited layers. Electrolessly deposited films may also be favored over PVD deposited films, because a thin or discontinuous PVD deposited layer will be formed in typical ≤45nm type features due to the fact that it is a line-of-sight type deposition process. Electroless deposition processes are also useful to form metal layers that have two or more metal components contained therein. In one aspect, it may be desirable to varying composition of the electrolessly deposited layer that contains two or more metal components. An exemplary process and hardware that may be used to form a metal layer having a varying composition is described in the commonly assigned United States Patent Application Serial No. 11/040,962 [APPM 8926], filed 1/22/2005, which is incorporated by reference herein in its entirety.

[0062] In one aspect, the thin metal layer 1526 is thick enough to reduce the terminal effect of the subsequently deposited second metal layer 1527 by use of an electrochemical plating process (ECP). In another aspect, the thin metal layer 1526 is thick enough to reduce or inhibit the diffusion of the material in the subsequently deposited second metal layer 1527 into the silicon junction 1520, or adjacent devices elements, and prevent diffusion of silicon in the silicon junction 1520 from diffusing into the second metal layer 1527. In one aspect, the thin metal layer 1526 is deposited to a thickness between about 10 Å and about 100 Å. In general, ECP deposition processes have advantages over CVD, ALD and PVD type processes, since the selection of the electrolyte components (*e.g.*, additives, acid concentration) and various process recipe parameters (*e.g.*, current density) apertures of varying sizes can be filled without forming voids or gaps in the deposited layer or incorporating carbon in the deposited film. Examples of exemplary electrochemical

deposition processes and hardware configuration are further described in the commonly assigned United States Patent Application number 6,596,151, and the commonly assigned copending United States Patent Application serial number 10/854,006, filed 5/25/2004 [APPM 7669.P4] and United States Patent Application serial number 10/616,284, filed 7/28/2003 [APPM 7669], which are all herein incorporated by reference.

[0063] In step 1010, a second metal layer 1527 is deposited on the thin metal layer 1526 to fill the contact level aperture 1510. In one embodiment, the second metal layer 1527 may be a metal alloy that contains one or more elements, such as copper (Cu), aluminum (Al), indium (In), molybdenum (Mo), tungsten (W), manganese (Mn), cobalt (Co), rhenium (Rh), ruthenium (Ru), or combinations thereof. In another embodiment, the second metal layer 1527 is a pure copper (Cu) layer. The second metal layer 1527 may be deposited by any conventional deposition technique, such as PVD, CVD, PECVD, ALD, PEALD, ECP, or electroless deposition processes. In general, the material from which the second metal layer 1527 is formed is selected so that it has a high electrical conductivity to reduce the overall resistance of the circuit formed using the contact level aperture 1510.

[0064] The formed device feature using the method steps 1001 may be advantageous since it combines the use of a thin metal layer 1526 and high conductivity second metal layer 1527 to form a device feature that has a lower resistivity than conventional tungsten deposited materials, while also inhibiting the diffusion of the second metal layer 1527 to unwanted regions of the device due to the barrier-like properties of the thin metal layer 1526.

Third Contact Fill Formation Process

[0065] Another novel method of filling a contact level feature is illustrated in Figures 5A-5F and 6. Figure 6 illustrates is a series of method steps 900 that are used to fill a contact level feature (*e.g.*, contact level aperture 1510) using the methods described in methods steps 1000 or 1001, plus some additional preprocessing steps 992-998. The steps 1002, 1005, 1008, 1009 and 1010 in the method step 900 are generally the same as the steps contained in the method steps 1000 or 1001 and thus are not recited below. One will note that the silicide layer

formation step 1003, the optional deposit a cobalt containing layer step 1004, and the optional metal removal step 1006 found in method steps 1000 and 1001 have been removed, since they are performed at different stages of the process sequence or they are may not be required. Figure 5A illustrates a silicon junction 1502 formed on a substrate 1490, wherein the silicon junction 1502 generally contains a doped silicon region 1498 that has an exposed surface 1499 on which the subsequent process steps will be performed.

[0066] Referring to Figures 5B and 6, in the deposit a metal containing layer step 992, or the first step of the method steps 900, a metal containing layer 1503 is deposited on the doped silicon region 1498 of the substrate 1490. In one embodiment, the metal containing layer 1503 is deposited using an electroless deposition process. For example, an electroless deposition process may be used to deposit a nickel containing layer on the doped silicon region 1498. An exemplary electroless nickel deposition process is further described in the commonly assigned US Provisional Patent Application Serial No. 60/703,633 [9916.L04], filed 7/29/2005, the commonly assigned US Provisional Patent Application Serial No. 60/703,538 [9916.L03], filed 7/29/2005, the commonly assigned US Provisional Applications Serial No. 60/709,564 [9916.L05], filed 8/19/2005, and the commonly assigned US Provisional Patent Application Serial No. 60/663,493 [9916L], filed 3/18/2005, which are all incorporated by reference herein in their entirety.

[0067] Referring to Figures 5D and 6, in the form the contact level aperture step 998 a contact level aperture 1510 is formed over the metal containing layer 1503 and the optional cobalt containing layer 1506 using conventional dielectric deposition, lithography and etching techniques. After step 998 is completed then the barrier deposition step 1002 can performed following the methods described in Figures 3 or 4.

Example - Nickel Electroless Chemistry

[0068] In one example, an electroless solution contains: nickel sulfate with a concentration of about 60 mM; dimethylaminoborane (DMAB) in a concentration of about 14 mM; citric acid in a concentration of about 60 mM; diethanolamine (DEA) in a concentration of between about 33 mM and about 115 mM; glycine in a concentration between about 5 mM to about 50 mM; boric acid in a concentration

between about 5 mM and about 10 mM; lactic acid in a concentration of about 120 mM; tetramethyl ammonium hydroxide (TMAH) in a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 9.2 to about 9.6, such as about 9.4. The electroless deposition process may be conducted at a temperature in a range from about 35°C to about 120°C, preferably from about 80°C to about 85°C. The water may be degassed, preheated and/or deionized water. Degassing the water reduces the oxygen concentration of the subsequently formed electroless solution. An electroless solution with a low oxygen concentration (*e.g.,* less than about 100 ppm) may be used during the deposition process. Preheated water allows forming the electroless solution at a predetermined temperature just below the temperature used to initiate the deposition process, thereby shortening the process time.

[0069] Referring to Figure 6, next an optional silicide formation process step 994, is used to reduce the contact resistance between the metal containing layer 1503 deposited on the surface 1499 of the doped silicon region 1498 by causing the deposited metal containing layer 1503 to form a nickel silicide (Ni_xSi_y). The metal containing layer 1503 formed in step 992 should have a sufficient thickness to form a good electrical contact (*e.g.*, ohmic contact) between the subsequently deposited layers (*e.g.*, barrier layer 1521) and the doped silicon region 1498 in the silicon junction 1502. Typical silicide formation processes include heating a substrate 1490 to a temperature that will cause the nickel in the metal containing layer 1503 to form a nickel silicide. Generally, the silicide formation process step 994 is performed in a vacuum or inert environment to prevent the oxidation of the surface of the metal containing layer 1503.

[0070] Referring to Figures 5C and 6, in the optional deposit a cobalt containing layer step 996, a cobalt containing layer 1506 is deposited on the metal containing layer 1503. In one embodiment, step 996 is used to form a cobalt alloy layer, such as CoB, CoP, CoWP, CoWB, CoMoP, CoMoB, CoReB, or CoReP using electroless deposition techniques further described in the copending US Provisional Patent Application Serial No. 60/703,538 [APPM 9916.L03], filed 7/29/2005, the copending US Patent Application Serial No. 11/040,962 [APPM 8926], filed 1/22/2005, the copending US Patent Application Serial No. 10/967,644 [APPM 8660], filed

10/15/04, and the copending US Patent Application Serial No. 10/967,919 [APPM 8660.02], filed 10/18/2004, which are all incorporated by reference herein in their entirety. The addition of the cobalt containing layer 1506 layer over the metal containing layer 1503 will help to isolate the nickel silicide layer formed during step 994 from being attacked during the subsequent deposition dielectric etch step(s) (*e.g.*, step 998).

Examples - Cobalt Electroless Chemistries

[0071] In one aspect, an electroless solution for depositing cobalt boride contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (*e.g.,* TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit cobalt boride may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 80°C, and more preferably from about 65°C to about 75°C, such as about 70°C.

[0072] In one aspect, an electroless solution for depositing metallic cobalt contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; hydrazine hydrate with a concentration in a range from about 100 mM to about 2 M, preferably from about 200 mM to about 1 M, and more preferably from about 300 mM to about 700 mM, such as about 500 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 70 mM, such as about 50 mM; and an optional pH adjusting agent (*e.g.,* TMAH) with a concentration to adjust the

electroless solution to a have pH value in a range from about 10 to about 14, preferably from about 11.5 to about 13, and more preferably from about 12.2 to about 12.8, such as about 12.5. In one example, a pH value is about 11.5 or higher, preferably, about 12.0 or higher, and more preferably, about 12.5 or higher. The electroless deposition process to deposit metallic cobalt may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 90°C, and more preferably from about 70°C to about 80°C, such as about 75°C.

[0073] The "water" component used in any of the above examples may be degassed, preheated and/or deionized water. Degassing the water reduces the oxygen concentration of the subsequently formed electroless solution. An electroless solution with a low oxygen concentration (*e.g.,* less than about 100 ppm) may be used during the deposition process. Preheated water allows forming the electroless solution at a predetermined temperature just below the temperature used to initiate the deposition process, thereby shortening the process time.

Metal Layer Electroless Deposition Solution(s)

[0074] In one aspect, the metal layer electroless deposition solution, which is used to form the metal layer 1525 or thin metal layer 1526 generally contains two metal ion sources and reducing agent that is used to form a high conductivity metal alloy layer. In one embodiment, one of the metal ion sources is copper ion that is added to the metal layer deposition solution.

[0075] In one embodiment, the metal layer electroless deposition solution is an aqueous solution that may contain a copper source, a second metal ion source, a reductant, a complexing agent, and a pH adjusting agent. The copper ion source within the metal layer electroless deposition solution may have a concentration in a range from about 5 mM to about 100 mM, preferably from about 25 mM to about 75 mM. Copper sources provide copper ions (*e.g.,* Cu^{1+} or Cu^{2+}) dissolved within the electroless solution to be reduced out as the deposited copper-containing material. Useful copper sources include copper sulfate, copper chloride, copper acetate, copper phosphate, copper pyrophosphate, copper fluoroborate, copper formate, derivatives thereof, hydrates thereof or combinations thereof.

[0076] In one embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is an aluminum ion source, to form a metal layer that contains predominantly copper and small amounts of aluminum. Sources of aluminum that can be added to the metal layer electroless deposition solution may be aluminum ammonium sulfate ($AlNH_4(SO_4)_2 \bullet 12H_2O$), potassium alum dodecahydrate ($AlK(SO_4)_2 \bullet 12H_2O$), aluminum sulfate hexadecahydrate ($Al_2(SO_4)_3 \bullet 16H_2O$), derivatives thereof, or combinations thereof. In one embodiment, the metal layer electroless deposition solution contains about 7 grams/liter of a copper sulfate ($CuSO_4$) and between about 0.5 grams/liter and about 6 grams/liter of aluminum ammonium sulfate. In another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is an indium ion source, to form a metal layer that contains predominantly copper and small amounts of indium. Typical sources of indium that can be added to the metal layer electroless deposition solution may be indium(III) sulfate hydrate ($In_2(SO_4)_3 \bullet xH_2O$) and Indium(III) nitrate hydrate ($In(NO_3)_3 \bullet xH_2O$), derivatives thereof, or combinations thereof. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a tungsten ion source, to form a metal layer that contains predominantly copper and small amounts of tungsten. The tungsten source may include various tungstate salts, such as ammonium tungstate ($(NH_4)_2WO_4$), or other WO_4^{2-} sources, derivatives thereof and/or combinations thereof. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a molybdenum ion source, to form a metal layer that contains predominantly copper and small amounts of molybdenum. A typical molybdenum source is molybdenum sulfate. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a magnesium ion source, to form a metal layer that contains predominantly copper and small amounts of magnesium. The magnesium sources may include magnesium sulfate, magnesium acetate tetrahydrate ($(CH_3COO)_2Mg \bullet 4H_2O$), manganous sulfate, manganous acetate, manganous trifluoroacetate or other Mg^{2+} sources, derivatives thereof, or combinations thereof. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a beryllium ion source, to form a

metal layer that contains predominantly copper and small amounts of beryllium. The beryllium sources may include beryllium sulfate or other Be^{2+} sources, derivatives thereof, or combinations thereof. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a titanium ion source, to form a metal layer that contains predominantly copper and small amounts of titanium. The titanium sources generally include ion sources that contain Ti^{3+} and Ti^{2+} complexes. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a gallium ion source, to form a metal layer that contains predominantly copper and small amounts of gallium. The gallium sources may include gallium sulfate or other $Ga^{1+,}$ Ga2+, or Ga+3 sources. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a boron ion source, to form a metal layer that contains predominantly copper and small amounts of boron. The boron sources may include tetramethylammonium borohydride or dimethylaminoborane (DMAB). In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a phosphorous ion source, to form a metal layer that contains predominantly copper and small amounts of phosphorus. The phosphorus sources may include a hypophosphite salt such as tetramethylamonium hypophosphite or ammonium hypophosphite. In yet another embodiment, the metal layer electroless deposition solution contains a copper ion source and a second ion source that is a tin ion source, to form a metal layer that contains predominantly copper and small amounts of tin. The tin sources may include tin sulfate ($SnSO_4$) or other Sn^{2+} or Sn^{4+}sources.

[0077] The reducing agent, or reductant, within the metal layer electroless deposition solution may have a concentration in a range from about 10 mM to about 2 M, preferably from about 20 mM to about 500 mM. Reductants provide electrons to induce chemical reduction of the metal ions that form and deposit the metal alloy, which in one embodiment is a copper-containing alloy material. Reductants may include organic reductants (*e.g.,* formaldehyde or glyoxylic acid), hydrazine, organic hydrazines (*e.g.,* methyl hydrazine), hypophosphite sources (*e.g.,* hypophosphorous acid (H_3PO_2), ammonium hypophosphite ($(NH_4)_{4-x}H_xPO_2$) and salts thereof),

borane sources (*e.g.,* dimethylamine borane complex ($(CH_3)_2NH•BH_3$), DMAB), trimethylamine borane complex ($(CH_3)_3N•BH_3$), TMAB), *tert*-butylamine borane complex ($^tBuNH_2•BH_3$), tetrahydrofuran borane complex ($THF•BH_3$), pyridine borane complex ($C_5H_5N•BH_3$), ammonia borane complex ($NH_3•BH_3$), borane (BH_3), diborane (B_2H_6), tetraethylammonium borohydride ($(C_2H_5)_4N(BH_4)$), derivatives thereof, complexes thereof or combinations thereof. In one embodiment, the metal layer electroless deposition solution contains glyoxylic acid in a range between about 5g/L and about 30g/L. In another embodiment, the formulation may also contain formate ion, generated as by the neutralization of formic acid or simply by the use of cupric formate at the copper precursor.

[0078] In one embodiment, it is desirable to form an electroless plating solution that is optimized to perform a single wafer puddle plating process. Single use electroless puddle plating processes have advantages over re-circulating electroless deposition processes, since the deposition rate can be made more aggressive (i.e., higher deposition rate) without the issue of particle growth in the electroless plating solution or wafer-to-wafer electrolyte solution variation due to bath depletion. To meet the current cost-of-ownership (CoO) requirements, much higher deposition rate are required when performing electroless deposition fill processes. One such chemistry that can be used to obtain high deposition rates is a formulation such as, the novel copper formulation described below.

[0079] Polymeric additives are generally added to the metal layer electroless deposition solution to suppress the metal deposition on the field region (*e.g.*, item 1505 Figure 2C) by initially adsorbing onto underlying catalytic surfaces (*e.g.,* barrier layer 1521) and therefore suppressing the rate of deposition. An exemplary polymeric additive, due to its size (*e.g.*, molecular weight), will generally have a limited ability to diffuse into and thus inhibit the growth of the deposited film in the recess of the contact level aperture 1510, but will be able to suppress the growth of the deposited film on the field region. The polymeric additives may have a concentration in a range from about 0.5 parts-per-million (ppm) to 500 ppm. In one aspect, the polymeric additives generally include poly(4-ammonium styrenesulfonic acid), poly(acrylic acid-co-maleic acid), 4-vinylphenol-co-hydroxyethyl methacrylate, Poly(acrylic acid-*co*-acrylamide) potassium salt, Poly[2,6-bis(hydroxymethyl)-4-methylphenol-co-4-hydroxybenzoic acid], Poly(acrylamide-*co*-

diallyldimethylammonium chloride), Poly(vinylpyridine), Poly(2-acrylamido-2-methyl-1-propanesulfonic acid), Poly(anilinesulfonic acid), Poly(4-vinylphenol), derivatives thereof, and/or combinations thereof.

[0080] In one embodiment, additives such as polyethylene glycol (PEG), polypropylene glycol (PPG), polyoxyethylene-polyoxypropylene copolymer (POCP), benzotriazole (BTA), dipyridyl, dimethyl dipyridyl, derivatives thereof or combinations thereof are added to metal layer electroless deposition solution. The additives, or "suppressors," can be added to the electroless deposition solution in a concentration in a range between about 20 ppb and about 600 ppm. In another aspect, a PEG type additive is added in a concentration range of about 0.05 to about 1 g/l.

[0081] In one aspect, one or more of the following chelators or complexing agents, may also be added to the metal layer electroless deposition solution which include: amino acids, carboxylic acids, dicarboxylic acids, polycarboxylic acids, amino acids, amines, diamines, polyamines, alkylamines, alkanolamines and alkoxyamines. The additional complexing agents may have a concentration in a range from about 10 mM to about 2 M, preferably from about 20 mM to about 300 mM. Complexing agents may include, but are not limited to citric acid, citrates, glycolic acid, glycine, malonic acid, maleic acid, lactic acid, ethylenediaminetetraacetic acid (EDTA), ethylenediamine (EDA), triethylene tetramine (TETA), diaminoethane, monoethanolamine, diethanolamine (DEA), triethanolamine (TEA), hydroxylamine hydrochloride, and ammonia, derivatives thereof, salts thereof or combinations thereof.

[0082] In one embodiment, the metal layer electroless deposition solution contains EDTA in a ratio relative to copper that is less than about 6:1 (*e.g.*, EDTA concentration to Cu concentration), and more preferably at a ratio of about 2:1. In one embodiment, the EDTA concentration in the metal layer electroless deposition solution is in a range between about 5 g/L and about 30 g/L, and the copper concentration is in a range between about 2g/L and about 12 g/L. The use of EDTA at the lower concentration will help to maintain a consistent deposition rate throughout a deposition process that uses a single use electroless puddle plating type process. Traditional, electroless copper electroless plating processes employ higher EDTA to copper concentrations to achieve much greater bath stability at the expense of deposition rate. These traditional electroless plating baths are harder to

use since their ability to modulate fill characteristics is significantly reduced due to the adsorption of additives on the exposed surface. The high concentration of EDTA when used in a single use electroless puddle plating processes will greatly affect the deposition rates near the end of the electroless process due to the EDTA concentration increase as the water evaporates from the puddle during processing, and also due to the drop in copper concentration as it is plated out in the contact level aperture 1510 and on the field region 1505. A single use electroless puddle plating processes may be advantageous, due to ability to use solutions that have improved deposition rates without the issue of particle growth in the electroless plating solution or wafer-to-wafer electrolyte solution variation due to bath depletion.

[0083] A pH adjusting agent is added to adjust the electroless solution to a pH value in a range from about 4 to about 14. In on embodiment, the pH of the metal layer electroless deposition solution is maintained within a range of about 11 and about 14, and more preferably at a pH of about 12.5. In one embodiment, the pH of the metal layer electroless deposition solution is maintained within a range of about 11 and about 14 at the processing temperature which may be between about 60°C and about 85°C. The pH adjusting agent may be a basic compound to increase the pH value of the electroless solution and include tetraalkylammonium hydroxides (*e.g.,* tetramethylammonium hydroxide ($(CH_3)_4NOH$, TMAH). The pH adjusting agent may be dissolved in water prior to adjusting the pH value of the electroless solution. Other pH adjusting and buffering agents include various organic amines, particularly tertiary amines and hindred amines (*e.g.*, triethylamines ($N(C_2H_5)_3$)).

[0084] In another embodiment, the metal layer electroless deposition solution is an aqueous solution that may contain a copper source, a reductant, a complexing agent, a pH adjusting agent, additives including levelers, and an optional surfactant as a wetting agent. The addition of the additives including levelers may be especially useful when using the metal layer electroless deposition solution to fill the contact level aperture 1510 via an electroless deposition process, such as steps 1008 and 1010, which are described above. Levelers within the metal layer electroless deposition solution are used to achieve different deposition thickness as a function of leveler concentration and feature geometry. The leveler within the metal layer electroless deposition solution may have a concentration in a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm.

Examples of levelers that may be employed in an electroless solution include, but are not limited to alkylpolyimines and organic sulfonates, such as 1-(2-hydroxyethyl)-2-imidazolidinethione (HIT), 4-mercaptopyridine, 2-mercaptothiazoline, ethylene thiourea, thiourea or derivatives thereof. The metal layer electroless deposition solution may also contain brighteners or accelerators and suppressors as alternative additives to provide further control of the deposition process. The role of accelerators is to achieve a smoothly deposited surface of the copper-containing layer 120. The accelerator within the metal layer electroless deposition solution has a concentration in a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm. Traditional accelerators used in electrochemical plating baths may be inhibitors when used in electroless plating baths. In one aspect, traditional "accelerators" that are useful in an electroless solution for metal layer 1525 may include sulfur-based compounds such as bis(3-sulfopropyl) disulfide (SPS), 3-mercapto-1-propane sulfonic acid (MPSA), aminoethane sulfonic acids, thiourea, derivatives thereof, combinations thereof. The "accelerators" may be used in conjunction with the polymeric additives to help promote the growth in the bottom of the contact level feature 1510 (*e.g.*, near to the silicon junction 1502) versus the field region 1505. In one aspect, quinolines may be used as an accelerator. Examples of some quinolines include that may be useful include, but are not limited to 6-Hydroxyquinoline, 8-Hydroxyquinoline, and 8-Hydroxy-7-iodo-5-quinolinesulfonic acid.

[0085] Also, an optional surfactant may be added to the metal layer electroless deposition solution. The surfactant is a wetting agent to reduce the surface tension between the plating solution and the substrate surface. Surfactants are generally added to the electroless solution at a concentration of about 1,000 ppm or less, preferably about 800 ppm or less, such as from about 20 ppb to about 600 ppm. The surfactant may have ionic or non-ionic characteristics. A preferred surfactant includes dodecyl sulfates, such as sodium dodecyl sulfate (SDS). Other surfactants that may be used in the electroless deposition solution include glycol ether based surfactants (*e.g.,* polyethylene glycol). For example, a glycol ether based surfactants may contain polyoxyethylene units, such as TRITON® 100, available from Dow Chemical Company. A nonylphenol ethoxylate surfactant is useful in the electroless deposition solution, such as TERGITOL®, available from Dow Chemical

Company or IGEPAL-630, available from GAF Corporation. In one aspect a cationic surfactant, such as dodecyltrimethylammonium bromide ($CH_3(CH_2)_{11}N(CH_3)_3Br$) may be used in the metal layer electroless deposition solution. Other useful surfactants may contain phosphate units, for example, sodium poly(oxyethylene) phenyl ether phosphate, such as RHODAFAC® RE-610, available from Rhodia, Inc. The surfactants may be single compounds or a mixture of compounds of molecules containing varying length of hydrocarbon chains.

[0086] The electroless deposition process to deposit metal alloy layer (*e.g.*, 1525 or 1526) may use either a pre-mixed solution or an in-line mixing process that combines solution components to generate the metal layer electroless deposition solution. The electroless deposition process may be conducted at a temperature in a range from about 35°C to about 85°C. A chamber useful to conduct an electroless deposition process for depositing copper-containing layers is the electroless deposition process cell, further described in the commonly assigned U.S. Patent Application Serial Number 10/965,220, entitled, "Apparatus for Electroless Deposition," filed on October 14, 2004, U.S. Patent Application Serial Number 10/996,342, entitled, "Apparatus for Electroless Deposition of Metals on Semiconductor Wafers," filed on November 22, 2004, U.S. Provisional Patent Application Serial Number 60/575,553, entitled, "Face Up Electroless Plating Cell," filed on May 28, 2004, and U.S. Provisional Patent Application Serial Number 60/575,558, entitled, "Face Down Electroless Plating Cell," filed on May 28, 2004, which are each incorporated by reference to the extent not inconsistent with the claimed aspects and description herein.

Novel Copper Formulation Solution – Copper Formate Solution

[0087] An example of a novel copper formulation that has been optimized for a single wafer/single use puddle plating process is described below. Notable features/differences from conventional electroless plating baths is: 1) the presence of formate ions that are may provide a secondary pathway for Cu deposition, and 2) a electroless solution that contains high reducing agent to Cu ion and EDTA ratio that is believed to permit more effective "leveling" of the deposited film due to competition between additives and reducing agent for surface sites. Use of this novel copper formulation at temperatures of about 80 °C, or at higher pH values allows even faster deposition rates without noticeable loss of film quality.

[0088] In one embodiment, the novel copper formulation may include:

0.03 M $Cu(HCO_2)_2$
0.06 M EDTA
0.20 M glyoxylic acid
500 ppm PEG (4000 MW)

[0089] The plating process is performed at a plating temperature of about 70 °C, and a pH at room temperature of about 12.8, and/or a pH of about 12.3 at a temperature of about 70 °C. The initiation time was less than about 30 seconds using this solution.

[0090] In one example, using a barrier layer 1521 containing a metal layer stack of Ti/TiN/Ru on Silicon substrates using the novel copper formulation the following results were achieved. (*i.e.*, 5 minute plating process)

	Conventional Bath	Novel Copper Formulation
R_s Resistance (Pre-anneal)	0.8721	0.4575
R_s Resistance (Post-anneal)	0.7745	0.3629
pH	12.3 at 70 °C	12.3 at 70 °C
Bath Temp. (°C)	70	70
Anneal (minutes/°C)	20/400	20/400

[0091] The conventional bath was a glyoxylic acid type electroless solution published in the literature.

ELECTROLESS DEPOSITION PROCESSES AND COMPOSITIONS FOR HIGH ASPECT RATIO CONTACTS

[0092] Embodiments of the invention further provide methods of forming a device over a tungsten-containing contact plug. In one aspect, a process of capping and filling defects formed in a tungsten-containing contact plug that have been exposed during a subsequent chemical mechanical polishing (CMP) process is performed. Defects that are present in the tungsten-containing contact plug may include gaps, voids, and/or seams (hereafter gaps). In one embodiment, gaps are plugged or capped with a material that will be able to withstand subsequent thermal processing

and inhibit displacement of the formed void therein. Gaps may be filled, or plugged, by employing selective deposition process that include chemical vapor deposition (CVD), atomic layer deposition (ALD), and electroless deposition processes. Preferably, the material used to fill the gaps or voids may include nickel, cobalt, tungsten and alloys thereof. In another embodiment, the method may include the steps of pretreating and then subsequently filling the gap by use of a CVD, ALD or electroless process using a conductive material such as nickel, ruthenium, cobalt, tungsten and alloys thereof.

[0093] In an alternative embodiment, a gap may be filled with a dielectric material. In one example, a spin-on-glass (SOG) is deposited by a spin coating process. SOG materials typically include silicon dioxide (SiO_2) or doped SiO_2 materials. In another example, hafnium silicate is deposited by a vapor deposition process.

[0094] In another embodiment, the gaps within a tungsten plug are filled during a later process. For example, the gap is temporally ignored, a dielectric layer is deposited on the substrate surface covering the gap and a second aperture is formed therein by an etching process over the tungsten plug and revealing the gap. A barrier layer (*e.g.,* tantalum-containing) and a seed layer (*e.g.,* copper) are sequential deposited by vapor deposition processes, such as physical vapor deposition (PVD) process.

Capping Process

[0095] Gaps within a tungsten-containing contact plug may be filled with a material that will be stable during subsequent semiconductor fabrication processes and inhibit the creation voids in the subsequent deposited metal layers. Gaps may be capped by employing selective vapor deposition processes (*e.g.,* CVD or ALD) or liquid deposition processes (*e.g.,* electroless) to deposit a capping material, such as nickel, cobalt, tungsten and alloys thereof.

[0096] Figure 7A illustrates a cross-sectional view of substrate 200 following a CMP process, as discussed above while forming a tungsten-containing contact plug depicted in Figures 1A-1D. Substrate 200 contains contact layer 202 (*e.g.,* MOS device source region, drain region, or gate region), dielectric layer 204 and plug 203 that includes tungsten layer 206 and gap 210 therein. The gap 210, which may be a

seam, void or other defect, is created in tungsten layer 206 during the formation of the plug 203 (*e.g.*, tungsten CVD process) and is then exposed during the subsequent CMP process.

[0097] Dielectric layer 204 may contain a semiconductor material that includes silicon or silicon-containing materials. Dielectric layer 204 may be an insulating material such as silicon dioxide, silicon nitride, silicon-on-insulator (SOI), silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, California. Contact layer 202 may contain a doped silicon layer. Tungsten layer 206 may contain tungsten, tungsten alloys or a tungsten-containing material that includes tungsten and oxygen, nitrogen, boron, silicon or combinations thereof. Due to the exposure to the atmospheric environment, the surface of the tungsten layer 206 may contain contaminates or oxides thereon.

[0098] Figure 7B depicts a capping layer 230 deposited on substrate 200 that covers gap 210 to form void 214. Capping layer 230 may be composed of a conductive material or a dielectric material that will withstand subsequent thermal processing and inhibit displacement of void 214 into the subsequently deposited layers. Preferably, capping layer 230 contains a metal deposited by a liquid deposition process or a vapor deposition process. In one example, capping layer 230 is a nickel-containing layer deposited by an electroless deposition solution. In another example, capping layer 230 is a cobalt-containing layer (*e.g.,* CoW-alloy) deposited by an electroless deposition solution. In another example, capping layer 230 is a nickel-containing layer deposited by a CVD process. In a further example, capping layer 230 is a dielectric material, such as a hafnium silicate layer deposited by a CVD process.

[0099] Conductive layer 212 is deposited on the surface of substrate 200 containing capping layer 230 and dielectric layer 204, as depicted in Figure 7C. Layer 220 is deposited on conductive layer 212. Conductive layer 212 may contain copper, tungsten, aluminum or an alloy thereof, while layer 220 may contain a dielectric material (*e.g.,* silicon-containing) or an additional conductive material. Preferably, conductive layer 212 contains copper and layer 220 is a dielectric layer. Preferably, the capping layer 230 is formed from a material that does not readily deform, form an alloy with the conductive layer 212, or change state so that the

physical properties or electrical properties of the material in the capping layer 230 remain unchanged after subsequent semiconductor processing steps have been performed on the substrate. In one aspect, the materials used to form the capping layer 230 and conductive layer 212 are selected so that they resist migration of the deposited material into the void 214 and the integrity of conductive layer 212 is preserved. Capping layer 230 is composed of a material that withstands being exposed to a temperature of about 500 °C or higher, preferably about 700 °C or higher.

[00100] In other embodiments, substrate 200 may contain additional layers of material depending on the overall architecture of the electronic device. For example, dielectric layer 204 may contain a barrier layer (not shown) thereon prior to the deposition of conductive layer 212 and/or conductive layer 212 may also contain a barrier layer (not shown) thereon prior to the deposition of layer 220.

[00101] In one aspect, a CMP process may be performed on the substrate 200 to planarize the dielectric layer 204, capping layer 230 and tungsten layer 206. A planar surface may improve the device performance and reduce device to device variability due to the reduction in thickness variation of the conductive layer 212 near the capping layer 230, if the conductive layer 212 and capping layer 230 are formed from different materials.

[00102] A capping layer 230 containing a cobalt-tungsten alloy or a nickel-containing material may be deposited by an electroless process that utilizes either a pre-mixed solution or an in-line mixing process that combines solution components to generate the electroless solution. In one example, an electroless solution used to deposit a cobalt-tungsten alloy may contain a cobalt source, a tungsten source, a citrate source, a hypophosphite source, a borane reductant and other additives. In another example, an electroless solution used to deposit a nickel-containing material may contain a nickel source, a citrate source, a borane reductant and other complexing agents and additives. Other electroless deposition solutions and processes useful for depositing cobalt-tungsten alloys are further described in the commonly assigned U.S. Patent Application Serial Number 10/967,919, entitled, "Selective Self-initiating Electroless Capping of Copper with Cobalt-containing Alloys," filed on October 18, 2004, which is incorporated by reference to the extent not inconsistent with the claimed aspects and description herein. Examples of

cobalt-tungsten alloys that may electrolessly deposited include, but are not limited to cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof. Examples of nickel alloys that may electrolessly deposited include, but are not limited to nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), nickel rhenium boride (NiReB), derivatives thereof, or combinations thereof. In one aspect, the capping layer 230 preferably has a resistivity below about 10 microohm-cm and thus will have a resistivity similar to the material deposited in the tungsten layer 206. The resistance (R) of a circuit is equal to the resistivity (ρ) of the conductive material through which the current passes times the length (L) of the feature divided by the cross-sectional area (A) of the circuit through which the current passes (*i.e.*, $R = \rho (L/A)$). Therefore, the addition of a capping layer 230 that is conductive, preferably metallic, will reduce the resistance of the circuit that utilizes the plug 203 (*i.e.*, increase the effective cross-sectional area of the plug 203).

Filling Process

[00103] In an alternative embodiment, to fill a gap formed within a tungsten-containing contact plug, the gap may be pretreated and filled with a material prior to depositing a conductive layer thereon (*e.g.*, element 350 in Figure 8H). The fill material inhibits void displacement that may otherwise occur by migration of material from a conductive layer deposited over the gap, as depicted in Figure 1F. The gap(s) may be plugged by employing selective vapor deposition processes (*e.g.*, CVD or ALD), liquid deposition processes (*e.g.*, electroless- or electroplating) or spin coating processes. Materials useful to fill the gap(s) may include conductive materials, such as nickel, ruthenium, cobalt, tungsten and alloys thereof, as well as dielectric materials, such as spin-on-glass (SOG).

[00104] Figure 8A illustrates a cross-sectional view of substrate 300 following a CMP process, as discussed above while forming a tungsten-containing contact plug depicted in Figure 1D. Substrate 300 contains contact layer 302 (*e.g.*, MOS device source or drain regions), dielectric layer 304 and plug 303 that includes tungsten

layer 306 and gap 310 formed therein. The gap 310, which may be a seam, void or other defect, is created in tungsten layer 306 during the formation of the plug 303 (*e.g.*, tungsten CVD process) and is generally exposed during the subsequent CMP process. During the CMP process or during a later exposure to oxidizing component(s), such as, components found in an ashing process, a wet clean process or ambient conditions, a tungsten oxide surface 312 will form on the tungsten layer 306. Tungsten oxide surface 312 may be continuous or discontinuous across tungsten layer 306 and include a surface terminate with oxygen, hydrogen, hydroxides, metals and combinations thereof.

[00105] Figures 8A-8D illustrate cross-sectional views of an electronic device at different stages of an interconnect fabrication sequence incorporating one embodiment of the invention to pretreat and subsequently fill the gap 310 with a conductive material. Figure 8B illustrates substrate 300 after performing a pretreatment process to remove the tungsten oxide surface 312 and expose the metallic tungsten-containing surface 314. In one aspect of the embodiment, tungsten oxide surface 312 is chemically reduced to tungsten metal. For example, tungsten oxide surface 312 is exposed to a hydrogen plasma to remove the oxides and form a metallic tungsten-containing surface 314. In another aspect, the tungsten oxide surface 312 is exposed to vapor deposition process containing diborane to remove the oxides and form metallic tungsten-containing surface 314 containing tungsten boride. In another aspect, the tungsten oxide surface 312 is exposed to wet clean process to further oxidize and remove tungstate ions while leaving behind a metallic tungsten-containing surface 314. Additives, such as surface chelators, may be used within the wet clean solution that adhere to the freshly prepared metallic tungsten-containing surface 314 and inhibit oxidization.

[00106] A plasma pretreatment process is conducted for a predetermined time to reduce tungsten oxide surface 312 and form a metallic tungsten-containing surface 314. A plasma pretreatment process may occur for about 5 minutes or less, preferably in a range from about 1 second to about 60 seconds, more preferably from about 5 seconds to about 30 seconds. During the pretreatment process, the substrate is maintained at a temperature in a range from about 20 °C to about 150 °C, preferably from about 50 °C to about 100 °C. The process chamber is maintained at a pressure in a range from about 0.1 Torr to about 750 Torr,

preferably from about 1 Torr to about 100 Torr, and more preferably from about 10 Torr to about 30 Torr.

[00107] The plasma treatment process may be conducted in a process chamber capable of plasma vapor deposition techniques. For example, the substrate may be placed into a plasma enhanced ALD (PE-ALD), a plasma enhanced CVD (PE-CVD) or high density plasma CVD (HDP-CVD) chamber, such as the ULTIMA HDP-CVD™, available from Applied Materials Inc., located in Santa Clara, California. An inductively coupled plasma generating device, capacitively coupled plasma generating device, or combination thereof may be used in a plasma chamber to carryout the plasma treatment process. During processing the tungsten oxide surface 312 is exposed to a reducing plasma containing a reductant to form the metallic tungsten-containing surface 314. The reductant may be diluted in a carrier gas and include hydrogen, diborane, silane, disilane, phosphine, derivatives thereof and combinations thereof. In one aspect, a carrier gas is delivered to the process chamber during the plasma pretreatment process. Carrier gases may be selected so as to also act as a purge gas for the removal of volatile reactants and/or by-products from the process chamber. Carrier gases or purge gases include helium, argon, hydrogen, forming gas and combinations thereof. The carrier gas may be provided at a flow rate in a range from about 100 sccm to about 5,000 sccm, preferably from about 500 sccm to about 2,500 sccm. The reductant may be provided at a flow rate in a range from about 5 sccm to about 500 sccm, preferably from about 10 sccm to about 100 sccm. The plasma may be formed using an RF power delivered to the plasma generating devices (*e.g.*, showerhead in a capacitively coupled chamber or a substrate support) utilized in the plasma chamber where the RF power ranges from 100 W to 10,000 W at an RF frequency between about 0.4 kHz and about 10 GHz. In one aspect, the plasma is formed using a showerhead RF power setting and a substrate support RF power setting that is in a range from about 500 W to about 5,000 W at a frequency of about 13.56 MHz.

[00108] In an exemplary plasma pretreatment process, a substrate containing tungsten oxide is heated to about 50 °C and the process chamber is maintained at a pressure of about 10 Torr. A reducing plasma is exposed to the substrate containing hydrogen at a flow rate of about 1,000 sccm. The substrate is exposed to

the reducing plasma for about 30 seconds to form a treated and reduced tungsten-containing layer.

[00109] In another exemplary plasma pretreatment process, a substrate containing tungsten oxide is heated to about 50 °C and the process chamber is maintained at a pressure of about 10 Torr. A reducing plasma is exposed to the substrate at a flow rate of about 500 sccm, whereas the reducing plasma contains diborane at a flow rate of about 50 sccm and a helium carrier gas at the flow rate of about 450 sccm. The substrate is exposed to the reducing plasma for about 30 seconds to form a treated and reduced tungsten-containing layer.

[00110] In another embodiment, the tungsten oxide surface 312 is exposed to a reducing vapor to form metallic tungsten-containing surface 314 to perform a vapor deposition process type pretreatment process. The reductant may include borane, diborane, borane-alkylsulfides, such as borane-dimethylsulfide ($BH_3 \bullet (CH_3)_2S$), alkyboranes (*e.g.,* ethylborane), phosphine, alkylposphines (*e.g.,* dimethylphosphine), silane, disilane, trisilane, alkylsilanes (*e.g.,* methylsilane), ammonia, hydrazine, hydrogen, derivatives thereof or combinations thereof. Preferably, the reductant is diborane, phosphine, silane, hydrazine, hydrogen or combinations thereof. In one aspect of the pretreatment process, the tungsten oxide surface 312 is exposed to a reducing vapor process for a predetermined time to form metallic tungsten-containing surface 314. The reducing vapor process may occur for about 5 minutes or less, preferably in a range from about 1 second to about 120 seconds, more preferably from about 5 seconds to about 90 seconds. During the reducing vapor process, the substrate is maintained at a temperature in a range from about 20 °C to about 150 °C, preferably from about 50 °C to about 100 °C. The process chamber is maintained at a pressure in a range from about 0.1 Torr to about 750 Torr, preferably from about 1 Torr to about 100 Torr, and more preferably from about 10 Torr to about 30 Torr. In one aspect, a reductant may be exposed to tungsten oxide surface 312 directly or diluted in a carrier gas. During the reducing vapor process, a carrier gas flow is established within the process chamber and exposed to the substrate. Carrier gases may be selected so as to also act as a purge gas for the removal of volatile reactants and/or by-products from the process chamber. Carrier gases or purge gases include helium, argon, nitrogen, hydrogen, forming gas and combinations thereof. The carrier gas may be provided at a flow

rate in a range from about 100 sccm to about 5,000 sccm, preferably from about 500 sccm to about 2,500 sccm. The reductant may be provided at a flow rate in a range from about 5 sccm to about 500 sccm, preferably from about 10 sccm to about 100 sccm.

[00111] The reducing vapor process may be conducted in a process chamber capable of vapor deposition, such as an ALD process chamber or a CVD process chamber. A process chamber useful for ALD during the reducing vapor process is described in commonly assigned United States Patent Application No. 6,916,398 and 6,878,206, which are both incorporated herein by reference.

[00112] In another embodiment of the pretreatment process, the tungsten oxide surface 312 is exposed to wet clean process to further oxidize and remove tungstate ion while leaving behind a metallic tungsten-containing surface 314. During a typical wet clean process a wet clean solution is dispensed across or sprayed on the surface of substrate 300. The wet clean process may be an in situ process performed in the same processing cell as a subsequent electroless deposition process. Alternatively, substrate 300 may be wet cleaned in a separate processing cell from the subsequent electroless deposition processing cell. The wet clean process usually includes an acidic wet clean solution with a pH of about 4 or less, preferably, in a range from about 1.5 to about 3. The tungsten oxide surface 312 typically requires an aggressive cleaning at low pH values. The pH of the wet clean solution is usually adjusted by adding an acid or a base to the predetermined value. The acid may include hydrochloric acid (HCl), hydrogen fluoride (HF), sulfuric acid (H_2SO_4), nitric acid (HNO_3), phosphoric acid (HPO_4), derivatives thereof and combinations thereof. The base may include a hydroxide salt, ammonia or an amine, such as diethanolamine (DEA), triethanolamine (TEA), derivatives thereof, salts thereof and combinations thereof. The wet clean solution also contains at least one chelator or complexing agent, such as a carboxylic acid or carboxylate, for example, a citrate, oxalic acid, glycine, salts thereof and combinations thereof. In one example, the wet clean solution contains about 0.05 M to about 0.5 M of citric acid and optionally up to about 0.25 M of methanesulfonic acid.

[00113] In one embodiment, the pretreatment process is used to etch and remove a portion of the tungsten oxide surface 312 to increase the size of the gap 310 in an effort to improve the ability of the subsequent deposition process steps (discussed

below) to access and fill the gap 310. In one aspect, the process of increasing the gap 310 is performed using a wet clean process for a desired period of time.

[00114] Once tungsten oxide surface 312 is removed or reduced to reveal metallic tungsten-containing surface 314 by the processes described herein, a fill material 320 may be deposited thereon to fill the gap 310, as illustrated in Figure 8C. The fill material 320 may be composed of a conductive material or a dielectric material. Preferably, fill material 320 contains a metal deposited by a liquid deposition process or a vapor deposition process. In one example, fill material 320 is a nickel-containing layer deposited by an electroless deposition solution. In another example, fill material 320 is a cobalt-containing layer (*e.g.,* CoW-alloy) deposited by an electroless deposition solution. In another example, fill material 320 is a nickel-containing layer deposited by a CVD process. Preferably, the capping layer 320 is formed from a material that does not readily deform, form an alloy with the conductive layer 350, or change state so that the physical properties or electrical properties of the material in the capping layer 320 remain unchanged after subsequent semiconductor processing steps have been performed on the substrate. It is generally desirable to fill the gap 310 so that no gaps or voids are formed in the plug 303 or plug 321, and thus integrity of conductive layer 350 is preserved during subsequent semiconductor processing steps. In one aspect, the material used to form the fill material 320 is selected so that it can withstands exposure to temperature of about 500 °C or higher, preferably about 700 °C or higher.

[00115] Figure 8D depicts substrate 300 after several fabrication processes have been performed on its surface to form the subsequent metal interconnect layer (*e.g.*, M1 layer). As shown in Figure 8D, a dielectric layer 324 was deposited on the surface of substrate 300 and etched to reveal fill material 320 and an upper surface tungsten layer 306. Then a barrier layer 323 was deposited on dielectric layer 324 and seed/adhesion layer 325 is deposited on barrier layer 323, each by a vapor deposition process, such as a PVD process or an ALD process. The barrier layer 323 typically will contain metals, such as titanium, titanium nitride, titanium silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, alloys thereof, derivatives thereof or combinations thereof. The seed/adhesion layer 325 typically will contain metals, such as tungsten, copper, ruthenium, titanium, tantalum, alloys thereof or combinations thereof. In one aspect, as shown in Figure 8D, the barrier layer 323

and seed/adhesion layer 325 were removed from the surface of the fill material 320 and an upper surface tungsten layer 306 by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers. The removal of the barrier layer 323 and seed/adhesion layer 325 will help reduce the resistance of the circuit formed in the shown device, since the barrier layer 323 and seed/adhesion layer 325 are usually contain materials that have a resistivity higher than typical interconnect metals (*e.g.*, conductive layer 350), such as copper.

[00116] Next a conductive layer 350 is deposited onto substrate 300 to form a plug 321 (or via) that is in electrical contact with plug 303. Conductive layer 350 may contain copper, tungsten, aluminum or an alloy thereof. Preferably, conductive layer 350 contains copper or a copper alloy. Conductive layer 350 may be deposited by a vapor deposition process (*e.g.,* CVD or PVD) or a liquid deposition process (*e.g.,* electroless or electroplating).

[00117] In one aspect, a CMP process may be performed on the substrate 300 to planarize the dielectric layer 304, capping layer 330 and tungsten layer 306. A planar surface may improve the device performance and reduce device to device variability.

[00118] In one aspect, a fill material 320 containing a cobalt-tungsten alloy or nickel alloy may be deposited by an electroless process that exposes the substrate to an electroless solution within a process chamber. An example of an electroless solution for depositing a cobalt-tungsten alloy may contain a cobalt source, a tungsten source, a citrate source, a hypophosphite source, a borane reductant and other additives. Examples of cobalt-tungsten alloys that may electrolessly deposited include, but are not limited to cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof. Examples of nickel alloys that may electrolessly deposited include, but are not limited to nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), nickel rhenium boride (NiReB), derivatives thereof, or combinations thereof. Other electroless deposition solutions for cobalt-tungsten alloys are further described in

the commonly assigned U.S. Patent Application Serial Number 10/967,919, entitled, "Selective Self-initiating Electroless Capping of Copper with Cobalt-containing Alloys," filed on October 18, 2004, which is incorporated by reference to the extent not inconsistent with the claimed aspects and description herein. In another example, an electroless solution to deposit a nickel-containing material may contain a nickel source, a citrate source, a borane reductant and other complexing agents and additives. An exemplary electroless deposition process cell that may be one or more of the electroless deposition processes described herein is further described in the commonly assigned and copending United States Patent Application Serial No. 10/996,342, filed 11/22/04 and United States Patent Application Serial No. 11/175,251, filed 07/06/05, which are both incorporated by reference in their entirety.

[00119] In one aspect, the fill material 320 preferably has a resistivity below about 10 microohm-cm and thus will have a resistivity similar to the material deposited in the tungsten layer 306. The resistance (R) of a circuit is equal to the resistivity (ρ) of the conductive material through which the current passes times the length (L) of the feature divided by the cross-sectional area (A) of the circuit through which the current passes (*i.e.*, $R = \rho (L/A)$). Therefore, the addition of a fill material 320 that is conductive, preferably metallic, will reduce the resistance of the circuit that utilizes the plug 303 (*i.e.*, increase the effective cross-sectional area of the plug 303) and thus improve the device performance and reliability (*e.g.*, reduces resistive heating effects).

Ruthenium Containing Layer Deposition Process Sequence

[00120] In an alternative embodiment, Figures 8A, and 8E-8H illustrate cross-sectional views of an electronic device at different stages of an interconnect fabrication sequence that are used to pretreat and subsequently fill gap 310 with a fill material 320. Figure 8E illustrates substrate 300 after a pretreatment process has been performed on the substrate 300 shown in Figure 8A. In one aspect of the pretreatment process, a ruthenium oxide layer 316 is deposited on the tungsten oxide surface 312 using a ruthenium tetroxide (RuO_4) containing gas. Thereafter, ruthenium oxide layer 316 may be chemically reduced to form ruthenium-containing layer 318 on tungsten oxide surface 312, as illustrated in Figure 8F.

[00121] Ruthenium tetroxide may be delivered to the substrate in a vapor deposition process, such as an ozone generation process, or in a liquid deposition process, such as an aqueous solution or suspension. Preferably, ruthenium tetroxide is generated by exposing a ruthenium-containing source to an oxidizing gas. Ruthenium tetroxide is a strong oxidant and therefore readily reacts with any exposed tungsten and/or tungsten oxide layers to form a consistent and catalytic active layer of ruthenium oxide or metallic ruthenium. An example of an exemplary process used to form ruthenium tetraoxide and deposit a ruthenium containing layer on the surface of the substrate is further described in the commonly assigned United States Patent Application Serial No. 11/228,425, filed 09/15/05, which is incorporated by reference in its entirety. In one example, ruthenium tetroxide is formed by flowing an ozone containing gas, preferably >12 vol% ozone, across a metallic ruthenium source material (*e.g.*, powdered ruthenium metal). The formed ruthenium tetraoxide is then delivered and separated from the other components in the ruthenium tetraoxide containing gas by use of a cold trap. Thereafter, the cold trap is purged of the unwanted gases and then warmed to a temperature to sublime the ruthenium tetroxide while a flow of inert gas is passed therethrough. The vaporized ruthenium tetroxide saturates the inert gas to form a ruthenium tetraoxide deposition gas. In an exemplary vapor deposition process, a deposition gas containing ruthenium tetroxide is delivered to a substrate having a tungsten oxide layer formed thereon. During the process, the substrate is maintained at a temperature between of about 100 °C and about 450 °C, and more preferably a temperature between about 200 °C and about 400 °C. A ruthenium containing layer can be selectively or non-selectively deposited on certain preferred materials by adjusting the temperature of the substrate during processing (e.g., < 180 °C (selective); > 200 (non-selective)). After exposing the tungsten oxide layer to the ruthenium tetroxide containing gas for about 30 seconds, a ruthenium oxide layer is formed on the tungsten oxide layer.

[00122] In Figure 8F, the ruthenium oxide layer 316 is exposed to a reductant forming ruthenium-containing layer 318. In this step the ruthenium oxide is chemically reduced to ruthenium metal. For example, ruthenium oxide layer 316 is exposed to a hydrogen plasma to remove the oxygen and form metallic ruthenium-containing layer 318. In another example, ruthenium oxide layer 316 is exposed to a

vapor deposition process containing diborane to remove oxygen and form ruthenium-containing layer 318 containing ruthenium boride. In another example, ruthenium oxide layer 316 is exposed to phosphine through a vapor deposition process to remove oxygen and form ruthenium-containing layer 318 containing ruthenium phosphide.

[00123] Next the fill material 320 is deposited on the ruthenium-containing layer 318 to fill gap 310 as illustrated in Figure 8G. The deposition processes and the compositions of fill material 320 are described above in conjunction with Figure 8C. Also, Figure 8H depicts substrate 300 after several subsequent fabrication processes have been formed on the substrate, which is similarly described above in conjunction with Figure 8D.

Dielectric Gap Fill Process

[00124] In an alternative embodiment, the gap 310 is filled with a dielectric material as illustrated by cross-sectional views shown in Figures 8A, 8I-8K. Figure 8A depicts substrate 300 with plug 303 that contains tungsten material 306, tungsten oxide surface 312 and gap 310 therein. Optionally, a pretreatment process to remove tungsten oxide surface 312 and reveal the surface of tungsten material 306, as described in conjunction with Figure 8B, may be performed before depositing a dielectric fill material 330 into the gap 310. Preferably, a pretreatment process is not conducted and dielectric fill material 330 is deposited on substrate 300 to fill gap 310, as depicted in Figure 8I. Dielectric material 330 may be deposited on substrate 300 by a spin-coating process or by a vapor deposition process.

[00125] In one example, dielectric fill material 330 is spin-on-glass (SOG) deposited by a spin-coating process. Dielectric fill material 330 containing SOG is formed by a polymerization reaction of precursor compounds that are dissolved in an organic solution. The isolated dielectric compound is useful to fill gap 310. Preferably, dielectric fill material 330 is a silicate or a polysiloxane and may contain a metal such as titanium, zirconium hafnium and/or vanadium. Therefore, the composition of a SOG used as dielectric fill material 330 may include silicon, carbon, oxygen, titanium, zirconium, hafnium, vanadium or combinations thereof. Substrate 300 is generally exposed to a thermal annealing, or curing, process following the SOG deposition process. Additional compositions of SOG and processes to deposit

SOG into vias or trenches is described in J.W. Lutze et al., "Spin-on-glass for 200 nm trench isolation structures," *J. Micromech. Microeng,* vol. 1, pp. 46-51 (1991), which is herein incorporated by reference.

[00126] In another example, dielectric fill material 330 is a silicon-containing material or a metal-containing material deposited by an ALD process or a CVD process. Examples of dielectric fill material 330 deposited by vapor deposition processes include silicon oxide, silicon oxynitride, aluminum oxide, tantalum oxide, hafnium oxide, hafnium silicate, zirconium oxide, zirconium silicate, titanium oxide, titanium silicate, derivates thereof and combinations thereof. Additional compositions of dielectric fill material 330 and vapor deposition processes to deposit dielectric fill material 330 is described the commonly assigned U.S. Patent Application Serial No. 10/406,833, entitled, "Method for Hafnium Silicon Oxynitride Deposition," filed April 4, 2003, and published as U.S. Publication No. 20030235961 and U.S. Patent Application Serial No. 11/127,767, entitled, "Apparatuses and Methods for Atomic Layer Deposition of Hafnium-Containing High-K Materials," filed May 12, 2005, which are both herein incorporated by reference.

[00127] A planarization process, such as a chemical mechanical polishing (CMP) process or etching process may be performed to remove an excess dielectric fill material 330 deposited on the surface of substrate 300 (*i.e.*, field region 307) and expose the upper surface tungsten layer 306, as depicted in Figure 8J. Therefore, gap 310 remains filled with dielectric fill material 330 while substantially flush with the surface substrate 300.

[00128] Figure 8K depicts substrate 300 after several fabrication processes. Dielectric layer 324 is deposited on the surface of substrate 300 and etched to reveal fill dielectric fill material 330 and an upper surface tungsten layer 306. Barrier layer 323 is deposited on dielectric layer 324 and seed/adhesion layer 325 is deposited on barrier layer 323, each by a vapor deposition process, such as a PVD process or an ALD process. In one aspect, as shown in Figure 8K, the barrier layer 323 and seed/adhesion layer 325 were removed from the surface of the dielectric layer 324 and an upper surface tungsten layer 306 by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers. Conductive layer 350 is deposited onto substrate 300 forming plug 321 in contact with plug 303.

[00129] Preferably, the dielectric fill material 330 is formed from a material that does not readily deform, form an alloy with the conductive layer 350, or change state so that the physical properties or electrical properties of the material in the dielectric fill material 330 remain unchanged after subsequent semiconductor processing steps have been performed on the substrate. It is generally desirable to fill the gap 310 so that no gaps or voids are formed in the plug 303 or plug 321, and thus integrity of conductive layer 350 is preserved during subsequent semiconductor processing steps. In one aspect, the material used to form the dielectric fill material 330 is selected so that it can withstands exposure to temperature of about 500°C or higher, preferably about 700°C or higher, and more preferably about 1,000°C or higher.

[00130] The process steps illustrated in Figures 8A-8K are not intended to be limiting as to the scope of the invention, since substrate 300 may contain one or more additional or intermediate layers of material without varying from the basic scope of the invention described herein. For example, the sidewalls of the gap 310 formed in the dielectric layer 304 may be covered by a barrier layer or an adhesion layer (not shown) prior to the deposition of tungsten layer 306.

Interconnect Formation Process

[00131] In another embodiment, a process is used to initiate on a tungsten containing contact plug to form an interconnect feature (see item # 321 in Figures 8H and 8K and item # 443 in Figure 9F). As shown in Figures 9A-9F, an interconnect plug 443 is formed over the plug 403 so that an electrical connection can be made between the contact layer 402, the interconnect plug 443 and any subsequently deposited layers, such as the M2 and above interconnects (not shown). In this case, any gaps formed within a tungsten-containing contact plug is postponed until the subsequent metal layer(s) are formed over the plug 403 (see Figure 9A). While Figures 9A-9F illustrates a tungsten-containing contact plug that has a gap 410 formed therein, this configuration is not intended to be limiting as to the scope of the invention since the methods described herein may be useful to create an interconnect feature over a tungsten-containing contact plug that does not contain this type of defect. In general this process requires the deposition of dielectric layer over the plug 403 formed on the substrate 400. Then various conventional lithographic patterning and etching techniques are used to form an

aperture 405 (or via) so that an interconnect layer can be deposited on the plug 403. In one aspect, various materials may be used to fill the gap 410 and aperture 405, which may include conductive materials, such as copper, nickel, ruthenium, cobalt, tungsten and alloys thereof.

[00132] Figure 9A illustrates a cross-sectional view of substrate 400 following a CMP process, as discussed above during processes forming a tungsten-containing contact plug depicted in Figure 1D. Substrate 400 contains contact layer 402, dielectric layer 404 and plug 403 that includes tungsten layer 406 formed in the gap 410. The gap 410, which may be a seam, void or other defect, is created in tungsten layer 406 during the formation of the plug 403 (*e.g.*, tungsten CVD process) and is then exposed during the subsequent CMP process. The surface of the tungsten layer 406 may contain a tungsten oxide layer 412 that is formed by atmospheric oxidation or exposure to an oxidizer, such as during an ashing process. The tungsten oxide layer 412 may be continuous or discontinuous across tungsten layer 406 and include a surface terminated with oxygen, hydrogen, hydroxides and combinations thereof. Optionally, the tungsten oxide layer 412 may be removed by a reduction process or a pre-clean process as described above to form a metallic tungsten-containing surface (not shown), substantially free of tungsten oxide layer 412.

[00133] Figure 9B illustrates substrate 400 after a dielectric layer 420 has been formed on the dielectric layer 404 and plug 403. Generally, a void 411 will be formed as the deposited dielectric layer 420 seals off the gap 410 formed in the plug 403. In some cases the dielectric layer 420 may coat the inside surface of void 411 forming dielectric surface 418. In other cases the gap 410 may be completely filled by dielectric material 420 and thus void 411 does not exist (not shown).

[00134] The dielectric layer 420 and the dielectric surface 418 are composed of a dielectric material that may include silicon dioxide, silicon nitride, SOI, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, California. The dielectric material forming dielectric layer 420 and dielectric surface 418 may be deposited by a vapor deposition process such as CVD or plasma-enhanced-CVD (PE-CVD). In one example, a TEOS CVD process, utilizing the precursor tetraethyl orthosilicate ($Si(OC_2H_5)_4$ or TEOS), is conducted to deposit

a silicon oxide material at about 700 °C. In another example, a TEOS PE-CVD process is conducted to deposit a silicon oxide material at about 500 °C.

[00135] Figure 9C illustrates substrate 400 after the dielectric layer 420 has been masked and etched, using conventional techniques, to form a via or aperture 405 to reveal plug 403 and gap 410. In one aspect, the gap 410 may contain a dielectric coating, or dielectric surface 418, as shown. Alternatively, dielectric surface 418 may be removed during the etching process to remove dielectric layer 420 (not shown). In this case a wet or dry etching process(es) may be performed to remove the dielectric surface 418 material from the surface of the gap 410.

[00136] In one embodiment, not shown in Figures 9A-9F, a pretreatment process is performed to remove the tungsten oxide surface 412 after the dielectric surface 418 has been removed, but prior to depositing the barrier layer 430. In this case the tungsten oxide surface 412 is removed to expose a metallic tungsten-containing surface (*e.g.*, similar to the item 314 in Figure 8B). In one aspect, tungsten oxide surface 412 is chemically reduced to tungsten metal. For example, tungsten oxide surface 412 is exposed to a hydrogen plasma to remove the oxides and form a metallic tungsten-containing surface. In another aspect, the tungsten oxide surface 412 is exposed to vapor deposition process containing diborane to remove the oxides and form metallic tungsten-containing surface containing tungsten boride. In another aspect, the tungsten oxide surface 412 is exposed to wet clean process to further oxidize and remove tungstate ions while leaving behind a metallic tungsten-containing surface. Processes that may be used to perform the pretreatment process are discussed above in conjunction with Figures 8A-8C.

[00137] Thereafter, as illustrated in Figure 9D, barrier layer 430 is deposited on substrate 400, including on dielectric layer 420, aperture 405 and the gap 410. Barrier layer 430 may contain a material that acts as an adhesion and/or diffusion barrier layer for the subsequently deposited materials deposited thereon, such as copper. Materials to form barrier layer 430 may include tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Barrier layer 430 may be deposited by vapor deposition process that includes PVD, ALD or CVD. Preferably, barrier layer 430 is a tantalum-containing compound deposited by a PVD process. In one aspect, not shown, the barrier layer 430 may be removed from the surface of

the plug 403 by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers.

[00138] Figure 9E illustrates the substrate 400 after an optional seed layer 440 has been deposited on barrier layer 430 and into gap 410. The optional seed layer 440 may increase adhesion or promote nucleation sites for subsequently deposited bulk-fill materials. The seed layer 440 may be a continuous layer or a non-continuous layer across the surface of barrier layer 430. Therefore, barrier layer 430 may be exposed if seed layer 440 is a non-continuous layer. Seed layer 440 may contain a metal, such as, copper, tungsten, tantalum, titanium, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Seed layer 440 may be deposited by a vapor deposition process that includes PVD, ALD and CVD or a liquid deposition process that includes electroless or electroplating. Preferably, seed layer 440 is a copper-containing compound deposited by a PVD process.

[00139] Figure 9F illustrates substrate 400 after a bulk fill layer 450 has been deposited on seed layer 440, thus filling gap 410 and aperture 405. The deposition of bulk fill layer 450 completes the formation of interconnect plug 443 that is in electrical contact to plug 403. Bulk fill layer 450 may contain a conductive metal that includes copper (Cu), tungsten (W), aluminum (Al), ruthenium (Ru), nickel (Ni), cobalt (Co), alloys thereof, derivatives thereof or combinations thereof. Bulk fill layer 450 may be deposited by a vapor deposition process that includes PVD and CVD or a liquid deposition process that includes electroless or electroplating. In one example, bulk fill layer 450 is a copper-containing compound deposited by a PVD process. In another example, bulk fill layer 450 is a tungsten-containing compound deposited by a CVD process. In another example, bulk fill layer 450 is a nickel-containing compound deposited by an electroless deposition process. In another example, bulk fill layer 450 is a cobalt-tungsten alloy deposited by an electroless deposition process. In another example, bulk fill layer 450 is a copper-containing compound deposited by an electroless deposition process. In another example, bulk fill layer 450 is a copper-containing compound deposited by an electroplating process. An exemplary electroplating deposition process and apparatus that may be in one or more of the electroplating deposition processes described herein is further described in the commonly assigned and copending United States Patent Application Serial No. 10/268,284 [APPM 7669], filed 10/09/02 and United States

Patent Application Serial No. 110/616,284 [APPM 7669P1], filed 07/08/03, which are both incorporated by reference in their entirety.

Alternate Interconnect Formation Process

[00140] In another embodiment, a process is used to initiate on a tungsten containing contact plug to form an interconnect feature 505. Figures 10A-10G illustrate the process of forming an interconnect plug 543 (See Figures 10D and 5G) over the plug 503 so that an electrical connection can be made between the contact layer 502, the interconnect plug 543 and any subsequently deposited layers, such as the M2 interconnect layers (not shown). In general this process starts by depositing a dielectric layer over the plug 503 that was previously formed on the substrate 500. Then various conventional lithographic patterning and etching techniques are used to form an aperture 505 (or via) so that an interconnect layer (*i.e.*, bulk fill layer 550) can be deposited on the plug 503.

[00141] Figure 10A illustrates a cross-sectional view of substrate 500 after a CMP process has been performed on a tungsten-containing contact plug. Substrate 500 contains contact layer 502, dielectric layer 504 and plug 503 that includes tungsten layer 506. The surface 512 of the tungsten layer 506 may contain a tungsten oxide layer that is formed by atmospheric oxidation or exposure to an oxidizer, such as during an ashing process. The tungsten oxide layer may be continuous or discontinuous across tungsten layer 506 and include a surface terminated with oxygen, hydrogen, hydroxides and combinations thereof. Optionally, the tungsten oxide layer may be removed by a reduction process or a pre-clean process as described above to form a metallic tungsten-containing surface (not shown), substantially free of tungsten oxide layer.

[00142] Figure 10B illustrates substrate 500 after a dielectric layer 520 has been formed on the dielectric layer 504 and plug 503. The dielectric layer 520 may be composed of a dielectric material that may include silicon dioxide, silicon nitride, SOI, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, California. The dielectric material forming dielectric layer 520 may be deposited by a vapor deposition process such as CVD or plasma-enhanced-CVD (PE-CVD). In one example, a TEOS CVD process, utilizing the

precursor tetraethyl orthosilicate ($Si(OC_2H_5)_4$ or TEOS), is conducted to deposit a silicon oxide material at about 700 °C. In another example, a TEOS PE-CVD process is conducted to deposit a silicon oxide material at about 500 °C.

[00143] Figure 10C illustrates substrate 500 after the dielectric layer 520 has been masked and etched, using conventional techniques, to form a via or aperture 505 to reveal plug 503. In general, it is desirable to assure that all of the dielectric layer 520 is removed from the exposed regions of the surface 512 of the plug 503.

[00144] In one embodiment, not shown in Figures 10A-10F, a pretreatment process is performed to remove the tungsten oxide layer on the surface 512 after the dielectric material has been removed, but prior to depositing the barrier layer 530 or bulk fill layer 550. In this case the tungsten oxide on the surface 512 is removed to expose a metallic tungsten-containing surface (*e.g.*, similar to the item 314 in Figure 8B). In one aspect, tungsten oxide is chemically reduced to tungsten metal. For example, tungsten oxide is exposed to a hydrogen plasma to remove the oxides and form a metallic tungsten-containing surface. In another aspect, the tungsten oxide is exposed to vapor deposition process containing diborane to remove the oxides and form metallic tungsten-containing surface containing tungsten boride. In another aspect, the tungsten oxide is exposed to wet clean process to further oxidize and remove tungstate ions while leaving behind a metallic tungsten-containing surface. Processes that may be used to perform the pretreatment process are discussed above in conjunction with Figures 8A-8C.

Pretreatment Process Example

[00145] In one embodiment of the pretreatment process, various processing steps 3000 (see Figure 15) are used to prepare the surface of the substrate prior to depositing the bulk fill layer 550. In one embodiment, the processing steps 3000 generally includes 1) an oxide removal step, 2) a surface preparation step, 3) an activation step, 4) an optional activation rinse step, and 5) an optional chelating rinse step. Each of the steps will be discussed in turn.

[00146] In the first step of the pretreatment process, or step 3002, the surface 512 is exposed to a clean solution to remove leftover etch residues from the formation of the interconnect feature 505 and/or any left over dielectric material (Item # 520 Figure 5B). In one aspect, the clean solution may be useful to remove some of the

tungsten oxides formed on the surface 512, but cleaning solutions that are too aggressive will aggressively attack commonly used dielectric layer 520 materials. The preparation of the surface 512 typically requires a clean solution that has a low pH. The pH of the clean solution is usually adjusted by adding an acid or a base (*e.g.*, DEA, TEA) to the predetermined value. The clean process usually includes an acidic clean solution with a pH of about 4 or less, preferably, in a range from about 1.5 to about 3. The acid may include hydrochloric acid (HCl), hydrogen fluoride (HF), sulfuric acid (H_2SO_4), nitric acid (HNO_3), phosphoric acid (HPO_4), derivatives thereof and combinations thereof. In one aspect, the clean solution contains between about 0.1 wt% and about 5 wt% of hydrofluoric acid (HF). Preferably, the clean solution contains about 0.5 wt% of hydrofluoric acid (HF). During a typical clean process a clean solution is dispensed across or sprayed on the surface of substrate 500 at a temperature at or near room temperature. The time the clean solution is in contact with the surface of the substrate to achieve a desired result may depend on the prior processing steps the substrate has gone through and the concentration of the clean solution components. For example, an aqueous solution that contains about 0.5 wt% of hydrofluoric acid (HF) may only require about a 30 second exposure to the substrate surface.

[00147] In the second step of the pretreatment process, or step 3003, the surface 512 is exposed to surface preparation step that is adapted to further normalize the surface 512 prior to performing the subsequent deposition steps. It is believed that exposure of the surface 512 to a tungstate source will tend to normalize the activity of all the exposed regions across the substrate surface so that they all behave similarly in the subsequent processing steps. In this step a preparation solution containing tungstic acid (H_2WO_4) and/or various tungstate salts, or other water soluble WO_4^{2-} sources, hydrates thereof, derivatives thereof or combinations thereof are dispensed on the substrate surface to promote the bonding of the subsequent layers to the substrate surface. In one aspect, the preparation solution contains tungstic acid in a concentration between about 0.002 M and about 0.1 M, and has an adjusted pH of between about 12 and about 13 by the addition of a base (*e.g.*, TMAH). Preferably, the tungstic acid concentration in the preparation solution is between about 0.06 and about 0.1 M and the pH is about 12.5. In one aspect, the preparation solution is dispensed on the surface of the substrate at a temperature at

or near room temperature (*e.g.*, ~20 °C). The time the preparation solution is in contact with the surface of the substrate to achieve a desired result may depend on the prior processing steps the substrate has gone through and the concentration of the processing solution components. For example, an aqueous solution that contains about 10 g/l of tungstic acid and has adjusted pH of about 12.5 may only require between about a 30 second and about a 45 second exposure to the substrate surface.

[00148] In the third step of the pretreatment process, or step 3004, prior to the deposition of the bulk fill layer 550 the surface 512 is activated using an activation solution. During this step, an initiation layer (not shown) may be formed on the surface 512 by displacement plating of a catalytic metal such a palladium, platinum, ruthenium, osmium, rhodium or iridium. Typical procedures for cleaning and displacement plating of tungsten with palladium employ dilute aqueous acid solutions of palladium salts such as palladium chloride, palladium nitrate or palladium sulfate. An example of a suitable acidic activation solution is one prepared by addition of about 4 ml of a 10 wt% $Pd(NO_3)_2$ in 10% nitric acid to 1 liter of deionized water. In another example, an activation solution contains about 120 ppm palladium chloride and sufficient hydrochloric acid to provide a pH in a range from about 1.5 to about 3. Substrates to be activated are exposed to the activation solution for about 30 seconds at room or ambient temperature.

[00149] Next an optional rinse process (step 3005) is used to activate the initiation layer, clean the substrate surface and/or remove remaining contaminants from any of the early processes. In this step a rinse activation solution is dispensed on the substrate surface to activate the initiation layer formed in the third step. In one aspect, the rinse activation solution is a reducing solution (*e.g.*, DMAB, glyoxylic acid) that is delivered to the substrate surface for wetting, cleaning and thermally equilibrating the substrate surface. In one aspect, one liter of a rinse activation solution containing about 1.2 g DMAB and about 3.3 g of 50% H_3PO_2 to DI water at ambient temperature, and enough 25% TMAH to adjust the pH to about 9.25, is dispensed on the substrate surface. In another aspect, a rinse activation solution may contain about 1.2 g/L DMAB, 7.2 g/L of citric acid, 0.1 g/L of hydroxypyridine (a stabilizer), and about 3.3 g/L of 50% H_3PO_2, DI water, and then adding 25% TMAH to adjust the pH to about 9.25. In one aspect, the rinse activation solution contains

DMAB in a concentration from about 1 mM to about 200 mM, and preferably, about 20 mM. In one example, the rinse process may be for about 30 seconds.

[00150] Next an optional chelating process (step 3006) that uses a chelating solution is dispensed on the substrate surface to clean the substrate surface and/or remove remaining contaminants from any of the early processes. The chelating solution is used to remove and prevent particles from forming on the activated surface. In one aspect, a room temperature chelating solution containing about 0.1 M of citric acid is dispensed on and/or remains in contact with the substrate surface for about 30 seconds.

[00151] One will note that a rinse process will general follow each process steps described above, to reduce the interaction of the various chemicals. The rinse process includes rinsing the substrate surface with deionized water at or near room temperature. The substrate will be rinsed for a period from about 1 second to about 30 seconds, preferably from about 5 seconds to about 10 seconds.

[00152] Referring to Figure 5D, a bulk fill layer 550 is then deposited on the surface 512 of the plug 503 to fill the aperture 505. In this configuration the bulk fill layer 550 may be selectively deposited so that the plug 543 is filled from the bottom up, thus preventing defects from being formed in the plug 543 from the growth of the film on the side walls of the aperture 505 (*e.g.*, typically described as "pinch off"). In one aspect, the bulk fill layer 550 may be selectively deposited on the surface 512 by use of a vapor deposition process that includes ALD or CVD. Preferably, the bulk fill layer 550 is selectively deposited using an electroless deposition process. In one aspect, electrolessly deposited films are preferred, since they will not contain the amount of carbon that CVD and ALD deposited films contain due to the incorporation of the CVD or ALD precursor materials in the deposited film. The incorporation of carbon in the deposited film will affect the resistivity and adhesion of the deposited layer to prior or subsequently deposited layers. Electrolessly deposited films are also favored over PVD deposited films, since PVD deposited films will tend to "pinch off" at the top of the aperture 505, since PVD it is a line-of-sight type deposition process. Electroless deposition processes are also useful to form metal layers that have two or more metal components contained therein. In one aspect, it may be desirable to varying composition of the electrolessly deposited

layer that contains two or more metal components. An exemplary process and hardware that may be used to form a metal layer having a varying composition is described in the commonly assigned United States Patent Application Serial No. 11/040,962 [APPM 8926], filed 1/22/2005, which is incorporated by reference herein in its entirety. The bulk fill layer 550 may contain a conductive metal that includes copper (Cu), tungsten (W), aluminum (Al), ruthenium (Ru), nickel (Ni), cobalt (Co), alloys thereof, derivatives thereof or combinations thereof. In one aspect, the bulk fill layer 550 may include cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB), derivatives thereof or combinations thereof. Preferably, bulk fill layer 550 is a nickel boride compound deposited by a an electroless deposition process.

[00153] In another embodiment, as shown in Figure 10E, after forming the aperture 505 (see Figure 10C) a barrier layer 530 is deposited on substrate 500, including on dielectric layer 520, and aperture 505. Barrier layer 530 may contain a material that acts as an adhesion and/or diffusion barrier layer for the subsequently deposited materials deposited thereon, such as copper. Materials to form barrier layer 530 may include tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Barrier layer 530 may be deposited by vapor deposition process that includes PVD, ALD or CVD. Preferably, barrier layer 530 is a tantalum-containing compound deposited by a PVD process. In one aspect, not shown, the barrier layer 530 may be removed from the surface of the plug 503 by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers.

[00154] Figure 10F illustrates the substrate 500 after an optional seed layer 540 has been deposited on barrier layer 530. The optional seed layer 540 may increase adhesion or promote nucleation sites for subsequently deposited bulk-fill layer 550. The seed layer 540 may be a continuous layer or a non-continuous layer across the

surface of barrier layer 530. Therefore, barrier layer 530 may be exposed if seed layer 540 is a non-continuous layer. Seed layer 540 may contain a metal, such as, copper, tungsten, tantalum, titanium, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Seed layer 540 may be deposited by a vapor deposition process that includes PVD, ALD and CVD or a liquid deposition process that includes electroless or electroplating. Preferably, seed layer 540 is a copper-containing compound deposited by a PVD process.

[00155] Figure 10G illustrates substrate 500 after a bulk fill layer 550 has been deposited on seed layer 540, thus the aperture 505. The deposition of bulk fill layer 550 completes the formation of interconnect plug 543 that is in electrical contact to plug 503. Bulk fill layer 550 may contain a conductive as described above. Bulk fill layer 550 may be deposited by a vapor deposition process that includes PVD and CVD or a liquid deposition process that includes electroless or electroplating. In one embodiment, the bulk fill layer 550 is a copper-containing compound deposited by a PVD process. In another example, bulk fill layer 550 is a tungsten-containing compound deposited by a CVD process. In another example, bulk fill layer 550 is a nickel-containing compound deposited by an electroless deposition process. In another example, bulk fill layer 550 is a cobalt-tungsten alloy deposited by an electroless deposition process. In another example, bulk fill layer 550 is a copper-containing compound deposited by an electroless deposition process. In another example, bulk fill layer 550 is a copper-containing compound deposited by an electroplating process.

Examples of Electroless Process Solutions

[00156] The following are a examples of various electroless chemistries and processes that may be used to form the fill material 230, fill material 320, seed/adhesion layer 325, conductive layer 350, seed layer 440, bulk fill layer 450, seed layer 540, and/or bulk fill layer 550.

Electroless Nickel Deposition Chemistries and Processes

[00157] In one example, an electroless deposition solution useful to form nickel-containing material contains a nickel source, a reductant, at least one complexing agent, a pH adjusting agent, water and optional additives and surfactants. Nickel-containing material may be deposited by an electroless process utilizing either a pre-

mixed electroless deposition solution or an in-line mixing process that combines solution components to generate the electroless solution.

[00158] The nickel source within the electroless deposition solution may have a concentration within a range from about 20 mM to about 200 mM, preferably from about 40 mM to about 80 mM, and more preferably from about 50 mM to about 70 mM, such as about 60 mM. Nickel sources provide nickel ions (*e.g.*, Ni^{2+}) dissolved within the electroless solution and later reduced out as the deposited nickel-containing material. Useful nickel sources include nickel sulfate, nickel chloride, nickel acetate, nickel phosphate, derivatives thereof, hydrates thereof or combinations thereof. In a preferred embodiment, nickel sulfate hexahydrate ($NiSO_4 \bullet 6H_2O$) is used in the electroless solution to deposit nickel-containing materials.

[00159] The reductant within the electroless deposition solution may have a concentration within a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 5 mM to about 20 mM, such as about 14 mM. Reductants provide electrons to induce chemical reduction of the nickel ions that form and deposit the nickel-containing material. Reductants may include organic reductants (*e.g.*, formaldehyde or glyoxylic acid), hydrazine, organic hydrazines (*e.g.*, methyl hydrazine), hypophosphite sources (*e.g.*, hypophosphorous acid (H_3PO_2), ammonium hypophosphite ($(NH_4)_{4-x}H_xPO_2$) and salts thereof), borane sources (*e.g.*, dimethylamine borane complex ($(CH_3)_2NH \bullet BH_3$), DMAB), trimethylamine borane complex ($(CH_3)_3N \bullet BH_3$), TMAB), tert-butylamine borane complex ($^tBuNH_2 \bullet BH_3$), tetrahydrofuran borane complex ($THF \bullet BH_3$), pyridine borane complex ($C_5H_5N \bullet BH_3$), ammonia borane complex ($NH_3 \bullet BH_3$), borane (BH_3), diborane (B_2H_6), derivatives thereof, complexes thereof or combinations thereof. In a preferred embodiment, DMAB is used as a reductant in the electroless solution for depositing nickel-containing materials.

[00160] Chelators or complexing agents are in the electroless solution to complex nickel ions thereby stabilizing the solubility and reduction of nickel ions. The complexing agents may have a concentration within a range from about 50 mM to about 2 M, preferably from about 100 mM to about 1 M, and more preferably from about 200 mM to about 500 mM. Complexing agents generally may have functional

groups, such as carboxylic acids, dicarboxylic acids, polycarboxylic acids, amino acids, amines, diamines, polyamines, alkylamines, alkanolamines and alkoxyamines. Complexing agents may include citric acid, citrates, glycolic acid, glycine, malonic acid, maleic acid, lactic acid, ethylenediaminetetraacetic acid (EDTA), ethylenediamine (EDA), triethylene tetramine (TETA), diaminoethane, monoethanolamine, diethanolamine (DEA), triethanolamine (TEA), hydroxylamine hydrochloride, ammonia, ammonium chloride, derivatives thereof, salts thereof or combinations thereof. Usually, the electroless solution contains more than one complexing agent. Preferably, the electroless solution contains at least citric acid or citrate salts, more preferably, the electroless solution also contains DEA, glycine and/or lactic acid. In one example, the electroless solution contains about 60 mM of citric acid, 60 mM of DEA, 15 mM of glycine and 120 mM of lactic acid.

[00161] A pH adjusting agent is added to adjust the electroless solution to a pH value within a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 9.2 to about 9.6, such as about 9.4. The pH adjusting agent may be an acidic compound to decrease the pH value of the electroless solution and include hydrochloric acid, sulfuric acid, phosphoric acid, derivatives thereof or combinations thereof. Alternatively, the pH adjusting agent may be a basic compound to increase the pH value of the electroless solution and include metal hydroxides, tetraalkylammonium hydroxides (*e.g.,* tetramethylammonium hydroxide ($(CH_3)_4NOH$, TMAH) or tetraethylammonium hydroxide ($(CH_3CH_2)_4NOH$, TEAH)), ammonium hydroxide, DEA, TEA, derivatives thereof or combinations thereof. The pH adjusting agent may be dissolved in water prior to adjusting the pH value of the electroless solution. In one example, a 25 wt% aqueous solution of TMAH is used as a pH adjusting agent. In another example, both TMAH and DEA are used to adjust the pH value of an electroless solution.

[00162] The optional additives may include levelers, accelerators and suppressors. Levelers within the electroless solution are used to achieve different deposition thickness as a function of leveler concentration and feature geometry while depositing nickel-containing materials. The leveler within the electroless deposition solution may have a concentration within a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm. Examples of levelers that may be employed in an electroless solution include, but are not limited

to alkylpolyimines and organic sulfonates, such as 1-(2-hydroxyethyl)-2-imidazolidinethione (HIT), 4-mercaptopyridine, 2-mercaptothiazoline, ethylene thiourea, thiourea or derivatives thereof. The electroless deposition solution may contain brighteners or accelerators and suppressors as alternative additives to provide further control of the deposition process. The role of accelerators is to achieve a smoothly deposited surface of the nickel-containing material. The accelerator within the electroless deposition solution has a concentration within a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm. Accelerators that are useful in an electroless solution for depositing nickel-containing materials may include sulfur-based compounds such as bis(3-sulfopropyl) disulfide (SPS), 3-mercapto-1-propane sulfonic acid (MPSA), aminoethane sulfonic acids, thiourea, derivatives thereof, combinations thereof. Suppressors are used to suppress nickel deposition by initially adsorbing onto underlying catalytic surfaces and therefore blocking access to the catalyst of the reaction. Suppressors generally may include polyethylene glycol (PEG), polypropylene glycol (PPG), polyoxyethylene-polyoxypropylene copolymer (POCP), benzotriazole (BTA), dipyridyl, dimethyl dipyridyl, derivatives thereof or combinations thereof. The suppressor within the electroless deposition solution may have a concentration within a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm.

[00163] The electroless solution may contain boric acid as an additional additive. Boric acid is added to provide additional buffering and to stabilize the composition of the solution. Boric acid is an oxidation by-product from the chemical reactions of borane reductants (*e.g.,* DMAB). Therefore, an electroless solution containing boric acid is more normalized at the start of the deposition process since a less steep dissipation gradient exist as additional boric acid is formed from the borane reductant. Boric acid is preferably within the electroless deposition solution at concentration within a range from about 1 mM to about 50 mM, preferably from about 2 mM to about 20 M, and more preferably from about 3 mM to about 15 mM, such as about 5 mM.

[00164] Also, an optional surfactant may be added to the electroless solution. The surfactant is a wetting agent to reduce the surface tension between the electroless solution and the substrate surface. Surfactants are generally added to the

electroless solution at a concentration of about 1,000 ppm or less, preferably about 800 ppm or less, such as from about 20 ppb to about 600 ppm. The surfactant may have ionic or non-ionic characteristics. A preferred surfactant includes dodecyl sulfates, such as sodium dodecyl sulfate (SDS). Other surfactants that may be used in the electroless deposition solution include glycol ether based surfactants (*e.g.,* polyethylene glycol). For example, a glycol ether based surfactants may contain polyoxyethylene units, such as TRITON® 100, available from Dow Chemical Company. A nonylphenol ethoxylate surfactant is useful in the electroless deposition solution, such as TERGITOL®, available from Dow Chemical Company or IGEPAL-630, available from GAF Corporation. Other useful surfactants may contain phosphate units, for example, sodium poly(oxyethylene) phenyl ether phosphate, such as RHODAFAC® RE-610, available from Rhodia, Inc. The surfactants may be single compounds or a mixture of compounds of molecules containing varying length of hydrocarbon chains.

[00165] An electroless process to deposit nickel-containing materials may utilize an in-line mixing process to form the electroless solution. The process may contain the addition of two, three, four or more componential solutions to form the electroless solution. In one example, the electroless solution is formed by combining a buffered cleaning solution, a nickel-containing solution, a reducing solution and water, where each solution is a concentrate and water is added to reach a predetermined concentration of the final solution. In another example, the electroless solution is formed by combining a buffered cleaning solution, a nickel-containing solution and a reducing solution, where each of the solutions are pre-diluted and therefore do not require additional water. In another example, the electroless solution is formed by combining a buffered nickel-containing solution, a reducing solution and water, where a buffered cleaning solution and a nickel-containing solution are combined to form the buffered nickel-containing solution. Further details of in-line mixing processes and componential solutions are further described in the commonly assigned, U.S. Patent Application Serial No. 10/967,919, entitled, "Selective Self-initiating Electroless Capping of Copper with Cobalt-containing Alloys," filed on October 18, 2004, and published as US 2005-0136193, which is incorporated by reference to the extent not inconsistent with the claimed aspects and description herein.

[00166] A buffered cleaning solution usually contains water, at least one complexing agent, additives and a pH adjusting agent. The complexing agent within the buffered cleaning solution is at a concentration from about 0.2 M to about 3 M, preferably from about 0.5 M to about 2 M. The additive within the buffered cleaning solution is at a concentration from about 10 mM to about 1 M, preferably from about 50 mM to about 500 mM. The pH adjusting agent is at a concentration to provide the buffered cleaning solution with a pH value in a range from about 7.5 to about 11, preferably from about 8 to about 10, and more preferably from about 9.2 to about 9.6, such as about 9.4. In one example, a buffered cleaning solution contains water, about 1.15 M of DEA, about 375 mM of citric acid, about 300 mM of glycine, about 100 mM of boric acid and a concentration of TMAH to adjust the pH value to about 9.4. In another example, a buffered cleaning solution contains water, about 330 mM of DEA, about 300 mM of citric acid, about 150 mM of glycine, about 50 mM of boric acid and a concentration of TMAH to adjust the pH value to about 9.4.

[00167] A nickel-containing solution usually contains water, a nickel source, at least one complexing agent and a pH adjusting agent. The nickel source within the nickel-containing solution is at a concentration from about 50 mM to about 1 M, preferably from about 100 mM to about 500 mM, such as about 300 mM. The complexing agent within the nickel-containing solution is at a concentration from about 0.2 M to about 2 M, preferably from about 0.5 M to about 1 M. The pH adjusting agent is at a concentration to provide the nickel-containing solution with a pH value in a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 9.2 to about 9.6, such as about 9.4. In one example, a nickel-containing solution contains water, about 100 mM of citric acid, about 300 mM of nickel sulfate, about 600 mM of 85% lactic acid and a concentration of TMAH to adjust the pH value to about 9.4.

[00168] A reducing solution usually contains water, at least one reductant, at least one complexing agent and a pH adjusting agent. The reductant within the reducing solution is at a concentration from about 10 mM to about 500 mM, preferably from about 50 mM to about 100 mM, such as about 70 mM. The complexing agent within the reducing solution is at a concentration from about 1 mM to about 50 mM, preferably from about 5 mM to about 15 mM, such as about 10 mM. The pH adjusting agent is at a concentration to provide the reducing solution with a pH value

in a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 9.2 to about 9.6, such as about 9.4. In one example, a reducing solution contains water, about 10 mM of citric acid, about 70 mM of DMAB and a concentration of TMAH to adjust the pH value to about 9.4.

[00169] The electroless solution is preferably formed by in-line mixing process that combines various volumetric ratios of the buffered cleaning solution, the nickel-containing solution, the reducing solution and water. In one example, 1 volumetric equivalent of a buffered cleaning solution, 4 volumetric equivalents of a nickel-containing solution, 4 volumetric equivalents of a reducing solution and 11 volumetric equivalents of deionized water are in-line mixed to form an electroless solution. That is, the volumetric ratio of the buffered cleaning solution, the nickel-containing solution, the reducing solution and the deionized water is 1:4:4:11 (5%, 20%, 20%, 55% of electroless solution). In other examples of an electroless solution, a volumetric ratio of the buffered cleaning solution, the nickel-containing solution, the reducing solution and the water is 1:2:2:5 (10%, 20%, 20%, 50% of electroless solution) and 1:1:1:3 (16.7%, 16.7%, 16.7%, 50% of electroless solution).

[00170] In one embodiment, an electroless solution contains: nickel sulfate with a concentration in a range from about 20 mM to about 200 mM, preferably from about 40 mM to about 80 mM, and more preferably from about 50 mM to about 70 mM, such as about 60 mM; DMAB with a concentration in a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 5 mM to about 20 mM, such as about 14 mM; citric acid with a concentration in a range from about 5 mM to about 500 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 40 mM to about 80 mM, such as about 60 mM; DEA with a concentration in a range from about 5 mM to about 500 mM, preferably from about 10 mM to about 200 mM, such as about 60 mM; glycine with a concentration in a range from about 1 mM to about 150 mM, preferably from about 2 mM to about 80 mM, and more preferably from about 5 mM to about 50 mM, such as about 15 mM; boric acid with a concentration in a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 3 mM to about 20 mM, such as about 5 mM; lactic acid with a concentration in a range from about 10 mM to about 500 mM, preferably from about 50 mM to about 200 mM, and more preferably from about 100 mM to

about 140 mM, such as about 120 mM; TMAH with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 9.2 to about 9.6, such as about 9.4.

[00171] In one embodiment, citrate is a preferred complexing agent and is present in each componential solution, such as the buffered cleaning solution, the nickel-containing solution and the reducing solution. Citrate may be added as citric acid and/or as a citrate salt. Citrate plays an important role of buffering each of the individual componential solutions while being combined to form the plating solution. Citrates generally have poor solubility in water at high concentrations, while the componential solutions may have relatively concentrated solutions. If a substantial citrate concentration of the final electroless solution is desired, a single componential solution may not be capable of completely containing all the dissolved citrate. Therefore, the citrate may be dissolved in each componential solution to assure no formation of citrate precipitate, and subsequently combined with water forming the electroless solution at a final concentration.

[00172] The electroless deposition process may be conducted at a temperature in a range from about 35°C to about 120°C, preferably from about 60°C to about 100°C. In one example, the temperature is from about 80°C to about 85°C. In another example, the temperature is from about 65°C to about 70°C. The water may be degassed, preheated and/or deionized water. Degassing the water reduces the oxygen concentration of the subsequently formed electroless solution. An electroless solution with a low oxygen concentration (*e.g.,* less than about 100 ppm) may be used during the deposition process. Preheated water allows forming the electroless solution at a predetermined temperature just below the temperature used to initiate the deposition process, thereby shortening the process time.

[00173] The substrate may be exposed to a chemical mechanical polishing (CMP) process prior to the pretreatment and deposition processes described herein. Usually, the CMP process is conducted in a first process chamber, the nickel-containing layer or cobalt-tungsten alloy layer is deposited in a second process chamber and the first and second process chambers are on the same CMP tool. In one example, the second process chamber is in fluid communication to an in-line

mixing system that combines stock solutions used in the pretreatment process and/or the electroless deposition processes.

[00174] A "substrate surface" as used herein refers to any substrate or material surface formed on a substrate upon which film processing is performed. For example, a substrate surface on which processing may be performed include materials such as monocrystalline, polycrystalline or amorphous silicon, strained silicon, silicon on insulator (SOI), doped silicon, silicon germanium, germanium, gallium arsenide, glass, sapphire, silicon oxide, silicon nitride, silicon oxynitride and/or carbon doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, California. Substrates may have various dimensions, such as 200 mm or 300 mm diameter wafers, as well as, rectangular or square panes. Embodiments of the processes described herein deposit nickel-containing materials on many types of substrates and surfaces. Substrates on which embodiments of the invention may be useful include, but are not limited to semiconductor wafers, such as crystalline silicon (*e.g.,* Si<100> or Si<111>), silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, doped or undoped silicon wafers, and patterned or non-patterned wafers. Substrates made of glass or plastic, which, for example, are commonly used to fabricate flat panel displays and other similar devices, are also included.

[00175] A chamber useful to conduct an electroless deposition process for depositing a cobalt-tungsten material, a cobalt-nickel material or a nickel-containing material is the electroless deposition process cell, further described in the commonly assigned U.S. Patent Application Serial No. 10/965,220, entitled "Apparatus for Electroless Deposition," filed on October 14, 2004, and published as US 2005-0081785, U.S. Patent Application Serial No. 10/996,342, entitled, "Apparatus for Electroless Deposition of Metals on Semiconductor Wafers," filed on November 22, 2004, U.S. Patent Application Serial No. 11/043,442, entitled, "Apparatus for Electroless Deposition of Metals onto Semiconductor Substrates," filed on January 26, 2005, and U.S. Patent Application Serial No. 11/040,962, entitled "Method and Apparatus for Selectively Changing Thin Film Composition During Electroless Deposition in a Single Chamber," filed on January 22, 2005, which are each

incorporated by reference to the extent not inconsistent with the claimed aspects and description herein.

Examples of Cobalt and Nickel Electroless Deposition Chemistries

Cobalt

[00176] In one embodiment, an electroless solution for depositing metallic cobalt contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; hydrazine hydrate with a concentration in a range from about 100 mM to about 2 M, preferably from about 200 mM to about 1 M, and more preferably from about 300 mM to about 700 mM, such as about 500 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 70 mM, such as about 50 mM; and an optional pH adjusting agent (*e.g.,* TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 10 to about 14, preferably from about 11.5 to about 13, and more preferably from about 12.2 to about 12.8, such as about 12.5. In one example, a pH value is about 11.5 or higher, preferably, about 12.0 or higher, and more preferably, about 12.5 or higher. The electroless deposition process to deposit metallic cobalt may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 90°C, and more preferably from about 70°C to about 80°C, such as about 75°C.

Cobalt Boride

[00177] In one embodiment, an electroless solution for depositing cobalt boride contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM;

and an optional pH adjusting agent (*e.g.,* TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit cobalt boride may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 80°C, and more preferably from about 65°C to about 75°C, such as about 70°C.

Cobalt Tungsten Boride

[00178] In one embodiment, an electroless solution for depositing cobalt tungsten boride contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; tungstic acid or tungstate salt with a tungstate concentration in a range from about 0.1 mM to about 10 mM, preferably from about 0.5 mM to about 5 mM, and more preferably from about 1 mM to about 3 mM, such as about 2 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (*e.g.,* TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit cobalt tungsten boride may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 80°C, and more preferably from about 65°C to about 75°C, such as about 70°C.

Nickel Boride

[00179] In one embodiment, an electroless solution for depositing nickel boride contains: nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 80 mM, such as about 60 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from

about 10 mM to about 50 mM, such as about 28 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 60 mM, such as about 58 mM; boric acid with a concentration in a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 3 mM to about 20 mM, such as about 5 mM; lactic acid or lactate salt with a lactate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 150 mM, such as about 120 mM; glycine with a concentration in a range from about 1 mM to about 150 mM, preferably from about 2 mM to about 80 mM, and more preferably from about 5 mM to about 50 mM, such as about 15 mM; diethanolamine (DEA) with a concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 150 mM, such as about 58 mM and an optional pH adjusting agent (*e.g.,* TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit nickel boride may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 80°C, and more preferably from about 65°C to about 75°C, such as about 70°C.

Nickel Tungsten Boride

[00180] In one embodiment, an electroless solution for depositing nickel tungsten boride contains: nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; tungstic acid or tungstate salt with a tungstate concentration in a range from about 0.1 mM to about 10 mM, preferably from about 0.5 mM to about 5 mM, and more preferably from about 1 mM to about 3 mM, such as about 2 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 40 mM to about 60 mM, such as about 50 mM; lactic acid or lactate salt with a lactate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 40 mM to about 60

mM, such as about 50 mM; and an optional pH adjusting agent (*e.g.*, TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit nickel tungsten boride may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 80°C, and more preferably from about 65°C to about 75°C, such as about 70°C.

Cobalt Nickel Boride

[00181] In one embodiment, an electroless solution for depositing cobalt nickel boride contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (*e.g.*, TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit cobalt nickel boride may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 80°C, and more preferably from about 65°C to about 75°C, such as about 70°C.

Cobalt Nickel

[00182] In one embodiment, an electroless solution for depositing cobalt nickel contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5

mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; hydrazine hydrate with a concentration in a range from about 100 mM to about 2 M, preferably from about 200 mM to about 1 M, and more preferably from about 300 mM to about 700 mM, such as about 500 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (*e.g.,* TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 10 to about 14, preferably from about 11.5 to about 13, and more preferably from about 12.2 to about 12.8, such as about 12.5. The electroless deposition process to deposit cobalt nickel may be conducted at a temperature within a range from about 35°C to about 100°C, preferably from about 60°C to about 90°C, and more preferably from about 70°C to about 80°C, such as about 75°C.

IN-SITU SILICIDATION METALLIZATION PROCESS

[00183] Embodiments of the invention further provide a simplified method of filling contact level features formed in a semiconductor device. In general the method includes a novel method of forming a contact level feature that contains a silicide interface and a tungsten CVD deposited layer. The processes discussed below are less complex and less time consuming than other conventional contact level interconnect formation processes and thus will have an improved device yield.

[00184] A simplified example of a conductive interconnect is typical MOS device shown in Figure 11. In the illustrated MOS structure, the conductive N+ source and drain regions 1402 and 1404 are formed in a P-type silicon substrate 1400, which are adjacent to the field oxide portions 1406. A gate oxide layer 1408 and a polysilicon gate electrode 1410 are formed over silicon substrate 1400 in between source and drain regions 1402 and 1404 with oxide spacers 1412 formed on the sidewalls of polysilicon gate electrode 1410. A dielectric material 1422 may be deposited over the formed structure and etched to provide a contact level aperture 1420. The contact level apertures 1420 are then filled with a thin barrier layer 1405 and a contact material 1407. The barrier layer 1405 may be tungsten, cobalt or titanium and titanium nitride stack that is typically deposited using a physical vapor deposition (PVD) process. The contact material 1407, which is typically a tungsten

containing layer, is formed using a chemical vapor deposition (CVD) or atomic layer deposition (ALD) techniques. After depositing the barrier layer 1405 a silicide layer 1403 is formed at the interface of the source and drain regions 1402 and 1404 by allowing the deposited barrier layer 1405 metal to form a silicide during a high temperature thermal anneal step (*e.g.*, ~800-1000 °C). The contact level apertures 1420 thus provide a low resistance interconnect between various parts of the device (*e.g.*, source region, drain region) and the layers above (not shown).

1. Silicidation During Tungsten Deposition Process

[00185] Figure 12 illustrates a series of method steps 2000 that may be used to fill a contact level feature. Figure 13A illustrates a cross-sectional view of substrate 1500 having a contact level aperture 1510 formed into dielectric layer 1504. The dielectric layer 1504 contains an insulating material that includes silicon dioxide, silicon nitride, SOI, BPSG, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, California. Contact level aperture 1510 may be formed in dielectric layer 1504 using conventional lithography and etching techniques to expose the silicon junction 1502, such as a MOS type source or drain interface. Silicon junction 1502 is generally a doped silicon region, such as a N+ or P+ doped silicon region.

[00186] An oxide surface 1512 is usually formed at the silicon junction 1502 during previous etching and ashing processes used to form contact level aperture 1510. Oxide surface 1512 may be a continuous layer or a discontinuous layer across the surface of silicon junction 1502 and include a surface terminated with oxygen, hydrogen, hydroxides, a metal or combinations thereof. In examples wherein silicon junction 1502 contains a silicon-containing material, oxide surface 1512 is usually a silicon oxide surface. Also, in examples wherein silicon junction 1502 contains a metal-containing material, oxide surface 1512 is usually a metal oxide surface.

[00187] The first step of the method steps 2000 includes a pretreatment process step 2002, to remove the oxide layer so subsequent processes can be preformed on the surface of the silicon junction 1502. In this process step the substrate 1500 is exposed to a pretreatment process to form a treated surface (not shown) on the silicon junction 1502, which is substantially free of oxide surface 1512. In one

example, the silicon junction 1502 contains a silicon-containing material and treated surface contains a hydride-terminus surface, such as a silicon hydride layer. In another example, the silicon junction 1502 contains a metal-containing material and the treated surface contains a reduced metal surface. The various processes that may be used to perform the pretreatment process step 2002 on the surface of the silicon junction 1502 are described below (see Pretreatment Process).

[00188] The second step of the method steps 2000 includes a metal deposition step 2004, that is used to form a metal layer 1514 over the silicon junction 1502. In one aspect, the metal layer 1514 is a nickel containing layer. The metal deposition step 2004 may be performed by use of a PVD, CVD, plasma enhanced CVD, ALD, plasma enhanced ALD or electroless deposition process to form the nickel layer. In one aspect, when a non-selective deposition process is used, such as a PVD, non-selective CVD, non-selective plasma enhanced CVD, non-selective ALD, and/or non-selective plasma enhanced ALD process(es), the method steps 2000 may include an optional nickel removal step 2006. The optional metal removal step includes the step of removing any deposited nickel from the field region 1505 (Figures 13A-B) by use of a wet clean process, CMP process, electrochemical process or other comparable material removal processes.

[00189] In one aspect of method steps 2000, as shown in Figure 13C, the metal deposition step 2004 is performed using a selective nickel deposition process to deposit the metal layer 1514 over the silicon junction 1502. In this case the selectively deposited electroless nickel layer is only formed over the silicon junction 1502. An exemplary selective electroless deposition process is described below. In this case there is generally no need to perform the optional metal removal step 2006, since the metal layer 1514 will be selectively deposited at the surface of the silicon junction 1502.

[00190] The last step of the method steps 2000 is the deposit a tungsten containing layer to fill the contact level aperture 1510 using a CVD tungsten deposition process that is performed at a temperature that will cause at least some portion of the metal layer 1514 to form a metal silicide layer 1515 (*e.g.*, NiSi, Ni_2Si). The tungsten CVD deposition process used in step 2010 is performed using conventional tungsten hexafluoride (WF_6) precursor chemistries at a temperature in the range between about 300 °C and about 450 °C. Preferably, the CVD tungsten

deposition process temperature is about 350 °C. A conventional CVD process generally involves the simultaneous introduction of gas phase reactants, such as tungsten precursor (typically tungsten hexafluoride) and a hydrogen containing gas (*e.g.*, H_2), near a heated wafer surface while a vacuum is applied to the system. The reaction is driven by the energy provided by the heated wafer and the free energy change of the chemical reaction. In this step a tungsten layer 1520 is directly deposited on the metal layer 1514 formed on the silicon junction 1502 during step 2004. In one aspect, the metal layer 1514 is deposited to a thickness between about 10 Å and about 100 Å. In one aspect of step 2010, at the end of the tungsten deposition process a metal silicide layer 1515 (*e.g.*, nickel silicide (Ni_xSi)) is formed having sufficient thickness to form a good electrical contact (*e.g.*, ohmic contact) between the tungsten layer 1520 and the silicon junction 1502. A metal silicide layer is formed as the metal layer 1514 reacts with the silicon atoms found at the silicon junction 1502 interface, thus consuming at least a portion of the metal layer 1514 and some of the silicon atoms at the silicon junction. Since tungsten hexafluoride tends to attack the exposed metal layer 1514 during the early stages of the deposition process, it is desirable to assure that the metal layer 1514 thickness is large enough to assure that enough material remains at the silicon junction 1502 after the deposited tungsten layer 1520 has covered the exposed metal layer 1514 to assure that a good silicide contact can be formed.

2. Cobalt Containing Barrier Layer Fill Process

[00191] The second novel method, illustrated in Figure 14, is a series of method steps 2001 that are used to fill a contact level feature. Figure 13A illustrates a cross-sectional view of substrate 1500 having a contact level aperture 1510 formed into dielectric layer 1504. The dielectric layer 1504 contains an insulating material that includes silicon dioxide, silicon nitride, SOI, BPSG, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, California. Contact level aperture 1510 may be formed in dielectric layer 1504 using conventional lithography and etching techniques to expose the silicon junction 1502, such as a source or drain interface. Silicon junction 1502 is generally doped silicon region, such as a N+ or P+ doped silicon region.

[00192] An oxide surface 1512 is usually formed at the silicon junction 1502 during previous etching and ashing processes used to form contact level aperture 1510. Oxide surface 1512 may be a continuous layer or a discontinuous layer across the surface of silicon junction 1502 and include a surface terminated with oxygen, hydrogen, hydroxides, a metal or combinations thereof. In examples wherein silicon junction 1502 contains a silicon-containing material, oxide surface 1512 is usually a silicon oxide surface. Also, in examples wherein silicon junction 1502 contains a metal-containing material, oxide surface 1512 is usually a metal oxide surface.

[00193] The first step of the method steps 2001 includes a pretreatment process step 2002, to remove the oxide layer so subsequent processes can be preformed on the surface of the silicon junction 1502. In this process step the substrate 1500 is exposed to a pretreatment process to form a treated surface (not shown) on the silicon junction 1502, which is substantially free of oxide surface 1512. In one example, the silicon junction 1502 contains a silicon-containing material and treated surface contains a hydride-terminus surface, such as a silicon hydride layer. In another example, the silicon junction 1502 contains a metal-containing material and the treated surface contains a reduced metal surface. The various processes that may be used to perform the pretreatment process step 2002 on the surface of the silicon junction 1502 are described below.

[00194] The second step of the method steps 2001 includes a metal deposition step 2004 (Figure 13C), that is used to deposit a metal layer 1514 over the silicon junction 1502. In one embodiment, the metal layer is a cobalt containing or nickel containing layer. The metal deposition step 2004 may be performed by use of a PVD, CVD, plasma enhanced CVD, ALD, plasma enhanced ALD or electroless deposition process to form a metal containing layer. In one aspect, when a non-selective deposition process is used, such as a PVD, non-selective CVD, non-selective plasma enhanced CVD, non-selective ALD, and/or non-selective plasma enhanced ALD process(es), the method steps 2001 may include an optional metal removal step 2006. The optional metal removal step includes the step of removing any deposited metal(s) from the field region 1505 (Figure 13A-B) by use of a by use of a wet clean process, conventional CMP process, electrochemical process and/or other comparable material removal process.

[00195] In one aspect of method steps 2000, as shown in Figures 13C, the metal deposition step 2004 is performed using a selective deposition process to deposit the metal layer 1514 over the silicon junction 1502. In this case the selectively deposited electroless metal layer is only formed over the silicon junction 1502. An exemplary selective electrochemical deposition of a nickel containing layer is described below. In this case there is generally no need to perform the optional metal removal step 2006, since the metal layer 1514 will be selectively deposited at the surface of the silicon junction 1502.

[00196] In one aspect, the metal layer 1514 is a nickel containing layer. For example, a nickel film is formed on the Si surface using a galvanic plating bath. To perform this process the films are created from a plating bath which contains a nickel(II) salt, such as nickel sulfate, an electrolyte such as tetramethylammonium sulfate, and a wetting agent such as diethanolamine, adjusted to basic pH with tetramethylammonium hydroxide (TMAH) and maintained at temperatures above 60 °C. The wetting agent may be part of the electrolyte. No reducing agent is required to be added. During the galvanic deposition of Ni on silicon (Si), the surface of the Si acts as a reducing agent. In other embodiments, a sacrificial element or structure attached to the silicon may act as a reducing agent. The addition of a wetting agent to the galvanic system eliminates the need for galvanic displacement plating schemes on Si (see attached PDFs). Therefore, a superficial oxidation of the Si surface with a hydrochloric acid/peroxide mixture (HPM), ethanol, or other pre-treatments which allow the galvanic solution to wet the oxide free Si surface (the Si-H surface is very hydrophobic) is not needed. The formation of a nickel film on Si by this method is self-limiting, which allows a mechanism of film thickness control.

[00197] The next process step in the method steps 2001, is a step that uses a conventional thermal processing techniques to cause the deposited metal layer 1514 to form a metal silicide layer 1515 at the silicon junction 1502 (see step 2007). Typically, the conventional thermal processing techniques include performing an RTP or furnace anneal step at temperatures greater than about 250 °C for a desired period of time to cause a desired thickness of the metal silicide to form at the silicon junction 1502. An RTP system that may useful for completing aspects of this invention described herein may be purchased from Applied Materials Inc. of Santa Clara, California.

[00198] The next process step in the method steps 2001 is a selective barrier layer deposition step 2008 (Figure 13F), which generally causes a metal containing layer 1518 to be deposited over the metal silicide layer 1515 formed on the silicon junction 1502. The barrier layer provides for protection of the silicide layer during the tungsten deposition process. In one aspect, the barrier layer is selectively deposited using an electroless deposition process. The barrier layer could also be a PVD tungsten layer followed by a CVD tungsten. The barrier layer deposition step 2008 may be performed by use of a PVD, CVD, plasma enhanced CVD, ALD, plasma enhanced ALD or electroless deposition process to form a cobalt containing layer in the contact level aperture 1510. In one aspect, the metal containing layer 1518 is a cobalt containing layer. In one aspect, as shown in Figure 13F, cobalt containing layer deposition step 2008 is adapted to selectively deposit the metal containing layer 1518 on the metal silicide layer 1515. In one aspect, the selective barrier layer deposition step 2008 is performed using an electroless deposition process to selectively deposit a layer that contains, for example, a cobalt-tungsten alloy (*e.g.*, CoW, CoWP, CoWB, CoWPB). An example of an electroless solution used to deposit a cobalt-tungsten alloy may contain a cobalt source, a tungsten source, a citrate source, a hypophosphite source, a borane reductant and other additives. Other electroless deposition solutions that may be used to deposit a cobalt-tungsten alloy are further described in the commonly assigned U.S. Patent Application Serial Number 10/967,919, entitled, "Selective Self-initiating Electroless Capping of Copper with Cobalt-containing Alloys," filed on October 18, 2004, which is incorporated by reference to the extent not inconsistent with the claimed aspects and description herein. Exemplary electroless deposition process cell may be the same process cells/chambers as described in the capping processes described herein.

[00199] The final step in the method steps 2001 is a CVD tungsten deposition process that is used to fill the contact level aperture 1510. The tungsten CVD deposition process used in step 2010 is generally performed using conventional tungsten hexafluoride (WF_6) precursor chemistries to fill the contact level aperture 1510. In this step a tungsten layer 1520 is directly deposited on the metal containing layer 1518. A selective tungsten CVD process can also be used.

Exemplary Pretreatment Process

[00200] Figure 13A illustrates a cross-sectional view of substrate 1500 having a via or aperture 1510 formed into dielectric layer 1504. Aperture 1510 may be formed in dielectric layer 1504 using conventional lithography and etching techniques to expose the silicon containing layer 1502, such as a source region, drain region or gate region of a MOS device. The silicon containing layer 1502 may be a silicon-containing material or a metal-containing material.

[00201] In some examples, silicon containing layer 1502 is a silicon-containing material that may also contain germanium, carbon, boron, phosphorous, arsenic or combinations thereof. For example, silicon containing layer 1502 may contain silicon, silicon carbide, silicon germanium, silicon germanium carbide, combinations thereof or doped variants thereof. In another embodiment, silicon containing layer 1502 contains a metal silicide or silicon dopant material (e.g., N-type or P-type dopants).

[00202] Substrate 1500 is exposed to a pretreatment process to form treated surface 1514 of silicon containing layer 1502, substantially free of oxide surface 1512 (not shown). In one example, silicon containing layer 1502 contains a silicon-containing material and treated surface 1514 contains a hydride-terminus surface, such as a silicon hydride layer.

[00203] In one embodiment, substrate 1500 is exposed to a wet clean process to remove oxide surface 1512 and to form treated surface 1514. In one example, oxide surface 1512 is removed by a HF-last solution to form treated surface 1514 as a substantially oxide-free, silicon hydride surface. In another example, oxide surface 1512 is removed during a liquid reduction process to form treated surface 1514 as a substantially oxide-free, metallic surface. In another example, oxide surface 1512 is exposed to a hydrogen plasma to form treated surface 1514 as a substantially oxide-free, silicon hydride surface.

[00204] During one embodiment of a pretreatment process, substrate 1500 is exposed to a wet-clean process for a predetermined time to remove oxide surface 1512 and form treated surface 1514. A wet clean process may include dispensing a wet clean solution across or sprayed on the surface of substrate 1500. The wet clean process may be an in situ process performed in the same processing cell as a

subsequent electroless deposition process. Alternatively, substrate 1500 may be wet cleaned in a separate processing cell from the subsequent electroless deposition processing cell. An example of an exemplary electroless deposition processing cell is further described in the US Patent Application Serial No. 10/996,342 [APPM 9032], filed 11/22/2004, and US Patent Application Serial No. 11/043,442 [APPM 8024.P1], filed 1/26/2005, which are all incorporated by reference herein in their entirety. In one example, the wet-clean process utilizes an HF-last solution containing water, HF and optional additives including chelators, surfactants, reductants, other acids or combinations thereof. The hydrogen fluoride concentration of a wet-clean solution may be within a range from about 10 ppm to about 5 wt%, preferably from about 50 ppm to about 2 wt%, and more preferably, from about 100 to about 1 wt%, for example, about 0.5 wt%.

[00205] A wet-clean pretreatment process may occur for about 10 minutes or less, such as within a range from about 15 seconds to about 5 minutes, preferably from about 30 seconds to about 4 minutes, and more preferably from about 1 minute to about 3 minutes. During the pretreatment process, the substrate is maintained at a temperature within a range from about 15 °C to about 50 °C, preferably about room temperature (*e.g.,* 20°C). The wet-clean process may be performed in a TEMPEST™ wet-clean system, available from Applied Materials, Inc., located in Santa Clara, California.

[00206] In another embodiment of a pretreatment process, substrate 1500 is exposed to a liquid reduction process containing a metal-reductant to form treated surface 1514. The metal-reductant may be a Ti^{3+} compound, such as titanium citrate. In an alternative embodiment of a pretreatment process, substrate 1500 is exposed to a plasma process for a predetermined time to reduce oxide surface 1512 and form treated surface 1514.

[00207] While foregoing is directed to the preferred embodiment of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims:

1. A method for depositing a material on a contact level feature formed on a substrate, comprising:

providing a substrate that has one or more contact level features that have an exposed silicide layer formed on a silicon containing region;

depositing a barrier layer over the surface of the exposed silicide layer, wherein the depositing the barrier layer comprises:

depositing a first metal layer on the exposed silicide layer; and

depositing a second metal layer over the first metal layer, wherein the second metal layer contains a metal selected from a group consisting of ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) and platinum (Pt); and

filling the contact level feature with a metal containing layer.

2. The method of claim 1, further comprising electrolessly depositing a third metal layer on the doped silicon containing region prior to providing the substrate, wherein the third metal layer is used to form at least a portion of the exposed silicide layer.

3. The method of claim 2, further comprising heating the substrate to a temperature that causes an element in the third metal layer to form at least a portion of the exposed silicide layer on the silicon containing region.

4. The method of claim 1, further comprising depositing a cobalt containing layer on the exposed silicide layer, wherein the exposed silicide layer comprises a nickel silicide.

5. The method of claim 4, wherein the thickness of the cobalt containing layer is between about 5 angstroms and about 50 angstroms.

6. The method of claim 2, wherein the third metal layer contains an element selected from a group consisting of titanium (Ti), cobalt (Co), nickel (Ni), tungsten (W), molybdenum (Mo), and tantalum (Ta).

7. The method of claim 1, wherein the thickness of the barrier layer deposited on the on the exposed silicide layer is between about 10 angstroms and about 100 angstroms.

8. The method of claim 2, wherein the thickness of the third metal layer deposited on the on the doped silicon containing region is between about 5 angstroms and about 50 angstroms.

9. The method of claim 1, wherein the barrier layer deposited on the exposed silicide layer has a resistivity less than about 10×10^{-6} ohm-cm.

10. The method of claim 1, wherein the metal containing layer is a copper containing layer.

11. The method of claim 10, wherein the copper containing layer comprises copper and aluminum, wherein the copper containing layer is deposited using an electroless solution that contains about 7 grams/liter of a copper ion source and between about 0.5 and about 6 grams/liter of an aluminum ion source.

12. The method of claim 10, wherein the metal containing layer further comprises copper and an element selected from a group consisting of aluminum (Al), indium (In), molybdenum (Mo), tungsten (W), manganese (Mn), cobalt (Co), palladium (Pd), nickel (Ni), tin (Sn), and ruthenium (Ru).

13. The method of claim 1, wherein the first metal layer contains an element selected from a group consisting of titanium (Ti), cobalt (Co), nickel (Ni), tungsten (W), molybdenum (Mo), nitrogen (N), and tantalum (Ta).

14. The method of claim 1, wherein the second metal layer comprises ruthenium and tantalum.

15. The method of claim 14, wherein the second metal layer comprises between about 70% and about 95% ruthenium and the balance tantalum.

16. The method of claim 1, further comprising depositing a third metal layer on the first metal layer prior to depositing the second metal layer.

17. The method of claim 16, wherein the first metal layer is a titanium containing layer, the third metal layer is a titanium nitride containing layer and the second metal layer is a ruthenium containing layer.

18. The method of claim 1, wherein the metal containing layer is a copper containing layer that is deposited by an electrochemical deposition process.

19. A method for depositing a material on a contact level feature formed on a substrate, comprising:

providing a substrate that has one or more contact level features that have an exposed silicide layer formed on a doped silicon containing region;

depositing a barrier layer over the surface of the exposed silicide layer, wherein the depositing the barrier layer comprises:

depositing a first metal layer on the exposed silicide layer; and

depositing a second metal layer over the first metal layer, wherein the second metal layer contains a metal selected from a group consisting of ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) and platinum (Pt);

electrolessly depositing a first copper containing layer on the barrier layer; and

depositing a second copper containing layer on the first copper containing layer to fill the one or more contact level features.

20. The method of claim 19, wherein the second copper containing layer is generally pure copper layer deposited using an electrochemical deposition process.

21. The method of claim 19, wherein the first copper containing layer comprises copper and an element selected from a group consisting of aluminum (Al), indium (In), molybdenum (Mo), tungsten (W), manganese (Mn), cobalt (Co), palladium (Pd), nickel (Ni), tin (Sn), and ruthenium (Ru).

22. The method of claim 19, further comprising depositing a third metal layer on the first metal layer prior to depositing the second metal layer.

23. The method of claim 22, wherein the first metal layer is a titanium containing layer, the third metal layer is a titanium nitride containing layer and the second metal layer is a ruthenium containing layer.

24. The method of claim 19, wherein the second copper containing layer is deposited by an electrochemical deposition process.

25. A method for depositing a material on a contact level feature formed on a substrate, comprising:

depositing a barrier layer over the surfaces of one or more contact level features formed on the substrate; and

electrolessly depositing a copper containing layer on the barrier layer using a metal layer electroless deposition solution, wherein the metal layer electroless deposition solution comprises EDTA and copper ions at a concentration ratio of less than about 6:1.

26. A method for depositing a material on a contact level feature formed on a substrate, comprising:

electrolessly depositing a first metal containing layer on a doped silicon region on a surface of a substrate;

forming a contact level interconnect feature, wherein the process of forming the contact level interconnect comprises:

depositing a dielectric layer over a surface of the substrate and the first metal containing layer; and

forming one or more contact level features in the dielectric layer using conventional semiconductor processing methods, wherein the first metal containing layer is exposed at the bottom of one or more of the contact level features;

depositing a barrier layer over the surface of the first metal layer, wherein the depositing the barrier layer comprises:

depositing a second metal layer over the first metal layer, wherein the second metal layer contains a metal selected from a group consisting of ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) and platinum (Pt); and

electrolessly depositing a copper containing layer on the barrier layer.

27. The method of claim 26, wherein the first metal containing layer comprises an element selected from a group consisting of cobalt (Co) and nickel (Ni).

28. The method of claim 26, further comprising depositing a cobalt containing layer on the first metal containing layer, wherein the first metal containing layer comprises a nickel containing alloy.

29. The method of claim 28, further comprising heating the substrate to a temperature that causes the nickel containing layer to form a nickel silicide.

30. The method of claim 26, further comprising depositing a third metal layer on the first metal layer before depositing the second metal over the first metal layer.

31. The method of claim 30, wherein the third metal layer contains a metal selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), ruthenium (Ru), cobalt (Co), and nickel (Ni).

32. A method for depositing a material on a contact level feature formed on a substrate, comprising:

providing a substrate that has one or more contact level features that have an exposed doped silicon containing region;

depositing a first metal layer on the doped silicon containing region;

depositing a barrier layer over the surface of the first metal layer, wherein the depositing the barrier layer comprises:

depositing a second layer over the first layer, wherein the second layer comprises ruthenium and tantalum; and

filling the contact level feature with a metal containing layer.

33. The method of claim 32, wherein the barrier layer further comprises depositing a third layer on the first metal layer prior to depositing the second layer.

34. The method of claim 33, wherein the third layer contains a metal selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) and platinum (Pt).

35. The method of claim 32, wherein the metal containing layer comprises copper.

36. A method of forming an interconnect on a silicon substrate, comprising:

providing a substrate containing an exposed tungsten-containing contact plug exposed that has an exposed gap formed therein;

exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten-containing contact plug;

filling the exposed gap with a fill material.

37. The method of claim 36, wherein the pretreatment process comprises exposing the substrate to a wet-clean solution having a pH value of less than about 5.

38. The method of claim 37, wherein the wet-clean solution has a hydrogen fluoride concentration within a range from about 0.1 wt% to about 2 wt%.

39. The method of claim 37, wherein the wet-clean solution further comprises a complexing agent that is selected from the group consisting of citric acid, EDTA, EDA, carboxylic acids, amines, salts thereof, derivatives thereof and combinations thereof.

40. The method of claim 36, wherein the step of filling the exposed gap is completed using an electroless deposition process, wherein the fill material is selected from the group consisting of cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

41. The method of claim 36, wherein the fill material is selected from the group consisting of copper, cobalt, nickel and tungsten.

42. The method of claim 36, wherein the fill material is a dielectric material.

43. The method of claim 36, further comprising removing a portion of the exposed tungsten-containing contact plug to increase the size of the exposed gap.

44. The method of claim 43, wherein the step of removing a portion of the exposed tungsten-containing contact plug is performed using a wet-clean solution having a pH value of less than about 5.

45. A method of forming an interconnect on a silicon substrate, comprising:

providing a silicon substrate having a first dielectric layer which is disposed on a surface of the silicon substrate and a first aperture formed in the first dielectric layer, wherein a doped silicon containing region of the silicon substrate is exposed at the bottom of the first aperture;

filling the first aperture formed in the first dielectric layer with a tungsten containing layer, wherein the tungsten containing layer is in electrical communication with the doped silicon containing region;

removing an amount of the tungsten containing layer disposed on the first dielectric layer, wherein a gap formed in the tungsten containing layer during the step of filling the first aperture is exposed; and

depositing a material on the surface of the silicon substrate to substantially cover the gap formed in the tungsten containing layer.

46. The method of claim 45, further comprising exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten containing layer.

47. The method of claim 45, wherein the pretreatment process further comprises exposing the substrate to a wet-clean solution having a pH value of less than about 5.

48. The method of claim 47, wherein wet-clean solution further comprises a complexing agent that is selected from the group consisting of citric acid, EDTA, EDA, carboxylic acids, amines, salts thereof, derivatives thereof and combinations thereof.

49. The method of claim 45, wherein the material is selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

50. The method of claim 45, further comprising;

forming a second dielectric layer over the first dielectric layer and the tungsten containing layer disposed in the first aperture; and

forming a second aperture in the second dielectric layer that is in communication with the tungsten containing layer disposed in the first aperture, wherein the step of forming the second aperture is formed before the step of depositing a material on the surface of the silicon containing substrate is performed.

51. A method of forming an interconnect on a silicon substrate, comprising:

providing a substrate containing first dielectric layer that contains at least one tungsten-containing contact plug that has an exposed surface;

forming a second dielectric layer over the first dielectric layer and the tungsten-containing contact plug;

forming a second aperture in the second dielectric layer that is in communication with the exposed surface of the tungsten-containing contact plug; and

selectively filling the second aperture with a fill material.

52. The method of claim 51, further comprising depositing a first metal layer over the exposed surface of the tungsten-containing contact plug and the second aperture before selectively filling the second aperture.

53. The method of claim 51, wherein the tungsten-containing contact plug has an exposed gap that comprises a portion of the exposed surface of the tungsten-containing contact plug, wherein the second aperture is in communication with the exposed surface and the exposed gap.

54. The method of claim 51, further comprising exposing the substrate to a pretreatment process, wherein the pretreatment process is performed after forming the second aperture and is adapted to remove an oxide layer from the exposed surface of the tungsten-containing contact plug.

55. The method of claim 52, further comprising removing the second dielectric layer from the surface of the tungsten-containing contact plug before depositing the first metal layer.

56. The method of claim 51, further comprising exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten-containing contact plug before selectively filling the second aperture with the fill material.

57. The method of claim 51, wherein the pretreatment process further comprises exposing the substrate to a wet-clean solution having a pH value of less than about 5.

58. The method of claim 57, wherein wet-clean solution further comprises a complexing agent that is selected from the group consisting of citric acid, EDTA, EDA, carboxylic acids, amines, salts thereof, derivatives thereof and combinations thereof.

59. The method of claim 52, wherein the first metal layer is contains a metal selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

60. The method of claim 51, wherein the fill material is selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP),

nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

61. The method of claim 51, wherein the fill material is electrolessly deposited on the exposed surface of the tungsten-containing contact plug and is in contact with the second dielectric layer.

62. The method of claim 61, wherein the fill material contains a metal selected from the group consisting of cobalt and nickel.

63. The method of claim 53, further comprising filing the exposed gap with a second layer that contains a metal selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

64. A method for depositing a material on a substrate, comprising:

providing a silicon containing substrate that has one or more contact level features that have an exposed doped silicon containing region;

pretreating the exposed doped silicon containing region, wherein the pretreating process is adapted to remove an oxide layer from the exposed doped silicon containing region;

depositing a metal containing layer over a surface of the exposed doped silicon containing regions; and

depositing a tungsten layer over the metal containing layer at a temperature between about 300 °C and about 450 °C, wherein during the tungsten layer deposition process a metal silicide is formed.

65. The method of claim 64, wherein the metal containing layer contains an element selected from a group consisting of cobalt and nickel.

66. The method of claim 64, wherein the tungsten layer is deposited using a tungsten hexafluoride (WF_6) containing gas.

67. The method of claim 64, further comprises depositing a cobalt containing layer on the nickel containing layer prior to depositing the tungsten layer.

68. The method of claim 64, wherein the process of depositing a metal containing layer comprises electrolessly depositing a nickel-containing layer having a thickness between about 10 angstroms and about 100 angstroms.

69. A method for depositing a material on a substrate, comprising:

providing a silicon containing substrate that has one or more contact level features that have an exposed doped silicon containing region;

pretreating the exposed doped silicon containing region, wherein the pretreating process is adapted to remove an oxide layer from the exposed doped silicon containing region;

depositing a nickel containing layer over the bottom surface of the one or more contact level features;

forming a nickel silicide layer by exposing the deposited nickel containing layer and silicon containing substrate to temperatures greater the 250 °C;

depositing a cobalt containing layer over the nickel silicide layer; and

depositing a tungsten layer on the cobalt containing layer.

70. The method of claim 69, wherein the tungsten layer is deposited using a tungsten hexafluoride (WF_6) containing gas.

71. The method of claim 69, wherein the cobalt containing layer is a cobalt-tungsten alloy.

72. The method of claim 69, wherein the process of depositing a nickel containing layer comprises electrolessly depositing a nickel-containing layer having a thickness between about 10 angstroms and about 100 angstroms.

73. A method for depositing a material on a substrate, comprising:

providing a substrate that has one or more contact level features that have an exposed doped silicon containing region;

selectively depositing a metal containing layer over a surface of the exposed doped silicon containing regions; and

depositing a tungsten layer on the metal layer at a temperature between about 300 °C and about 450 °C, wherein during the process of depositing tungsten layer a metal silicide is formed at the surface of the exposed doped silicon containing region.

74. The method of claim 73, wherein the metal containing layer contains an element selected from a group consisting of cobalt and nickel.

75. The method of claim 73, wherein the tungsten layer is deposited using a tungsten hexafluoride (WF_6) containing gas.

76. The method of claim 73, wherein the process of selectively depositing a metal containing layer comprises electrolessly depositing a nickel-containing layer having a thickness between about 10 angstroms and about 100 angstroms.

77. A method of forming an interconnect on a silicon substrate, comprising:

providing a substrate having an aperture formed in a dielectric layer disposed on a surface of the substrate, wherein the aperture is in communication with an exposed surface of a tungsten-containing contact plug;

dispensing a clean solution on an the exposed surface of the tungsten-containing contact plug, wherein the clean solution comprises hydrogen fluoride;

disposing a preparation solution on the exposed surface of the tungsten-containing contact plug, wherein the preparation solution comprises a tungstate source;

depositing a initiation layer on the exposed surface of the tungsten-containing contact plug using an activation solution; and

selectively filling the second aperture with a fill material.

78. The method of claim 77, wherein the clean solution is an aqueous solution that has a hydrofluoric acid concentration in a range from about 0.1 wt% to about 0.5 wt%.

79. The method of claim 77, wherein the preparation solution is an aqueous solution that comprises a tungstate source that is selected from the group consisting of ammonium tungsten oxide, tungstic acid, water soluble WO_4^{2-} sources, derivatives thereof and combinations thereof.

80. The method of claim 77, wherein the preparation solution is an aqueous solution that has a tungstic acid concentration in a range from about 2 mM to about 100 mM.

81. The method of claim 77, further comprising dispensing a chelating solution on the exposed surface of the substrate, wherein the chelating solution comprises citric acid that is in a concentration between about 50 mM and about 300 mM.

82. The method of claim 77, wherein the initiation layer is deposited using an activation solution that contains a palladium source.

83. The method of claim 77, wherein the fill material contains a metal selected from the group consisting of cobalt and nickel.

84. The method of claim 77, wherein the fill material contains a metal selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP),

nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

85. The method of claim 77, further comprising activating the initiation layer using a rinse activation solution before selectively filling the second aperture with a fill material.

86. The method of claim 85, wherein rinse activation solution has a borane reductant concentration in a range from about 1 mM to about 200 mM.

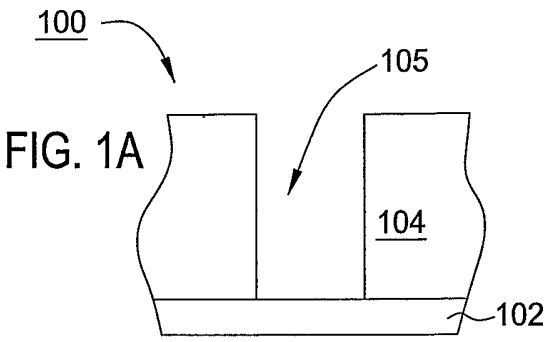


FIG. 1A

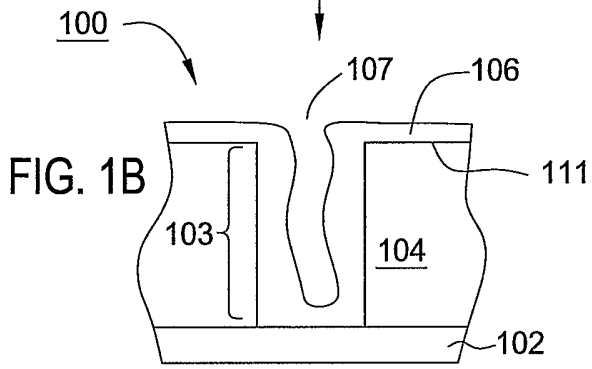


FIG. 1B

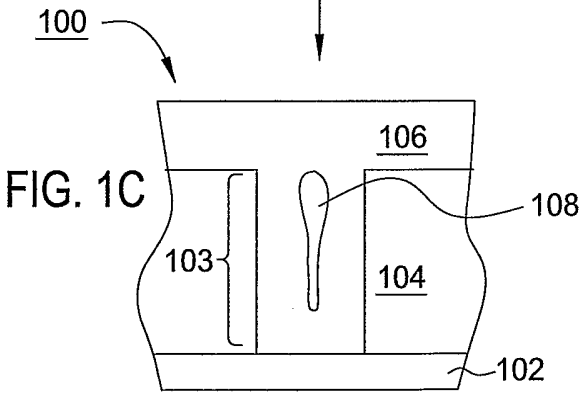


FIG. 1C

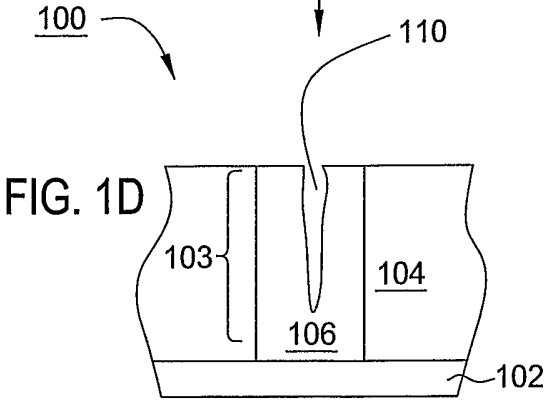


FIG. 1D

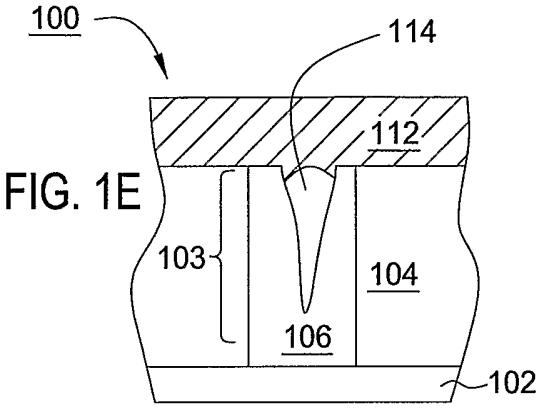


FIG. 1E

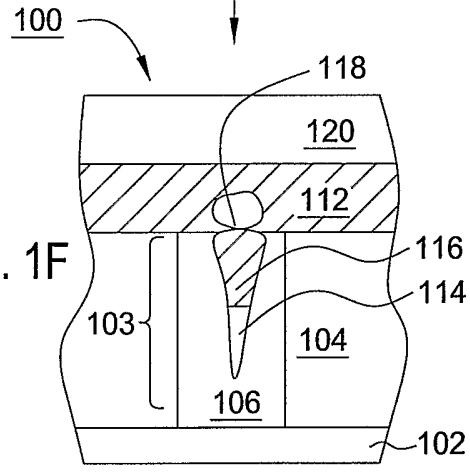


FIG. 1F

(PRIOR ART)

FIG. 2A

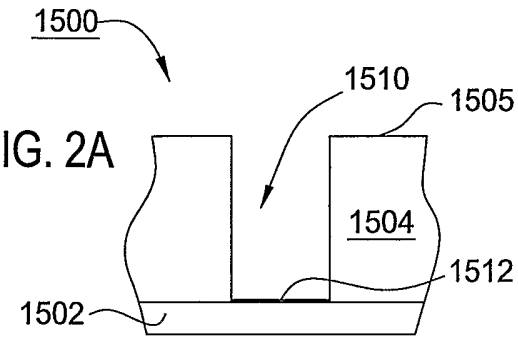


FIG. 2B

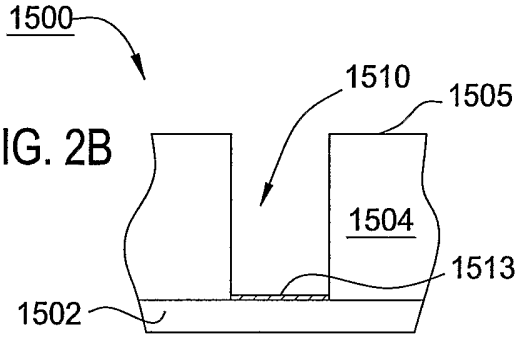


FIG. 2C

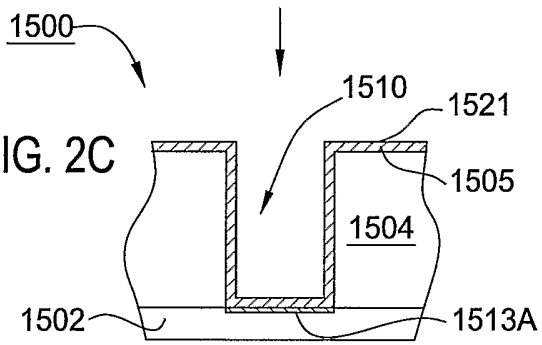


FIG. 2D

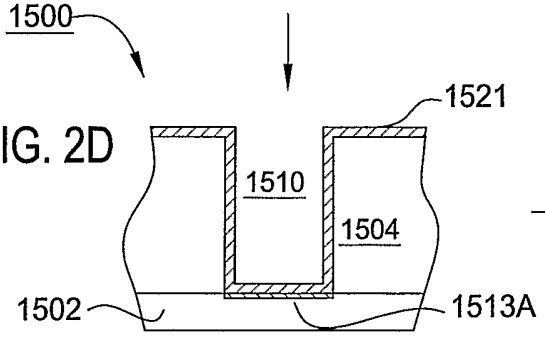


FIG. 2E

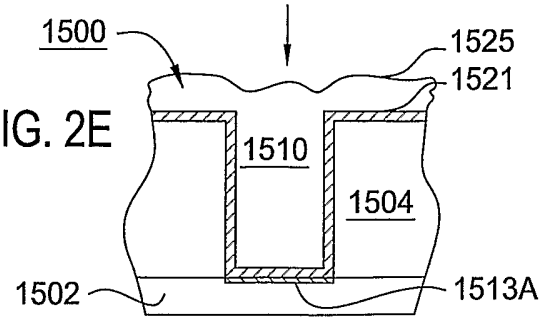


FIG. 2F

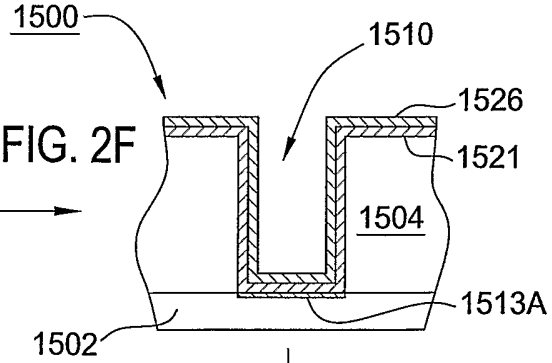
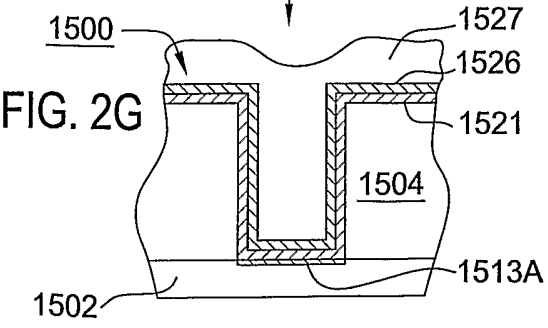


FIG. 2G



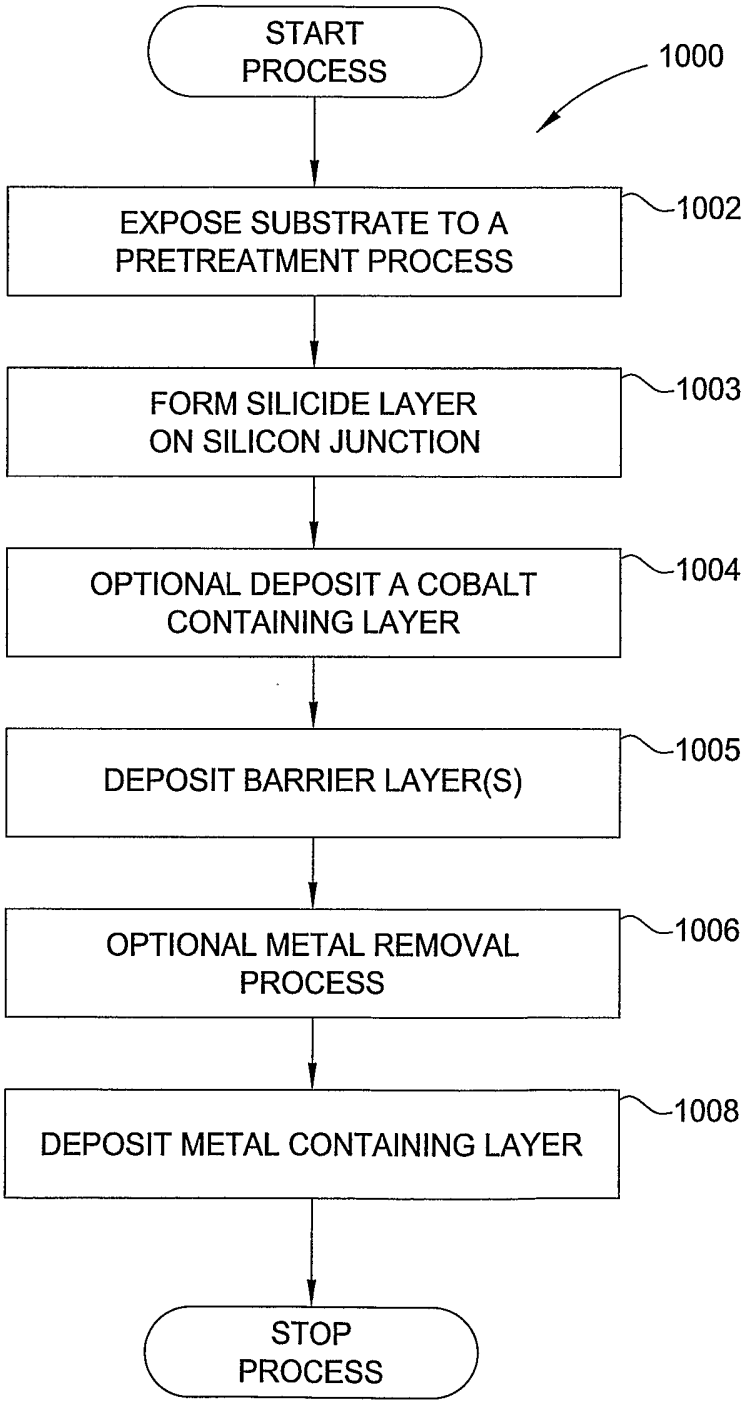

START PROCESS
1000
EXPOSE SUBSTRATE TO A PRETREATMENT PROCESS
1002
FORM SILICIDE LAYER ON SILICON JUNCTION
1003
OPTIONAL DEPOSIT A COBALT CONTAINING LAYER
1004
DEPOSIT BARRIER LAYER(S)
1005
OPTIONAL METAL REMOVAL PROCESS
1006
DEPOSIT METAL CONTAINING LAYER
1008
STOP PROCESS

FIG. 3

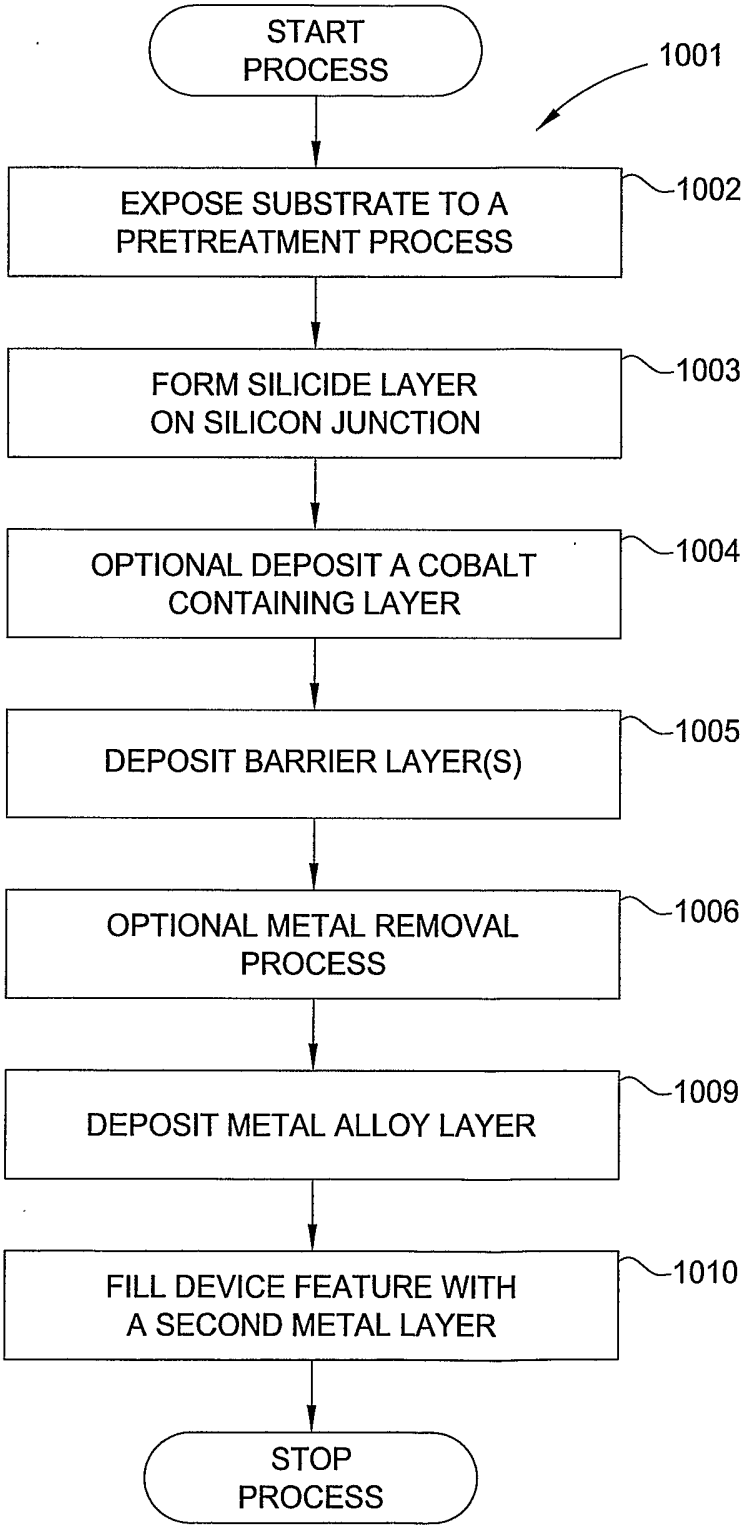

START PROCESS
1001
EXPOSE SUBSTRATE TO A PRETREATMENT PROCESS
1002
FORM SILICIDE LAYER ON SILICON JUNCTION
1003
OPTIONAL DEPOSIT A COBALT CONTAINING LAYER
1004
DEPOSIT BARRIER LAYER(S)
1005
OPTIONAL METAL REMOVAL PROCESS
1006
DEPOSIT METAL ALLOY LAYER
1009
FILL DEVICE FEATURE WITH A SECOND METAL LAYER
1010
STOP PROCESS

FIG. 4

FIG. 5A

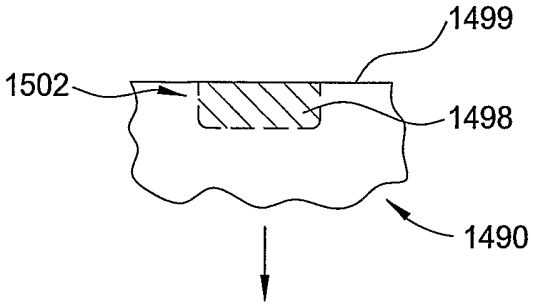


FIG. 5B

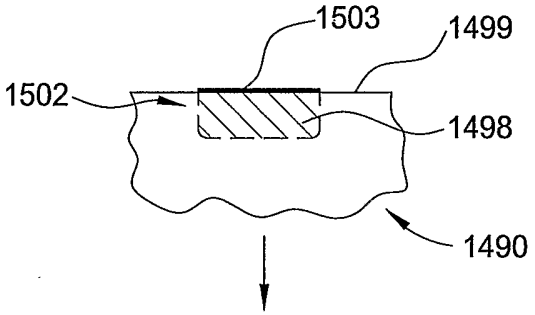


FIG. 5C

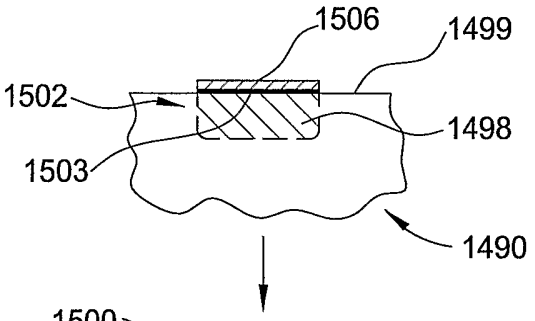
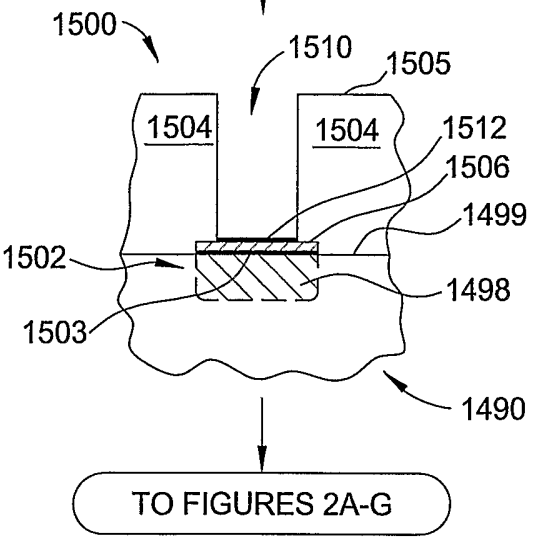


FIG. 5D



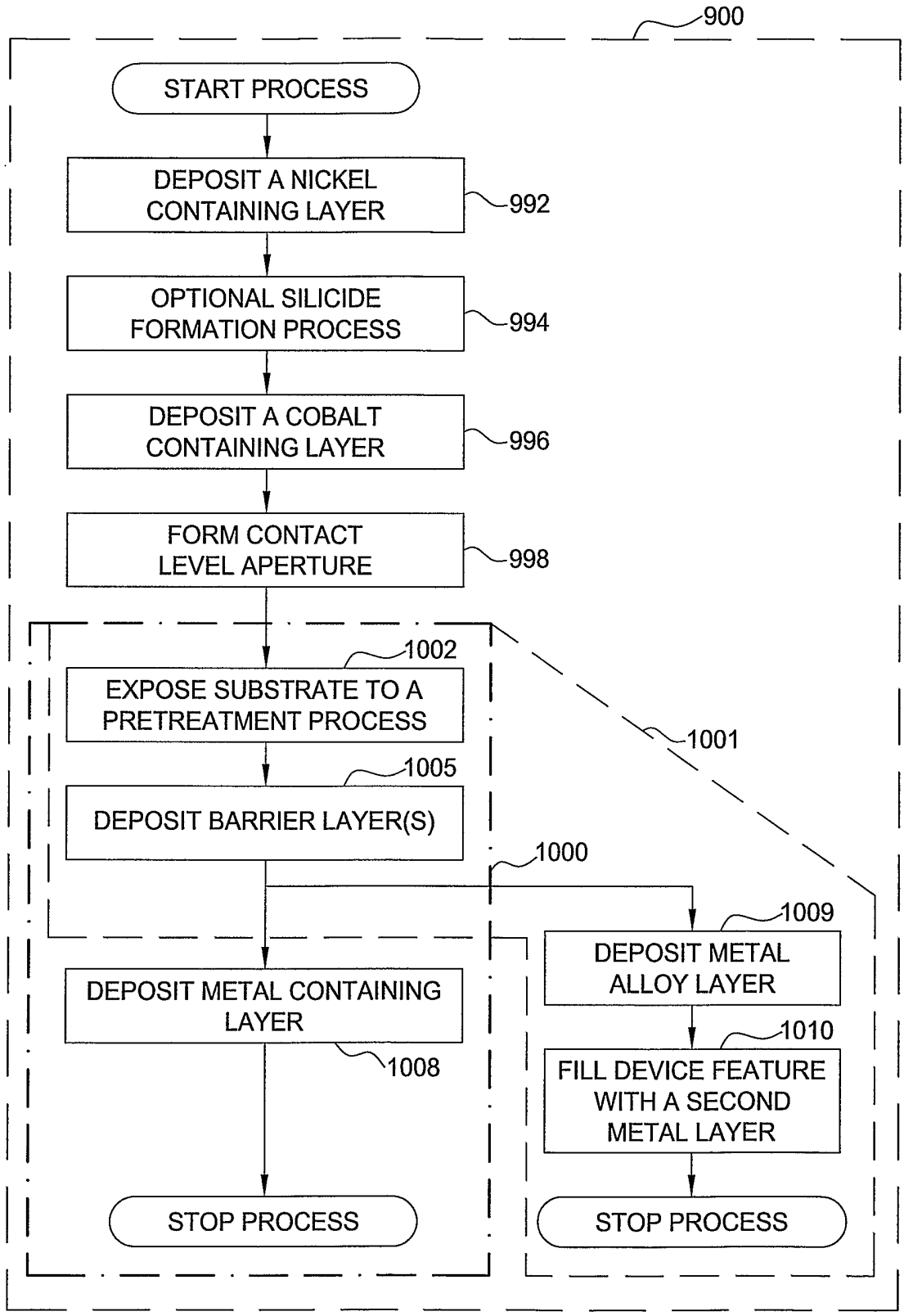

900
START PROCESS
DEPOSIT A NICKEL CONTAINING LAYER
992
OPTIONAL SILICIDE FORMATION PROCESS
994
DEPOSIT A COBALT CONTAINING LAYER
996
FORM CONTACT LEVEL APERTURE
998
1002
EXPOSE SUBSTRATE TO A PRETREATMENT PROCESS
1001
1005
DEPOSIT BARRIER LAYER(S)
1000
1009
DEPOSIT METAL ALLOY LAYER
DEPOSIT METAL CONTAINING LAYER
1010
FILL DEVICE FEATURE WITH A SECOND METAL LAYER
1008
STOP PROCESS
STOP PROCESS

FIG. 6

FIG. 7A

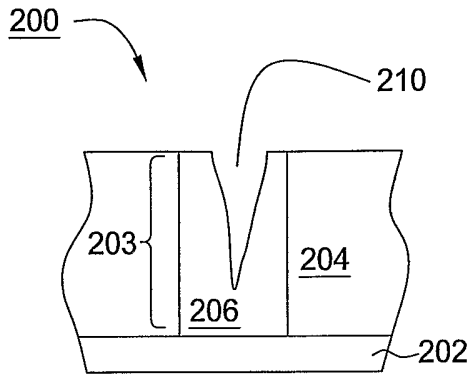


FIG. 7B

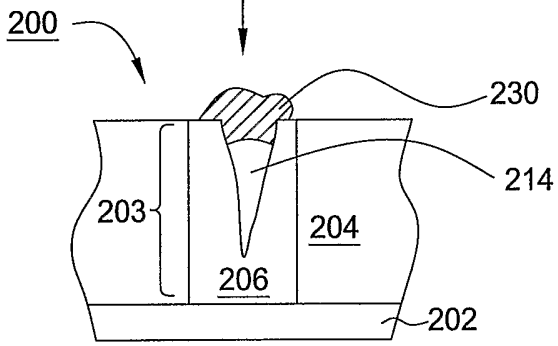
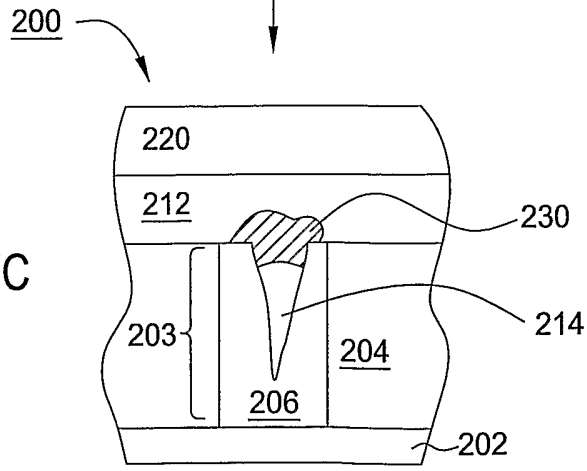


FIG. 7C



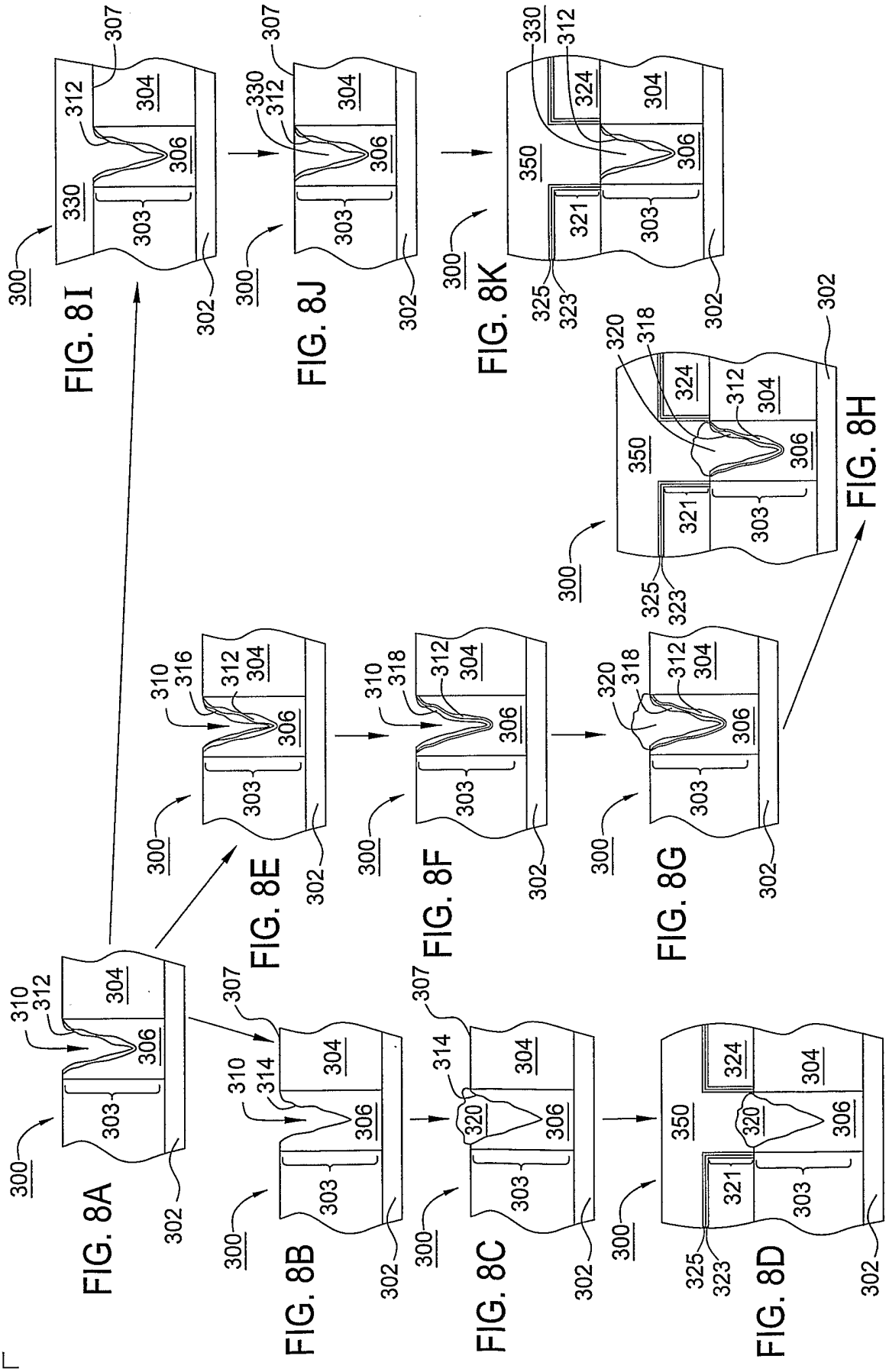


FIG. 8A
FIG. 8B
FIG. 8C
FIG. 8D
FIG. 8E
FIG. 8F
FIG. 8G
FIG. 8H
FIG. 8I
FIG. 8J
FIG. 8K
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FIG. 9A

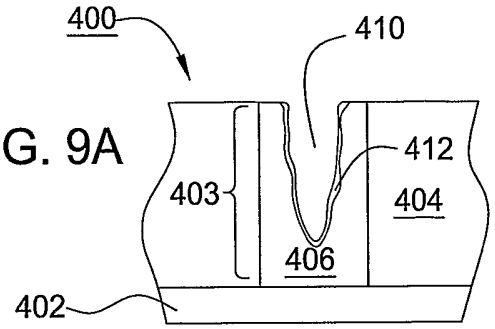


FIG. 9B

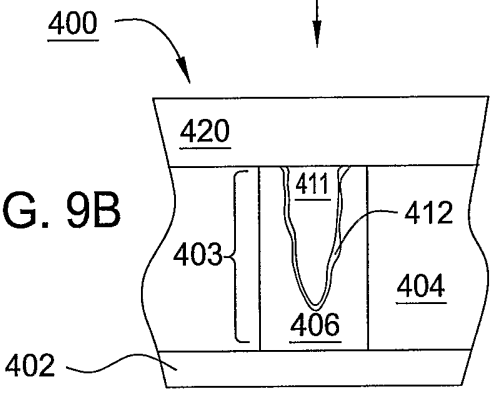


FIG. 9C

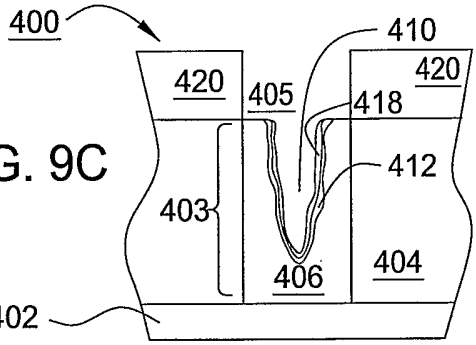


FIG. 9D

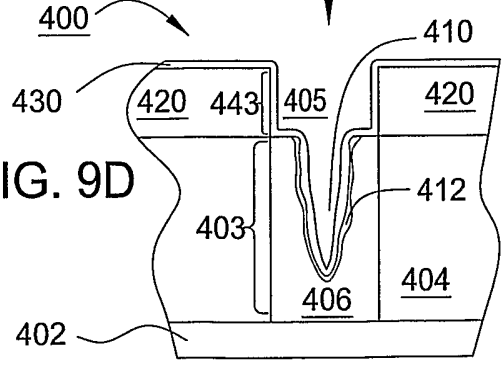


FIG. 9E

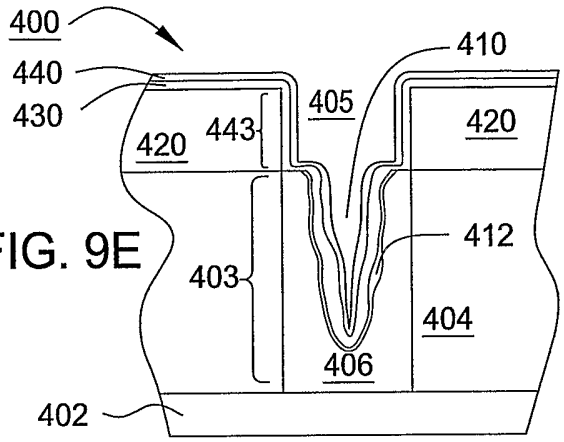
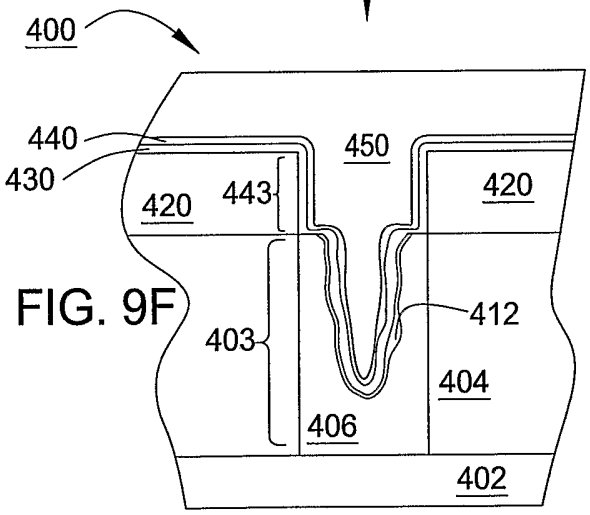


FIG. 9F



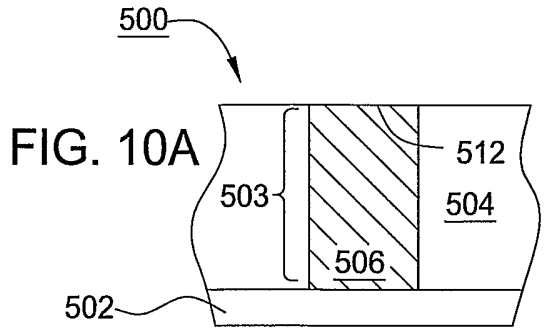


FIG. 10A

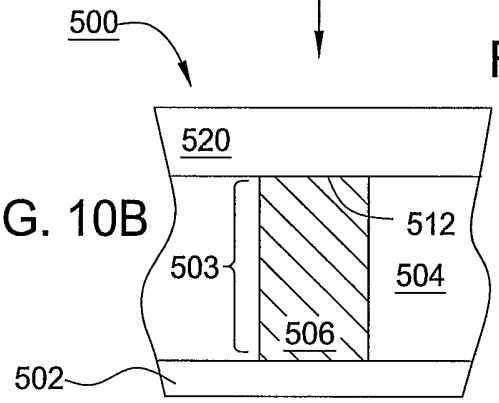


FIG. 10B

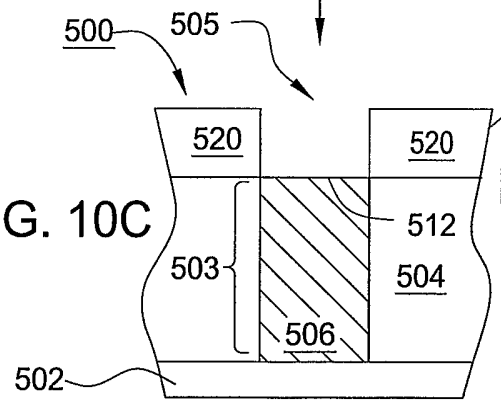


FIG. 10C

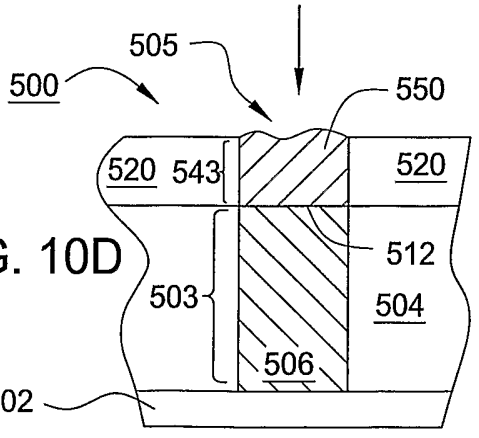


FIG. 10D

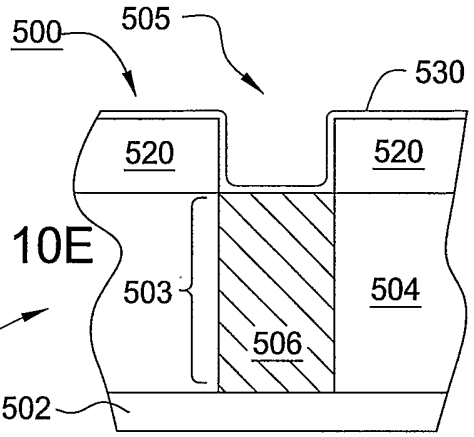


FIG. 10E

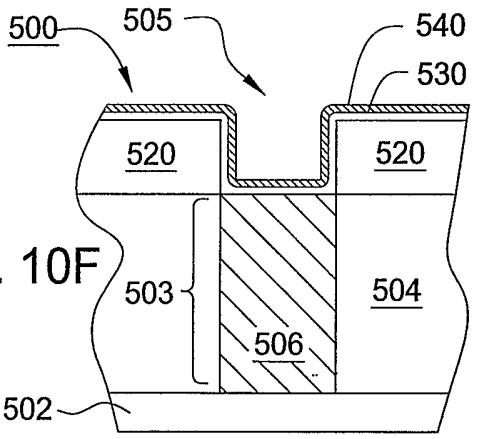


FIG. 10F

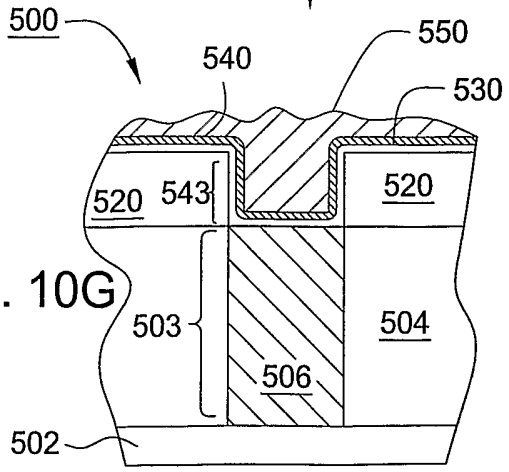


FIG. 10G

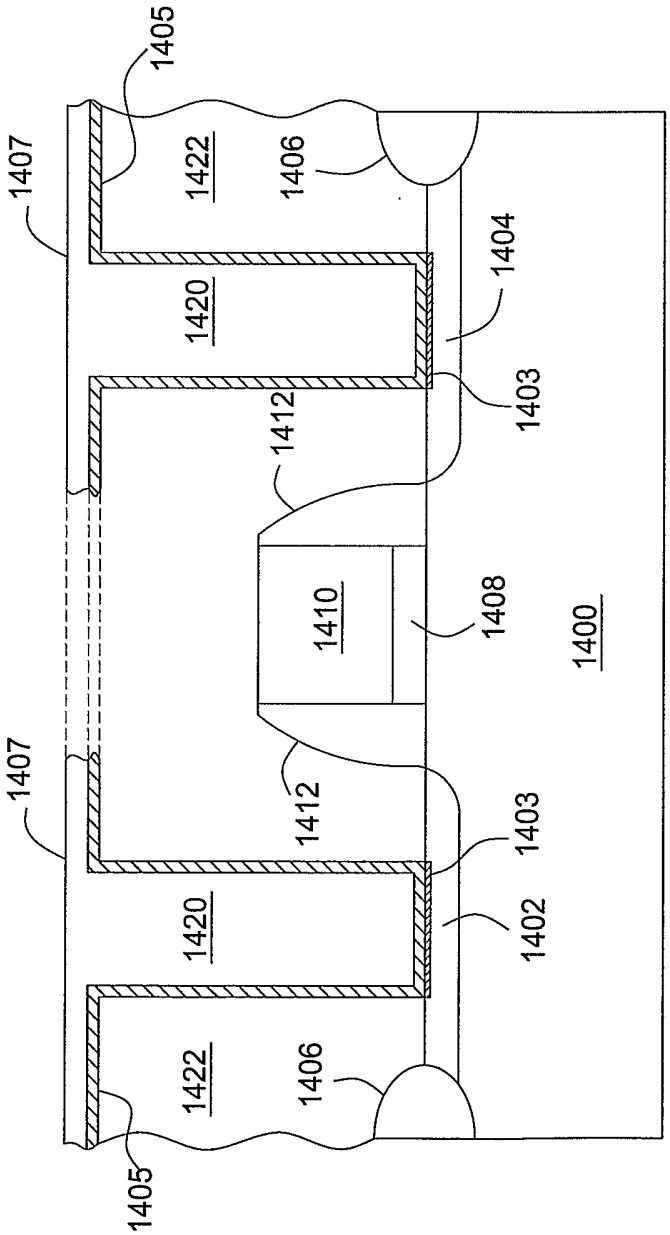

1405
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FIG. 11

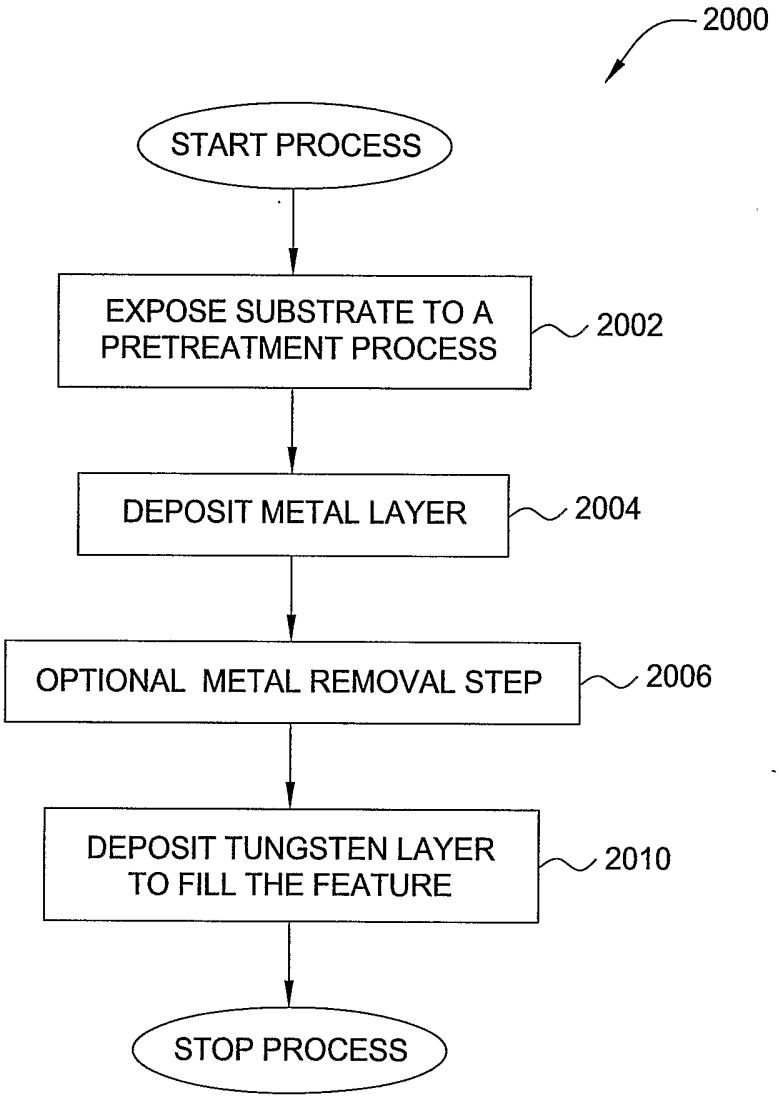
2000
START PROCESS
EXPOSE SUBSTRATE TO A PRETREATMENT PROCESS
2002
DEPOSIT METAL LAYER
2004
OPTIONAL METAL REMOVAL STEP
2006
DEPOSIT TUNGSTEN LAYER TO FILL THE FEATURE
2010
STOP PROCESS

FIG. 12

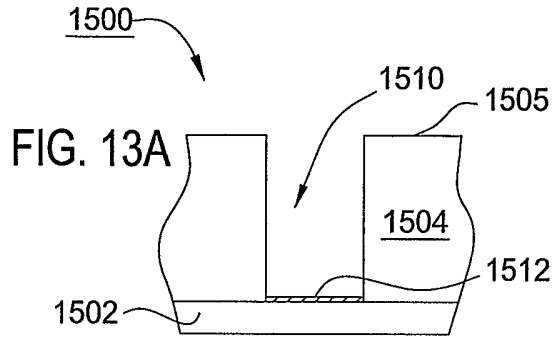

FIG. 13A

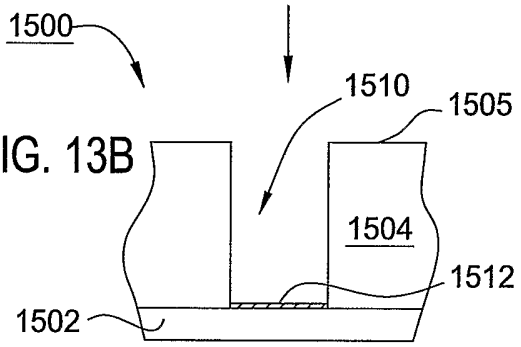

FIG. 13B

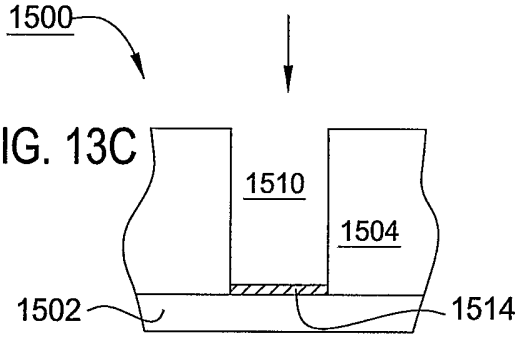

FIG. 13C

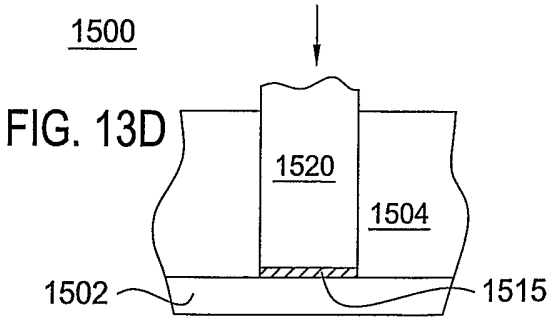

FIG. 13D

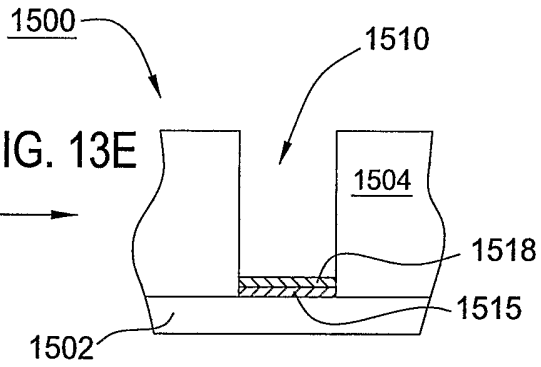

FIG. 13E

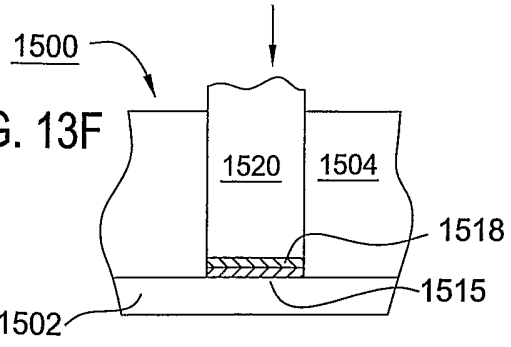

FIG. 13F

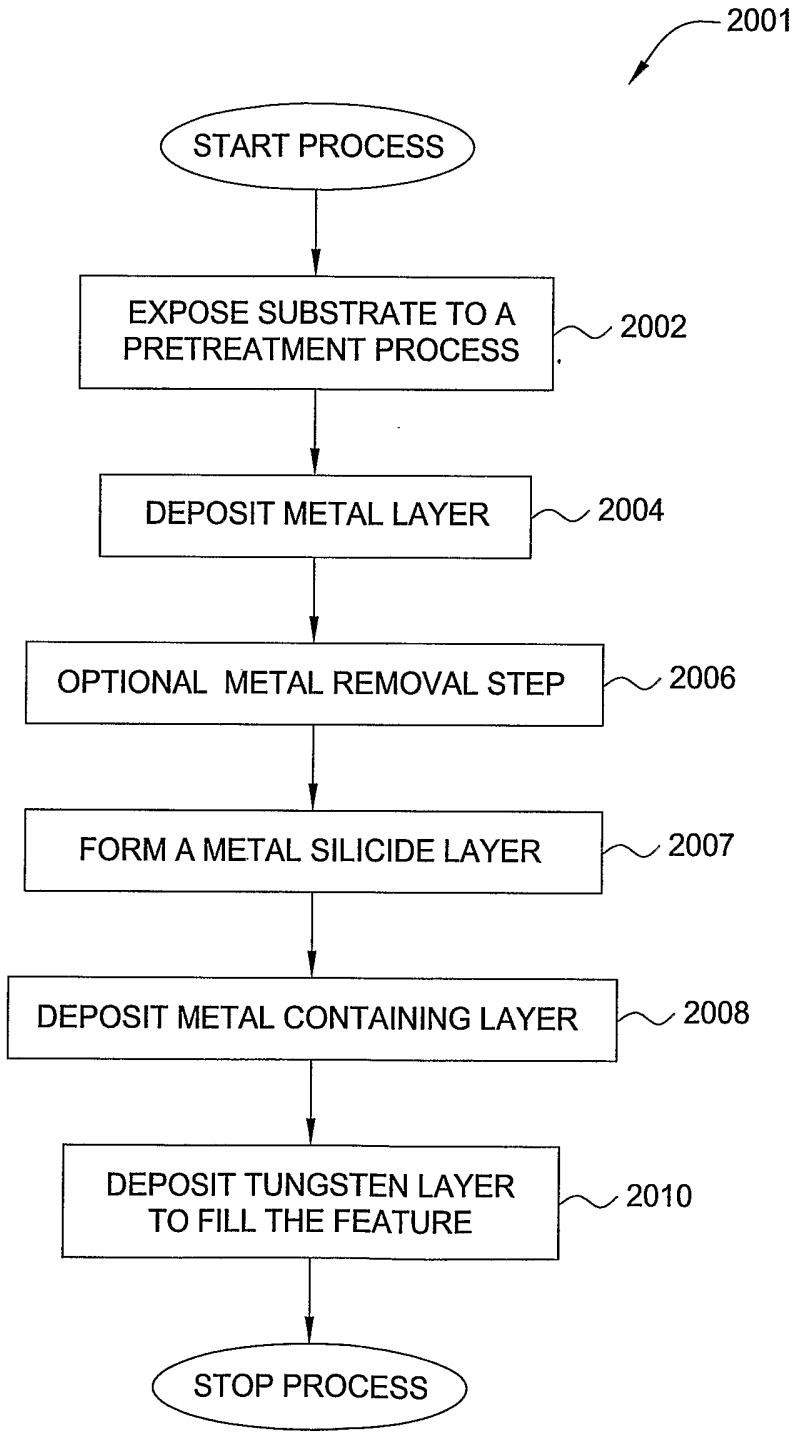
2001
START PROCESS
EXPOSE SUBSTRATE TO A PRETREATMENT PROCESS
2002
DEPOSIT METAL LAYER
2004
OPTIONAL METAL REMOVAL STEP
2006
FORM A METAL SILICIDE LAYER
2007
DEPOSIT METAL CONTAINING LAYER
2008
DEPOSIT TUNGSTEN LAYER TO FILL THE FEATURE
2010
STOP PROCESS

FIG. 14

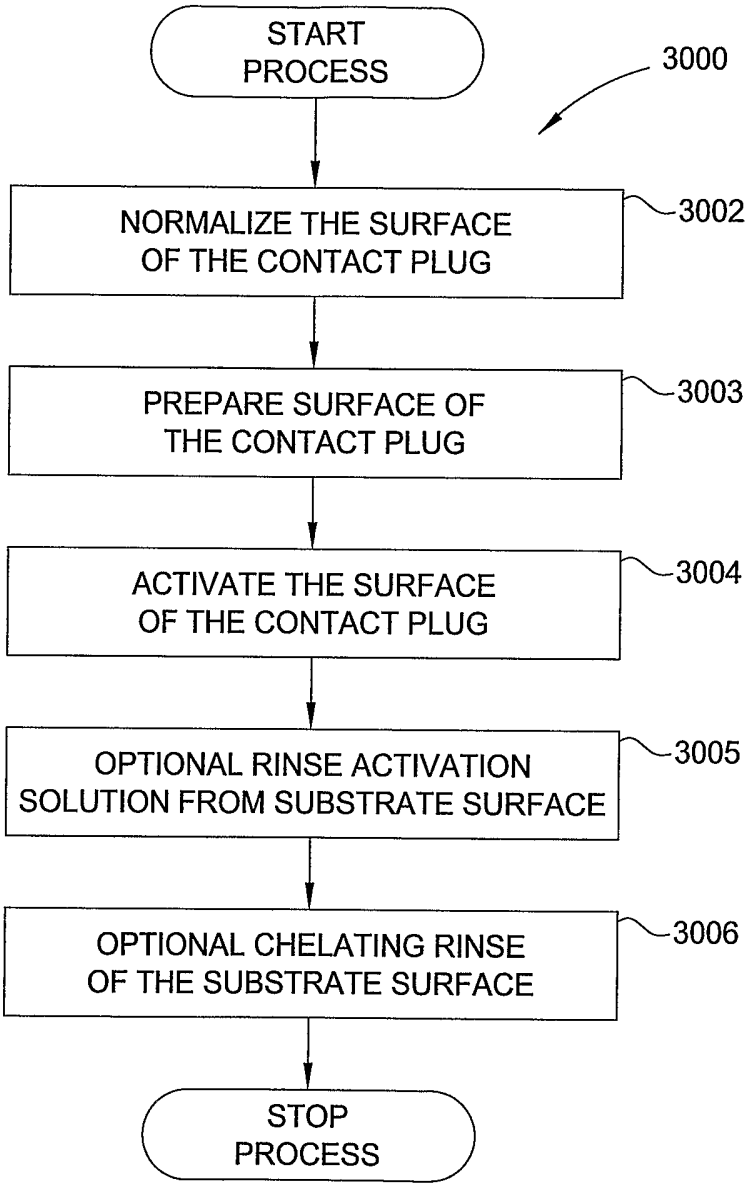
START PROCESS
3000
NORMALIZE THE SURFACE OF THE CONTACT PLUG
3002
PREPARE SURFACE OF THE CONTACT PLUG
3003
ACTIVATE THE SURFACE OF THE CONTACT PLUG
3004
OPTIONAL RINSE ACTIVATION SOLUTION FROM SUBSTRATE SURFACE
3005
OPTIONAL CHELATING RINSE OF THE SUBSTRATE SURFACE
3006
STOP PROCESS

FIG. 15