United States Defensive Publication [19] (H) [11] T954,006

Lee et al. [43] Jan. 4, 1977

[54] **ON-CHIP SUBSTRATE VOLTAGE GENERATOR**

[75] Inventors: **James M. Lee**, Wappingers Falls; **George Sonoda**, Poughkeepsie, both of N.Y.

[73] Assignee: **International Business Machines**, Armonk, N.Y.

[21] Appl. No.: **672,898**

[22] Filed: **Apr. 2, 1976**

Related U.S. Application Data

[63] Continuation of Ser. No. 567,213, April 11, 1975, abandoned, which is a continuation of Ser. No. 375,271, June 29, 1973, abandoned.

[51] **Int. Cl.**[2] **H03K 3/353**

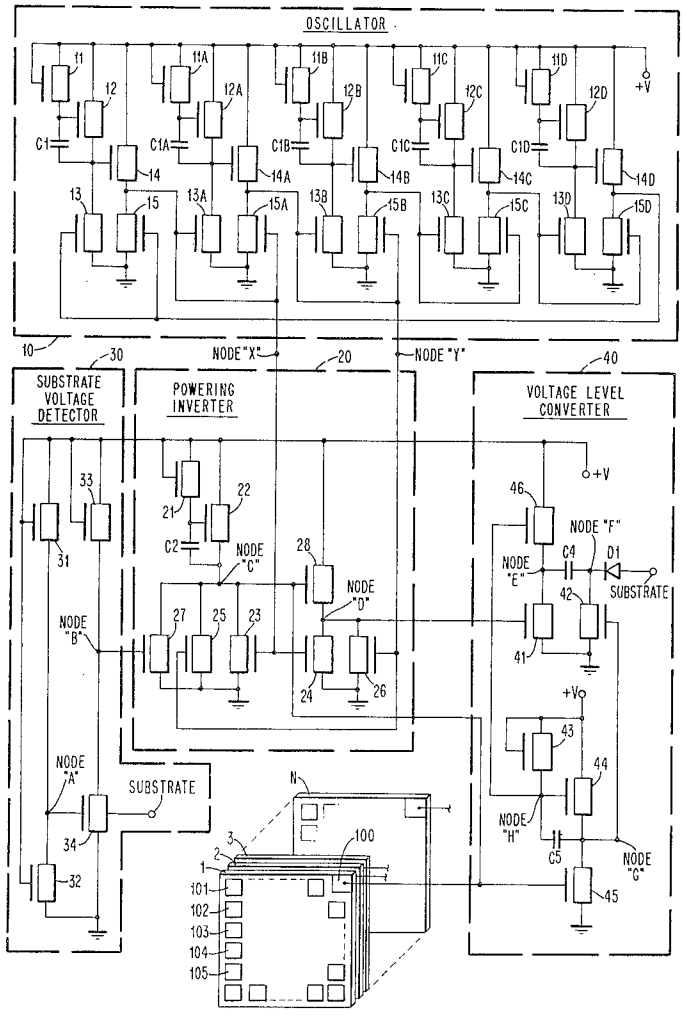
[52] **U.S. Cl.** **307/304**; 357/41; 331/57

[57] **ABSTRACT**

Disclosed is an apparatus for generating and controlling a desired substrate potential level or a semiconductor chip. A pulse source, such as an oscillator, provides a pulse train which, in combination with a control signal from the substrate voltage detector, selectively discharges a capacitor in a voltage level converter for obtaining a desired level of substrate potential. A feedback path through the substrate regulates the conductivity of a reference transistor in the substrate voltage detector providing the required control signal.

1 Claim, 3 Sheets Drawing, 17 Pages Specification

The file of this unexamined application may be inspected and copies thereof may be purchased (849 O.G. 1221, Apr. 9, 1968).



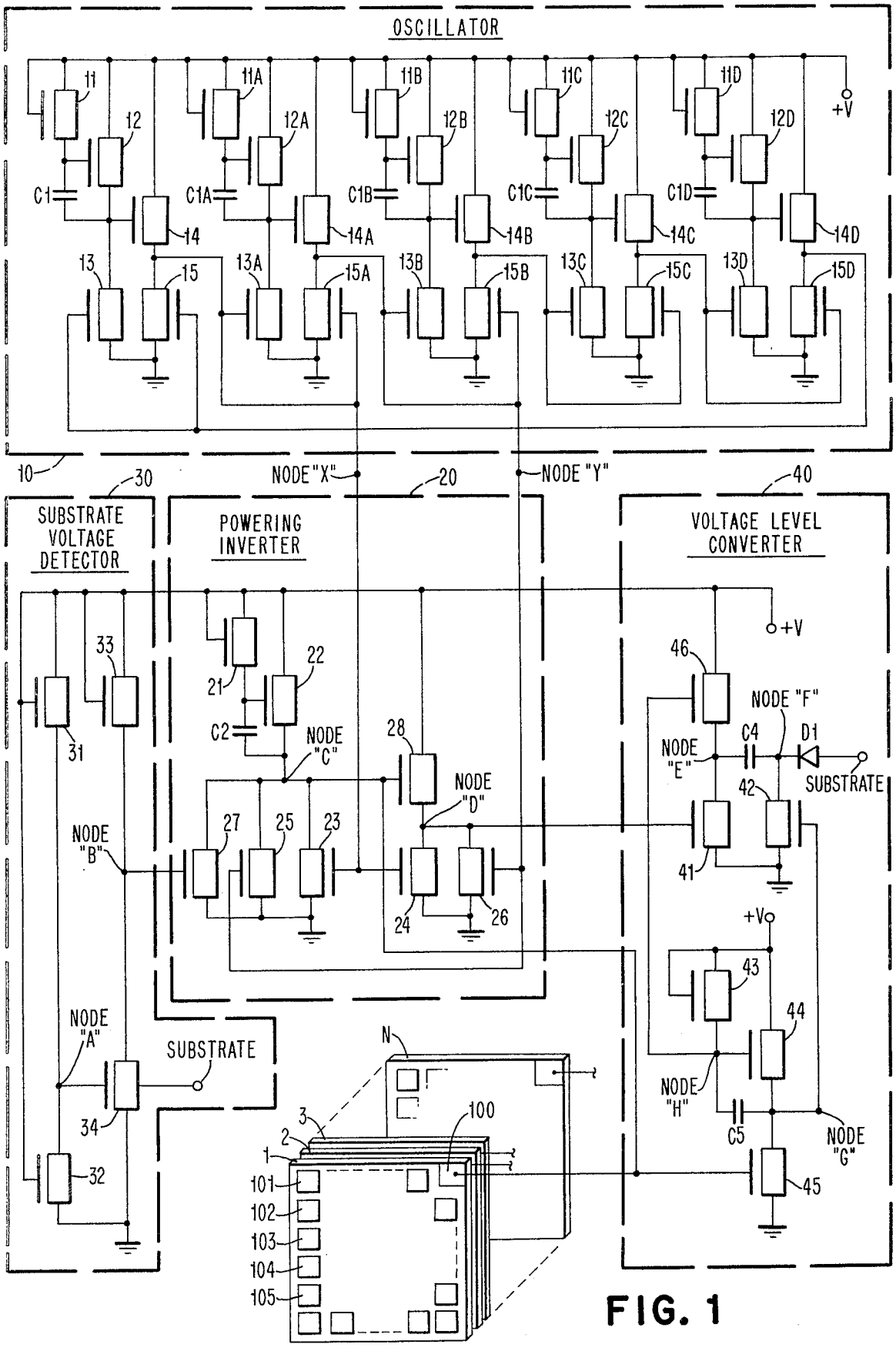

OSCILLATOR
11
11A
11B
11C
11D
12
12A
12B
12C
12D
+V
C1
C1A
C1B
C1C
C1D
14
14A
14B
14C
14D
13
13A
13B
13C
13D
15
15A
15B
15C
15D
10
30
NODE "X"
20
NODE "Y"
40
SUBSTRATE VOLTAGE DETECTOR
POWERING INVERTER
VOLTAGE LEVEL CONVERTER
33
31
21
22
C2
NODE "C"
28
NODE "D"
NODE "B"
27
25
23
24
26
46
NODE "F"
C4
D1
NODE "E"
SUBSTRATE
42
41
+V
43
44
NODE "H"
C5
NODE "G"
45
NODE "A"
SUBSTRATE
34
32
N
100
3
2
1
101
102
103
104
105

FIG. 1

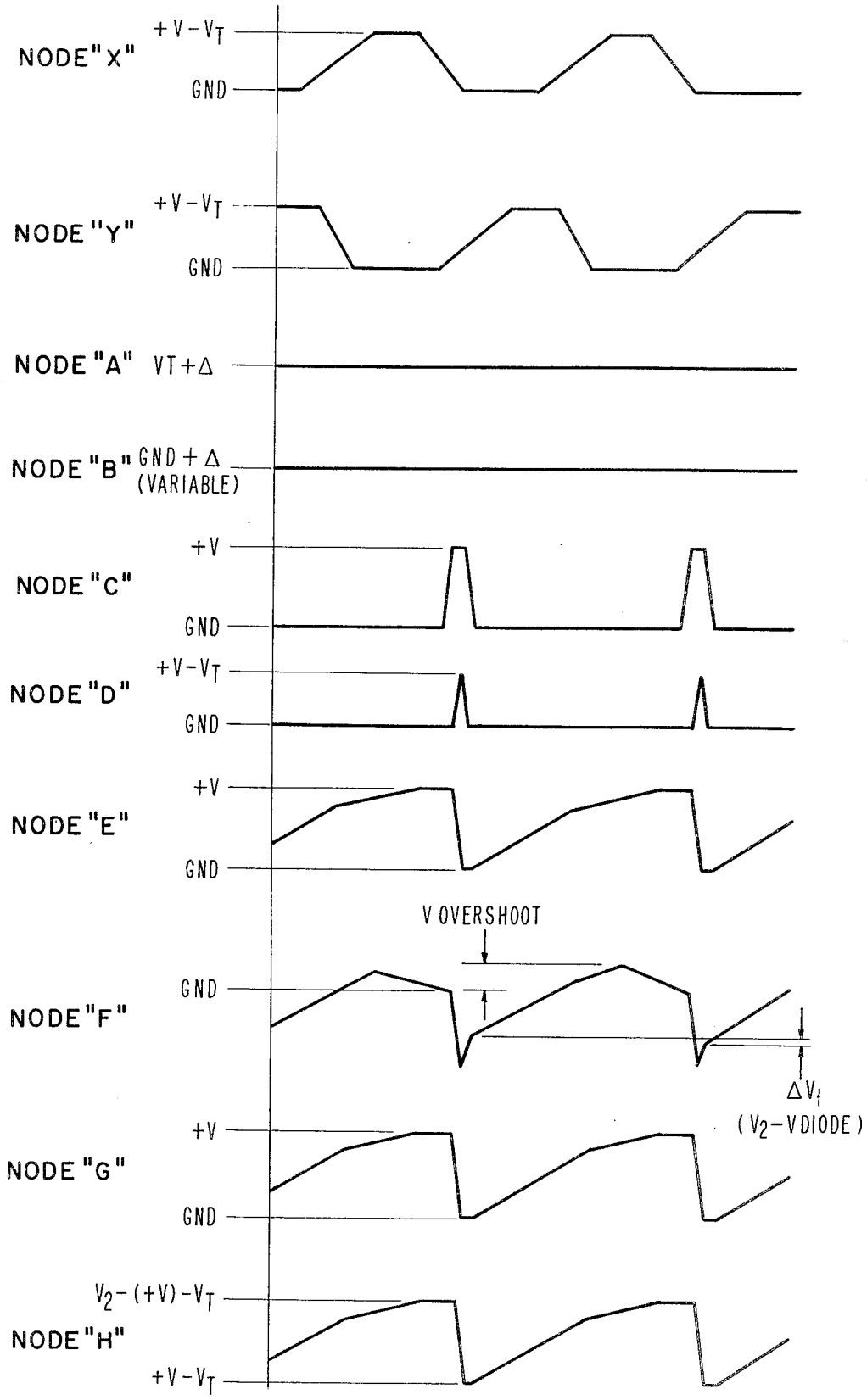

NODE "X"
+V-VT
GND
NODE "Y"
+V-VT
GND
NODE "A"
VT+Δ
NODE "B"
GND + Δ
(VARIABLE)
NODE "C"
+V
GND
NODE "D"
+V-VT
GND
NODE "E"
+V
GND
V OVERSHOOT
NODE "F"
GND
ΔV1
(V2-VDIODE)
NODE "G"
+V
GND
NODE "H"
V2-(+V)-VT
+V-VT

FIG. 2