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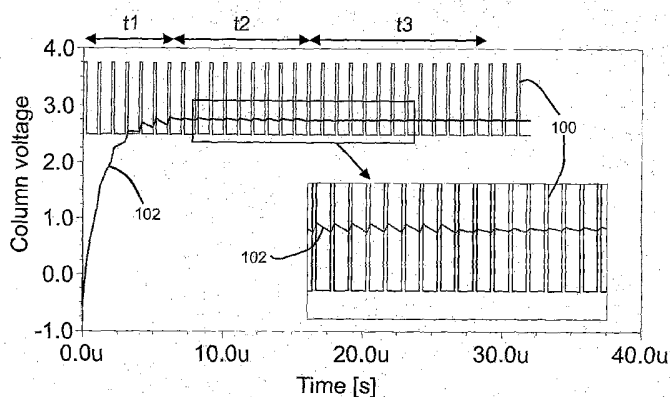
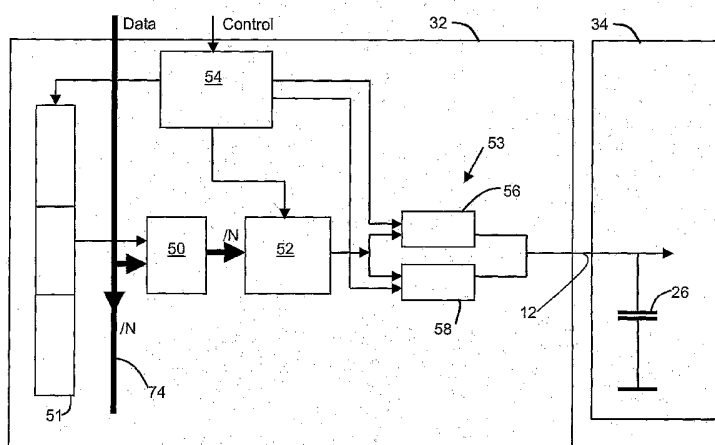
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(54) Title: ACTIVE MATRIX DISPLAY DEVICE



(57) Abstract: An active matrix display device uses column address circuitry for generating pulse width modulation (PWM) pixel drive signals. Filtering circuitry (53) provides low pass filtering of the PWM pixel drive signal, and is switchable between at least two filtering modes (56, 58) during each application of a pixel drive signal to a column conductor. The use of a PWM signal enables a column driver IC to be implemented using almost entirely digital circuit blocks so as to reduce chip area and reduce design times. The two or more stage filtering operation, during the loading of data onto the column for application to a pixel, allows the pixel to be charged in a short time and using a low frequency PWM signal.



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DESCRIPTION

ACTIVE MATRIX DISPLAY DEVICE

5 This invention relates to active matrix display devices, and relates in particular to the circuitry used for providing drive signals to the pixels of the display.

10 Active matrix display devices typically comprise an array of pixels arranged in rows and columns. Each row of pixels shares a row conductor which connects to the gates of the thin film transistors of the pixels in the row. Each column of pixels shares a column conductor, to which pixel drive signals are provided. The signal on the row conductor determines whether the transistor is turned on or off, and when the transistor is turned on, by a high
15 voltage pulse on the row conductor, a signal from the column conductor is allowed to pass on to an area of liquid crystal material, thereby altering the light transmission characteristics of the material. An additional storage capacitor may be provided as part of the pixel configuration to enable a voltage to be maintained on the liquid crystal material even after removal of the
20 row electrode pulse. US-A-5 130 829 discloses in more detail the design of an active matrix display device.

 The frame (field) period for active matrix display devices requires a row of pixels to be addressed in a short period of time, and this in turn imposes a requirement on the current driving capabilities of the transistor in order to
25 charge or discharge the liquid crystal material to the desired voltage level.

 The driver ICs, especially the column drivers, constitute a considerable part of the cost of active matrix LCDs. Most column driver ICs contain a significant number of analogue components - e.g. resistor chains and often buffer amplifiers. These analogue circuit blocks tend to be large due to their
30 complexity and need to use transistors with specific properties which may increase their size above the minimum. Also, the design of analogue circuit

blocks is more complex, takes longer and is more prone to performance problems than digital circuit elements.

In the article "An 8 bit digital driver for AMLCD's" by H. Okada et al., SID94 Digest, p347-350, 1994, a pulse width modulation (PWM) waveform is applied to the column of the display in order to provide an analogue column signal from a digital data input. The required low pass filtering function is provided by the combination of the pixel TFT and the pixel capacitance.

This approach has two problems. The first is that a waveform with a high frequency is applied to the display column so power is wasted in charging and discharging the column capacitance many times during each addressing period. The second is that the time constant of the pixel needs to meet two conflicting requirements - firstly it must be low enough to allow full pixel charging in the address period and secondly it must be large enough to allow correct filtering of the PWM waveform. This compromise can only be met by having a relatively high frequency for the PWM drive signal resulting in large power consumption and more difficulty in achieving high mark space ratios (because the pulse lengths become very short and the clock frequency needed to generate such short pulses is very high). In addition there are potential issues resulting from electromagnetic radiation from the column electrodes.

According to a first aspect of the invention, there is provided an active matrix display device comprising an array of pixels arranged in rows and columns, wherein each column of pixels shares a column conductor to which pixel drive signals are provided, wherein column address circuitry is provided for generating the pixel drive signals, the column address circuitry comprising:

circuitry for generating a pulse width modulation (PWM) pixel drive signal having an average value comprising the desired pixel drive level; and

filtering circuitry for providing low pass filtering of the PWM pixel drive signal, wherein the filtering circuitry is switchable between at least two filtering modes during each application of a pixel drive signal to a column conductor.

The use of a PWM signal (which can be a two level signal) enables a column driver IC to be implemented using almost entirely digital circuit blocks so as to reduce chip area and reduce design times. The approach is based on the known pulse width modulation (PWM) technique, but employs at least a two stage filtering operation, during the loading of data onto the column for application to a pixel. This allows the PWM signal frequency to be reduced.

The filtering circuitry is preferably switchable between at least a first mode in which the filtering circuitry has a first time constant and a second mode in which the filtering circuitry has a second, greater, time constant. This allows rapid charging of the pixel to a voltage close to the desired pixel drive signal level but with relatively poor smoothing, followed by improved smoothing.

An impedance of the filtering circuitry is preferably switchable between different values, for example a real (resistive) impedance may be switchable.

The filtering circuitry may comprise a plurality of transmission gates, each having different on-state impedances, and wherein each mode of the filtering circuitry employs a different transmission gate or combination of transmission gates for coupling the PWM pixel drive signal to the column conductor. The transmission gate impedance can be arranged to define a low pass filter in combination with the column capacitance, and by varying the transmission gate impedance for a given column capacitance, the filter characteristics, in particular the time constant, are varied.

The filtering circuitry may comprise at least one transmission gate, and wherein at least two modes of the filtering circuitry employ different control voltages for the switching of the transmission gate for coupling the PWM pixel drive signal to the column conductor. In this arrangement, the characteristics of a transmission gate are varied by changing the voltage drive conditions rather than physically switching between different impedances.

These techniques may be employed in combination, so that a multiple mode filtering operation can be carried out, with different combinations of transmission gate drive voltages and impedances.

The circuitry for generating a pulse width modulation (PWM) pixel drive signal may comprise a selection circuit which selects an upper and a lower voltage level for the PWM drive signal using a number K of bits of a digital pixel data signal. In this way, the PWM signal does not oscillate between only two levels, but oscillates between a pair of voltage levels which are selected depending on the desired pixel drive level. This reduces the required resolution of the mark:space ratio of the PWM signal. The number of bits may comprise the K (for example 2) most significant bits of the digital pixel data signal.

The circuitry for generating a pulse width modulation (PWM) pixel drive signal may further comprise circuitry for determining the mark:space ratio of the PWM signal, and this may use a number N-K of bits of the digital pixel data signal.

According to a second aspect of the invention, there is provided column address circuitry for driving the columns of an active matrix display, comprising:

circuitry for generating a pulse width modulation (PWM) pixel drive signal having an average value comprising the desired pixel drive level; and

filtering circuitry for providing low pass filtering of the PWM pixel drive signal, wherein the filtering circuitry is switchable between at least two filtering modes during each application of a pixel drive signal to a column conductor.

The invention also provides a method of generating a drive signal for an active matrix display pixel, the method comprising:

generating a pulse width modulation (PWM) signal having an average value comprising the desired pixel drive level to be applied to a pixel within a pixel address period;

low pass filtering the PWM pixel drive signal in a first mode with a first filter time constant for a first sub-period of the pixel address period; and

low pass filtering the PWM pixel drive signal in a second mode with a second, larger, filter time constant for a second sub-period of the pixel address period.

Examples of the invention will now be described in detail with reference to the accompanying drawings, in which:

Figure 1 shows one example of a known pixel configuration for an active matrix liquid crystal display;

5 Figure 2 is used to explain charge flow during pixel charging;

Figure 3 shows a display device including row and column driver circuitry;

Figure 4 shows a conventional column driver circuit;

Figure 5 shows a column driver circuit of the invention;

10 Figure 6 shows examples of PWM waveforms;

Figure 7 shows in greater detail the waveform generation block of the circuit of Figure 5;

Figure 8 shows in greater detail a filter used in circuit of Figure 5;

Figure 9 shows the output voltage waveform for the circuit of Figure 5;

15 Figure 10 shows examples of waveforms for switching transmission gates in the circuit of Figure 8; and

Figure 11 shows an example of a transmission gate.

Figure 1 shows a conventional pixel configuration for an active matrix liquid crystal display. The display is arranged as an array of pixels in rows and columns. Each row of pixels shares a common row conductor 10, and each column of pixels shares a common column conductor 12. Each pixel comprises a thin film transistor 14 and a liquid crystal cell 16 arranged in series between the column conductor 12 and a common potential 18. The transistor 14 is switched on and off by a signal provided on the row conductor 10. The row conductor 10 is thus connected to the gate 14a of each transistor 14 of the associated row of pixels. Each pixel may additionally comprise a storage capacitor 20 which is connected at one end 22 to the next row electrode, to the preceding row electrode, or to a separate capacitor electrode. This capacitor 20 helps to maintain the drive voltage across the liquid crystal cell 16 after the transistor 14 has been turned off. A higher total pixel capacitance is also

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desirable to reduce various effects, such as crosstalk, and to reduce the grey-level dependence of the pixel capacitance.

In order to drive the liquid crystal cell 16 to a desired voltage to obtain a required gray level, an appropriate signal is provided on the column conductor 12 in synchronism with a row address pulse on the row conductor 10. This row address pulse turns on the thin film transistor 14, thereby allowing the column conductor 12 to charge the liquid crystal cell 16 to the desired voltage, and also to charge the storage capacitor 20 to the same voltage.

Figure 2 shows the connection between the column driver 23 (which essentially comprises a voltage source 24 and a switch having resistance 25) and the pixel of the column in the selected row. The column has a column capacitance 26, which results, for example, from all of the cross overs of the column with the row conductors. The individual pixel has a pixel capacitance 27. The column drive signal results in charging of both capacitances 26 and 27. However the time constant for charging the column capacitor 26 (resistance 25 x capacitance 26) is much lower than the time constant for charging the pixel (TFT resistance x capacitance 27).

The column capacitance is charged in a short period and then, when the TFT 14 is turned on, the pixel charges with a longer time constant toward the column voltage, correct operation of the display occurring when the pixel voltage achieves a value very close to the column voltage before the TFT is turned off. The allowed voltage difference between column and pixel voltage at the end of the charging period depends on the exact details of the display (for example the LC characteristics) but is typically in the range 3 - 30mV.

At the end of the row address pulse, the transistor 14 is turned off. The storage capacitor 20 reduces the effect of liquid crystal leakage and reduces the percentage variation in the pixel capacitance caused by the voltage dependency of the liquid crystal cell capacitance. The rows are addressed sequentially so that all rows are addressed in one frame period, and refreshed in subsequent field periods.

As shown in Figure 3, the row address signals are provided by row driver circuitry 30, and the pixel drive signals are provided by column address circuitry 32, to the array 34 of display pixels.

Figure 4 shows a conventional column driver circuit. The number n of
5 different pixel drive signal levels are generated by a grey level generator 40, for example a resistor array. A switching matrix 42 controls the switching of the required level to each column and comprises an array of converters 43 for selecting one of the n grey levels based on a digital input from a latch 44. The digital input is derived from a RAM storing the required image data 45. Each
10 column is provided with a buffer 46 for holding a pixel in the column to the required drive signal level for the full duration of the row address period. The use of a large number of digital to analogue converters increases the substrate area required by the column driver IC and increases the complexity of the design of the circuit.

15 Figure 5 is a block diagram of the column driver circuit of the invention, and shows the circuitry required for generating the waveform for one column.

As in a conventional digital column driver, data intended for each column is latched into a data latch 50 from data bus 74 which carries N bit pixel data. A pulse from shift register 51 enables operation of the data latch 50
20 at the correct time when data intended for the display column driven by this block of the column driver is present on the data bus 74. In this design the latched data is used to control a waveform generator 52 which produces pulse width modulated waveforms. These waveforms oscillate between two voltage levels, and the mark:space ratio determines the average voltage of the
25 waveform, which is the intended output.

The PWM signal is provided to filtering circuitry 53 for providing low pass filtering of the PWM pixel drive signal in order to generate this average voltage and provide this to the column 12. The filtering circuitry 53 and the waveform generator 52 are controlled by a timing circuit 54.

30 The filtering circuitry 53 has two transmission gates 56, 58. The PWM output is routed to the column 12 through one or both of the gates, as will be explained in greater detail below. The gate or gates used to route the PWM

signal form a low pass filter in combination with the column capacitance 26. The filter arrangement 23 is switchable between at least two filtering modes during each application of a pixel drive signal to a column conductor.

The use of a PWM signal (which can be a two level signal) enables the column driver IC to be implemented using almost entirely digital circuit blocks, in particular without digital to analogue converters. The multi-mode filtering enables rapid column charging times with good smoothing and without requiring high frequency PWM signals.

Figure 6 shows examples of the waveforms which can be produced by the waveform generator 52. By way of example, the upper voltage limit VU is taken to be 4V and the lower voltage limit VL is taken to be 2V. The top plot has a mark space ratio of 1:5 and gives a mean voltage of 2.33V, and the lower plot has a mark space ratio of 1:1 and gives a mean voltage of 3V.

An example of the structure of the waveform generator 52 is shown in more detail in Figure 7. A voltage level generator 70 generates 2^K voltage levels, and a selection matrix 72 selects two of these levels to form the upper and lower voltage levels (VL and VU) of the PWM waveform. This selection is performed by the K most significant bits of the data. Thus, the data 74 (N bits wide) is divided into the K most significant bits 76 and the (K-N) least significant bits 78. The (K-N) least significant bits 78 are provided to a PWM waveform generator 80.

The voltage generator does not therefore generate all possible analogue outputs as in a conventional column driver. For example, in the case where $K=2$, the voltage generator provides 4 voltage levels, and the 2 most significant bits of the pixel data word determine which two levels (normally two adjacent levels) will form the upper and lower voltage rails for the PWM waveform. The remaining N-2 bits control the mark:space ratio. If the data input is 8 bits wide and 2 bits are used to select VL and VU then the remaining 6 bits will then be used to generate a waveform with a mark to space ratio varying between 1:63 and 64:0 (i.e. a DC level equal to VU).

The output of the PWM waveform generator 80 is used to control two transmission gates 82, 84. One of these 82 is for selectively providing the

voltage VU to the output and the other 84 is for selectively providing the voltage VL to the output. The two gates 82, 84 are operated in complementary manner, so that the control signal for one is the logical inverse of the control signal for the other, as provided by the inverter gate 86.

5 Depending on the exact design of the column driver, the voltage generator 70 may be within the column driver or the voltage levels may be generated externally and fed into the column driver.

Again, depending on the exact design of the column driver and the properties of the driven display a number of variations are possible. For
10 example the voltage levels used to generate VL and VU may be equally spaced or may be arranged to provide a non-linear transfer characteristic. Also, two separate sets of voltage levels may be provided for use in driving positive and negative polarities required to invert the LC voltage polarity.

The resulting pulse width modulated waveform switches between the
15 voltage levels, VU and VL, with a mark to space ratio of A:B has an average voltage level, VA, given by:

$$VA = VL + (VU - VL) \cdot A / (A + B)$$

20 Hence, by varying the ratio A/B the mean voltage VA can be varied between VL and VU. However, to derive a voltage at a level, VA, as required for driving an LCD pixel, the waveform must be passed through a low pass filter.

The output 88 of the waveform generator 52 is thus provided to the filter
25 block 53.

The filtering of the PWM waveforms to produce the required drive signal is performed using a combination of an impedance within the driver IC and the display column capacitance. Using this approach, the signal appearing on the display columns has a very small AC component so little power is consumed in
30 charging and discharging the column capacitance. There is still the potential issue of a conflict between arranging the time constant to allow column

charging in an acceptable time and keeping the PWM waveform frequency at an acceptable level.

The invention resolves this issue by switching the internal impedance in the column driver. The impedance is initially at a low value allowing rapid
5 column charging to a level close to the final desired level but with rather poor filtering. After a period, the impedance is switched to a higher level giving better filtering but still low enough that the column charges to a sufficiently accurate voltage. This is possible, despite the higher impedance, because the voltage change required from the initial approximate state to the final accurate
10 voltage is small.

Thus, a switched filter block is provided which implements the function of providing a switched time constant which low pass filters the PWM signal to provide an average DC level controllable by the mark:space ratio of the PWM waveform. An example of the switched filter block is shown in Figure 8, and
15 the filtered output is the signal provided onto the display column.

The PWM waveform 88 is provided to a pair of transmission gates 56, 58 (TG1, TG2), as also shown in Figure 5. For this example, the gate 56 has a lower impedance than the gate 58. The display column capacitance 26 forms a part of the low pass filter in combination with the gate impedance. In this
20 example, the switched impedance is thus provided by switching the impedance of a set of transmission gates interposed between the waveform generator and the display column 12, although a single gate with controllable impedance may be used.

In order to provide the transmission gates 56, 58 with different on
25 impedances, transistors with different width-length values in the two gates may be used. The gates are controlled by the signals TGC1 and TGC2 which are provided by the timing generator 54, and these signals switch the transmissions gates on and off. In the simplest case, these waveforms switch between two fixed levels, either between the power rails of the IC or between
30 levels determined by the values VL and VU of the PWM waveform currently being switched.

In a simple case, the Hi and Lo values of TGC1 and TGC2 are equal to VU and VL of the switched waveform. In the simplest case, the switching has two phases - TG1 on (low impedance) and TG2 on (high impedance), with the gates operated in complementary manner.

5 The plots in Figure 8 show a refinement of this in which the TGC1/2 waveforms have three phases during each row address period, represented by the times t1, t2 and t3. The states of the transmission gates during these periods are shown in the following table, again with TG1 having a lower on impedance than TG2.

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Period	TG1 state	TG2 state	Overall impedance
t1	On	On	Low
t2	On	Off	Medium
t3	Off	On	High

The resulting output waveform which is driven onto the display column is shown in Figure 9. Plot 100 shows the PWM waveform and plot 102 shows the column waveform after low pass filtering.

15 These waveforms illustrate the principle of operation. In this simulation VL and VU are 2.5V and 3.75V. The time period t1, t2 and t3 are 6.4 μ s, 9.6 μ s and 12.8 μ s respectively. The main waveforms show all 3 periods, t1, t2 and t3 and the inset shows more detail of the waveforms at the transition between the periods t2 and t3.

20 The PWM signal has a mark:space ratio of 1:4 and the repeat frequency is 1MHz. From Figure 9 it can be seen that, during the initial period (t1) when the transmission gates are in their lowest impedance state, there is a rapid charging of the column voltage from its initial value to a value close to the required final value.

25 However, it can be seen that there is still a large AC ripple on the signal. During period t2 the gate impedance rises and charging continues more slowly but brings the signal very close to the final desired value with a reduced level of AC ripple. During the final phase, t3, when only gate TG2 is on, the

impedance is even higher allowing a small final adjustment to the mean level to bring it to a final accurate value but the AC ripple is now very low - 10mV peak to peak.

In a modification to the approach described above the amplitude of the switch waveform TGC1 (and TGC2 if required) can be larger in period t1. As an example of this (and in fact as used in the simulation whose output is shown in Figure 9), TGC1 has an amplitude equal to the power rail of the column driver during period t1 while, during periods t2 and t3 the signals TGC1 and TGC2 switch between values equal to VL and VU. It is also possible for the signals TGC1 and TGC2 to switch between values equal to $VL - \delta VL$ and $VU - \delta VLU$.

Figure 10 shows two possible formats (Example 1 and Example 2) for the waveforms TGC1 and TGC2. For each example, the signal is shown for switching an n-channel transistor (left hand plots) and for switching a p-channel transistor (right hand plots) in complementary manner.

As shown in Figure 11, a transmission gate typically has both transistor types in parallel and switched with complementary signals. Thus, an n-channel TFT 110 and a p-channel TFT 112 are in parallel between the gate input 114 and output 116. The top waveform in Figure 11 is for application to the gate of the n-channel transistor 110 and the bottom waveform in Figure 11 is for application to the gate of the p-channel transistor 112. The pulses (such as 118) are for switching on the gate.

Example 1 in Figure 10 is a waveform as described above with 3 time periods, all switching voltages on the gates of the transmission gate transistors switching between the same values (VU and VL).

In Example 2, only transmission gate TG1 is switched on in periods t1 and t2 but, during t1, an n-channel device is driven to the power rail (VCC) and a p channel device is driven to ground, V0, turning the transistors on harder and hence producing a lower impedance. During T2 the impedance is increased by switching the drive to TG1 back to VU and VL. Finally, in period t3, TG1 is switched off and the higher impedance TG2 is switched on. The

modelling results shown in Figure 9 are for this case where $V_{CC} = 5V$ and $V_0 = 0V$.

In the example above, the frequency of the PWM signal is 1 MHz. This is only an example of the possible frequency, but which can easily be
5 achieved. The oscillations are filtered out before application to the column conductors, so that the column capacitance is not repeatedly charged during the pixel addressing operation.

The invention provides a column driver in which a PWM signal is used to create a waveform with an easily controllable average level, and employs
10 filtering using a filter consisting of a switched impedance transmission gate or gates plus the display column capacitance. The filter characteristics are varied during the line addressing period so that there is initially a low impedance allowing the column to charge rapidly to an approximate value. Later, the time constant of the filter is increased, reducing the charging rate but reducing the
15 AC ripple on the signal so that, an accurate column drive voltage with low AC ripple superimposed is finally achieved. This arrangement allows a simple, digital column driver design with no buffer amplifiers and a lower power than in cases where filtering is done at the pixel because the number and amplitude of transitions of column voltage during the line period is reduced.

It should be appreciated that there are many possible variations involving switching gate impedances other than the specific examples given
20 above. In the simplest case, two transmission gates can be used with only two phases - TG1 on and TG2 on in complementary manner.

It is possible to have more than two transmission gates and
25 correspondingly more switch periods where switching various combinations of gates produces more different impedance levels.

There are of course an infinite variety of relative values for the transmission gate switching periods, t_i .

The drive levels to the transmission gates may be different during
30 different switch periods (as described above) or may even change during a single switching period. In general, the levels decrease as time goes on to increase gate impedance. This can be done in steps or could be done

continuously using a ramped signal to drive the transmission gates for example.

In order to cope with a wide range of displays with different column capacitances, additional transmission gates may be added with a range of impedances and a sub-set pre-selected to match the display column capacitance. Alternatively, the transmission gate drive voltages may be adjusted to produce the correct impedances to match the column capacitance.

Other circuit elements such as single transistors can be used in place of transmission gates to provide a switched impedance.

The column driver circuit may have the components 50, 52, 53 for each column of the display, but with a shared timing and control circuit 54. Multiplexing schemes are also known which allow a reduction in the circuitry, and provide addressing of the columns in groups rather than all simultaneously. Known multiplexing schemes can be applied to the column architecture of the invention in routine manner, and these multiplexing architectures will not be discussed in this application.

The invention has been described in detail in connection with an LCD display. However, the invention may also be applied to other voltage-addressed displays.

Other features of the invention will be apparent to those skilled in the art.

CLAIMS

1. An active matrix display device comprising an array (34) of pixels arranged in rows and columns, wherein each column of pixels shares a column conductor (12) to which pixel drive signals are provided, wherein
5 column address circuitry (32) is provided for generating the pixel drive signals, the column address circuitry comprising:
circuitry (52) for generating a pulse width modulation (PWM) pixel drive signal having an average value comprising the desired pixel drive level; and
10 filtering circuitry (53) for providing low pass filtering of the PWM pixel drive signal, wherein the filtering circuitry is switchable between at least two filtering modes during each application of a pixel drive signal to a column conductor.
- 15 2. A device as claimed in claim 1, wherein the filtering circuitry (53) is switchable between at least a first mode in which the filtering circuitry has a first time constant and a second mode in which the filtering circuitry has a second, greater, time constant.
- 20 3. A device as claimed in claim 1 or 2, wherein an impedance of the filtering circuitry (53) is switchable.
4. A device as claimed in claim 3, wherein a real impedance is switchable.
- 25 5. A device as claimed in any preceding claim, wherein the filtering circuitry (53) comprises a plurality of transmission gates (56, 58), each having different on-state impedances, and wherein each mode of the filtering circuitry employs a different transmission gate or combination of transmission gates for coupling the PWM pixel drive signal to the column conductor.
- 30 6. A device as claimed in any preceding claim, wherein the filtering circuitry (53) comprises at least one transmission gate, and wherein at least

two modes of the filtering circuitry employ different control voltages for the switching of the transmission gate for coupling the PWM pixel drive signal to the column conductor.

5 7. A device as claimed in any preceding claim, wherein the circuitry (52) for generating a pulse width modulation (PWM) pixel drive signal comprises a selection circuit (72) which selects an upper (VU) and a lower (VL) voltage level for the PWM drive signal using a number K of bits of a digital pixel data signal.

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8. A device as claimed in claim 7, wherein the number of bits comprise the K most significant bits of the digital pixel data signal.

9. A device as claimed in claim 7 or 8, wherein the circuitry (52) for
15 generating a pulse width modulation (PWM) pixel drive signal further comprises circuitry (80) for determining the mark:space ratio of the PWM signal.

10. A device as claimed in claim 9, wherein the circuitry (80) for determining
20 the mark:space ratio selects the mark:space ratio using a number N-K of bits of the digital pixel data signal.

11. A device as claimed in any preceding claim, further comprising a
voltage level generator (70).

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12. A device as claimed in any preceding claim, comprising an active matrix LCD display device.

13. Column address circuitry for driving the columns of an active matrix
30 display, comprising:

circuitry (52) for generating a pulse width modulation (PWM) pixel drive signal having an average value comprising the desired pixel drive level; and

filtering circuitry (53) for providing low pass filtering of the PWM pixel drive signal, wherein the filtering circuitry is switchable between at least two filtering modes during each application of a pixel drive signal to a column conductor.

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14. A method of generating a drive signal for an active matrix display pixel, the method comprising:

generating a pulse width modulation (PWM) signal having an average value comprising the desired pixel drive level to be applied to a pixel within a pixel address period;

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low pass filtering the PWM pixel drive signal in a first mode with a first filter time constant for a first sub-period of the pixel address period; and

low pass filtering the PWM pixel drive signal in a second mode with a second, larger, filter time constant for a second sub-period of the pixel address

15

period.

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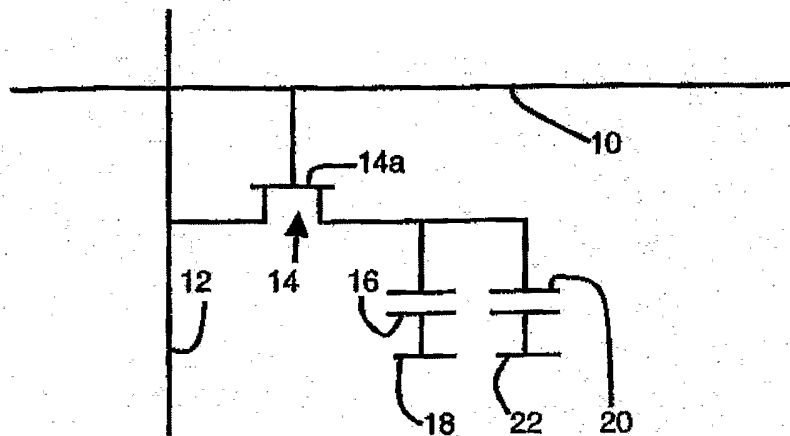


FIG. 1

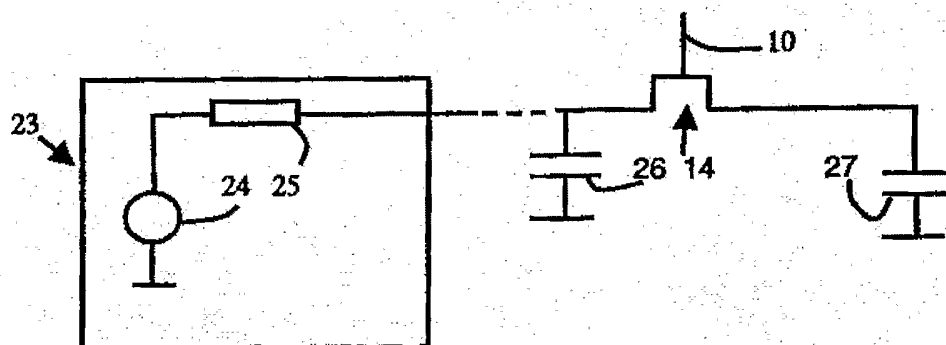


FIG. 2

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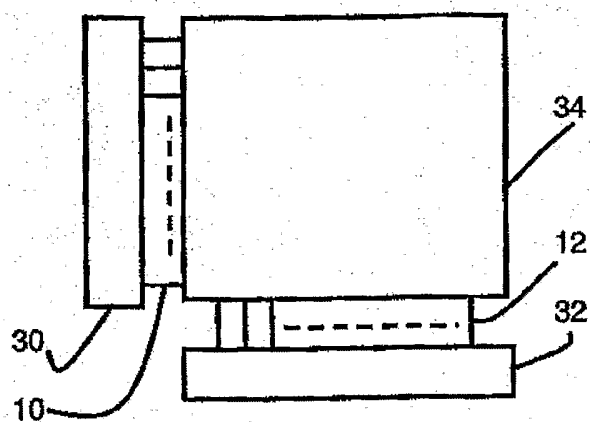


FIG. 3

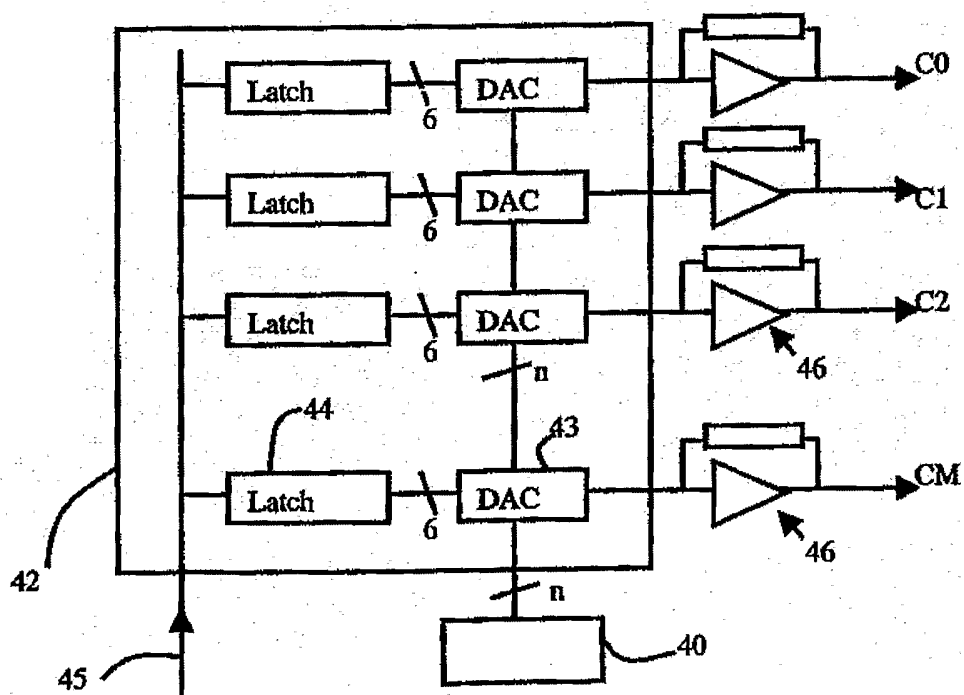


FIG. 4

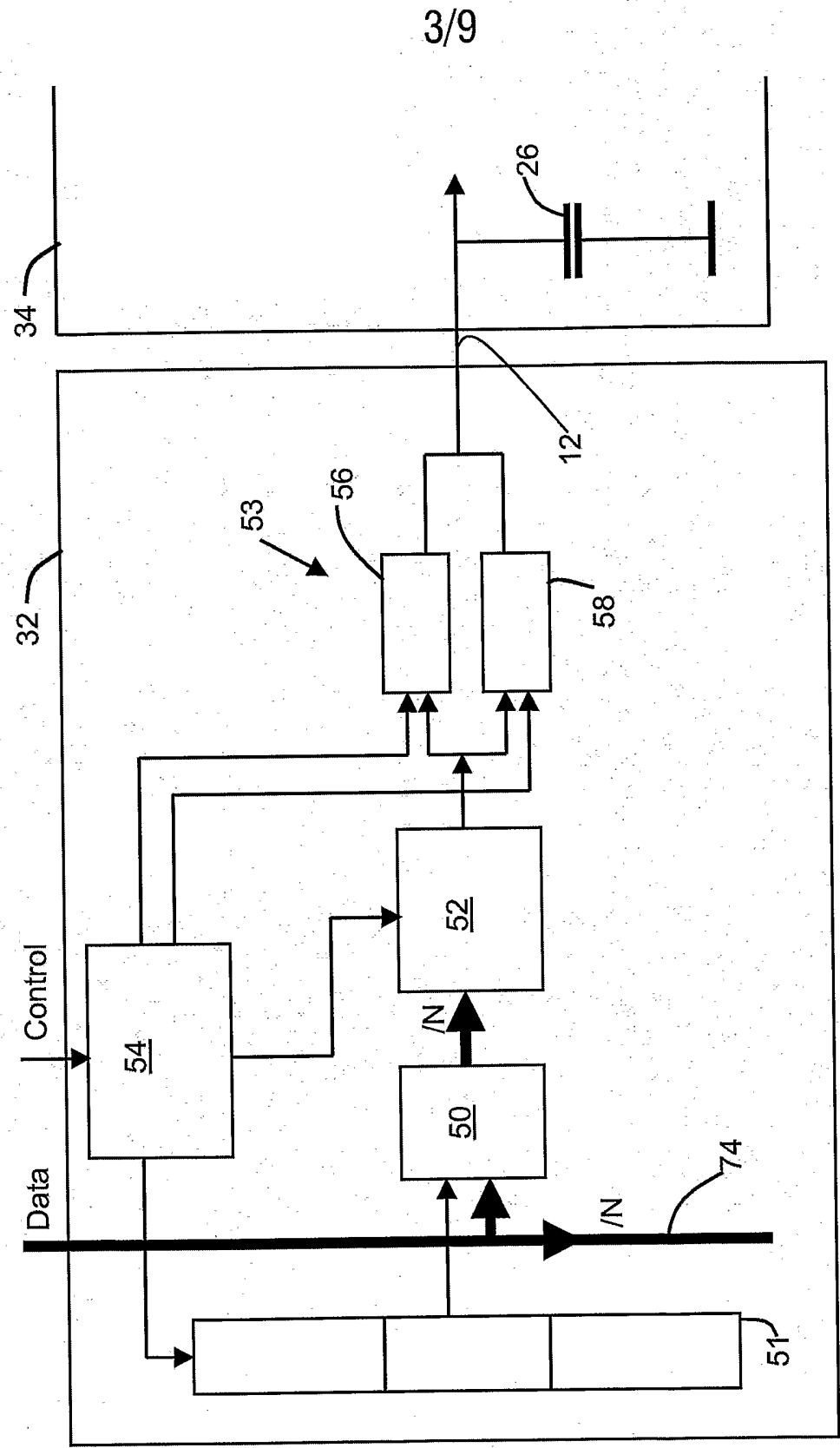


FIG.5

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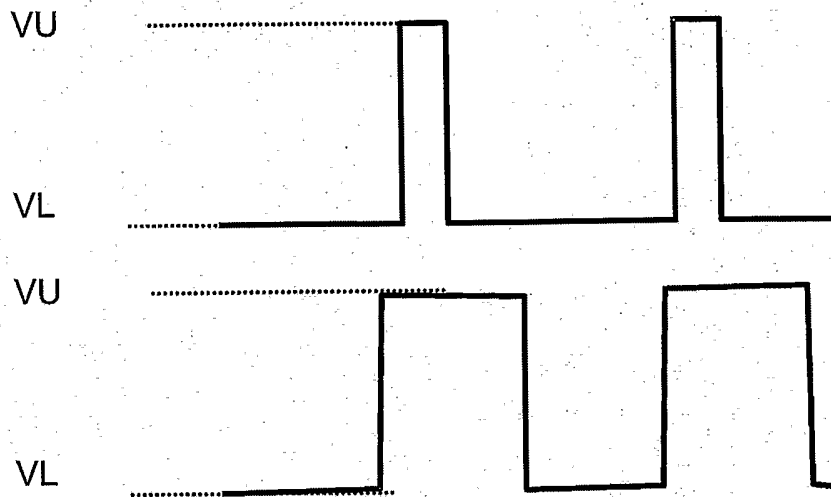


FIG.6

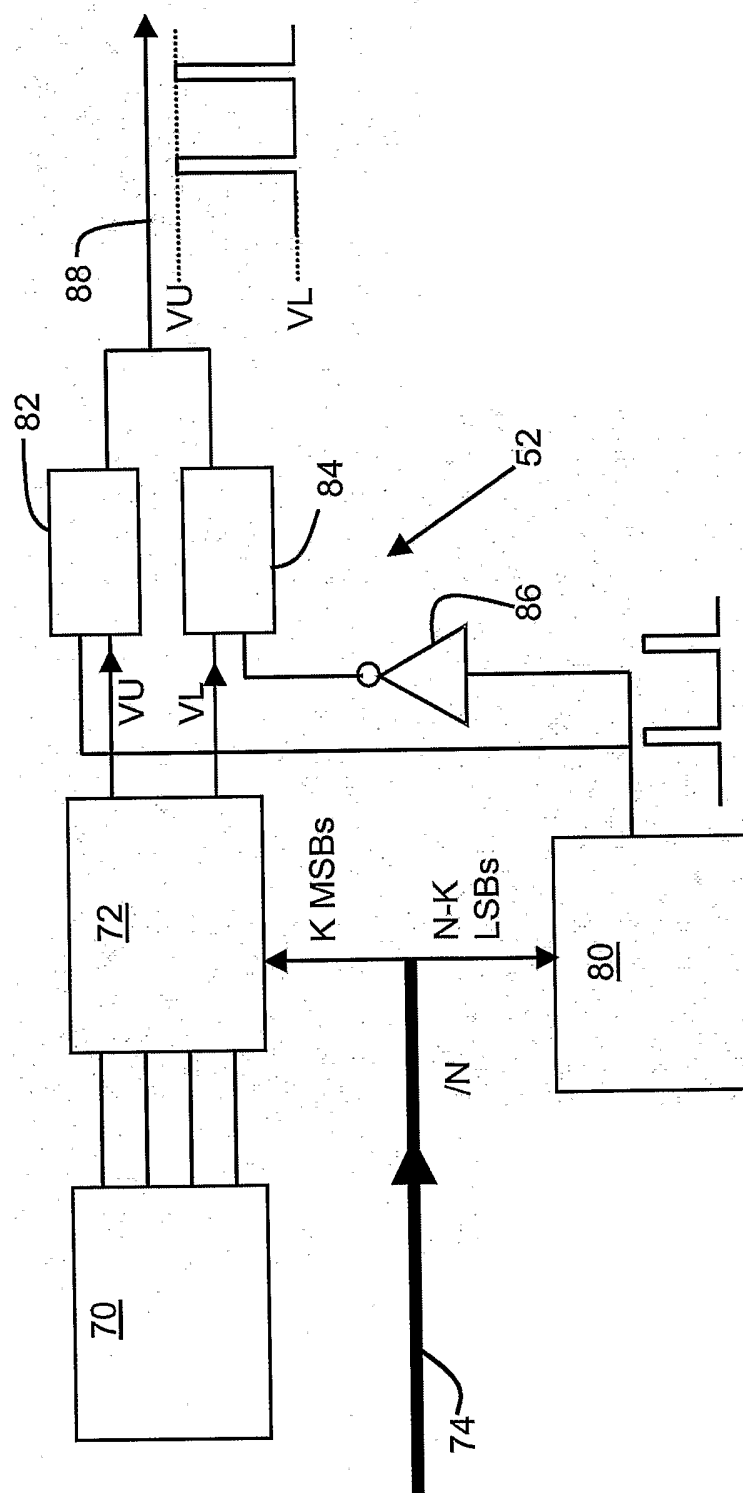


FIG. 7

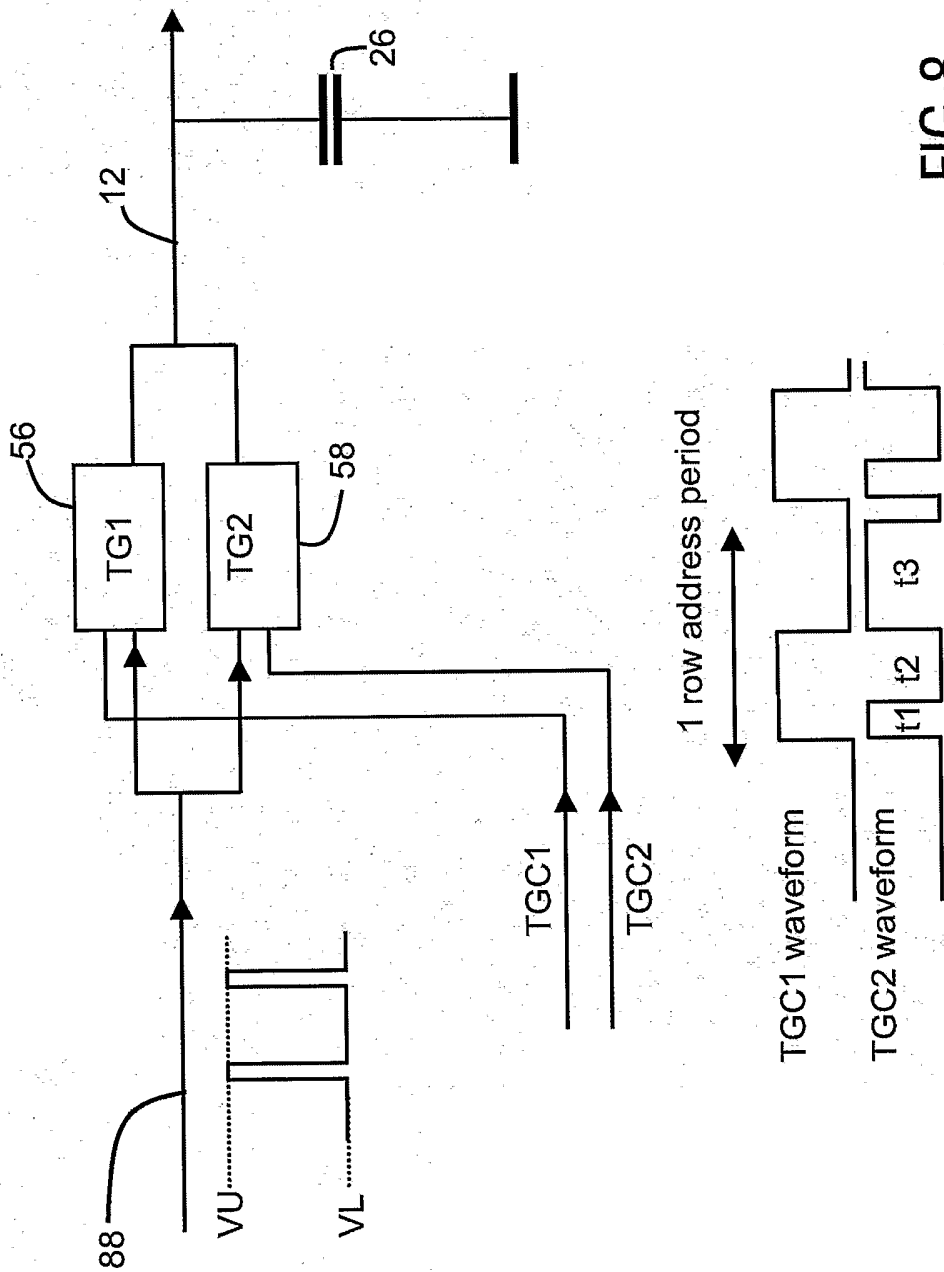


FIG. 8

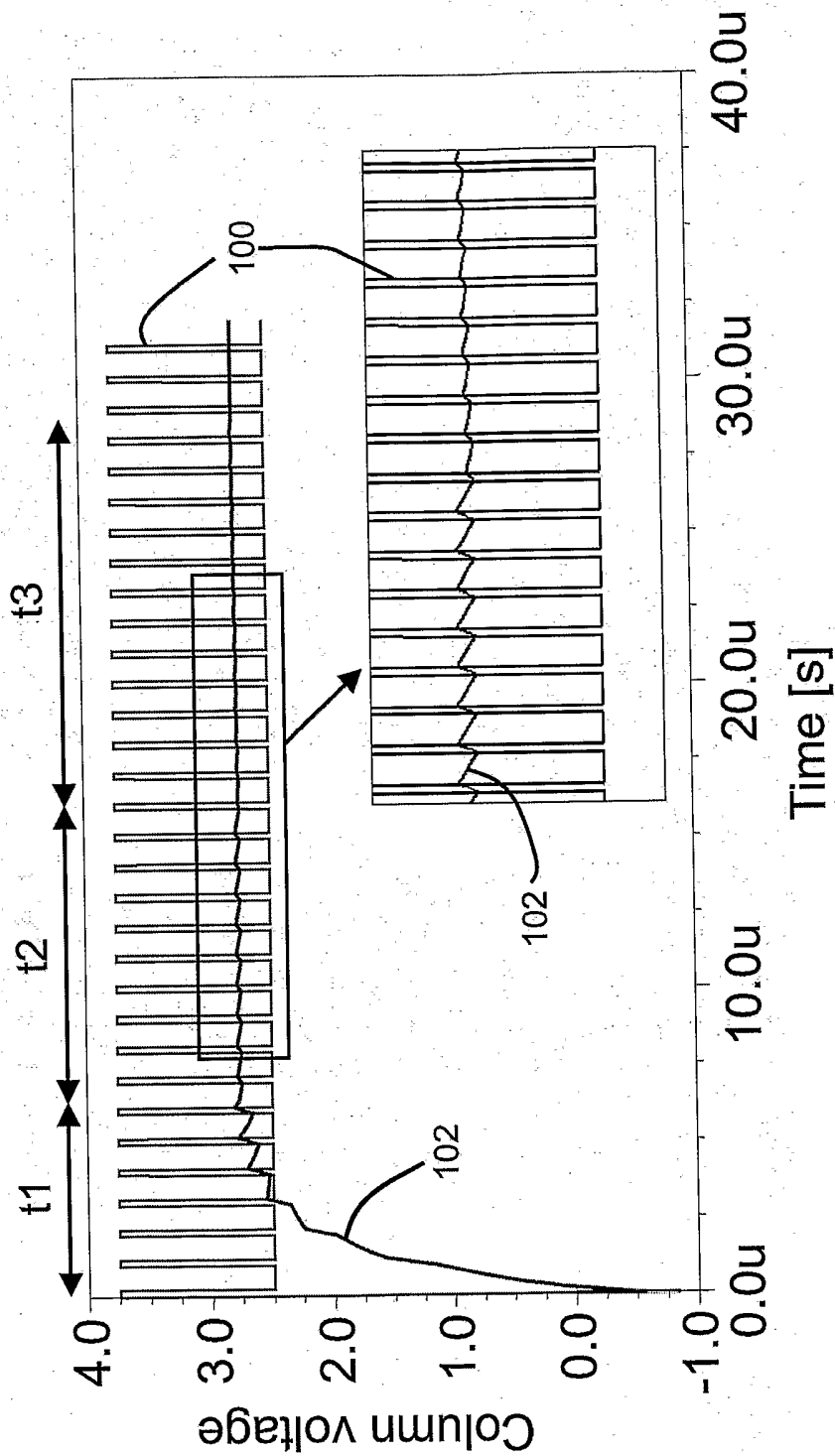


FIG. 9

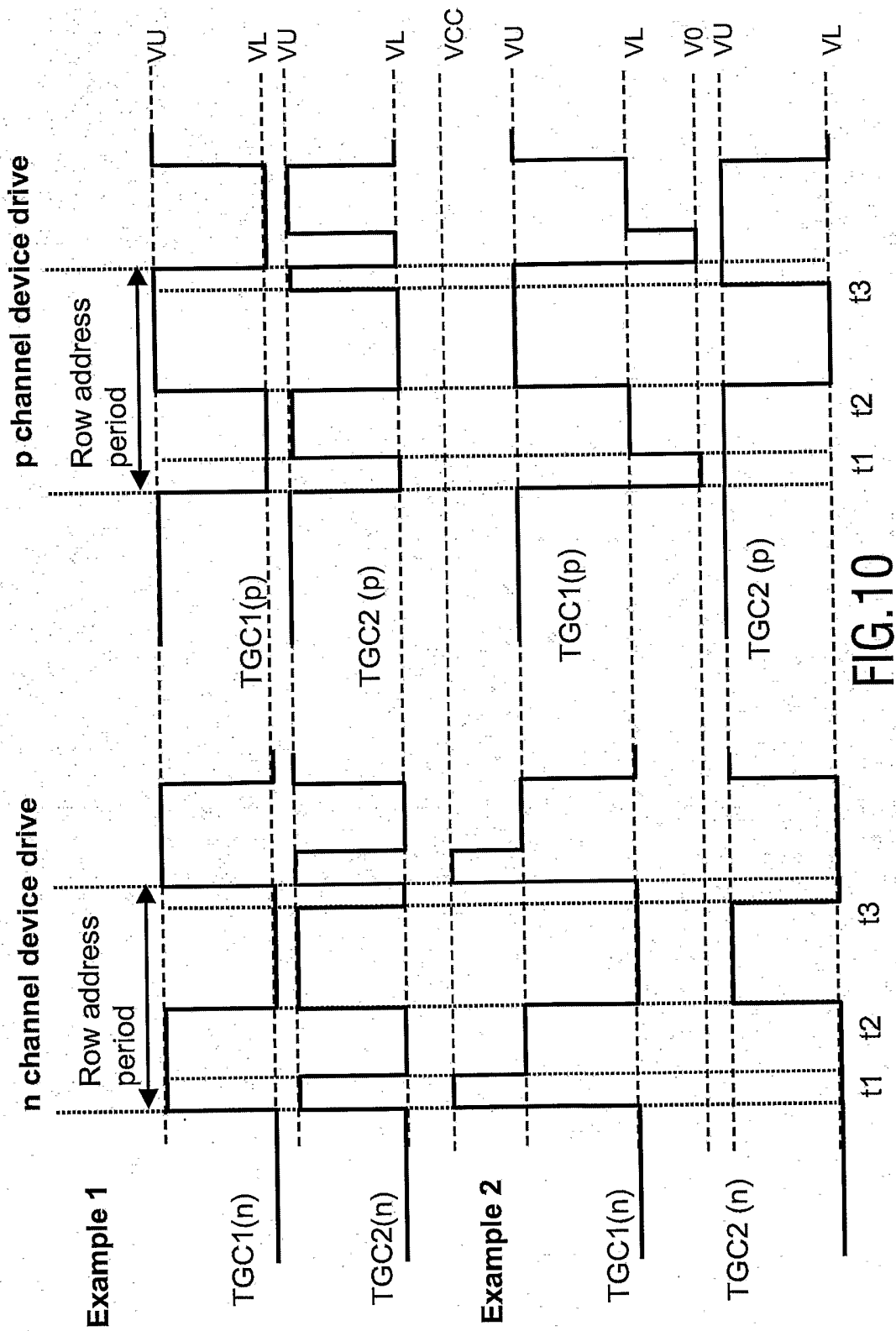


FIG.10

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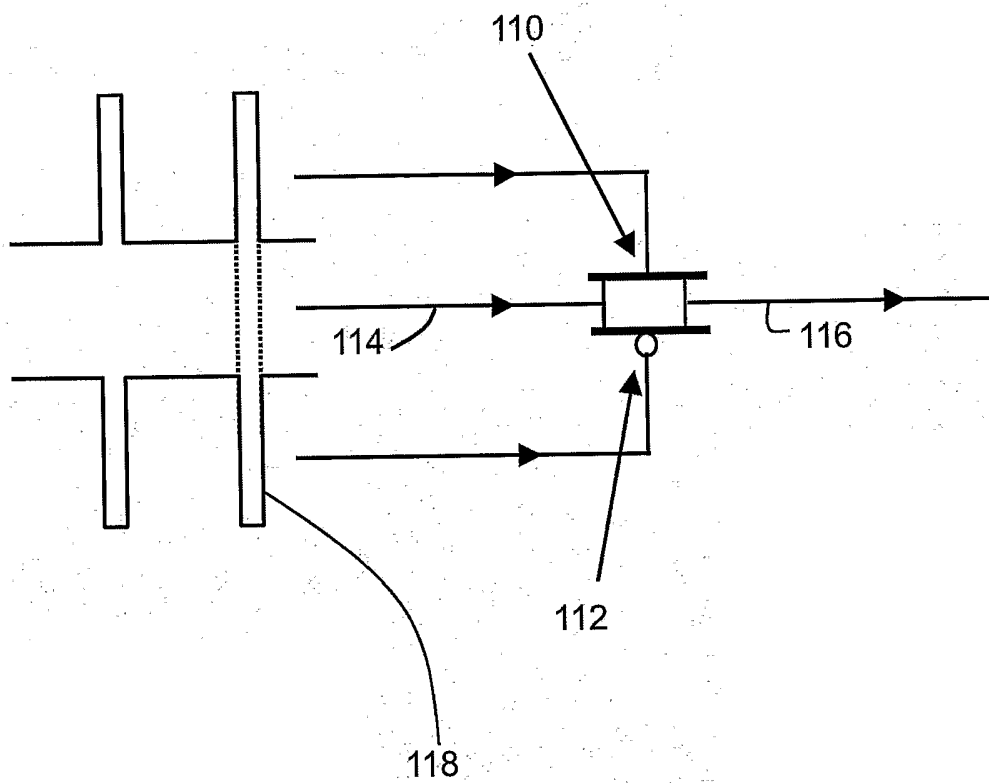


FIG.11

Internati plication No
PCT/IB2004/001706

According to International Patent Classification (IPC) or to both national classification and IPC

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 694 900 A (SHARP KK) 31 January 1996 (1996-01-31) page 9, line 48 - line 56; figure 9 figures 21,22	1-6, 12-14
Y	page 15, lines 10-40; figure 43 page 16, line 9 - line 40; figures 45,46	7-11
Y	EP 0 433 054 A (SHARP KK) 19 June 1991 (1991-06-19) column 5, line 25 - line 30; figures 3,4a-4c column 7, line 30 - line 33 column 8, line 14 - line 16 column 8, line 22 - line 25	7-11

☒ Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search

18 August 2004

Date of mailing of the international search report

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	OKADA H ET AL SOCIETY FOR INFORMATION DISPLAY: "AN 8-BIT DIGITAL DATA DRIVER FOR AMLCDS" SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS. SAN JOSE, JUNE 14 - 16, 1994, SANTA ANA, SID, US, vol. VOL. 25, 14 June 1994 (1994-06-14), pages 347-350, XP000462717 cited in the application figure 4	1
A	US 5 130 829 A (SHANNON JOHN M) 14 July 1992 (1992-07-14) cited in the application figures 1,2	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat pplication No
PCT/IB2004/001706

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0694900	A	31-01-1996	JP 3275991 B2	22-04-2002
			JP 8211853 A	20-08-1996
			CN 1122492 A ,B	15-05-1996
			EP 0694900 A2	31-01-1996
			US 6151006 A	21-11-2000
EP 0433054	A	19-06-1991	JP 2642204 B2	20-08-1997
			JP 3184018 A	12-08-1991
			AU 617258 B2	21-11-1991
			AU 6771290 A	29-08-1991
			BR 9006329 A	24-09-1991
			CN 1052565 A ,B	26-06-1991
			DE 69021027 D1	24-08-1995
			DE 69021027 T2	25-01-1996
			EP 0433054 A2	19-06-1991
			ES 2074143 T3	01-09-1995
			KR 9402295 B1	21-03-1994
			US 5162786 A	10-11-1992
US 5130829	A	14-07-1992	GB 2245741 A	08-01-1992
			EP 0464897 A2	08-01-1992
			JP 4233516 A	21-08-1992