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(54) Title: TUNNEL JUNCTION

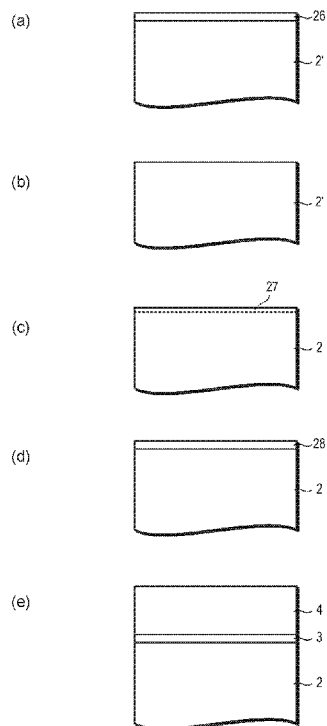


Fig. 6

(57) **Abstract:** A superconductor-insulator-semiconductor tunnel junction and a method of forming a superconductor-insulator-semiconductor tunnel junction are described. The method comprises removing a surface oxide layer from a surface of a layer of silicon, germanium or silicon-germanium alloy, for example, using a buffered hydrogen fluoride dip. The method comprises heating the layer of silicon, germanium or silicon-germanium alloy to at least 550 °C in a vacuum and forming a dielectric layer on the surface of the layer of silicon, germanium or silicon-germanium alloy, for example, by oxidation. The method comprises depositing a superconductor on the dielectric layer.



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Tunnel junction

Field of the Invention

5 The present invention relates to a tunnel junction and to a method of fabricating a tunnel junction.

Background

Semiconductor-superconductor tunnel junctions can be used for electron cooling at low temperatures, typically around or below 1K. Cooling power can be increased by
10 reducing the tunnel resistance. However, semiconductor-superconductor tunnel junction devices tend to suffer from a high sub-gap leakage if the tunnel resistance is reduced. Reference is made to A. M. Savin et al.: "Efficient electronic cooling in heavily doped silicon by quasiparticle tunneling", Applied Physics Letters, volume 79, pages 1471 to 1473 (2011).

15

The present invention seeks to provide an improved tunnel junction device, e.g. providing greater cooling.

Summary

According to a first aspect of the present invention there is provided a method of forming a superconductor-insulator-semiconductor tunnel junction. The method
5 comprises removing a surface oxide layer from a surface of a layer of silicon, germanium or silicon-germanium alloy, heating the layer of silicon, germanium or silicon-germanium alloy to at least 550 °C in a vacuum, forming a dielectric layer on the surface of the layer of silicon, germanium or silicon-germanium alloy and depositing a superconductor on the dielectric layer.

10

Introducing an insulator (i.e. a dielectric layer) between the semiconductor and the superconductor can help to reduce sub-gap leakage and so increase the cooling efficiency of the junction.

15 Heating the layer of silicon, germanium or silicon-germanium can be used to clean the surface of the layer, for example, by driving off terminating chemical species, such as hydrogen, from the surface of the layer.

Heating the layer of silicon, germanium or silicon-germanium, forming the dielectric
20 layer and depositing the superconductor may be steps which are carried out in a deposition system (which may include more than one chamber). The layer of silicon, germanium or silicon-germanium (which may be supported on a substrate) is not removed from the system between steps. Thus, the surface of the layer is not exposed to ambient conditions once the layer of silicon, germanium or silicon-germanium are
25 driven off by heating until the dielectric layer is formed and the superconductor deposited.

Forming the dielectric layer may comprise exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to one or more chemical species. Forming the
30 dielectric layer may comprise exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to a gas. Forming the dielectric layer may comprise exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to a mixture of gases or to a sequence of gases (such as oxygen and then nitrogen) and/or gas mixtures (such as a mixture of oxygen and nitrogen). Forming the dielectric layer may
35 comprise exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to oxygen, for example, in the form of (dry) pure oxygen gas (O₂). Forming the

dielectric layer may comprise exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to nitrogen, for example, in the form of (dry) pure nitrogen gas (N_2). The method may comprise exposing the surface of the layer of silicon, germanium or silicon-germanium alloy (for example, to oxygen gas) for a time of at least 1 minute, at least 2 minutes, at least 5 minutes or at least 10 minutes. The method may comprise exposing the surface of the layer for a time no more than 2 hours, no more than 1 hour or no more than 0.5 hours. For example, the method may comprise exposing the surface of the layer of silicon, germanium or silicon-germanium alloy for about 10 to 20 minutes.

10

Formation of the dielectric layer may be carried out at a pressure below atmospheric pressure. Formation of the dielectric layer may be carried out at a pressure between 200 mbar (20,000 Pa) and 400 mbar (40,000 Pa). Formation of the dielectric layer may be carried out at a temperature above room temperature. Forming the dielectric layer may be carried out at a temperature at or above 500 °C. For example, formation of the dielectric layer may be carried out at a temperature of about 550 °C.

15

Formation of the dielectric layer may be carried out at the same temperature at which the layer is heated.

20

At least a portion of the dielectric layer and a portion of the superconductor may react to form another dielectric material. For example, some or all of a layer of silicon dioxide may react with aluminium to form aluminium oxide.

Removing the surface oxide layer (or “native oxide layer”) may comprise using a wet etch. Removing the surface oxide layer may comprise using hydrogen fluoride. Removing the surface oxide layer may comprise using a dry etch.

25

The method may comprise loading or transferring the layer of silicon, germanium or silicon-germanium alloy (which may be supported on a substrate) into a deposition system after removing the surface oxide layer and before the surface oxide re-grows. The method may comprise loading or transferring the layer of silicon, germanium or silicon-germanium alloy into a deposition system after removing the surface oxide layer within 15 minutes or within 10 minutes.

30

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Heating the layer of silicon, germanium or silicon-germanium alloy may comprise heating the layer at a pressure no more than 10^{-6} mbar (10^{-4} Pa) or no more than 10^{-8} mbar (10^{-6} Pa). Heating the layer of silicon, germanium or silicon-germanium alloy may comprise heating the layer to at least 600 °C or at least 650 °C.

5

The superconductor may be aluminium. The superconductor may be selected from the group consisting of indium, molybdenum, niobium, tin, tantalum, titanium, vanadium and zinc.

10 The layer of silicon, germanium or silicon-germanium alloy may be degenerately doped. The layer may be doped n-type. The layer may be doped with phosphorus (P), arsenic (As) or antimony (Sb). The layer may be doped p-type. The layer may be doped to a concentration of at least $1 \times 10^{19} \text{cm}^{-3}$. The layer may be doped with a delta-doped layer. The layer of silicon, germanium or silicon-germanium alloy may be
15 strained.

The layer of silicon, germanium or silicon-germanium alloy may be a layer of silicon.

According to a second aspect of the present invention there is provided a
20 superconductor-insulator-semiconductor tunnel junction formed by the method.

According to a third aspect of the present invention there is provided a method of fabricating a device comprising the method of forming the superconductor-insulator-semiconductor tunnel junction.

25

According to a fourth aspect of the present invention there is provided a device formed by the method.

According to a fifth aspect of the present invention there is provided a superconductor-insulator-semiconductor junction wherein the semiconductor comprises silicon,
30 germanium or silicon-germanium alloy and the insulator comprises a layer of dielectric material. The tunnel junction exhibits a tunnel resistance which is less than $50 \text{ k}\Omega\mu\text{m}^2$ at a temperature which is at, or below, the transition temperature of the superconductor.

35

The tunnel junction may exhibit a tunnel resistance which is not more than $20 \text{ k}\Omega\mu\text{m}^2$ or not more than $10 \text{ k}\Omega\mu\text{m}^2$ at a temperature which is at, or below, the transition temperature of the superconductor.

5 A ratio of the density of states broadening factor for the junction without the dielectric layer and a broadening factor for the tunnel junction may be more than 10, or more than 100, or more than 1000 at a temperature which is at, or below, half of the transition temperature of the superconductor.

10 A broadening factor for the tunnel junction may be not more than 1×10^{-3} at a temperature which is at, or below, half of the transition temperature of the superconductor.

According to a sixth aspect of the present invention there is provided a superconductor-insulator-semiconductor tunnel junction wherein the semiconductor comprises silicon,
15 germanium or silicon-germanium alloy and the insulator comprises a layer of dielectric material. A ratio of a broadening factor for a tunnel junction without the dielectric layer and a broadening factor for the tunnel junction is more than 10, or more than 100, or more than 1000 at a temperature which is at, or below, half of the transition
20 temperature of the superconductor.

A broadening factor for the tunnel junction may be not more than 1×10^{-3} at a temperature which is at, or below, half of the transition temperature of the superconductor.

25

The dielectric material is or may comprise an oxide of silicon and/or an oxide of germanium. The dielectric material is or may comprise an oxide and/or nitride of the superconductor. The dielectric material is or may comprise a nitride of silicon and/or a nitride of germanium. The dielectric material is or may comprise a nitride of the
30 superconductor. The dielectric material is or may comprise an oxynitride of silicon or an oxynitride of germanium. The dielectric material is or may comprise an oxynitride of the superconductor.

The superconductor may be aluminium. The superconductor may be selected from the
35 group consisting of indium, molybdenum, niobium, tin, tantalum, titanium, vanadium

and zinc. The superconductor may be an elemental superconductor. The superconductor may be an alloy of elemental superconductors.

5 The dielectric layer may have a thickness no more than 5 nm, no more than 3 nm or no more than 2 nm.

According to a seventh aspect of the present invention there is provided a device comprising at least one tunnel junction.

10 The device may comprise two tunnel junctions arranged as superconductor-insulator-semiconductor-insulator-superconductor.

The device may be a bolometer or a thermometer.

15 According to an eighth aspect of the present invention there is provided an astronomical detection system comprising a tunnel junction or a device.

According to a ninth aspect of the present invention there is provided a biomedical imaging or detection system comprising a tunnel junction or a device.

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According to a tenth aspect of the present invention there is provided a security screening comprising a tunnel junction or a device.

25 According to an eleventh aspect of the present invention there is provided a remote sensing system comprising a tunnel junction or a device.

According to a twelfth aspect of the present invention there is provided a quantum information processing comprising a tunnel junction or a device.

Brief Description of the Drawings

Certain embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

- Figure 1 is an energy band diagram of a double junction superconductor-semiconductor-superconductor cooler;
- Figure 2 is a plot of density of states against energy for a superconductor-semiconductor junction;
- Figure 3 is a side view of superconductor-insulator-semiconductor junction;
- Figure 4 is a schematic block diagram of apparatus for forming the superconductor-insulator-semiconductor junction shown in Figure 3;
- Figure 5 is process flow diagram of a method of forming the superconductor-insulator-semiconductor junction shown in Figure 3;
- Figures 6a to 6e illustrate the superconductor-insulator-semiconductor junction at different stages during formation;
- Figure 7 shows plots of density of states broadening factor, Γ , against temperature for a semiconductor-superconductor junction and the junction shown in Figure 3;
- Figure 8 shows a plot of current against bias for the junction shown in Figure 3; and
- Figure 9 shows a plot of conductance against bias for the junction shown in Figure 3.

Detailed Description of Certain Embodiments

Referring to Figure 1, an energy diagram of a double junction superconductor-semiconductor-superconductor (S-Sm-S) cooler is shown which may be helpful for understanding the present invention.

- The cooler comprises a first superconductor in direct contact with a semiconductor resulting in a first Schottky barrier formed in the semiconductor at the interface with the first superconductor due to bending of the conduction band (CB) edge. The semiconductor is in direct contact with a second superconductor resulting in a second Schottky barrier at the interface with the second superconductor.

- A potential, V , applied between the superconductors is divided equally between the two junctions, which have equal tunnel resistance, R_T .

- As shown in Figure 1, electric current, I , flows from the first superconductor to the second superconductor, i.e. left to right. Hot electrons tunnel out of the semiconductor through the first (i.e. left-hand) junction and are replaced by cold electrons which enter

the semiconductor through the second (i.e. right-hand) junction. The current, I , is given by equation 1 below:

5

$$I = \frac{1}{2eR_T} \int_{-\infty}^{\infty} [f(E - eV/2, T_e) - f(E + eV/2, T_e)] g(E, \Gamma) dE. \quad (1)$$

where e is electron charge (1.6×10^{-19} C), R_T is the normal state tunnelling resistance, $f(E, T)$ is the Fermi-Dirac distribution function of electrons $f(E, T) = 1/[1 + \exp(E/k_B T)]$ and T_e is the electron temperature in the semiconductor. k_B is the Boltzmann constant (1.381×10^{-23} JK⁻¹) Reference is made to J. T. Muhonen et al.: "Micrometre-scale refrigerators", Reports on Progress in Physics, volume 75, page 046501 (2012), which is incorporated herein by reference.

15 The term $g(E, \Gamma)$ is the density of states within the superconductor and is given by equation 2 below:

$$g(E, \Gamma) = \left| \operatorname{Re} \left[\frac{E + i\Gamma}{\sqrt{(E + i\Gamma)^2 - \Delta^2}} \right] \right| \quad (2)$$

20

where E is energy of a state, Γ is the density of states broadening factor and Δ is half the superconducting energy gap, 2Δ . Reference is made to R. C. Dynes *et al.*: "Tunneling study of superconductivity near the metal-insulator transition", Physical Review Letters, volume 53, page 2437 (1984) and J. P. Pekola *et al.*: "Limitations in Cooling Electrons using Normal-Metal-Superconductor Tunnel Junctions", Physical Review Letters, volume 92, page 056804-1 (2012), which are incorporated herein by reference.

Equation 2 above helps explain the problem of sub-gap leakage.

30 Referring to Figure 2, a plot of density of states $g(E, \Gamma)$ against energy for different values of broadening factor (or "smoothing factor") is shown

Figure 2 shows that, as the Γ parameter is increased, the sub-gap density of states is increased and this increases the sub-gap proportion of the total junction current, as given by equation 1. Γ can be used as a figure of merit for semiconductor-superconductor tunnel junctions. Γ may not explicitly refer to the density of states of the superconductor, but may also quantify some other process, such as, a parallel leakage current through the junction.

The present invention is based on the insight that introducing an insulator (i.e. a dielectric layer) between a semiconductor and a superconductor reduces the Γ parameter by about two orders of magnitude in a semiconductor-superconductor junction. This helps to reduce the sub-gap leakage significantly thereby increasing, in the case of a cooler, the cooling efficiency of the junctions, and, in the case of a thermometer, sensitivity of the thermometer.

Referring to Figure 3, a semiconductor-insulator-superconductor junction 1 is shown which comprises a semiconductor 2, preferably silicon (Si), germanium (Ge) or silicon-germanium ($\text{Si}_{1-x}\text{Ge}_x$), a thin dielectric layer 3 in direct contact with the semiconductor 2 and a superconductor 4, such as aluminium (Al), in direct contact with the dielectric layer 3.

Integration of a thin insulating layer into the junction stack reduces the sub-gap leakage of the junction by at least an order of magnitude.

Referring also to Figure 4, the junction 1 is formed using an *in-situ* low-temperature, low-pressure oxidation process which is used to oxidise the surface of the semiconductor prior to depositing aluminium (as the superconductor) in an ultra-high vacuum sputter system 5. It is found that oxidation using a conventional silicon processing furnace or oxidation carried out at room temperature and low pressure does not reduce the sub-gap leakage.

Referring in particular to Figure 4, the vacuum sputter system 5 includes an exchange chamber 6 (or “load lock”), a first chamber 7 and a second chamber 8 separated by valves 9, 10, 11.

The exchange chamber 6 is evacuated using a turbo molecular pump 12 backed by a rotary pump (not shown).

The first chamber 7 houses a heater 13. A source 14 of pure, dry oxygen is connected to the first chamber 7 via a needle valve 15. The first chamber 7 is selectably evacuated using either a turbo molecular pump 16 backed by a rotary pump (not shown) or a
5 rotary pump 17.

In this case, a d.c. sputtering system is used. However, other forms of sputtering, e.g. r.f. sputtering or ion-beam sputtering, can be used.

10 The second chamber 8 houses a sputter target 18 (i.e. a source of superconducting material) which also serves as a cathode, an anode 19 and a power source 20 for applying biases to the cathode 18 and anode 19. An argon gas source 21 connected to the second chamber 8 via a needle valve 22. The second chamber 8 is evacuated using a turbo molecular pump 23 backed by a rotary pump (not shown).

15 As shown in Figure 4, a wafer (or “workpiece”) 25 is processed in the first and second chambers 7, 8.

Referring to Figures 4, 5 and 6a to 6e, a method of forming semiconductor-insulator-superconductor junction(s) will now be described.
20

The process starts with a degenerately doped silicon wafer 2' having a native oxide 26, as shown in Figure 6a.

25 The native oxide 26 removed by immersion in 1% hydrofluoric acid (HF) for 1 minute, followed by a rinse in deionised water and dry in nitrogen gas (step S1). The corresponding structure is shown in Figure 6b.

The stripped wafer 2' is placed in the load-lock 6 within 10 minutes of performing the oxide strip and is transferred to the first chamber 7 (step S2).
30

The pressure in the first chamber 7 is reduced to first pressure P_1 , about 10^{-8} mbar (10^{-6} Pa) (step S3), then the temperature is ramped to a first elevated temperature T_1 , 550 °C (step S4). The temperature and pressure are held for a period of time t_1 , 10 minutes
35 (step S5).

The temperature may be ramped up or down to a different temperature, T_2 , for oxidation (step S6). In this case, the temperature is maintained, i.e. $T_2=T_1$.

5 Chamber pumping is reduced via a high impedance line to the rotary vacuum pump 17 (step S7). Pure oxygen gas is admitted into the chamber 7 via a needle valve 15 and the pressure increased to a pressure P_2 , about 300 mbar (30,000 Pa) (step S8). A higher or lower oxidation pressure, P_2 , may be used. For example, the pressure may be between 200 mbar (20,000 Pa) and 400 mbar (40,000 Pa).

10 The pressure and temperature are maintained for a time t_2 , about 15 minutes (step S9), then the oxygen needle valve was closed (step S10), the high impedance pumping stopped, (step S11) and the turbo pump 16 used to reduce the pressure back to P_1 , i.e. around 10^{-8} mbar (10^{-6} Pa) (step S12).

15 As shown in Figures 6c and 6d, the process results in a surface region 27 of the silicon wafer 1' being oxidized to form a thin layer 28 of silicon dioxide (SiO_2).

Heating is stopped (step S13) and the chamber is allowed to cool to T_3 , about 90 °C (step S14). This can take approximately 2 hours.

20

The workpiece 25, i.e. the wafer 1 having a thin oxide 28 is moved, without breaking vacuum, to the second chamber 8 (step S15).

Referring to Figure 6e, a layer 4 of aluminium is d.c. sputtered, initially using a low
25 power (step S16 & S17).

The chamber is allowed to cool and the processed wafer is unloaded (step S18 & S19).

30 The dielectric layer 3 may comprise silicon dioxide. However, dielectric layer 3 may comprise aluminium oxide, i.e. resulting from a reaction between aluminium and silicon dioxide.

Referring to Figure 7, plots 31, 32 of density of states broadening factor, Γ , against temperature are shown.

35

A first plot 31 shows the temperature variation of the broadening factor, Γ , for the tunnel junction 1 is formed using an *in-situ* low-temperature, low-pressure oxidation process. A second plot 32 shows the temperature variation of the broadening factor, Γ , for a comparative example which is prepared in the same way, but without the *in-situ* low-temperature, low-pressure oxidation process.

Referring to Figures 8 and 9, the broadening factor, Γ , is found by obtaining a current-voltage (I-V) plot 33 and differentiating to obtain a conductance (dI/dV) plot 34.

The broadening factor, Γ is found by dividing the value of the mid-gap conductance by the value of the normal state conductance.

As shown in Figure 7, the *in-situ* low-temperature, low-pressure oxidation process has the effect of reducing the broadening factor, Γ .

Table 1 below shows values of tunnel resistance, R_T , and (where available) lowest electron temperature from a 300 mK bath for the tunnel junction structure.

Table 1

	Tunnel resistance ($\text{k}\Omega\mu\text{m}^2$)	Cooling power at 300 mK (mWm^{-2})	Gamma leakage parameter	Lowest electron temperature from 300 mK bath (mK)
Comparative example 1	10	70	1.5×10^{-2}	260
Comparative example 2	100	7	1×10^{-2}	175
Junction 1	42	26	1×10^{-3}	90
Comparative example 3	8,500	-	-	-

Comparative example 1 is a semiconductor-superconductor junction which is formed using a layer of unstrained silicon by stripping the native oxide and depositing aluminium directly on the silicon surface, i.e. without a silicon dioxide layer.

Comparative example 2 is a semiconductor-superconductor junction which is the same as comparative example 1, but strained silicon is used instead of unstrained silicon

Comparative example 3 is a semiconductor-insulator-superconductor junction which is formed using a layer of strained silicon by stripping the native oxide, forming a layer of

silicon dioxide on the silicon by dry oxidation in a furnace at atmospheric pressure and at 700 °C for 5 minutes and then loading the sample into the deposition system 5 (Figure 4) and depositing aluminium on the furnace-grown silicon dioxide layer.

5 Table 1 shows that junction 1, using the same material as comparative example 2 and an *in-situ* low-temperature, low-pressure oxidation process either reduces or at least does not increase tunnel resistance, while providing improved cooling power. When compared to comparative example 1, it should be noted that the electron-phonon conductance is much higher in that sample (which uses unstrained silicon) which can
10 explain the high cooling power, but smaller change in temperature.

Table 1 also shows that junction 1 exhibits improved cooling (namely from 300 mK to 90 mK).

15 When comparing tunnel resistances and cooling powers in Table 1, it can be seen that tunnel resistance is reduced from 100 kΩ to 42 kΩ using an *in-situ* low-temperature, low-pressure oxidation process. This alone implies an improvement in the cooling power by a factor of about 2.4. However, an improvement by a factor of 3.7 at 300 mK is observed. This is because of the improved gamma factor of the junction. Also, lower
20 gamma gives a slower decrease in cooling power as electron temperature is reduced.

The process may be explained as follows:

The hydrofluoric acid step removes the native oxide 26 and terminates the surface
25 silicon atoms with hydrogen (not shown). Once loaded into the high vacuum chamber, the temperature is ramped to 550 °C with the aim of driving off the hydrogen terminations. A higher temperature, for example 600 °C, 650 °C or more, can be used. This leaves a highly-reactive surface and so an oxide quickly forms when oxygen is introduced into the chamber 8. It is believed that oxidation quickly self-limits and
30 stops after a given period of time, i.e. a few minutes. The resulting silicon dioxide layer 28 has a thickness of no more than a few nanometres. Although the silicon dioxide layer 28 is expected to be stable, it is possible that the aluminium reacts to form aluminium dioxide. Regardless, a thin dielectric layer 3 is formed which is responsible for the superior performance the junction 1.

The resistance of the junction 1 can be quite low, i.e. about $1 \text{ k}\Omega\mu\text{m}^2$. Therefore, it is believed that oxidation of silicon pushes back dopants (i.e. away from the surface) forming a local high dopant concentration and this helps to reduce the tunnel barrier width.

5

Alternatively or additionally, there might be some de-pinning of the Fermi level at the interface which reduces the height of the tunnel barrier.

10

Alternatively or additionally, oxidation may occur more strongly at or around the sites of the dopants on and/or close to the semiconductor surface. These sites can be the origin of the sub-gap leakage and so oxidation may result in deactivation of the sites locally. A continuous thin oxide may be formed and the n-type dopant atoms at the surface are pushed into the silicon and/or deactivated inside the oxide. It is energetically more favourable for n-type dopants, such as arsenic and phosphorous P, to be in silicon than in silicon dioxide. This can result in an extremely highly doped, thin region next to the silicon dioxide-silicon interface.

15

Alternatively or additionally, the oxide layer formed between the semiconductor and the superconductor is believed to reduce proximity effects associated with a degenerately-doped semiconductor. A proximity effect is observed when a thin layer of normal metal, in close contact with a superconductor, becomes superconducting. Conversely, a superconductor can be turned normal (this is referred to as the “the inverse proximity effect”). In the case of superconductor-semiconductor junction, there may be a proximity effect between a degenerately-doped semiconductor and the superconductor, wherein states appear in the superconductor bandgap. Thus, it is believed that the formation of the oxide layer may result in a reduction of the proximity effect, thereby improving the superconductor density of states.

20

25

Although a process based on silicon, oxidation and aluminium has been described, the process can be varied as follows:

30

Aluminium need not be used as a superconductor. Instead, another elemental superconductor such as indium (In), molybdenum (Mo), niobium (Nb), tin (Sn), tantalum (Ta), titanium (Ti), vanadium (V), zinc (Zn) or other low-temperature superconductor. Thus, the dielectric layer 3 may comprise an oxide of the elemental superconductor.

35

Additionally or alternatively, oxidation need not be used. Nitridation or a mixture of oxidation and nitridation (or other sacrificial-based reaction of the semiconductor) may be used. Thus, the dielectric layer 3 may comprise silicon nitride or silicon oxynitride and/or a nitride or oxynitride of aluminium or other elemental superconductor.

Silicon need not be used. Instead, the semiconductor may be germanium (Ge). Thus, the dielectric layer 3 may comprise germanium oxide, germanium nitride, germanium oxynitride. The semiconductor may be silicon-germanium (SiGe).

10

The semiconductor need not be in the form of a wafer, but may be a layer, for example, an epitaxial layer. The layer may form part of homostructure or a heterostructure, for example, a layer of silicon or germanium formed on a layer of silicon-germanium.

15 The semiconductor may be formed in a structure which includes a buried oxide, for example silicon-on-insulator.

The semiconductor need not be n-type. Instead, it can be p-type.

20 The semiconductor need not be unstrained, but can be strained, for example, using process-induced strain or by virtue of a heterostructure which includes a layer of a different semiconductor having a different lattice constant and/or crystal structure.

A device, such as a cooler or thermometer, may include two or more junctions, for example, such as a superconductor-insulator-semiconductor-insulator-superconductor structure.

25

Claims

1. A method of forming a superconductor-insulator-semiconductor tunnel junction, the method comprising:
 - 5 removing a surface oxide layer from a surface of a layer of silicon, germanium or silicon-germanium alloy;
 - heating the layer of silicon, germanium or silicon-germanium alloy to at least 550 °C in a vacuum;
 - forming a dielectric layer on the surface of the layer of silicon, germanium or
 - 10 silicon-germanium alloy; and
 - depositing a superconductor on the dielectric layer.
2. A method according to claim 1, wherein forming the dielectric layer comprises exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to
- 15 one or more chemical species.
3. A method according to claim 1 or 2, wherein forming the dielectric layer comprises exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to a gas.
- 20 4. A method according to any preceding claim, wherein forming the dielectric layer comprises exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to a mixture of gases or to a sequence of gases and/or gas mixtures.
- 25 5. A method according to any preceding claim, wherein forming the dielectric layer comprises exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to oxygen.
6. A method according to any preceding claim, wherein forming the dielectric layer
- 30 comprises exposing the surface of the layer of silicon, germanium or silicon-germanium alloy to nitrogen.
7. A method according to any one of claims 2 to 6, comprising exposing the surface for a time of at least 1 minute, at least 2 minutes, at least 5 minutes or at least 10
- 35 minutes.

8. A method according to any one of claims 2 to 7, comprising exposing the surface for a time no more than 2 hours, no more than 1 hour or no more than 0.5 hours
9. A method according to any preceding claim, wherein forming the dielectric layer
5 is carried out at a pressure below atmospheric pressure.
10. A method according to any preceding claim, wherein forming the dielectric layer is carried out at a pressure between 200 mbar (20,000 Pa) and 400 mbar (40,000 Pa).
- 10 11. A method according to any preceding claim, wherein forming the dielectric layer is carried out at a temperature above room temperature.
12. A method according to any preceding claim, wherein forming the dielectric layer is carried out at a temperature at or above 500 °C.
- 15 13. A method according to any preceding claim, wherein at least a portion of the dielectric layer and a portion of the superconductor react to form another dielectric material.
- 20 14. A method according to any preceding claim, wherein removing the surface oxide layer comprises using a wet etch.
15. A method according to any preceding claim, wherein removing the surface oxide layer comprises using hydrogen fluoride.
- 25 16. A method according to any preceding, comprising loading or transferring the layer of silicon, germanium or silicon-germanium alloy into a deposition system after removing the surface oxide layer and before the surface oxide re-grows.
- 30 17. A method according to any preceding claim, wherein heating the layer of silicon, germanium or silicon-germanium alloy comprises heating the layer at a pressure no more than 10^{-6} mbar (10^{-4} Pa).
- 35 18. A method according to any preceding claim, wherein heating the layer of silicon, germanium or silicon-germanium alloy comprises heating the layer at a pressure no more than 10^{-8} mbar (10^{-6} Pa).

19. A method according to any preceding claim, wherein heating the layer of silicon, germanium or silicon-germanium alloy comprises heating the layer to at least 600 °C or at least 650 °C.

5

20. A method according to any one of claims 1 to 19, wherein the superconductor comprises aluminium.

21. A method according to any one of claims 1 to 19, wherein the superconductor is
10 selected from the group consisting of indium, molybdenum, niobium, tin, tantalum, titanium, vanadium and zinc.

22. A method according to any preceding claim, wherein the layer of silicon, germanium or silicon-germanium alloy is degenerately doped.

15

23. A method according to any preceding claim, wherein the layer of silicon, germanium or silicon-germanium alloy is strained.

24. A method of fabricating a device comprising a method of forming a
20 superconductor-insulator-semiconductor tunnel junction according to any preceding claim.

25. A method according to any preceding claim, wherein the layer of silicon, germanium or silicon-germanium alloy is a layer of silicon.

25

26. A tunnel junction formed by a method according to any one of claims 1 to 25.

27. A device formed by a method according to claim 26.

30 28. A superconductor-insulator-semiconductor tunnel junction wherein the semiconductor comprises silicon, germanium or silicon-germanium alloy and the insulator comprises a layer of dielectric material, wherein the tunnel junction exhibits a tunnel resistance less than 50 kΩμm² at a temperature which is at, or below, the transition temperature of the superconductor.

35

29. A tunnel junction according to claim 28, which exhibits a tunnel resistance no more than $10 \text{ k}\Omega\mu\text{m}^2$ at a temperature which is at or below the transition temperature of the superconductor.

5

30. A tunnel junction according to claim 28 or 29, wherein a ratio of broadening factor for a tunnel junction without the dielectric layer and a broadening factor for the tunnel junction is more than 10, or more than 100, or more than 1000 at a temperature which is at, or below, half of the transition temperature of the superconductor.

10

31. A tunnel junction according to claim 28, 29 or 30, wherein a broadening factor for the tunnel junction is no more than 1×10^{-3} at a temperature which is at, or below, half of the transition temperature of the superconductor.

15

32. A superconductor-insulator-semiconductor tunnel junction wherein the semiconductor comprises silicon, germanium or silicon-germanium alloy and the insulator comprises a layer of dielectric material, wherein a ratio of a broadening factor for a tunnel junction without the dielectric layer and a broadening factor for the tunnel junction is more than 10, or more than 100, or more than 1000 at a temperature which is at, or below, half of the transition temperature of the superconductor.

20

33. A tunnel junction according to claim 32, a broadening factor for the tunnel junction is no more than 1×10^{-3} at a temperature which is at, or below, half of the transition temperature of the superconductor.

25

34. A tunnel junction according to any one of claims 28 to 33, wherein the dielectric material is or comprises an oxide of silicon and/or an oxide of germanium.

35. A tunnel junction according to any one of claims 28 to 34, wherein the dielectric material is or comprises an oxide the superconductor.

30

36. A tunnel junction according to any one of claims 28 to 35, wherein the dielectric material is or comprises a nitride of silicon and/or a nitride of germanium.

37. A tunnel junction according to any one of claims 28 to 36, wherein the dielectric material is or comprises a nitride of the superconductor.

35

38. A tunnel junction according to any one of claims 28 to 37, wherein the dielectric material is or comprises an oxynitride of silicon and/or an oxynitride germanium.

5 39. A tunnel junction according to any one of claims 28 to 38, wherein the dielectric material is or comprises an oxynitride of the superconductor.

40. A tunnel junction according to any one of claims 28 to 39, wherein the superconductor is or comprises aluminium.

10

41. A tunnel junction according to any one of claims 28 to 39, wherein the superconductor is an elemental superconductor, such as indium, molybdenum, niobium, tin, tantalum, titanium, vanadium or zinc.

15 42. A tunnel junction according to any one of claims 28 to 41, wherein the dielectric layer has a thickness no more than 5 nm.

43. A tunnel junction according to any one of claims 28 to 42, wherein the dielectric layer has a thickness no more than 3 nm.

20

44. A tunnel junction according to any one of claims 28 to 43, wherein the dielectric layer has a thickness no more than 2 nm.

25 45. A device comprising at least one tunnel junction according to any one of claims 28 to 44.

46. A device according to claim 45 comprising two tunnel junctions according to any preceding claim arranged as superconductor-insulator-semiconductor-insulator-superconductor.

30

47. A device according to claim 45 or 46, which is a bolometer.

48. A device according to claim 45 or 46, which is a thermometer.

49. An astronomical detection and imaging system comprising one or more tunnel junctions according to claim 26 or any one of claims 28 to 44 or a device according to claim 27 or any one of claims 45 to 48.

5 50. A biomedical imaging or detection system comprising one or more tunnel junctions according to claim 26 or any one of claims 28 to 44 or a device according to claim 27 or any one of claims 45 to 48.

10 51. A security screening system comprising one or more tunnel junctions according to claim 26 or any one of claims 28 to 44 or a device according to claim 27 or any one of claims 45 to 48.

15 52. A remote sensing system comprising one or more tunnel junctions according to claim 26 or any one of claims 28 to 44 or a device according to claim 27 or any one of claims 45 to 48.

53. A quantum information processing system comprising one or more tunnel junctions according to claim 26 or any one of claims 28 to 44 or a device according to claim 27 or any one of claims 45 to 48.

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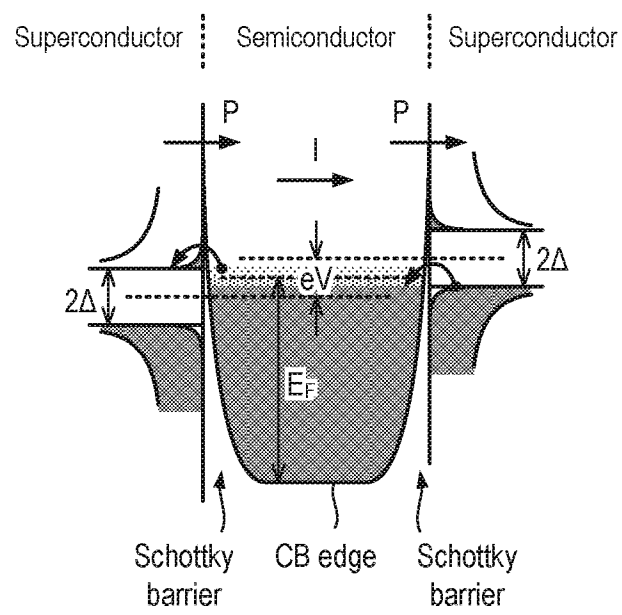


Fig. 1

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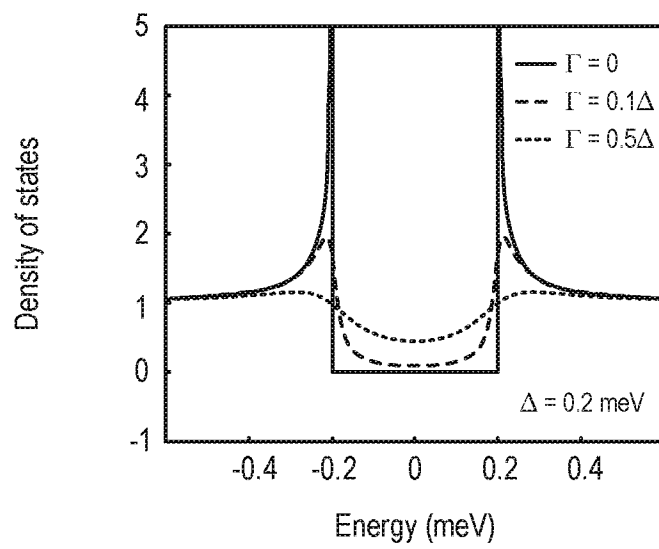


Fig. 2

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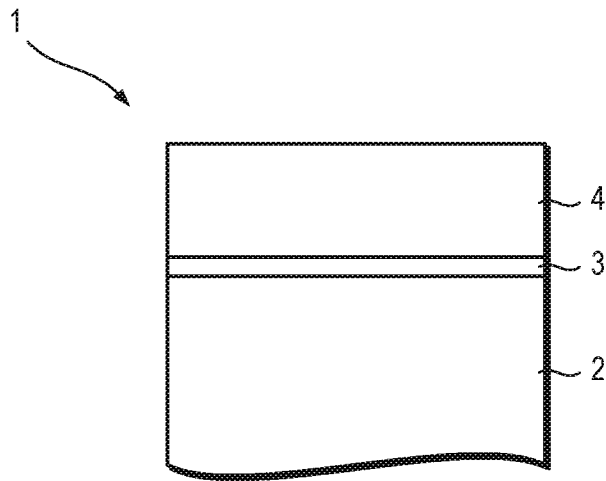


Fig. 3

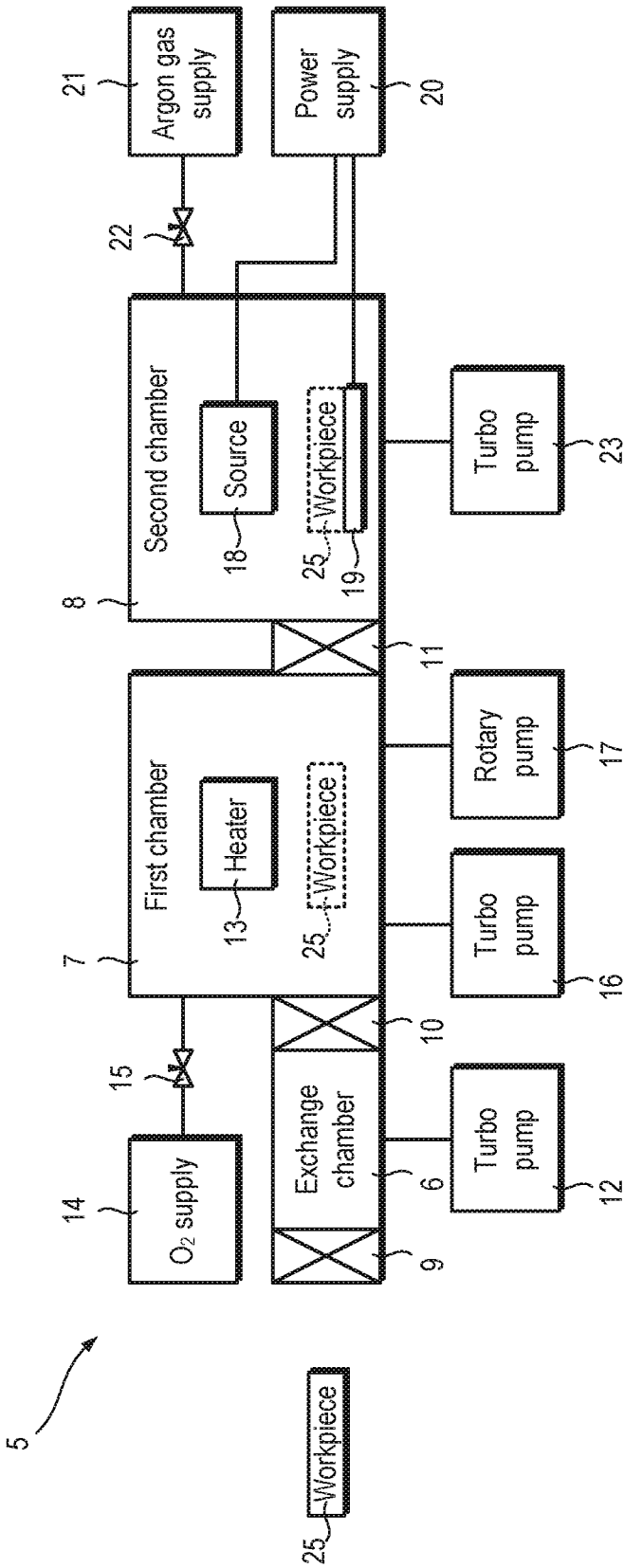


Fig. 4

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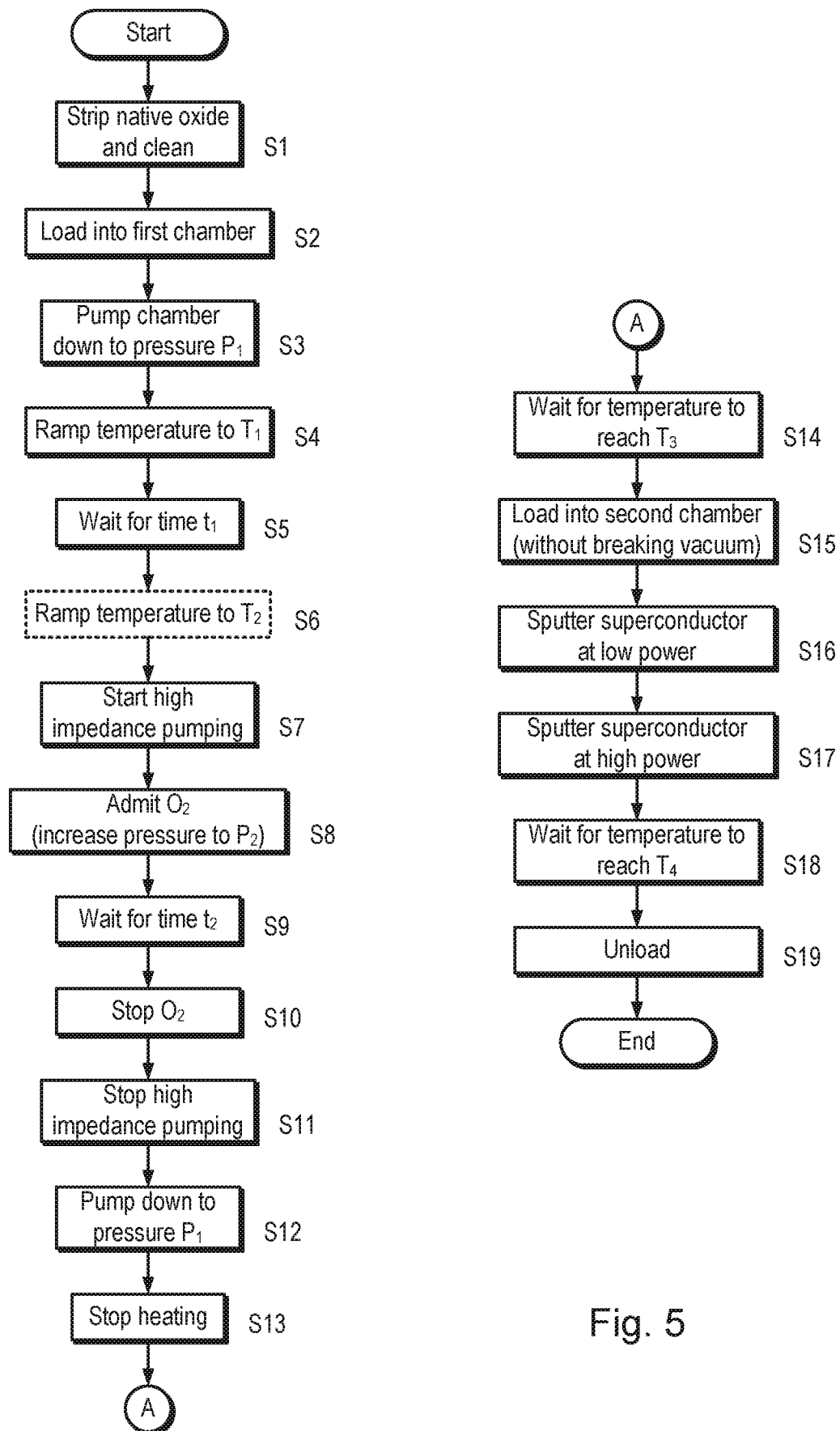


Fig. 5

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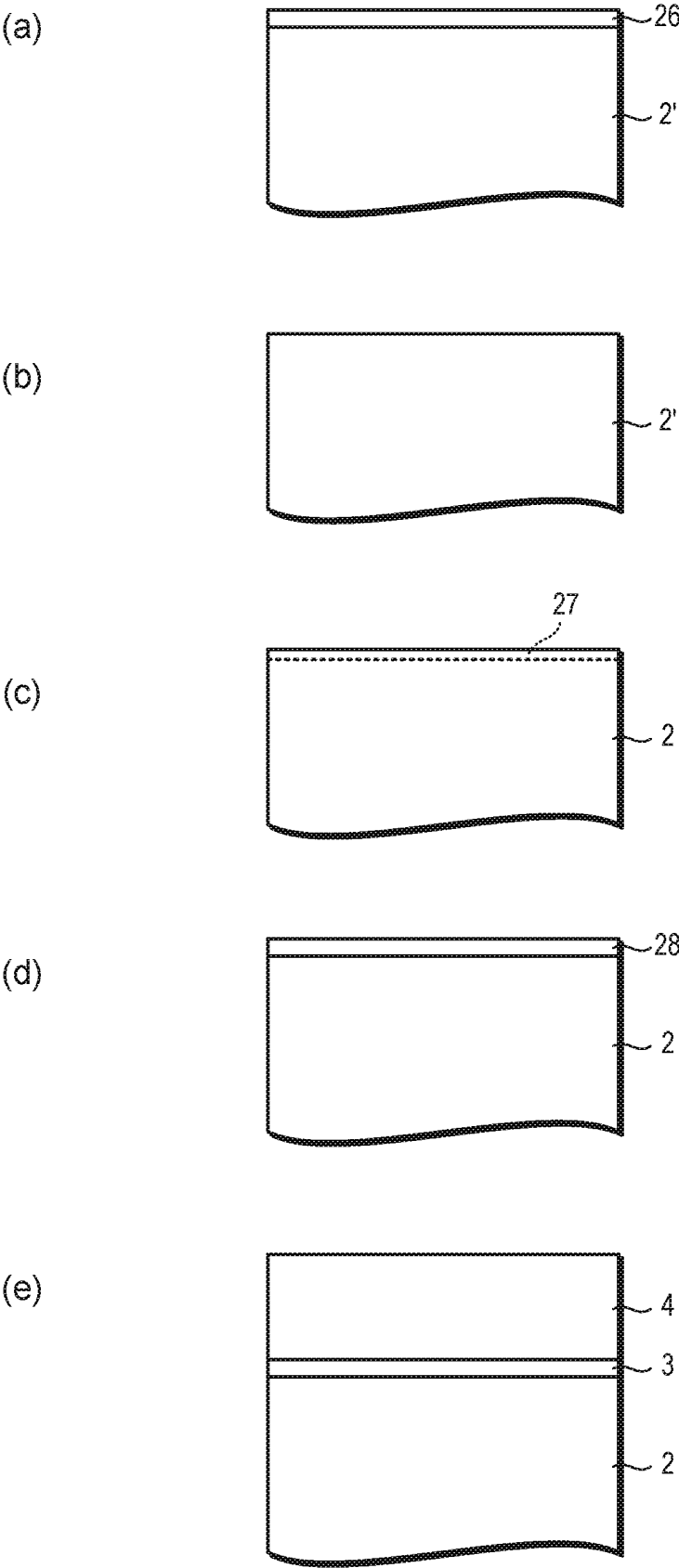


Fig. 6

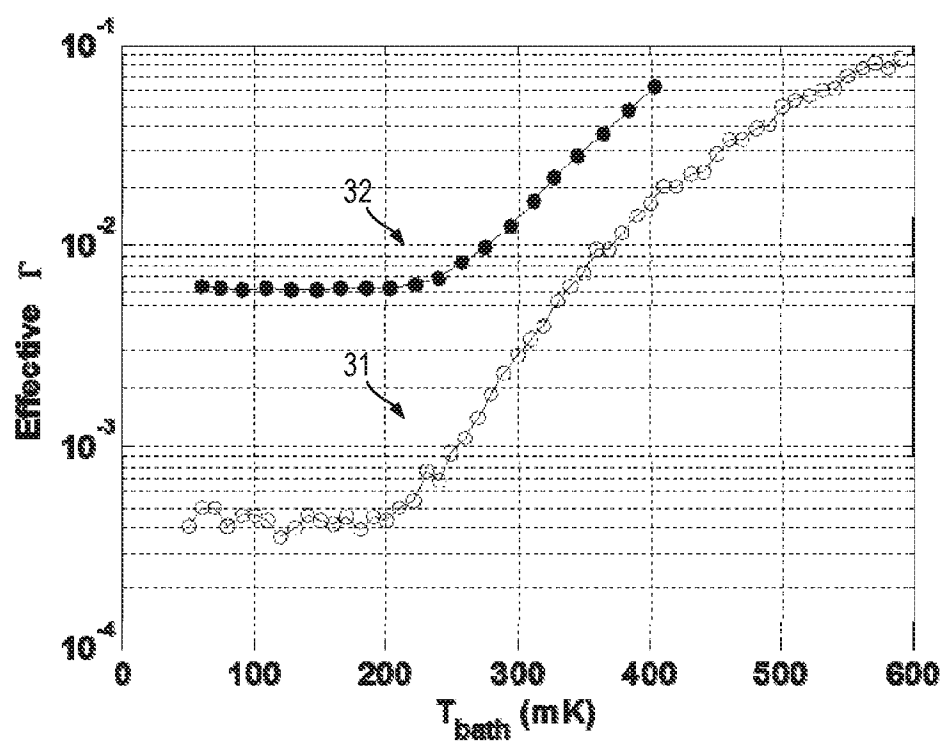


Fig. 7

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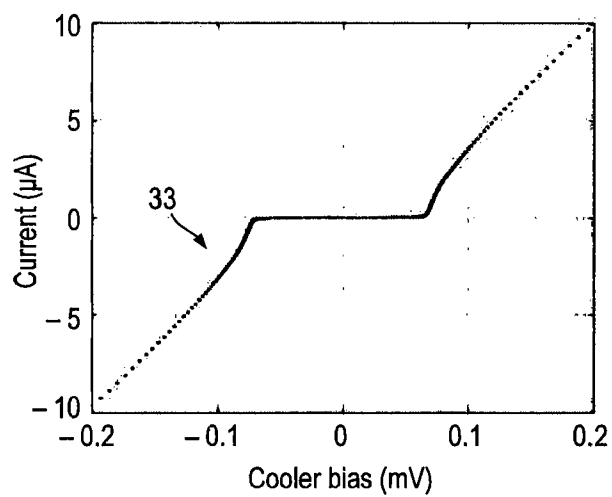


Fig. 8

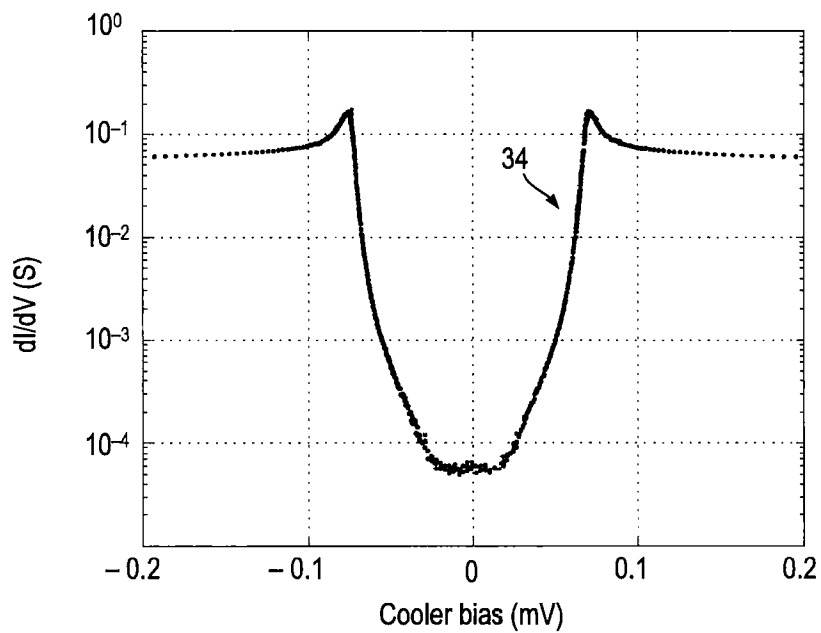


Fig. 9

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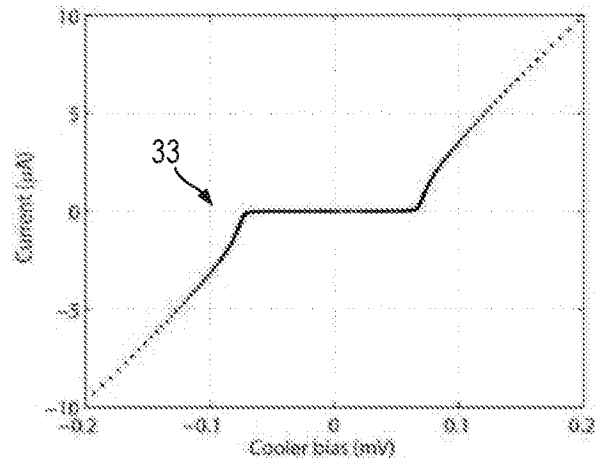


Fig. 8

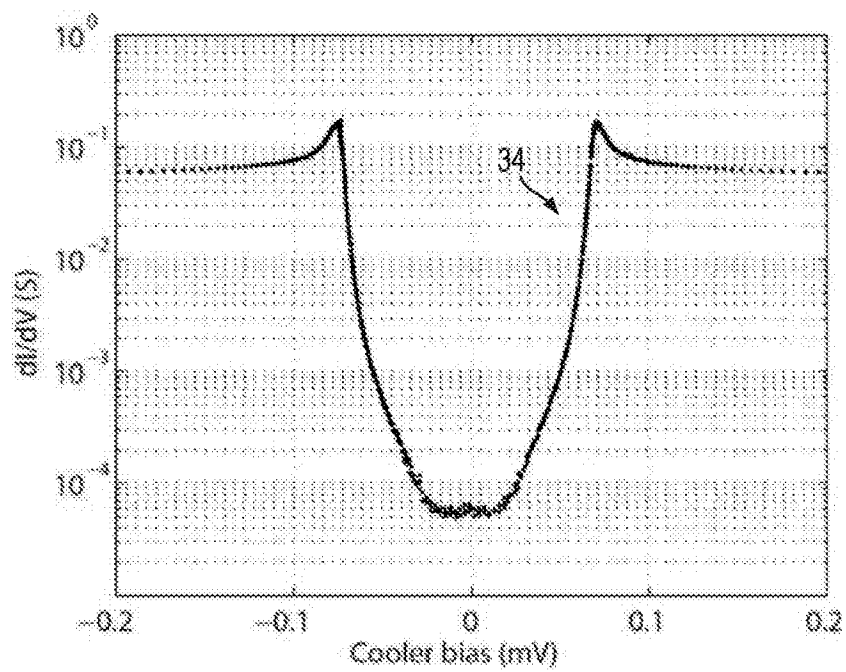


Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2014/053275

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L39/22 B01L7/00 H01L21/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L B01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99/66567 A1 (ISIS INNOVATION [GB]; BOOTH NORMAN EWART [GB]; ULLOM JOEL NATHAN [US];) 23 December 1999 (1999-12-23)	26-53
Y	figures 1,4,11 page 9, line 13 - page 10, line 4 page 24, line 1 - page 26, line 2 page 30, line 3 - line 22 page 36, line 1 - page 43, line 5 -----	1-25
Y	EP 0 196 155 A2 (STC PLC [GB]) 1 October 1986 (1986-10-01) page 2, line 10 - page 3, line 9 ----- -/-	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

16 January 2015

Date of mailing of the international search report

26/01/2015

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Gröger, Andreas

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2014/053275

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SAVIN A M ET AL: "Efficient electronic cooling in heavily doped silicon by quasiparticle tunneling", APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS, US, vol. 79, no. 10, 3 September 2001 (2001-09-03), pages 1471-1473, XP012028802, ISSN: 0003-6951, DOI: 10.1063/1.1399313 cited in the application figure 1 -----	1-53

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2014/053275

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			EP 1095412 A1 02-05-2001
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