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DYNAMIC REDUNDANCY METHOD FOR AN AUTOMATED LOGIC MAPPING SYSTEM

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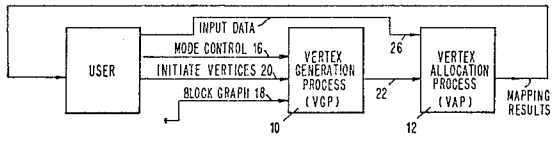
U.S. Cl. 444—1
8 Sheets Drawings. 36 Pages of Specification



An automated circuit design system and process are provided including a technique for introducing redundancy of circuit element groups during the allocation of the circuit element groups to modules. The redundancy technique, which is embodied as a computer algorithm, functions when the allocation of redoundable element such as a circuit element group is made to a container module such as a circuit chip, during a discrete step allocation procedure which is designed to produce a mapping of a set of connected circuit elements. A minimum condition for obtaining a successful mapping is that each element can be allocated to at least one module. The operation of the process is made redundant to reduce the number of elements by one, namely the allocated element. The consequence of the operation is that the connected elements said to be fed by the redundant element (referred to as sink elements) are each combined by union with the redundant element. Other concomitant results of the operation are that the connections previously required between the redundant element and its sink elements will not be needed should any of the sink elements be allocated to different modules, and each sink element has acquired the attributes of the redundant element.

FIG. 1

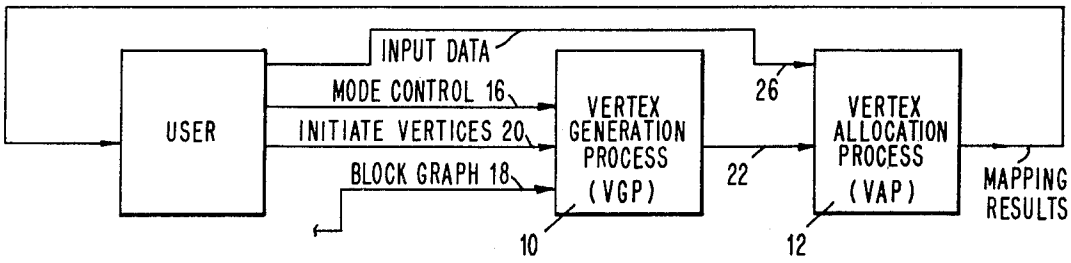


FIG. 4

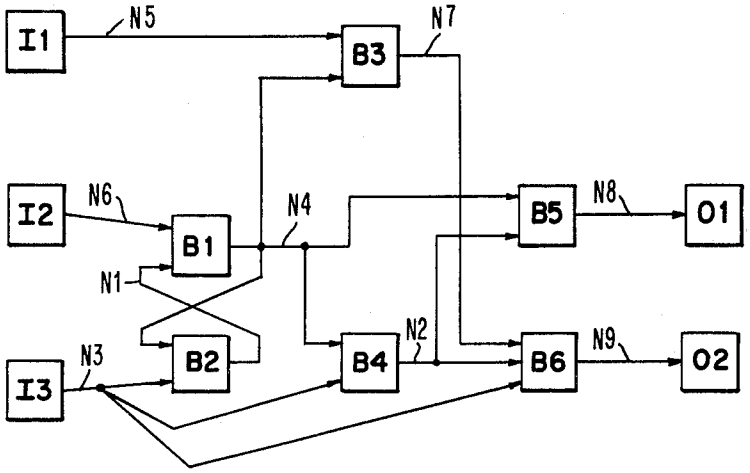


FIG. 4A

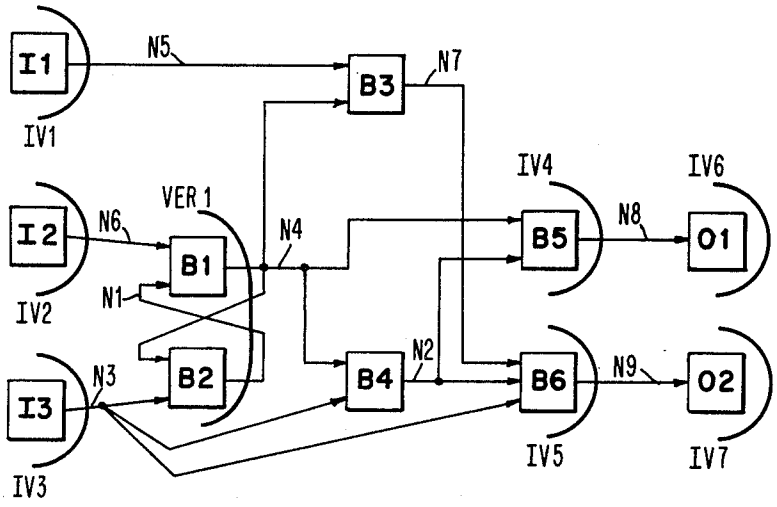


FIG. 2A

VERTEX GENERATION PROCESS (VGP)

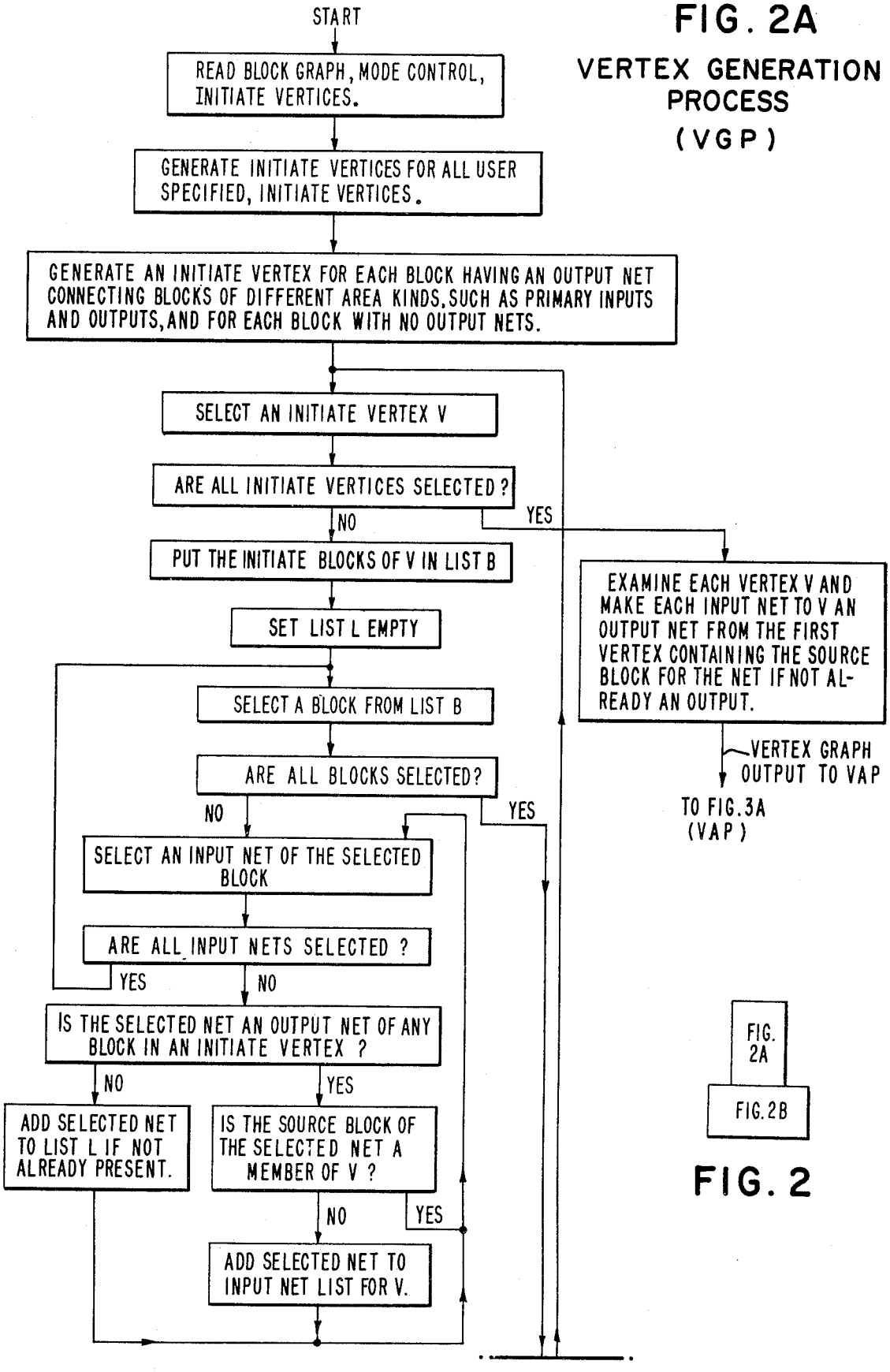


FIG. 2

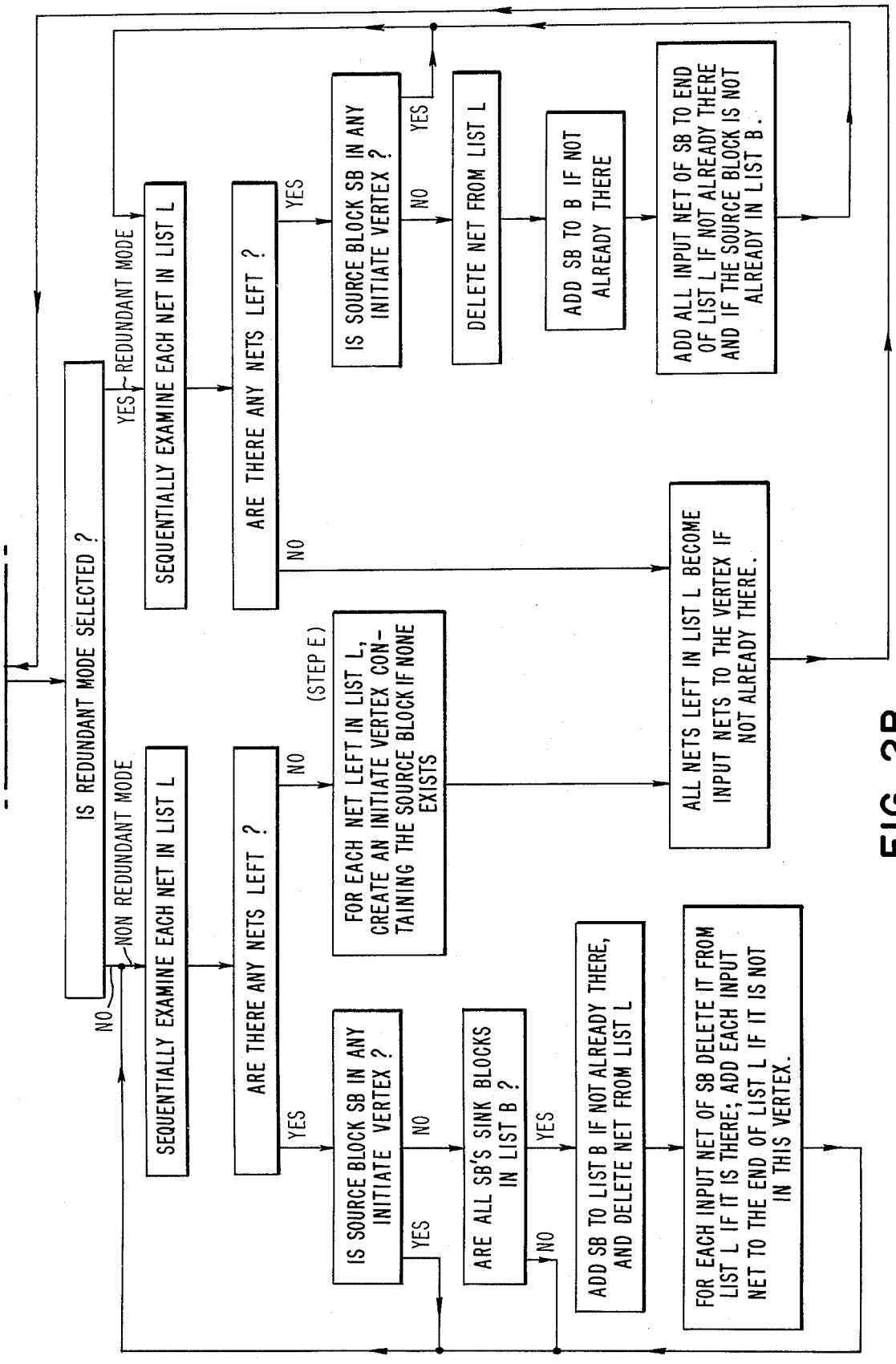

IS REDUNDANT MODE SELECTED ?
NON REDUNDANT MODE
YES
NO
REDUNDANT MODE
SEQUENTIALLY EXAMINE EACH NET IN LIST L
ARE THERE ANY NETS LEFT ?
YES
NO
IS SOURCE BLOCK SB IN ANY INITIATE VERTEX ?
YES
NO
DELETE NET FROM LIST L
ADD SB TO B IF NOT ALREADY THERE
ADD ALL INPUT NET OF SB TO END OF LIST L IF NOT ALREADY THERE AND IF THE SOURCE BLOCK IS NOT ALREADY IN LIST B.
SEQUENTIALLY EXAMINE EACH NET IN LIST L
ARE THERE ANY NETS LEFT ?
YES
NO
(STEP E)
FOR EACH NET LEFT IN LIST L, CREATE AN INITIATE VERTEX CONTAINING THE SOURCE BLOCK IF NONE EXISTS
ALL NETS LEFT IN LIST L BECOME INPUT NETS TO THE VERTEX IF NOT ALREADY THERE.
IS SOURCE BLOCK SB IN ANY INITIATE VERTEX ?
YES
NO
ARE ALL SB'S SINK BLOCKS IN LIST B ?
YES
NO
ADD SB TO LIST B IF NOT ALREADY THERE, AND DELETE NET FROM LIST L
FOR EACH INPUT NET OF SB DELETE IT FROM LIST L IF IT IS THERE; ADD EACH INPUT NET TO THE END OF LIST L IF IT IS NOT IN THIS VERTEX.

FIG. 2B

FIG. 3

FIG. 3A
FIG. 3B
FIG. 3C

FIG. 3A
VERTEX ALLOCATION PROCESS (VAP)

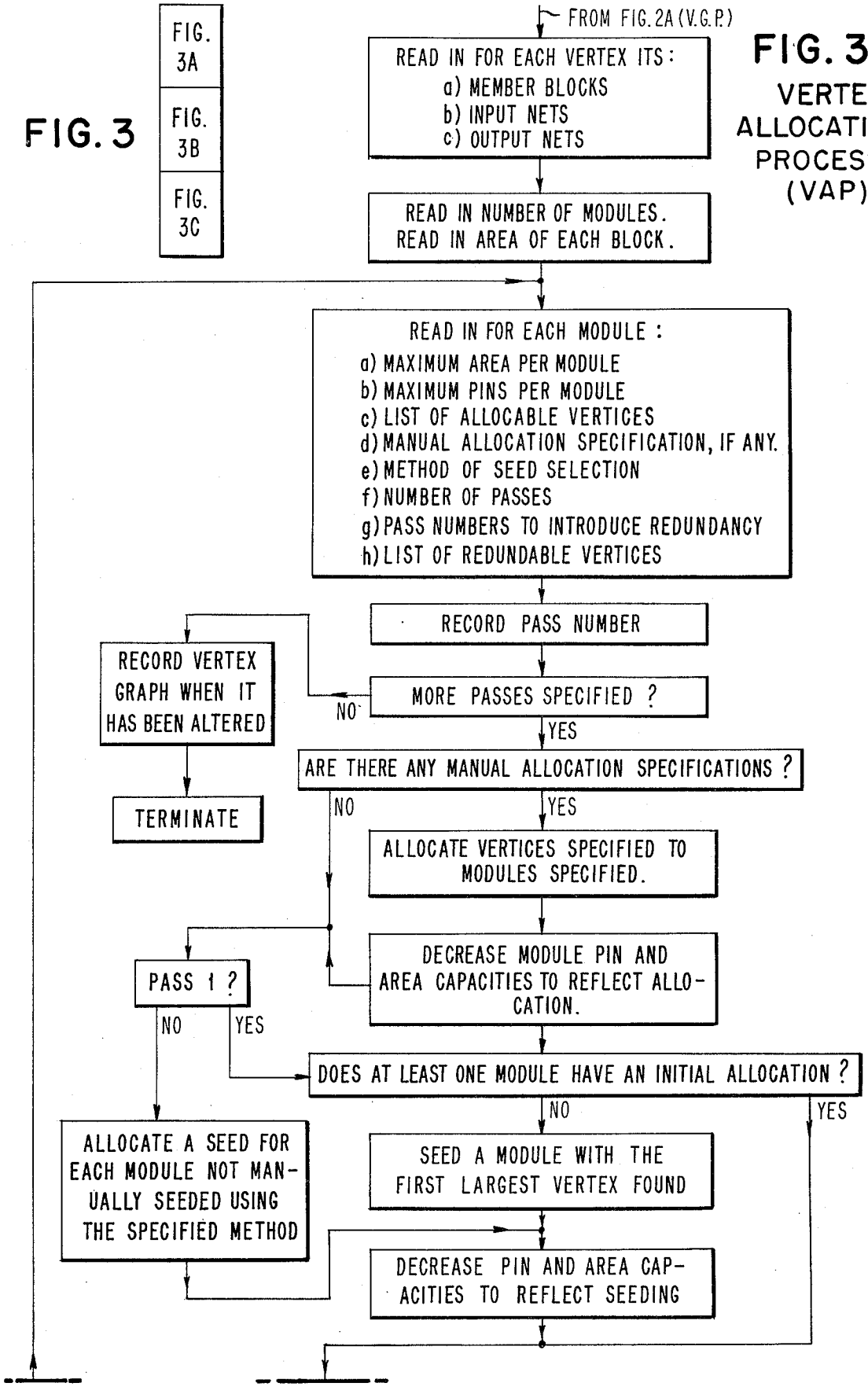


FIG. 3B

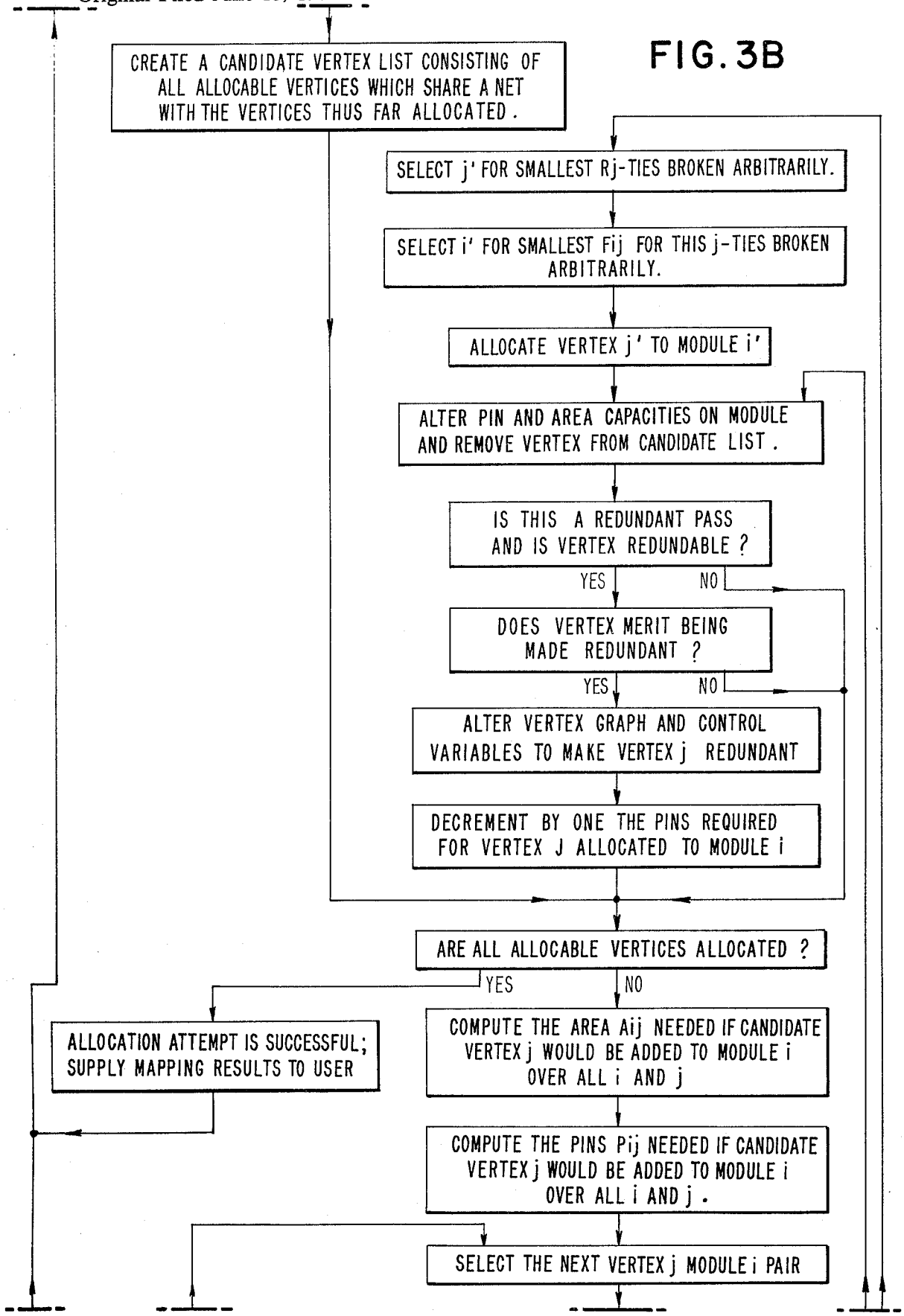

CREATE A CANDIDATE VERTEX LIST CONSISTING OF ALL ALLOCABLE VERTICES WHICH SHARE A NET WITH THE VERTICES THUS FAR ALLOCATED .
SELECT j' FOR SMALLEST Rj-TIES BROKEN ARBITRARILY.
SELECT i' FOR SMALLEST Fij FOR THIS j-TIES BROKEN ARBITRARILY.
ALLOCATE VERTEX j' TO MODULE i'
ALTER PIN AND AREA CAPACITIES ON MODULE AND REMOVE VERTEX FROM CANDIDATE LIST .
IS THIS A REDUNDANT PASS AND IS VERTEX REDUNDABLE ?
YES
NO
DOES VERTEX MERIT BEING MADE REDUNDANT ?
YES
NO
ALTER VERTEX GRAPH AND CONTROL VARIABLES TO MAKE VERTEX j REDUNDANT
DECREMENT BY ONE THE PINS REQUIRED FOR VERTEX J ALLOCATED TO MODULE i
ARE ALL ALLOCABLE VERTICES ALLOCATED ?
YES
NO
ALLOCATION ATTEMPT IS SUCCESSFUL; SUPPLY MAPPING RESULTS TO USER
COMPUTE THE AREA Aij NEEDED IF CANDIDATE VERTEX j WOULD BE ADDED TO MODULE i OVER ALL i AND j
COMPUTE THE PINS Pij NEEDED IF CANDIDATE VERTEX j WOULD BE ADDED TO MODULE i OVER ALL i AND j .
SELECT THE NEXT VERTEX j MODULE i PAIR

FIG.3C

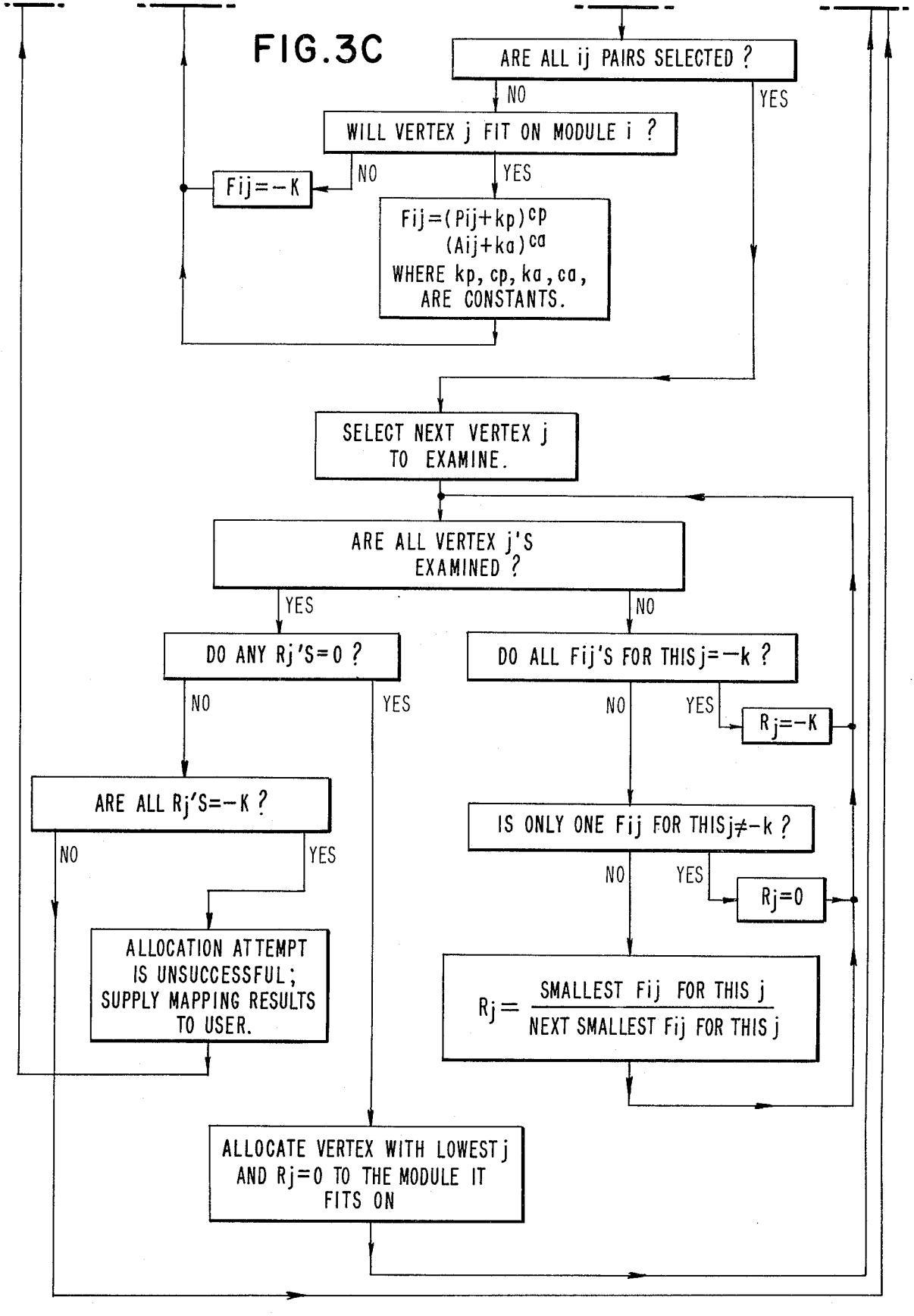

ARE ALL ij PAIRS SELECTED ?
NO
YES
WILL VERTEX j FIT ON MODULE i ?
NO
YES
Fij=-K
Fij=(Pij+kp)^cp (Aij+ka)^ca WHERE kp, cp, ka, ca, ARE CONSTANTS.
SELECT NEXT VERTEX j TO EXAMINE.
ARE ALL VERTEX j'S EXAMINED ?
YES
NO
DO ANY Rj'S=0 ?
DO ALL Fij'S FOR THIS j=-k ?
NO
YES
NO
YES
Rj=-K
ARE ALL Rj'S=-K ?
IS ONLY ONE Fij FOR THIS j≠-k ?
NO
YES
NO
YES
Rj=0
ALLOCATION ATTEMPT IS UNSUCCESSFUL; SUPPLY MAPPING RESULTS TO USER.
Rj = SMALLEST Fij FOR THIS j / NEXT SMALLEST Fij FOR THIS j
ALLOCATE VERTEX WITH LOWEST j AND Rj=0 TO THE MODULE IT FITS ON

FIG. 5

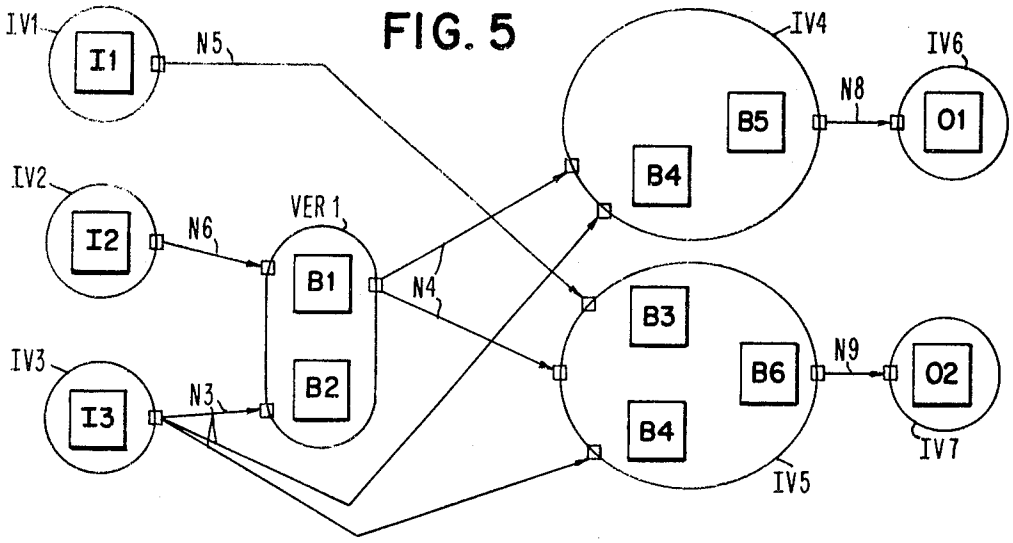


FIG. 6

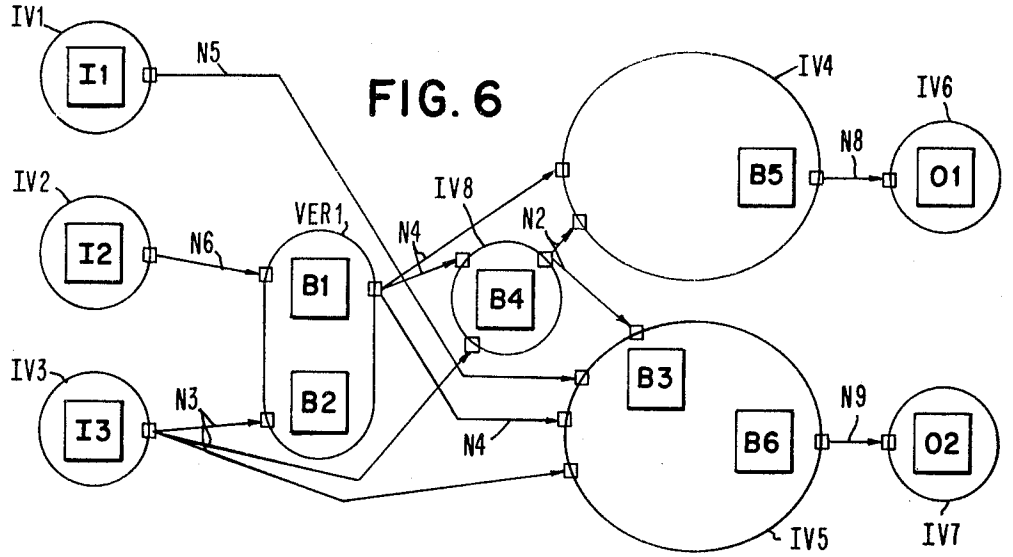
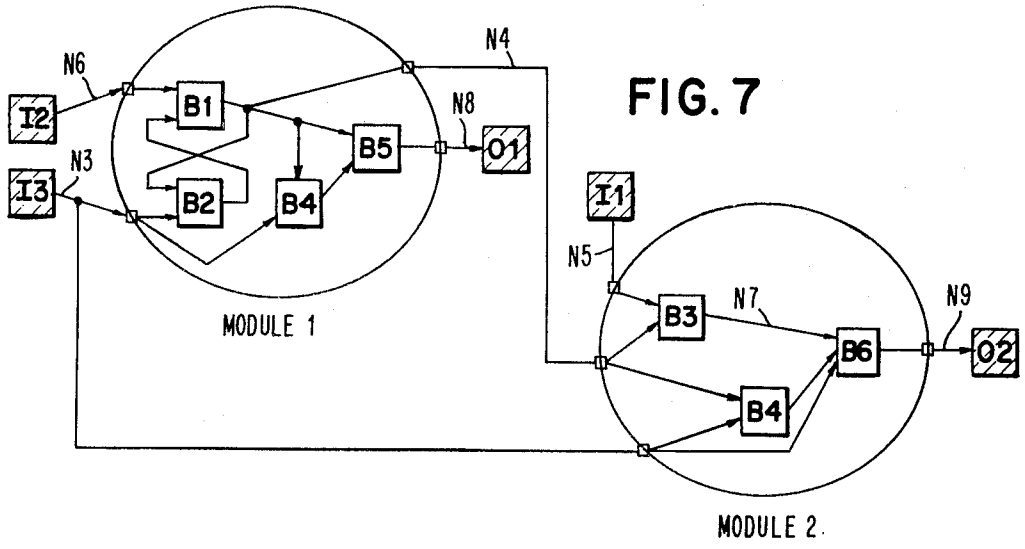


FIG. 7



	AREA	PINS
MODULE 1	2	1
MODULE 2	4	4

FIG. 8

	VER1	IV5	
MODULE 1	1	2	PINS Pij
MODULE 2	3	4	

FIG. 9

	VER1	IV5	
MODULE 1	2	2	AREA Aij
MODULE 2	2	3	

FIG. 10

	VER1	IV5	
MODULE 1	132	-K	Fij
MODULE 2	156	182	

FIG. 11A

VER1	IV5	
132	144	Fij
156	182	

FIG. 11B

	VER1	IV5
R	$\frac{132}{156}$	0

FIG. 12A

	VER 1	IV5
R	$\frac{132}{156} \approx .85$	$\frac{144}{182} \approx .78$

FIG. 12B