



(51) International Patent Classification:
H01L 23/62 (2006.01)

(21) International Application Number:
PCT/US2015/037762

(22) International Filing Date:
25 June 2015 (25.06.2015)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: TONG, Xiaohong; 2501 NW 229th Street, Hillsboro, Oregon 97229 (US). HAFEZ, Walid M.; 4060 NW Carlton Ct., Portland, Oregon 97229 (US). MA, Zhiyong; 2501 NW 229th Street, Hillsboro, Ohio 97124 (US). BAI, Peng; 2501 NW 229th Avenue, Hillsboro, Oregon 97124 (US). JAN, Chia-Hong; 12849 NW Lorraine Dr., Portland, Oregon 97229 (US). CHEN, Zhanping; 4745 NW 138th Place, Portland, Oregon 97229 (US).

(74) Agents: LINDEEN, Gordon et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

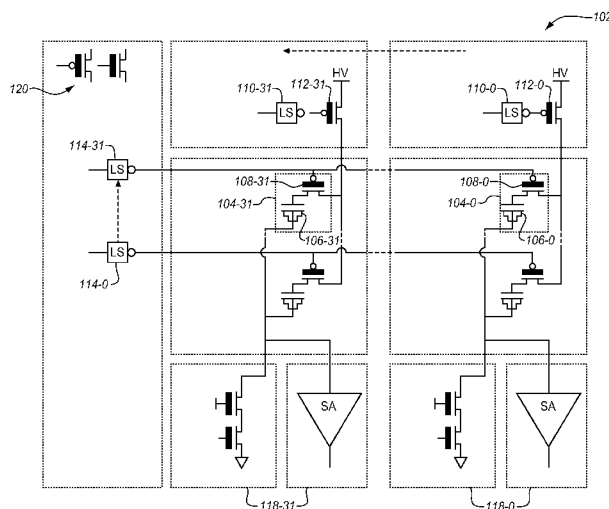
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: CONTROLLED MODIFICATION OF ANTIFUSE PROGRAMMING VOLTAGE

FIG. 1



(57) Abstract: The controlled modification of an antifuse programming voltage is described. In one example, an antifuse circuit is formed on a substrate, including a gate area of the antifuse circuit. A molecule is implanted into the gate area to damage the structure of the gate area. Electrodes are formed over the gate areas to connect the antifuse circuit to other components.

CONTROLLED MODIFICATION OF ANTIFUSE PROGRAMMING VOLTAGE

FIELD

The present description relates to antifuse circuits in semiconductor electronics and in particular to modifying the programming voltage of such a circuit.

BACKGROUND

Metal fuse and antifuse elements are used for a wide range of different electronic devices. One common use is in non-volatile memory arrays. They are also used in processors to set parameter and register values or to set codes, serial numbers, encryption keys and other values that are not to be changed later. Fuse and antifuse elements are used in bipolar, FinFET, and CMOS (Complementary Metal Oxide Semiconductor) device technologies, among others.

As an example, programmable memory devices such as PROM (programmable read-only memory) and OTPROM (one-time programmable read-only memory) are typically programmed by either destroying links (via a fuse) or creating links (via an antifuse) within the memory circuit. In PROMs, for instance, each memory location or bitcell contains a fuse and/or an antifuse, and is programmed by triggering one of the two. The programming is usually done after manufacturing of the memory device, and with a particular end-use or application in mind. Once conventional bitcell programming is performed, it is generally irreversible.

Fuse links are commonly implemented with resistive fuse elements that can be open-circuited or "blown" by applying an unusually high-current on an appropriate line. Antifuse links, on the other hand, are typically implemented with a thin barrier layer of non-conducting material (such as silicon dioxide) between two conducting layers or terminals. When a sufficiently high voltage is applied across the terminals, the silicon dioxide is damaged eliminating the barrier so that there is a low resistance conductive path between the two terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements. Figure 1 is a circuit diagram of a portion of an antifuse bit cell memory array according to an embodiment.

Figures 2-12 are side cross-sectional view diagrams of a first sequence of fabrication stages for an antifuse device with a modified programming voltage according to an embodiment.

Figures 13-19 are side cross-sectional view diagrams of a second sequence of fabrication stages for an antifuse device with a modified programming voltage according to an embodiment. Figure 20 is a block diagram of a computing device incorporating a tested semiconductor die according to an embodiment.

5

DETAILED DESCRIPTION

One use of anti-fuse technology is for one-time-programmable (OTP) memory arrays. These are typically constructed using polysilicon fuses, metal fuses, and oxide antifuses. Polysilicon and metal fuse arrays traditionally have larger footprints than oxide antifuse arrays, in part due to the large current required to fuse the element. Oxide antifuses rely on an oxide layer between conductive electrodes to form the fusing element. The oxide layer could be gate oxide in a MOS device. The electrodes could be the gate and the silicon substrate. For the MOS antifuse element, a diffusion layer is used for the source and drain regions, and a gate is formed on top of the diffusion layer and insulated from the diffusion layer by an oxide layer. The programming voltage breaks down the oxide insulation layer.

A driver circuit is used to program an antifuse circuit. The higher the programming voltage, the larger and more expensive the driver circuit may be. If there are many antifuse circuits, then the ease of programming is an important factor for the antifuse circuit design. A lower antifuse programming voltage has a simpler circuit design, lower manufacturing cost, reduced collateral damage in use, and may also allow in-field programming. The ability to lower the oxide breakdown voltage of antifuse elements relative to the devices used in the rest of the circuit also helps simplify the design, lower the cost and increase the reliability of the overall circuit.

The programming voltage of an antifuse circuit depends on the gate oxide breakdown voltage. Different circuit technologies may require different voltages. Metal gate and high K metal oxide antifuse circuits typically require a higher voltage than polysilicon gates that use silicon dioxide as the gate dielectric for the same technology node generation.

As described herein, an implant process may be used to lower the gate dielectric breakdown voltage for a high K metal gate oxide, a regular gate oxide, or any other gate dielectric material. The implant may be applied with other areas of a device masked so that the implant only affects the high K metal gate oxide of a fuse element. This provides a lower voltage antifuse programming circuit with less cost and complexity.

By implanting heavy molecules through and into a high K metal gate oxide the breakdown voltage on an antifuse circuit is lowered. A masking layer may be used to protect

other elements of the circuit. In this way, the antifuse elements have a lower breakdown voltage and the protected surrounding normal high K metal gates are not affected. This implanting is simpler and easier to control than changing the basic structure of the high K gate oxide or antifuse circuit.

5 Figure 1 is a simplified diagram of a portion of an antifuse circuit array 102. The array includes many devices, most of which are fabricated using conventional designs. Some of the devices relating to the antifuse functions are manufactured with gates with thick gate oxide 120 (Thick Gates) to handle high voltage. These devices are shown differently in the drawing figure as indicated by a special thick gate devices graphic legend 120. In the illustrated example, the
10 array has thirty-two antifuse cells 104-31 to 104-0, although only two cells are shown. There may be more or fewer cells than shown. The array may be part of a die specifically for antifuse cells or the array may be integrated into another system. Each cell 104 has an antifuse switch 106-31... 106-0 and a high voltage fuse signal driver 108-31... 108-0. Upon receiving an appropriate fuse signal, the driver 108 drives a high voltage through the gate of the antifuse
15 switch 106 to program the antifuse cell. By programming some antifuse cells and not others a sequence of zeros and ones may be programmed across an array to store identification numbers, encryption keys, operational parameters and other values.

 The cells of the array are accessed for programming using a column line selector 110-31... 110-0 for each column of the array and a row line selector 114-31... 114-0 for each row of
20 the array. Each column selector 110 is coupled to a high voltage line driver 112-31... 112-0 to send a high voltage on the selected line to an appropriate cell 104. Combining the column selection 110 and the row selection 114, a single cell 104 of the array may be selected for programming. As shown, the column selectors are coupled to the source of each cell's fuse voltage driver and the row selectors are coupled to the gate of each cell's fuse driver. When the
25 high voltage is applied to a source and the gate is opened, then the high voltage is driven through the gate oxide of the antifuse switch 106 to program the circuit.

 While the driver circuits operate at a high voltage, the rest of the system operates on a Vcc or Vss voltage 118-31... 118-0. This voltage is applied to the gates and sources of the antifuse cells 106 to read the value that was programmed into the cell. The high voltage circuit
30 is used for all of the antifuse programming and this uses devices at each cell and also on the column select for each column. The higher the programming voltage, the higher the requirement for the circuit to be able to handle the high voltage needed for the programming. Higher voltages require higher cost and higher complexity for the circuit design. Lowering the antifuse programming voltage reduces these costs.

Figures 2-12 are cross-sectional side view diagrams of a sequence of processing stages in a fabrication sequence for production of an antifuse circuit with a lowered programming voltage. Figure 2 is a first cross-sectional side view diagram of a process stage in a first fabrication sequence for production of an antifuse circuit with a lower programming voltage. Initially a substrate 202 is used. The substrate may be a silicon wafer upon which many dies are formed or the substrate may have a different size and be formed of a different material. In the illustrated example, two transistors are formed in the substrate as an example to show fabrication stages. Typically an array of transistors will be formed in the same substrate together with read, write, and programming circuits. Additional logic and memory circuits may also be formed in the substrate.

Figure 3 shows the substrate 202 of Figure 2 after an n-well 204 has been formed on one side. An n-type MOS transistor or NMOS transistor will be formed on this side, the right side, while a PMOS transistor will be formed on the left side. The material of the substrate forms a p-well for the left side transistor. Note that the process described here is different from normal MOS device formation. Normally a PMOS transistor would be formed in the n-well and a NMOS transistor would be formed in the p-well for a regular CMOS circuit and this process may also be used for antifuse element formation.

Figure 4 shows the addition of shallow trench isolation (STI) areas 206 on either side of the n-well. A third STI area 206 is formed on the left side of the n-well to define boundaries for the p-well. These areas may be added using photolithography, for example, by masking some areas, removing, depositing or implanting materials in the exposed areas and then removing the photoresist mask.

Figure 5 shows the substrate 202 with regular gate oxide (e.g., SiO₂ and variations) 208 deposited over the substrate and then a layer of polysilicon 210 deposited over the gate oxide. The Polysilicon layer is patterned using, for example, a dry etch so that the layers remain only where high k metal gate oxides and metal gates later will be. A nitride spacer 212 is then formed around each polysilicon gate with regular oxide next to the locations where the S/D (Source/Drain) implants will be.

Figure 6, shows the substrate 202 after forming source and drain areas 216 on both sides of the PMOS gate oxide and spacers by implantation. During this process the NMOS areas are all covered with an implant mask. At the stage shown in Figure 6, a new implant mask 214 has been formed and patterned to cover the PMOS areas.

An implantation 220 is then applied to the exposed NMOS areas to form the source and drain areas 224 for the NMOS device. As with the PMOS areas these are formed by masking the

other areas and then implanting an appropriate dopant. The structure has then been annealed to form conductive S/D contact areas 216 over the S/D areas for PMOS and contact areas 224 over the S/D of NMOS. Salicidation areas 218 and 222 are optionally formed to complete the source and drain implants on top of S/D areas of 216 and 224.

5 Figure 7 shows an ILD (Inter-Layer Dielectric) layer 230 deposited over the entire structure. This layer is then polished to expose the top of the polysilicon 210. In Figure 8, the polysilicon 210 and oxide 208 are removed from the gate areas. These have been used in the formation of the S/D areas and are optimized for the implantation process of Figure 6 but are not used later. In the illustrated example, the polysilicon gate and regular oxide layers have served
10 to protect the channel areas under the gate during the doping processes, as well as defining the metal gate position for the following process steps. The ILD 230 remains over the rest of the structure. The ILD may be SiO₂ or variations of it with different dopants or nitrides.

 In Figure 9, a high k metal oxide layer 232 is blanket deposited over the entire structure. This prepares the structure for the large molecule implant 234 of Figure 10. Areas outside of the
15 antifuse devices are covered with a protective layer such as photo resist so that only the antifuse elements are exposed for the implant 234. In Figure 10, the device is then implanted 234 with a heavy ion or molecule. In one example SiF₄ is used as the implant molecule. However a variety of other materials may be used instead, such as argon and nitrogen. The channel material may be formed of Si, Ge, II-V or any other semiconductor materials. This implantation modifies the
20 programming voltage for the antifuse circuitry by damaging the underlying structure. The programming voltage is lower than before the implant and allows the programming drivers to be built at lower cost and to be operated with less power.

 The implant process provides enough energy to penetrate the gate metal oxide 232, if present, and damage the metal gates. In this case, the gate areas of the eventual antifuse circuits
25 are defined by the high k metal oxide 232 that has been deposited between the spacers. The momentum of the implant particles (mass times velocity) determines the amount of damage that is done. The particles are driven so that they are not able to significantly penetrate the areas protected by the top protective ILD layer 230. As a result, only the gates are damaged. The gates are damaged enough to still operate but to have a lower breakdown voltage.

30 In the illustrated example, the metal gate oxides 232 are directly exposed to the implant 234. The polysilicon 210 applied earlier has been removed. However, this is not required. The polysilicon or another material may be used to provide an additional control over the effect of the implant process. The temperature, energy, molecule selection and other factors may be used to control the effect of the implant. These control factors may also be combined with an

additional layer in the gate (not shown) and the thickness and type of such a gate cover to more precisely control the effect of the implant. The described implant process is effective with high K metal gates to reduce the programming voltage. However, it may also be applied to other types of gates as mentioned above.

5 The heavy ion implantation may be performed in different ways. A plasma immersion ion implantation system may be used with SiF_4 at 4-6 keV to drive the ions into an electrostatically charged wafer. This may be followed by a short high temperature anneal for a few minutes at a temperature of 900°C or more.

10 In Figure 11, the gates are formed. After the implant process 234, new metal gate materials 242, 246 are applied for both types of transistors. Different metals with different work functions may be used for the n-type and p-type transistors. These may be performed by first masking all but one type of gate, depositing the desired material, then masking all but the other type of gate and depositing the other desired material. In this way different materials may be deposited. In addition, new metal gate contacts 244, 246 are applied over the gate dielectrics.
15 The gate metal layers and the high k metal oxide layer are then polished to remove the excess metals and leaving them only inside the metal gates.

 In Figure 12, an inter-layer dielectric layer 250 is formed over the entire structure and then polished. Electrodes 252 may be formed over the S/D contacts and electrodes 254 may be formed over the gate contacts. These may be formed, for example, by using a dry etch through
20 the ILD, followed by metal deposition of the etched areas, and then a polish to remove the excess metal. The electrodes may be used later to supply a breakdown voltage to program the antifuse circuit. Figure 12 shows a finished n-type and p-type antifuse transistor suitable for use in the array of Figure 1. There may be many such antifuse elements to form multiple arrays. The same principles may be applied to make other antifuse devices other than transistors. The devices may
25 be finished with additional layers for isolation, new circuitry devices, connections between devices etc. Interlayer dielectric layers and covers of various kinds may be applied as well depending on the other components to be formed on the die and the intended use of the device. The programming voltage necessary to break down the gate (the breakdown voltage) is determined by the gate oxide breakdown voltage for the particular antifuse element. For a high
30 K metal gate with a metal oxide dielectric, the breakdown voltage is typically higher than for a SiO_2 oxide gate. At the same time, the leakage current is lower for a high K metal gate. When a sufficiently high voltage is applied to the gate, the high electrical field breaks down at least a part of the gate oxide layer over the transistor channel and causes a conductive path to be formed through the oxide between the gate electrode and the underlying channel.

In addition to breaking through the gate material, some of the gate material may be transferred into the channel. This is in part caused by the heat generated by the discharge that breaks through the gate metal. The materials transfer and heat may fuse the metal gate and the silicon substrate together causing the gate of the programmed fuse bits to short to the substrate or channel of the device.

The gate oxide is weakened by the defects caused by the implant process. Implanting foreign materials into the gate oxide induces defects in the oxide. The weakened oxide has a lower breakdown voltage but it still has a low leakage current before breakdown. A SiF_4 implant as described herein may be used to reduce the breakdown voltage by as much as one third. As an example, the breakdown voltage may be 3V without using the implant operation and 2V after the implant operation. Thin metal gate oxide NMOS and PMOS structures show similar results.

The process of Figures 2-12 is shown as an example only. The implant may be applied to a variety of different structures made from a variety of different materials. The implant may be done at different times in the process other than that shown. The implant process may be applied to any metal or polysilicon gate fabrication process and to other types of antifuse circuits. By adjusting the oxide layers and adjusting the parameters of the implant process, the programming voltage may be controlled. Different amounts of implant may be used to obtain different programming voltages. For a system with different antifuse circuit structures, the implant process may be used to adjust the different types of antifuse circuits to fuse with the same or a similar programming voltage. Alternatively similar antifuse circuits may be implanted differently so that they have different programming voltages even with the same structure. The fabrication process examples are presented as planar CMOS devices on a silicon substrate. However the implant technique may also be applied to other types of antifuse structures such as FinFET and 3D transistor structures. In some cases, the implant may be driven at an angle to the top of the wafer so that the molecules strike a gate that has a vertical orientation.

Figures 13-19 are cross-sectional side view diagrams of an alternative sequence of processing stages in a second fabrication sequence for production of an antifuse circuit with a lowered programming voltage. In Figures 2-12 the gate was formed last, that is after the source and drain areas are formed. In this second fabrication sequence of Figures 13-19, the gates are formed first, that is before the source and drain areas are formed.

In Figure 13, a substrate 302 is used. The substrate may be silicon, or any other suitable material for forming semiconductor circuitry. Figure 14 shows the substrate 302 of Figure 13 after an n-well 304 has been formed on one side. Any number of wells may be formed, in this example only one well is formed for an n-well on the right and a p-well for the left side

transistor. Figure 15 shows the addition of shallow trench isolation (STI) areas 306 on either side of both wells. Thus there are three STI areas 306 on each side of both wells and a shared one between the wells.

Figure 16 shows the substrate 302 with the deposition of an oxide layer 308 over the entire surface of the structure. This may be a regular oxide or a high k metal oxide. Metal gates 310, 312 may be deposited for high k metal gate structures. Two different metals may be used with two different work functions, one for the n-type areas and a different one for the p-type areas, depending on the particular implementation. The metals are then covered in a polysilicon layer 314. For a polysilicon gate with a regular oxide, the polysilicon could be directly deposited on the oxide without the metal layers. The gate structures may be formed by patterning a mask layer and then etching away the poly and the metal layer underneath. This leaves the poly and metal stack, if present, only in the locations of the eventual gates that will be formed on the substrate. This leaves the gate oxide covering the gate areas and the metal oxide (or regular oxide) covering all of the other areas. The gate oxide together with the different work function metals, if present, and the polysilicon define the gate areas. The gate areas are the areas underneath and including the polysilicon 314.

In Figure 17, the device is then implanted 316 with a heavy ion or molecule, such as SiF₄, Argon and Nitrogen at an angle. This implant process is similar to that described for the first fabrication process with one important difference. This implant process damages primarily the corners of the metal gates 310, 312 to lower the breakdown voltage specifically in those areas. This is due to the angled implant that allows penetration of the heavy ions or molecules through the corners of the polysilicon and the metal layer where it is thin enough to penetrate by the implant ions at an angle. It also leaves impurities in the S/D areas beside the gates and in the channel under the gate. In the illustrated example, the gate oxide in the middle of the metal gates is not directly exposed to the implant 316 because of the additional polysilicon 314. The polysilicon moderates the effect of the implant on the gate oxide and other gate layers. Other layers may also be used to control the effect of the implant. After the implant process, metal gate oxide (or regular gate oxide) materials at corners of 314 are changed by the process and now have the lower breakdown voltage.

In Figure 18, the base oxide layer 308 is removed from all of the structure except for under the gates. The base oxide is protected by the metal gates 310, 312 and the polysilicon. Spacers 320, such as silicon nitride spacers, are optionally formed surrounding each gate.

Figure 19 shows the substrate 302 after depositing source and drain areas 332 for the NMOS device. These are formed by a patterned implant operation 324 with a suitable dopant.

A mask layer 322 protects one type of structure while the other one is implanted. The process is repeated for the other devices with a mask over the implanted structures. Metal contact layers 334 are formed by annealing the source and drain areas of both devices to allow for external connections to the devices. Salicidation areas are optionally formed on either side of the well 304.

Figure 20 shows that a protective layer 326 such as a dielectric oxide or ILD is applied over the entire surface of the substrate then polished to a flat surface. Vias may be etched to the gates 314. Electrodes 330 may then be formed over the gate contacts by filing the vias.

Additional electrodes are formed over the S/D areas 332. The antifuse devices are finished.

However, additional layers may be added to provide additional devices, routing, redistribution and other functions. Additional interlayer dielectric layers and covers may also be applied.

These devices may be used for all of the applications and configurations for which the devices of Figure 12 may be used.

Figure 21 illustrates a computing device 11 in accordance with one implementation. The computing device 11 houses a board 2. The board 2 may include a number of components, including but not limited to a processor 4 and at least one communication chip 6. The processor 4 is physically and electrically coupled to the board 2. In some implementations the at least one communication chip 6 is also physically and electrically coupled to the board 2. In further implementations, the communication chip 6 is part of the processor 4.

Depending on its applications, computing device 11 may include other components that may or may not be physically and electrically coupled to the board 2. These other components include, but are not limited to, volatile memory (e.g., DRAM) 8, non-volatile memory (e.g., ROM) 9, flash memory (not shown), a graphics processor 12, a digital signal processor (not shown), a crypto processor (not shown), a chipset 14, an antenna 16, a display 18 such as a touchscreen display, a touchscreen controller 20, a battery 22, an audio codec (not shown), a video codec (not shown), a power amplifier 24, a global positioning system (GPS) device 26, a compass 28, an accelerometer (not shown), a gyroscope (not shown), a speaker 30, a camera 32, and a mass storage device (such as hard disk drive) 10, compact disk (CD) (not shown), digital versatile disk (DVD) (not shown), and so forth). These components may be connected to the system board 2, mounted to the system board, or combined with any of the other components. The communication chip 6 enables wireless and/or wired communications for the transfer of data to and from the computing device 11. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-

solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 6 may implement any of a number of wireless or wired standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth,
5 Ethernet derivatives thereof, as well as any other wireless and wired protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 11 may include a plurality of communication chips 6. For instance, a first communication chip 6 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 6 may be
10 dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

In some implementations, the integrated circuit unit of the processor, memory devices, communication devices, or other components includes or is packaged with programmed antifuse circuits to contain operational parameters, configuration parameters, identification information,
15 encryption keys or other information as described herein. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In various implementations, the computing device 11 may be a laptop, a netbook, a
20 notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 11 may be any other electronic device that processes data including a wearable device.

Embodiments may be implemented as a part of one or more memory chips, controllers,
25 CPUs (Central Processing Unit), microchips or integrated circuits interconnected using a motherboard, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA).

References to “one embodiment”, “an embodiment”, “example embodiment”, “various
30 embodiments”, etc., indicate that the embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Further, some embodiments may have some, all, or none of the features described for other embodiments.

In the following description and claims, the term “coupled” along with its derivatives, may be used. “Coupled” is used to indicate that two or more elements co-operate or interact with each other, but they may or may not have intervening physical or electrical components between them.

5 As used in the claims, unless otherwise specified, the use of the ordinal adjectives “first”, “second”, “third”, etc., to describe a common element, merely indicate that different instances of like elements are being referred to, and are not intended to imply that the elements so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

10 The drawings and the forgoing description give examples of embodiments. Those skilled in the art will appreciate that one or more of the described elements may well be combined into a single functional element. Alternatively, certain elements may be split into multiple functional elements. Elements from one embodiment may be added to another embodiment. For example, orders of processes described herein may be changed and are not limited to the manner described herein. Moreover, the actions of any flow diagram need not be implemented in the order shown;
15 nor do all of the acts necessarily need to be performed. Also, those acts that are not dependent on other acts may be performed in parallel with the other acts. The scope of embodiments is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of embodiments is at least as broad as given by the following claims.

20 The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications. Some embodiments pertain to method that includes forming an antifuse circuit on a substrate, including forming a gate area of the antifuse circuit, implanting a molecule into the gate area to damage the structure of the gate area, forming
25 electrodes over the gate area to connect the antifuse circuit to other components.

Further embodiments include forming a gate dielectric and wherein implanting comprises implanting into the gate dielectric to damage the gate dielectric and a channel under the gate dielectric in the gate area.

30 In some embodiments forming a gate dielectric comprises forming a high K metal oxide gate dielectric.

In some embodiments the damaged gate dielectric comprises an antifuse element for the antifuse circuit.

Further embodiments include depositing a second gate dielectric and a polysilicon gate material over the gate area, doping source and drain areas, and removing the gate dielectric and polysilicon gate material after doping and before implanting.

Further embodiments include depositing a second gate dielectric over the gate after
5 removing the first gate dielectric and before implanting.

Further embodiments include forming a gate dielectric over the gate area and forming a gate material over the gate area before implanting and wherein implanting further damages the structure of the gate dielectric.

In some embodiments implanting comprises implanting a SiF₄ molecules into the gate
10 area.

In some embodiments implanting comprises a plasma immersion ion implantation. Further embodiments include applying a gate metal oxide over the gate area before implanting and then forming gate metal layers over the metal oxide after implanting.

Further embodiments include forming a polysilicon layer over the gate areas, implanting
15 source and drain areas beside the gate areas and removing the polysilicon layer over the gate areas before implanting.

Some embodiments pertain to an antifuse circuit that includes a source and a drain over a well, a channel between the source and the drain, the channel including an implanted molecule impurity, and a gate over the channel, the gate being damaged by the impurity molecule, so that
20 the gate has a reduced breakdown voltage due to the molecule.

In some embodiments the molecule is SiF₄.

In some embodiments the gate is a formed of a metal and a high K metal oxide gate dielectric.

Further embodiments include a gate dielectric over the channel.

Further embodiments include a damaged gate metal oxide between the channel and the
25 gate.

Further embodiments include a work function metal between the damaged gate metal oxide and the gate, the work function metal not being damaged by the impurity molecule.

Some embodiments pertain to a computing system that includes a processor, a mass
30 memory coupled to the processor, and a programmable read only memory coupled to the processor having a plurality of antifuse transistors, each antifuse transistor comprising a source and a drain over a well, a channel between the source and the drain, the channel including an implanted molecule impurity and a gate dielectric over the channel to form a gate, the gate

dielectric being damaged by the impurity molecule, so that the gate has a reduced breakdown voltage due to the molecule.

In some embodiments the programmable read only memory comprises a high voltage fuse signal driver to program each respective antifuse transistor.

5 Further embodiments include a gate metal over the channel and the gate dielectric.

CLAIMS

1. A method comprising:
forming an antifuse circuit on a substrate, including forming a gate area of the antifuse circuit;
implanting a molecule into the gate area to damage the structure of the gate area;
- 5 forming electrodes over the gate area to connect the antifuse circuit to other components.
2. The method of Claim 1, further comprising forming a gate dielectric and wherein
implanting comprises implanting into the gate dielectric to damage the gate dielectric and a
channel under the gate dielectric in the gate area.
3. The method of Claim 2, wherein forming a gate dielectric comprises forming a high K
10 metal oxide gate dielectric
4. The method of Claim 2 or 3, wherein the damaged gate dielectric comprises an antifuse
element for the antifuse circuit.
5. The method of any one or more of the above claims, further comprising:
depositing a second gate dielectric and a polysilicon gate material over the gate area;
- 15 doping source and drain areas; and
removing the gate dielectric and polysilicon gate material after doping and before implanting.
6. The method of Claim 5, further comprising depositing a second gate dielectric over the
gate after removing the first gate dielectric and before implanting.
7. The method of any one or more of the above claims, further comprising:
- 20 forming a gate dielectric over the gate area; and
forming a gate material over the gate area before implanting, and
wherein implanting further damages the structure of the gate dielectric.
8. The method of Claim 1, wherein implanting comprises implanting a SiF₄ molecules into
the gate area.
- 25 9. The method of any one or more of the above claims, wherein implanting comprises a
plasma immersion ion implantation.
10. The method of any one or more of the above claims, further comprising:
applying a gate metal oxide over the gate area before implanting; and
then forming gate metal layers over the metal oxide after implanting.
- 30 11. The method of Claim 10, further comprising:
forming a polysilicon layer over the gate areas;
implanting source and drain areas beside the gate areas; and
removing the polysilicon layer over the gate areas before implanting.
12. An antifuse circuit comprising:

a source and a drain over a well;

a channel between the source and the drain, the channel including an implanted molecule impurity; and

a gate over the channel, the gate being damaged by the impurity molecule, so that the gate has a reduced breakdown voltage due to the molecule.

13. The circuit of Claim 12, wherein the molecule is SiF₄.

14. The circuit of Claim 12 or 13, wherein the gate is a formed of a metal and a high K metal oxide gate dielectric.

15. The circuit of Claim 12, 13 or 14, further comprising a gate dielectric over the channel.

16. The circuit of Claim 15, further comprising a damaged gate metal oxide between the channel and the gate.

17. The circuit of Claim 15, further comprising a work function metal between the damaged gate metal oxide and the gate, the work function metal not being damaged by the impurity molecule.

18. A computing system comprising:

a processor;

a mass memory coupled to the processor; and

a programmable read only memory coupled to the processor having a plurality of antifuse transistors, each antifuse transistor comprising:

a source and a drain over a well;

a channel between the source and the drain, the channel including an implanted molecule impurity; and

a gate dielectric over the channel to form a gate, the gate dielectric being damaged by the impurity molecule, so that the gate has a reduced breakdown voltage due to the molecule.

19. The computing system of Claim 18, wherein the programmable read only memory comprises a high voltage fuse signal driver to program each respective antifuse transistor.

20. The computing system of Claim 18 or 19, further comprising a gate metal over the channel and the gate dielectric.

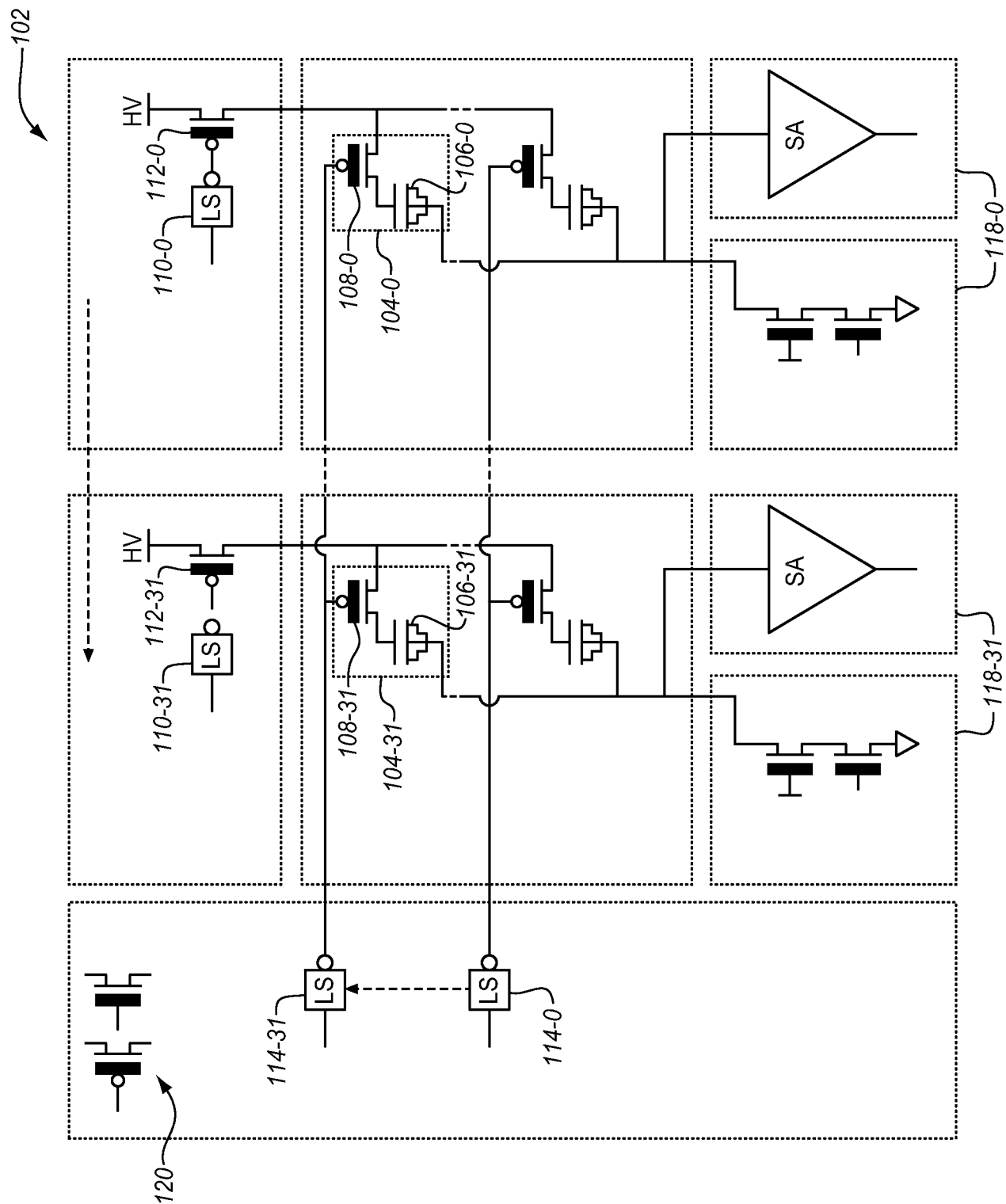


FIG. 1

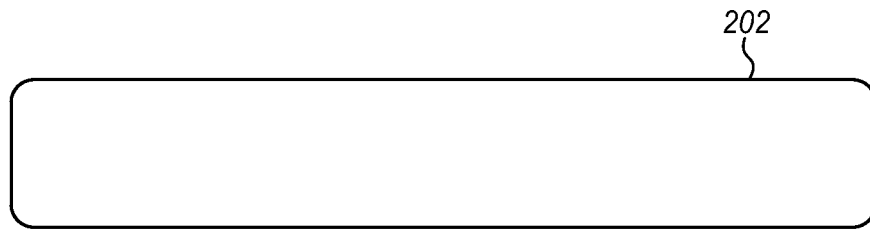


FIG. 2

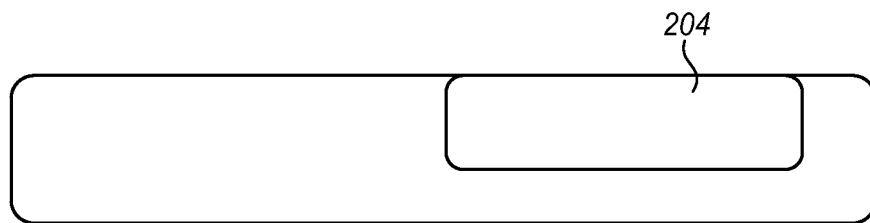


FIG. 3

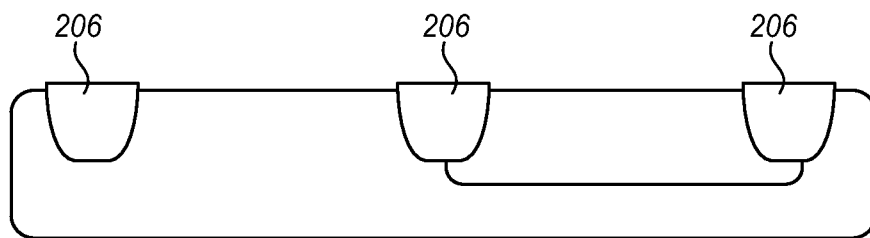


FIG. 4

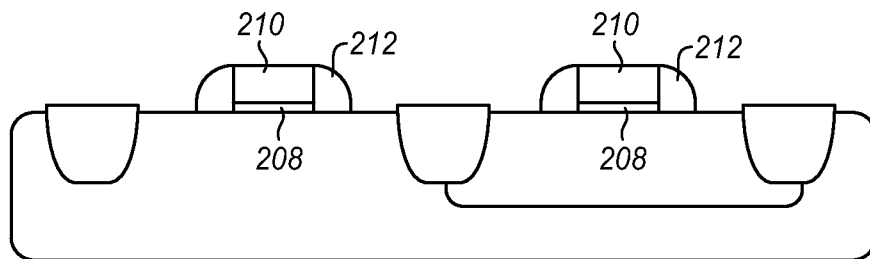


FIG. 5

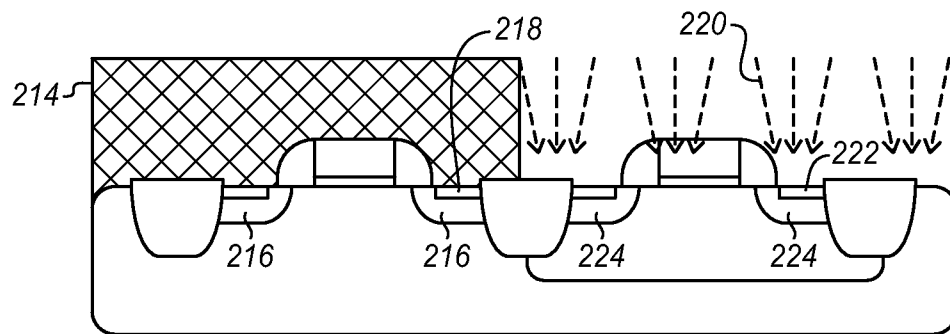


FIG. 6

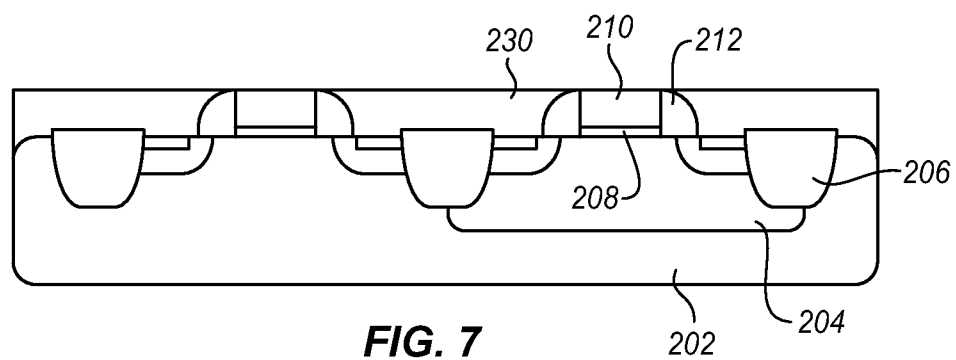


FIG. 7

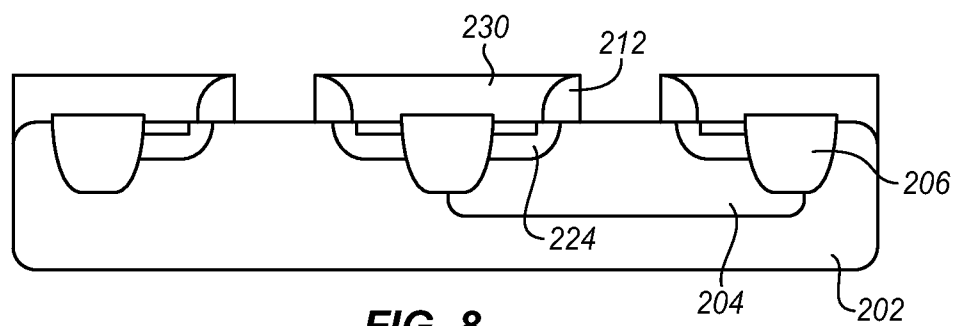


FIG. 8

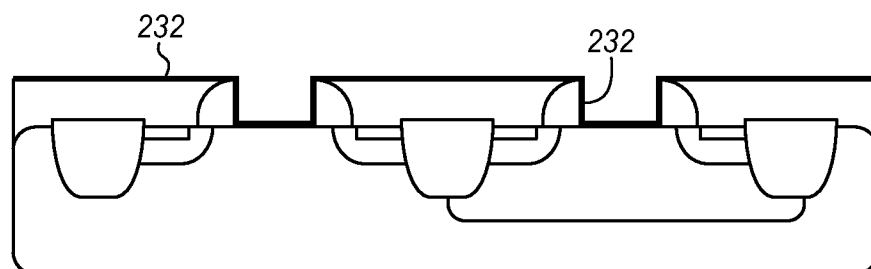


FIG. 9

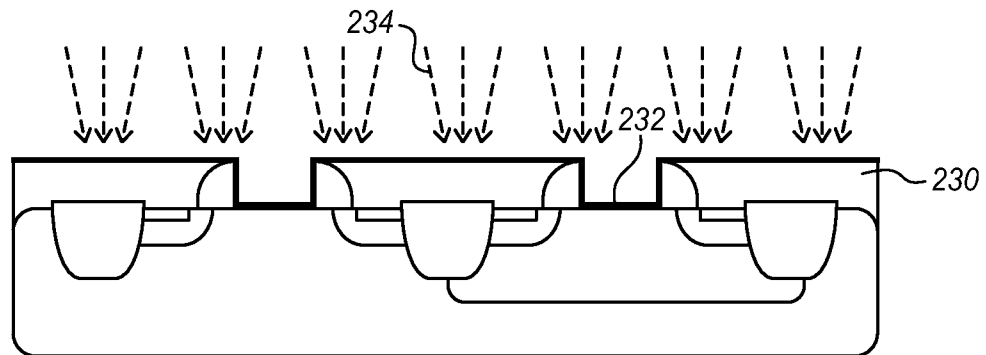


FIG. 10

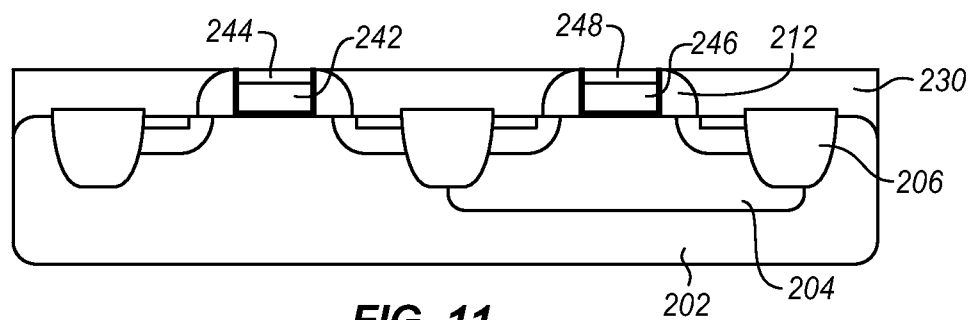


FIG. 11

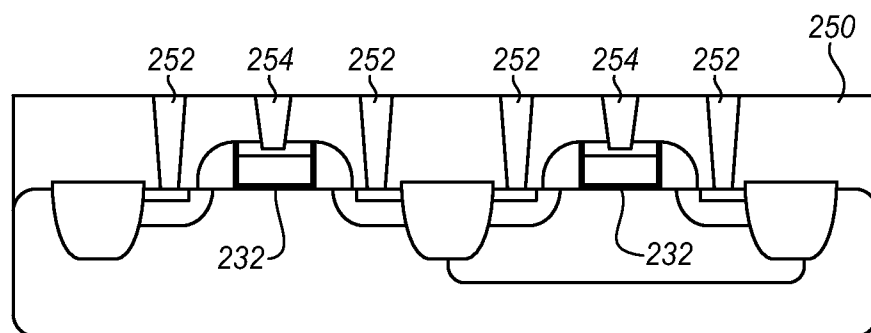


FIG. 12

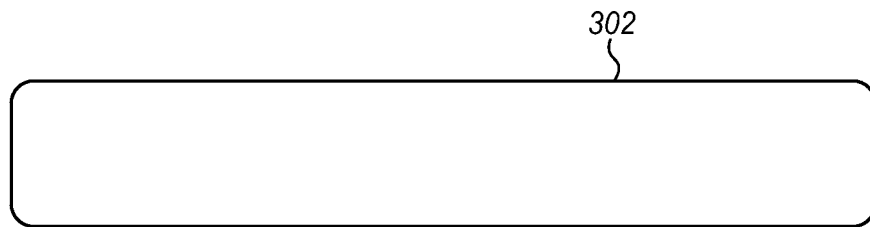


FIG. 13

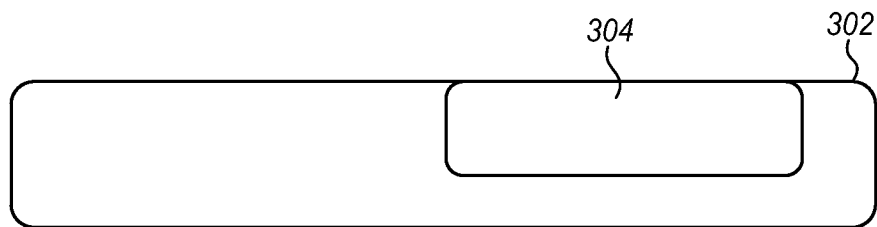


FIG. 14

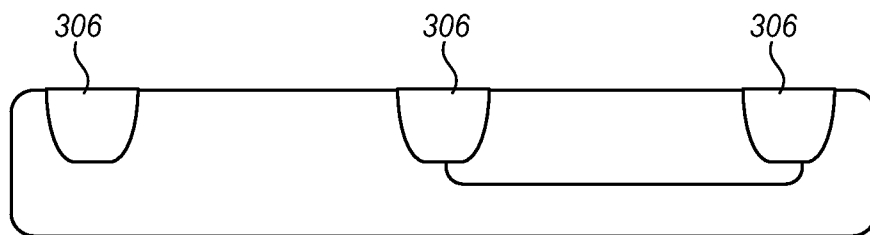


FIG. 15

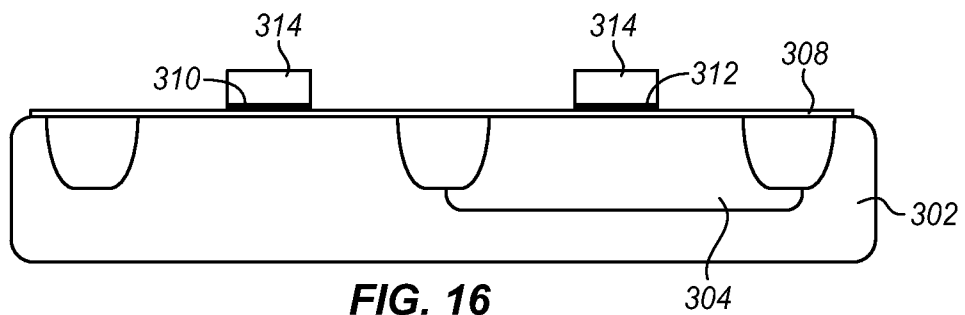


FIG. 16

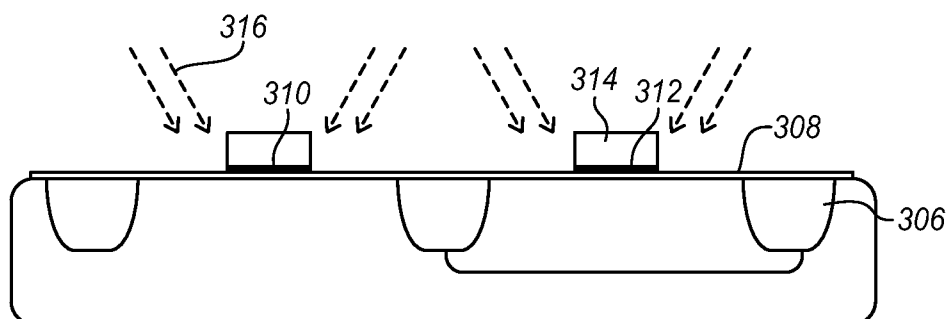


FIG. 17

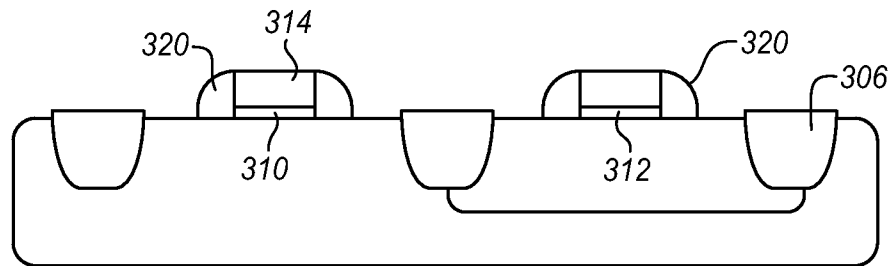


FIG. 18

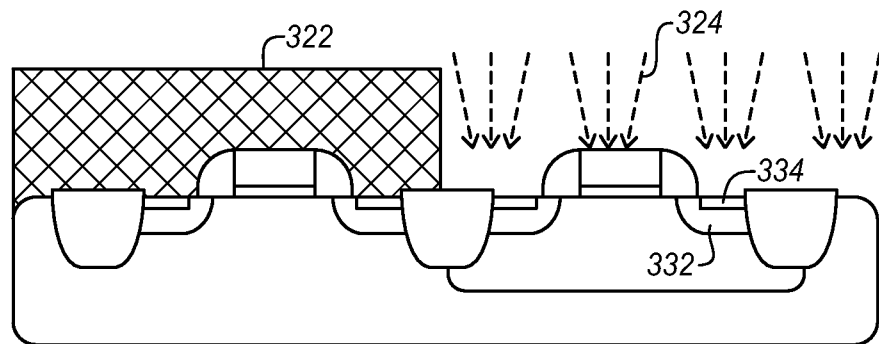


FIG. 19

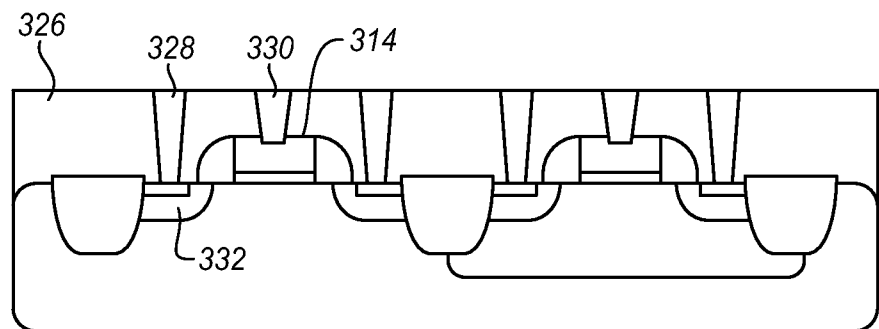
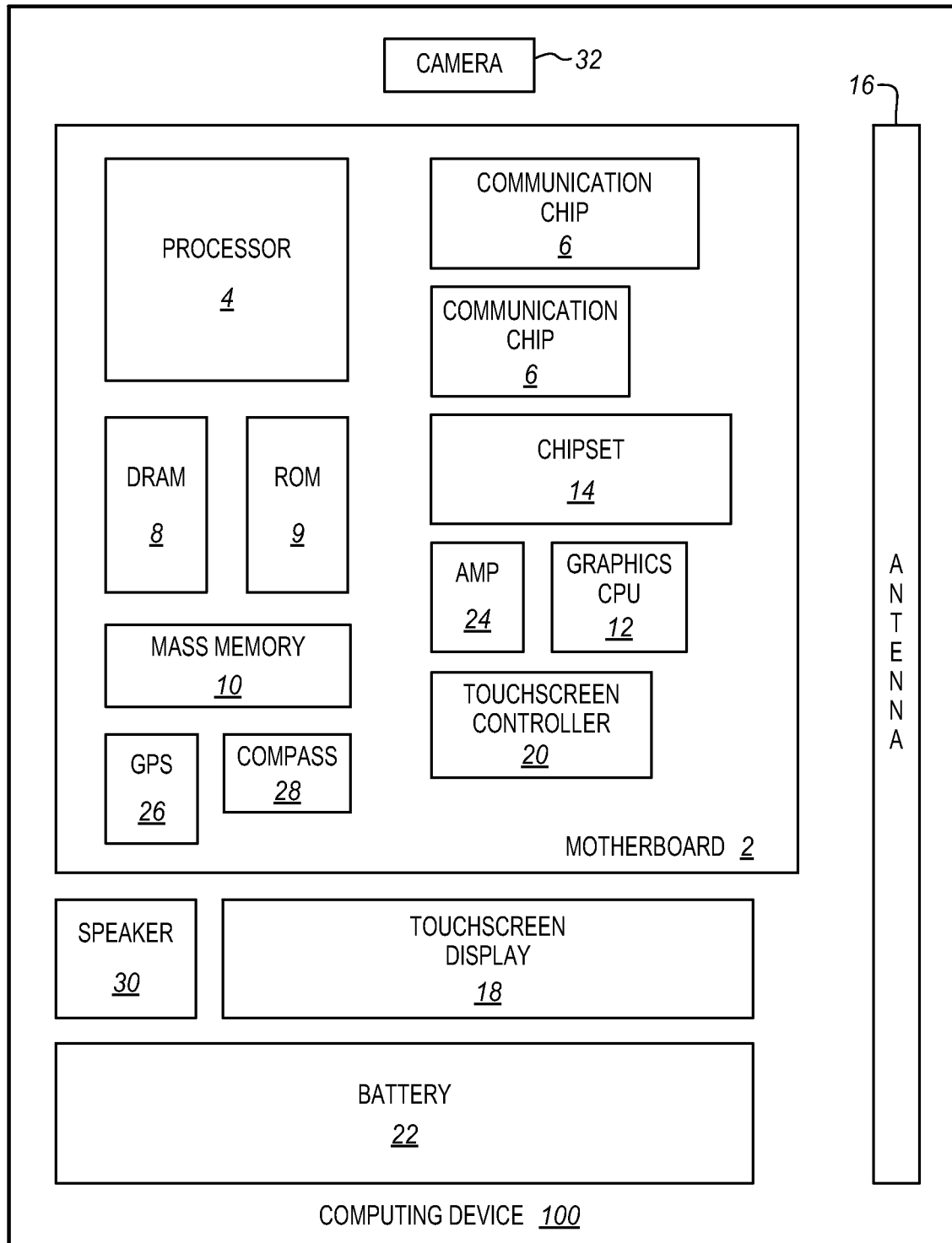


FIG. 20

FIG. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/037762**A. CLASSIFICATION OF SUBJECT MATTER****H01L 23/62(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/62; H01L 29/00; G06F 17/50; H03K 19/00; H01L 21/82; H01L 23/525

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: antifuse, implanting, reduce, breakdown voltage, high-k

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6096580 A (S. SUNDAR KUMAR IYER et al.) 01 August 2000	12-13
Y	See abstract, column 7, lines 8-16, claims 1, 3 and figures 13-14.	1-4, 8, 14, 18-20
Y	US 2014-0070364 A1 (YONG PARK et al.) 13 March 2014	1-4, 8, 14, 20
	See abstract, paragraphs [0027]-[0030] and figure 3.	
Y	US 2003-0131336 A1 (GREG A. BLODGETT) 10 July 2003	18-20
	See abstract, paragraphs [0012]-[0016] and claims 17, 25.	
A	US 2004-0051162 A1 (DURESETI CHIDAMBARRAO et al.) 18 March 2004	1-4, 8, 12-14, 18-20
	See abstract, paragraphs [0006]-[0009] and claim 1.	
A	US 2009-0189248 A1 (EIJI KITAMURA et al.) 30 July 2009	1-4, 8, 12-14, 18-20
	See abstract, paragraphs [0009]-[0010] and claim 1.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 March 2016 (30.03.2016)

Date of mailing of the international search report

31 March 2016 (31.03.2016)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 35208,
Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

LEE, EUN KYU

Telephone No. +82-42-481-3580



INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US2015/037762**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 6,11,16-17
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
The claims 6,11,16-17 are not clear since these claims refer to multiple dependent claims 5,10,15 which do not comply with PCT Rule 6.4(a).
3. ☒ Claims Nos.: 5,7,9-10,15
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/037762

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6096580 A	01/08/2000	None	
US 2014-0070364 A1	13/03/2014	CN 104620383 A US 8975724 B2 WO 2014-043566 A1	13/05/2015 10/03/2015 20/03/2014
US 2003-0131336 A1	10/07/2003	US 2006-0203580 A1 US 6553556 B1 US 7146585 B2	14/09/2006 22/04/2003 05/12/2006
US 2004-0051162 A1	18/03/2004	DE 10342028 A1 JP 2004-111957 A	25/03/2004 08/04/2004
US 2009-0189248 A1	30/07/2009	JP 2009-206490 A US 2012-0018841 A1 US 8729642 B2	10/09/2009 26/01/2012 20/05/2014