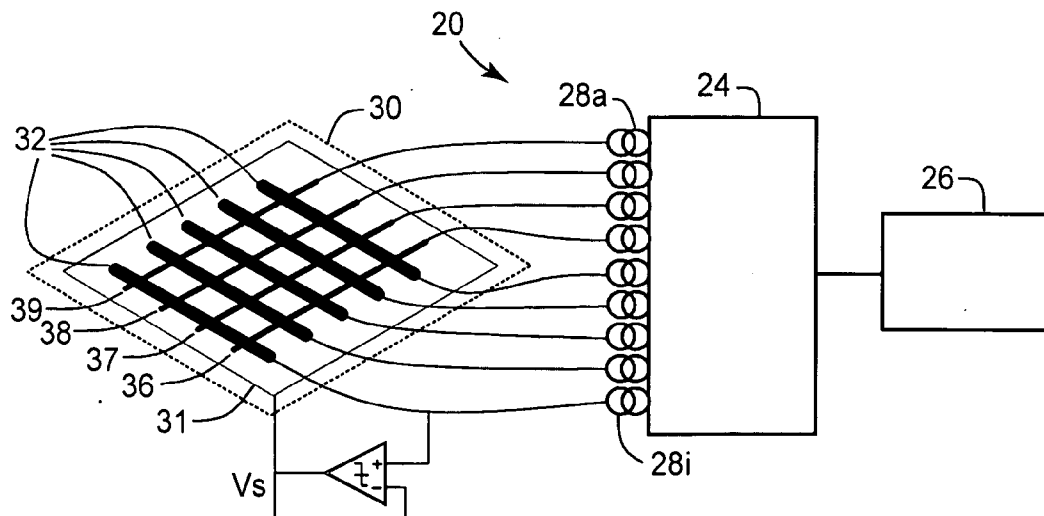




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GEAGHAN(10) **Pub. No.: US 2009/0167720 A1**(43) **Pub. Date: Jul. 2, 2009**(54) **MULTIPLE CAPACITANCE MEASURING
CIRCUITS AND METHODS**(75) Inventor: **Bernard O. GEAGHAN**, Salem,
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28, 2007.**Publication Classification**(51) **Int. Cl.**
G06F 3/045 (2006.01)(52) **U.S. Cl. 345/174**(57) **ABSTRACT**

In capacitance measurement circuits and methods that measure capacitances at multiple locations by ramping voltage signals between reference levels, the phase of the voltage signal ramping can be controlled, for example to mitigate currents flowing between measurement locations. Such capacitance measurement circuits and methods can be utilized in touch sensor devices that determine touch position based on capacitance measurements on multiple locations on a touch surface. Controlling the phase of the voltage signal ramps can include concurrently starting the voltage signal ramps, for example by effecting a delay on at least one signal channel that has reached a voltage threshold, or by regulating all the voltage ramps according to a fixed frequency.



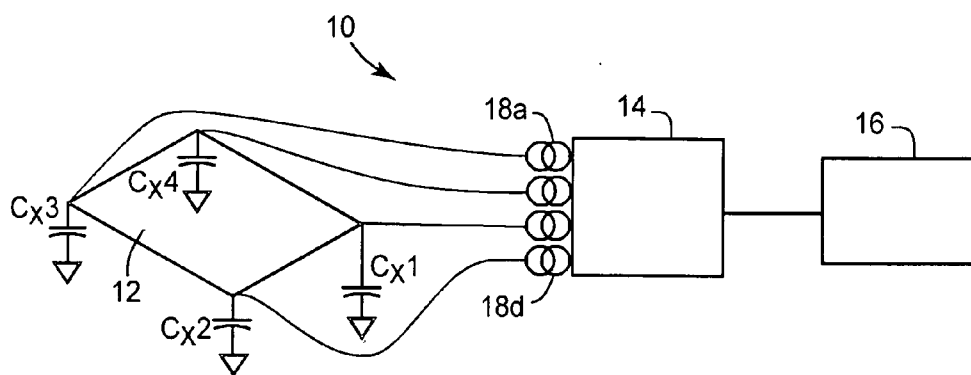


FIG. 1A

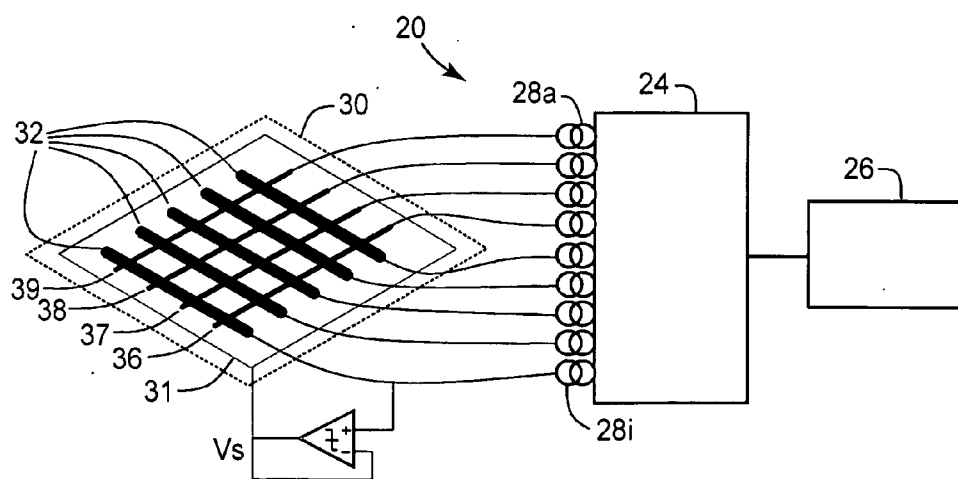


FIG. 1B

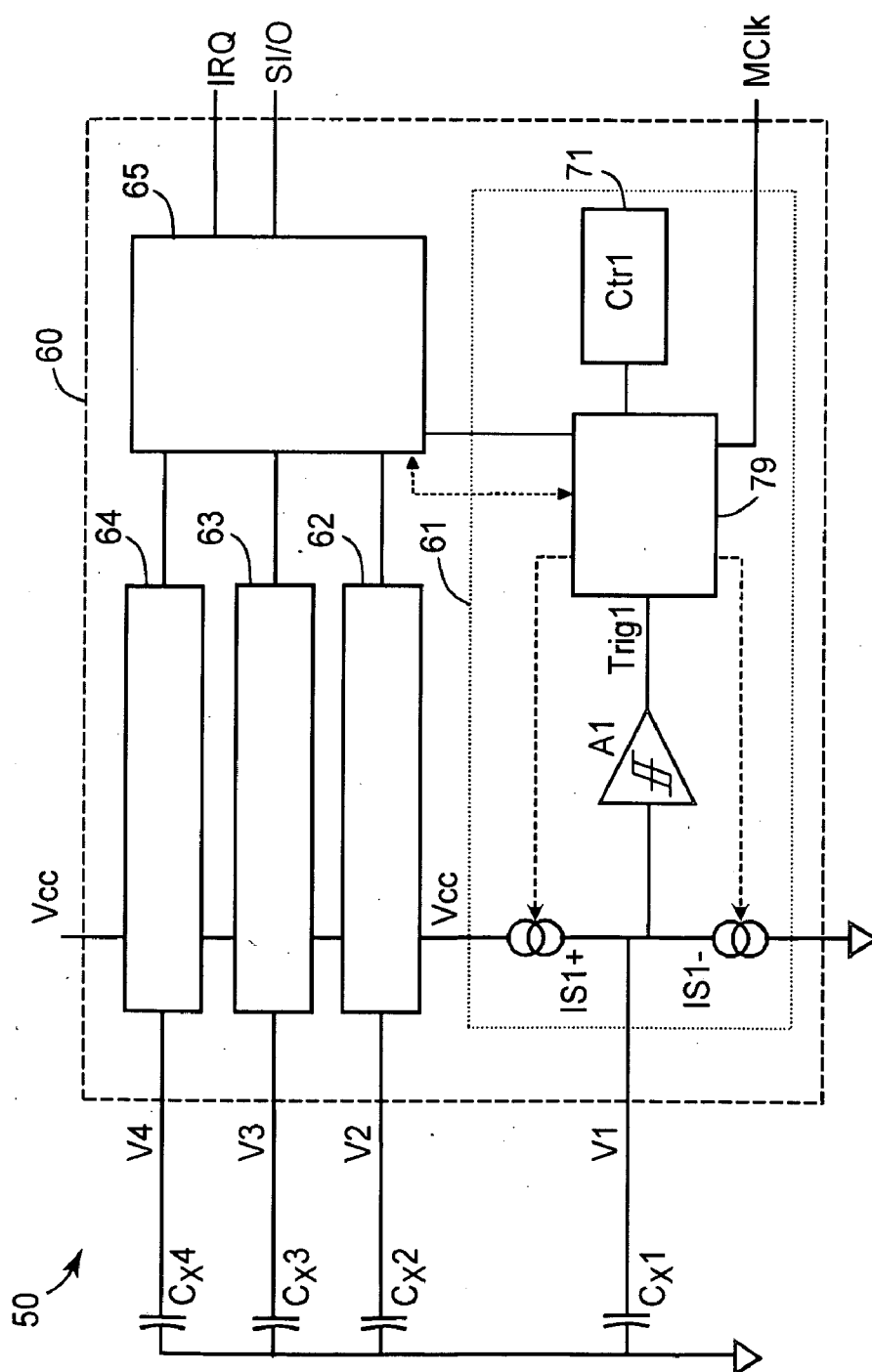


FIG. 2

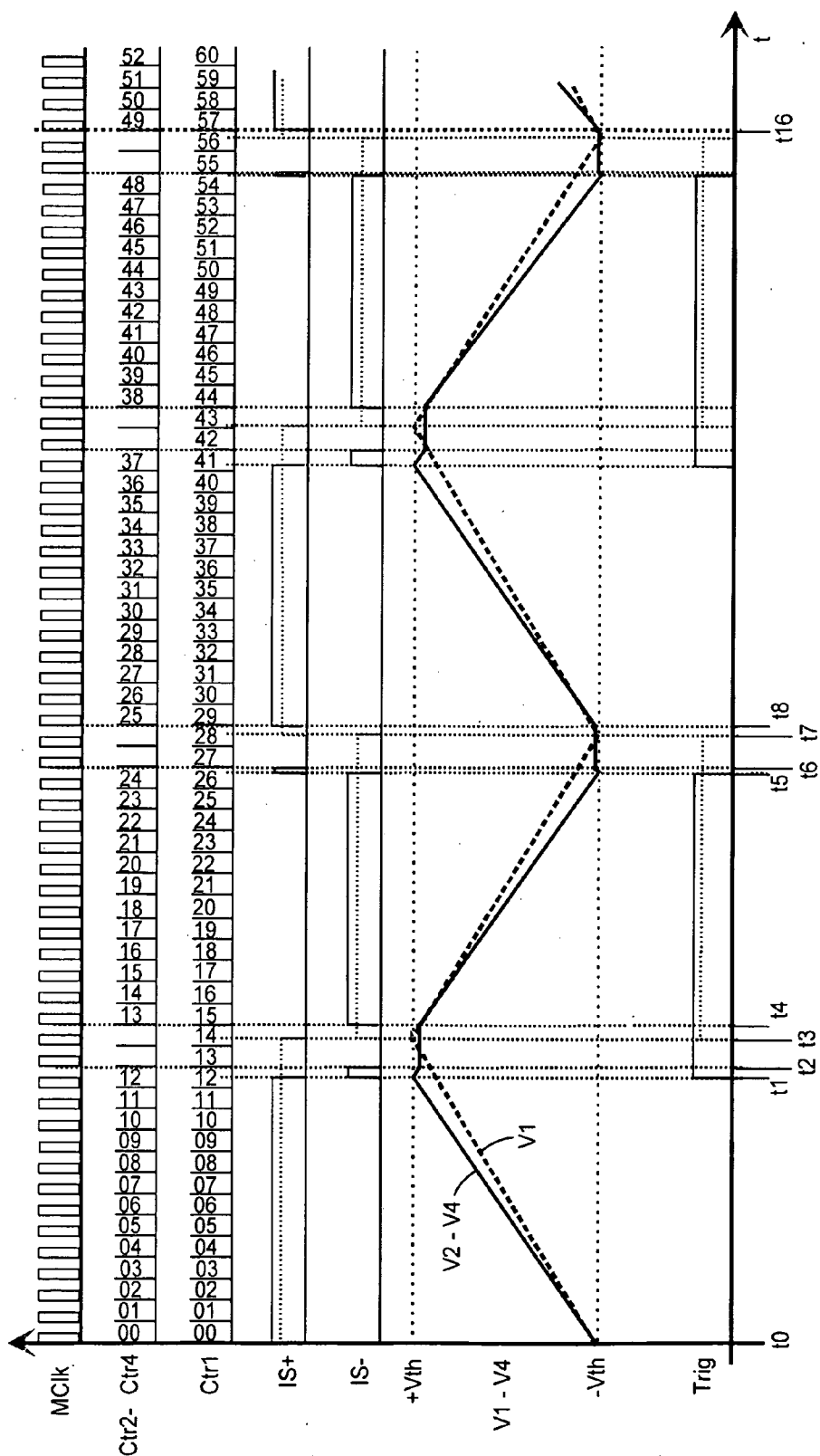


FIG. 3

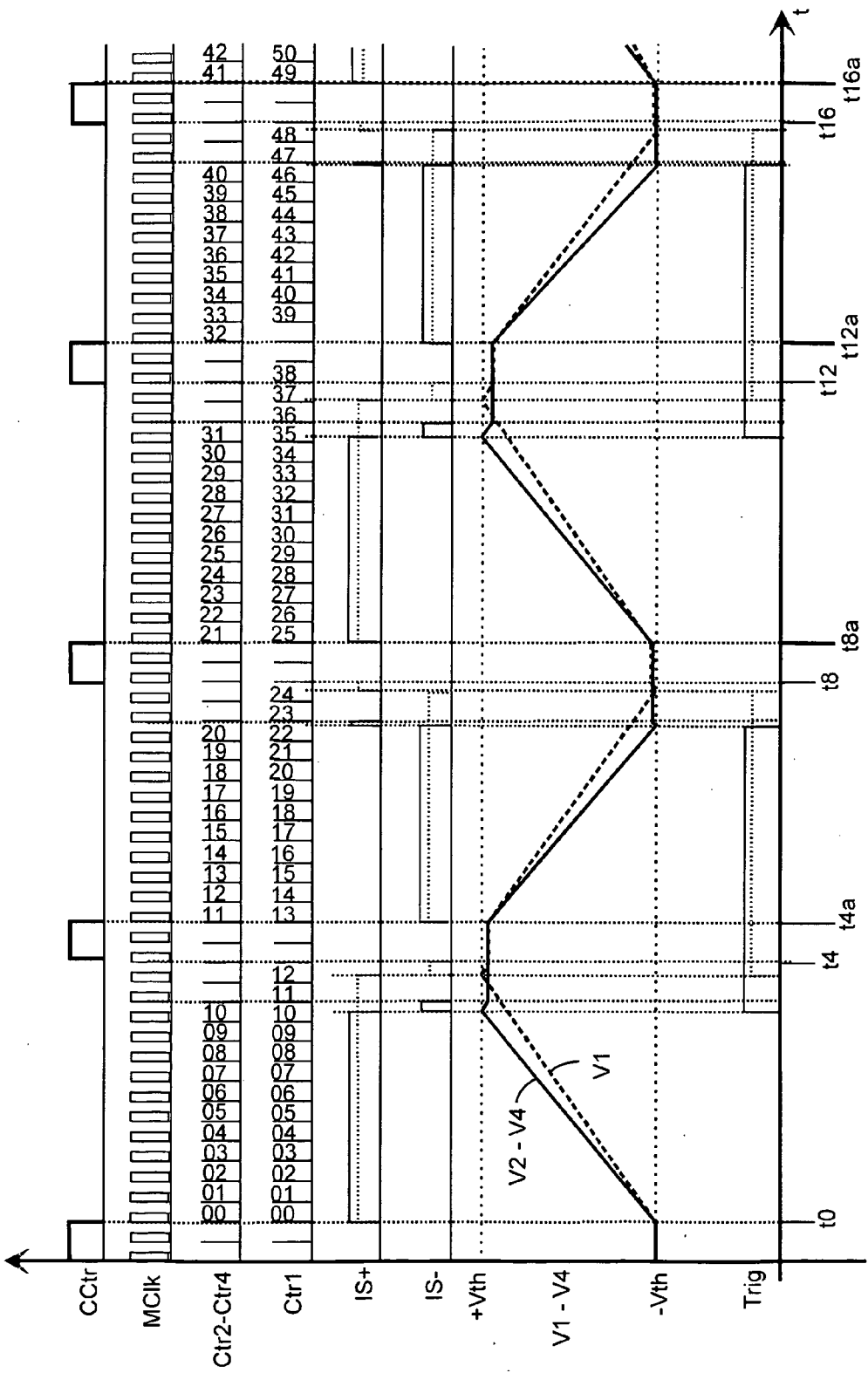
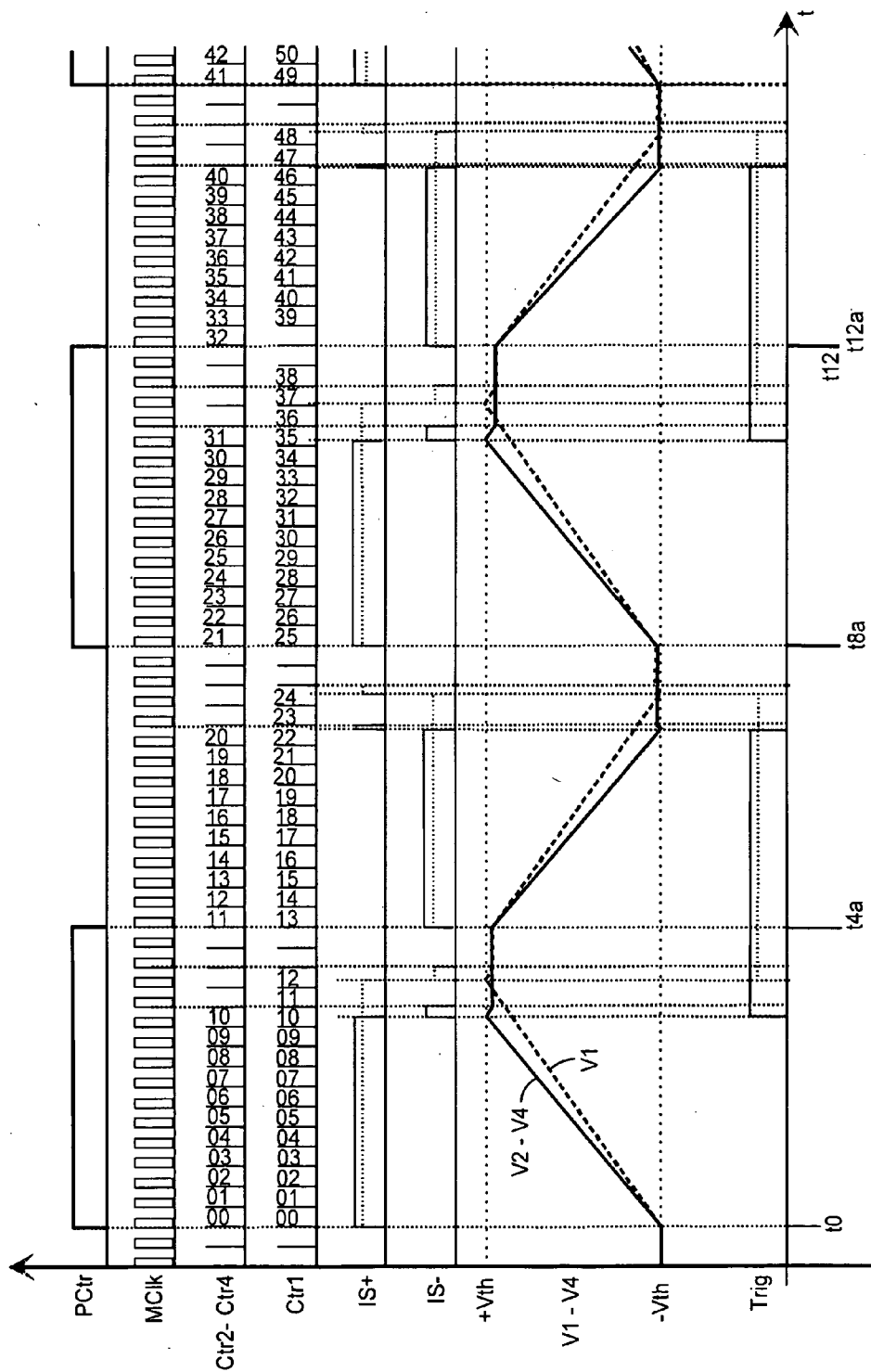


FIG. 4



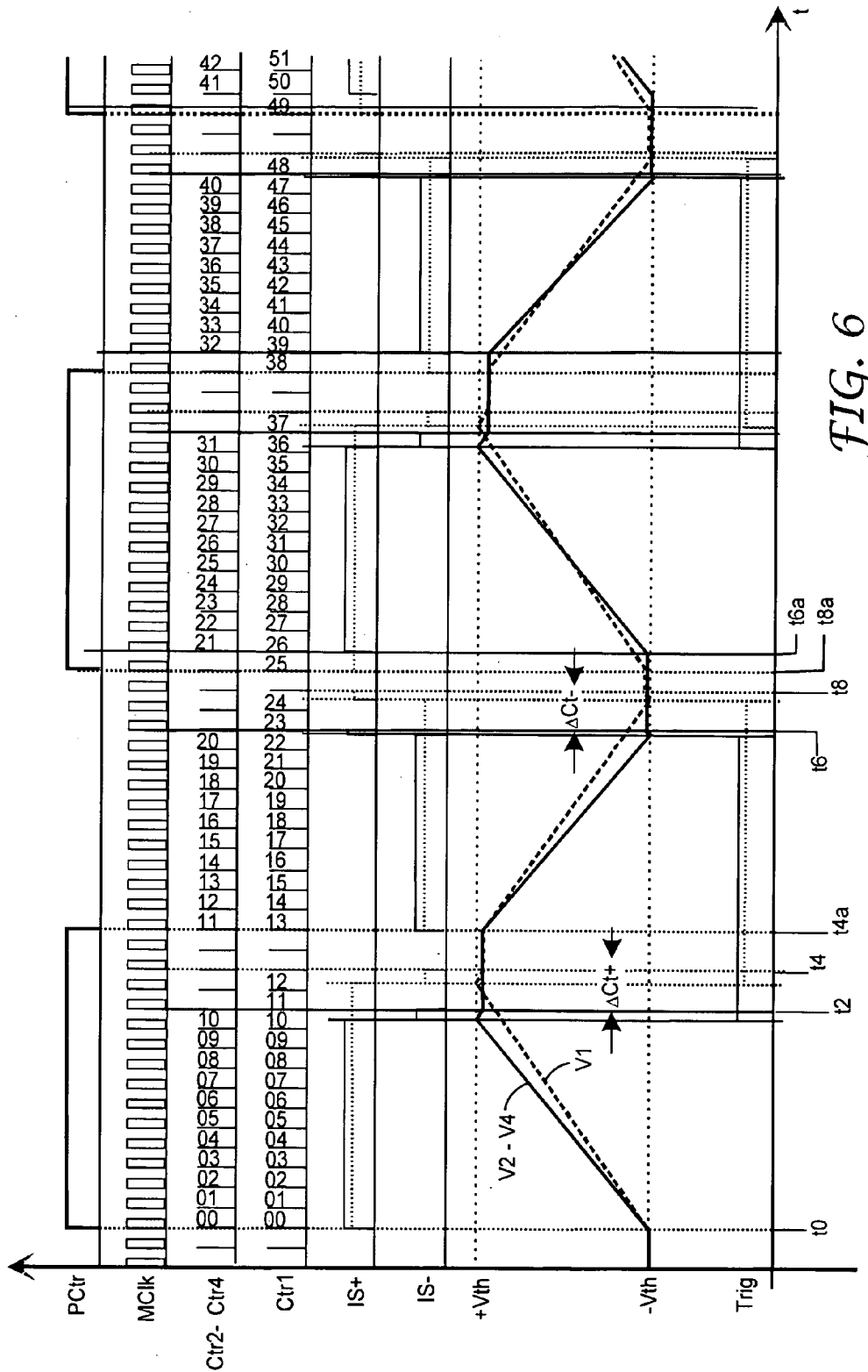


FIG. 6

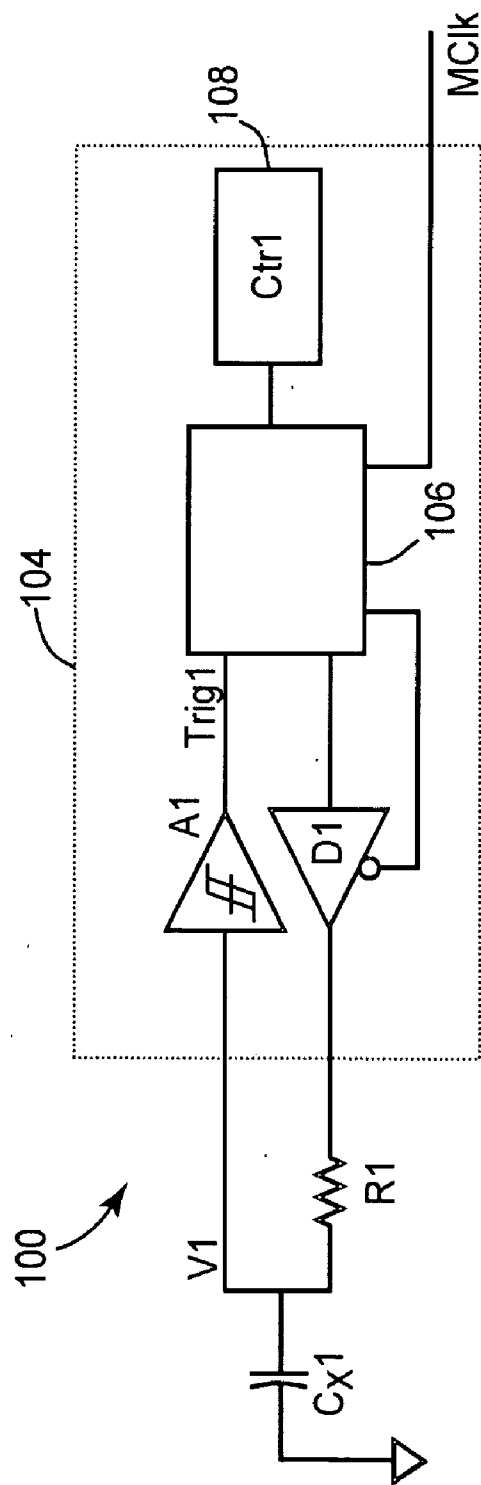


FIG. 7

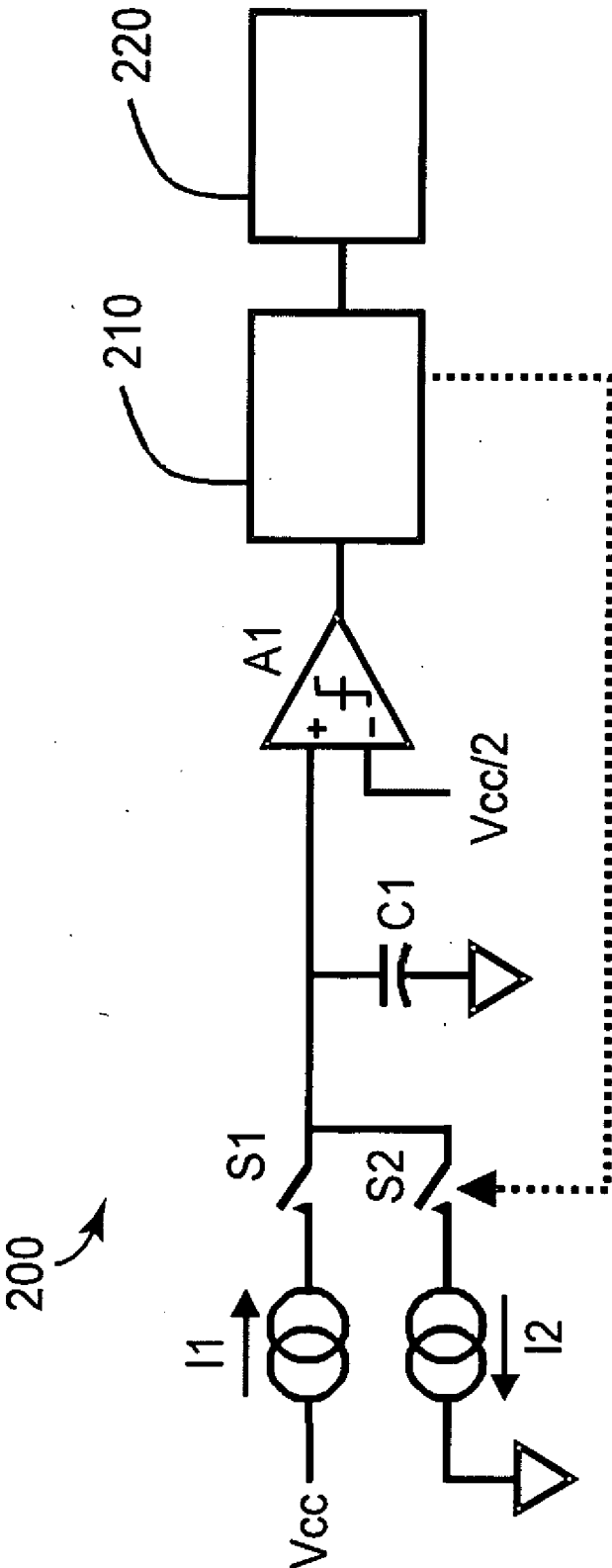


FIG. 8

MULTIPLE CAPACITANCE MEASURING CIRCUITS AND METHODS

CROSS REFERENCE TO RELATED APPLICATION

[0001] This patent document claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Patent Application Ser. No. 61/017,451, entitled "Multiple Capacitance Measuring Circuits and Methods" as was filed on Dec. 28, 2007, the disclosure of which is incorporated by reference herein in its entirety.

[0002] The present invention relates generally to circuits and methods for measuring multiple capacitances, and to systems such as capacitive touch sensing systems that utilize multiple capacitance measuring circuits and methods, and in particular to mitigating current flow between capacitance measurement locations in such circuits and methods.

BACKGROUND

[0003] Touch sensitive devices allow a user to conveniently interface with electronic systems and displays by reducing or eliminating the need for mechanical buttons, keypads, keyboards, and pointing devices. For example, a user can carry out a complicated sequence of instructions by simply touching an on-display touch screen at a location identified by an icon. In many touch sensitive devices, the input is sensed when a conductive object in the sensor is capacitively coupled to a conductive touch implement such as a user's finger. Such devices measure capacitance at multiple locations due to the touch disturbance, and use the measured capacitances to determine touch position.

SUMMARY OF THE INVENTION

[0004] In certain embodiments, the present invention provides methods (and corresponding circuitry) for use in a touch sensor device that measures capacitances at a plurality of locations on a touch surface in response to a touch object coupling to the touch surface at a touch position, the capacitances being measured by applying electrical charge to the plurality of locations to ramp respective voltage signals between a first reference level and a second reference level. Such methods include controlling the phase of the voltage signal ramps to mitigate currents flowing between the locations. In certain embodiments, controlling the phase of the voltage signal ramps includes concurrently starting the voltage signal ramps, for example by effecting a delay on at least one signal channel that has reached a voltage threshold, or by regulating all the voltage ramps according to a fixed frequency. In certain embodiments, time differentials between when respective voltage signal ramps reach a threshold level can be determined, and subsequent ramp starting times can be adjusted in response.

[0005] In certain embodiments, the present invention provides methods for use with a device that measures capacitances at a plurality of locations, each location associated with a capacitance measurement channel to ramp respective voltage signals on the respective capacitances. Such methods include (a) concurrently initiating forward-direction voltage signal ramps on multiple channels, and (b) effecting a delay on the forward-direction voltage signal ramp of at least one channel in response to reaching a voltage signal threshold. In certain embodiments, such methods can further include (c) concurrently initiating reverse-direction voltage signal ramps

on the multiple channels, and (d) effecting a delay on the reverse-direction voltage signal ramp of at least one channel in response to reaching a low voltage signal threshold. Such alternate forward and reverse ramping can be repeated a desired number of times.

[0006] In certain embodiments, the present invention provides capacitive touch sensor devices for determining touch position by measuring capacitances at a plurality of locations on a touch surface in response to a touch object coupling to the touch surface at the touch position. Such devices include circuitry associated with each location to ramp respective voltage signals between a first reference level and a second reference level by applying an electrical charge, and circuitry to control the phase of the voltage signal ramps to mitigate currents flowing between the locations.

[0007] The above summary of the present invention is not intended to describe each embodiment or every implementation of the present invention. Advantages and attainments, together with a more complete understanding of the invention, will become apparent and appreciated by referring to the following detailed description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present disclosure may be more completely understood and appreciated in consideration of the following detailed description of various embodiments in connection with the accompanying drawings, in which:

[0009] FIGS. 1A and 1B schematically show exemplary touch sensor systems useful in certain embodiments of the present invention;

[0010] FIG. 2 schematically shows an exemplary control circuit useful in certain embodiments of the present invention;

[0011] FIG. 3 schematically shows a timing diagram indicating operation of a multiple capacitance measurement circuit in accordance with certain embodiments of the present invention;

[0012] FIG. 4 schematically shows a timing diagram indicating operation of a multiple capacitance measurement circuit in accordance with certain embodiments of the present invention;

[0013] FIG. 5 schematically shows a timing diagram indicating operation of a multiple capacitance measurement circuit in accordance with certain embodiments of the present invention;

[0014] FIG. 6 schematically shows a timing diagram indicating operation of a multiple capacitance measurement circuit in accordance with certain embodiments of the present invention;

[0015] FIG. 7 schematically shows a portion of an exemplary control circuit useful in certain embodiments of the present invention; and

[0016] FIG. 8 schematically shows an exemplary accumulator circuit useful in certain embodiments of the present invention.

[0017] While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It is to be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all

modifications, equivalents, and alternatives falling within the scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF EMBODIMENTS

[0018] In the following description of the illustrated embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration, various embodiments in which the invention may be practiced. It is to be understood that the embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

[0019] In certain embodiments, the present disclosure is generally directed to mitigating current flow between capacitance measurement locations in multiple capacitance measurement circuits and methods. When voltage signal ramps are used to determine capacitance at multiple locations, current flow between measurement locations can be mitigated by controlling the phase of the voltage signal ramps. For example, individual voltage ramp cycles can be concurrently initiated to keep the ramps in phase. In certain embodiments, this can be accomplished by effecting a delay in measurement channels that have reached a voltage ramp threshold until other measurement channels have also reached the threshold. Alternatively or in addition, the voltage signal ramps can be regulated by a preset ramping period so that they are kept in phase. Alternatively or in addition, detected differences in ramping periods can be used to adjust the relative start times of subsequent ramping periods, for example to match the voltage levels of the ramps in the middle of the respective ramp periods to reduce the net current flow between measurement locations. These and other techniques can be used, including any suitable combinations or permutations thereof, as will be appreciated by those skilled in the art based on the descriptions provided herein.

[0020] Without loss of generality, and for the purpose of efficient illustration, it is useful to describe various aspects of the present invention in terms of touch sensor system environments. It will be recognized, however, that such descriptions are merely exemplary and not limiting, and that aspects of the present invention can be suitably implemented in many applications where multiple capacitances are measured, and relative magnitudes or ratios of measured capacitances are calculated. Examples include instruments, pressure gauges, and measurement of small distances, areas, and moisture.

[0021] FIGS. 1A and 1B illustrate touch sensor examples of capacitance measurement devices suitable for implementing various embodiments of the present invention. In certain applications, the devices shown determine information related to a touch object coupled to the sensor surface by measuring capacitance, or relative capacitance, at a plurality of locations on the sensor surface due to the presence of the touch object. For example, device 10 in FIG. 1A represents a 4-wire capacitive sensor system (also called analog capacitive) in which capacitances C_{x1} through C_{x4} , shown located at the corners of sensor 12, are measured by controller 14. Sensor 12 can be a continuous resistive layer (such as the capacitive touch sensors commercially available from 3M Touch Systems, Inc. under the trade designation Cleartek), a patterned or segmented resistive layer (such as sensors disclosed in co-assigned U.S. Ser. No. 11/734,553, filed on Apr. 12, 2007, which is hereby fully incorporated into this document), or any other suitable sensor. As another example, device 20 in FIG. 1B represents a matrix capacitive sensor system that includes orthogonal sets of electrodes, and a

controller 24 that measures the capacitance on each of the electrodes (such as disclosed in U.S. Pat. Publication 2007/0074913, which is hereby fully incorporated into this document). Embodiments of the present invention can also be used to measure capacitance for button and switch applications (individually or in an array), for linear slider controls, and so forth.

[0022] As indicated, system 10 in FIG. 1A shows a 4-wire touch embodiment, including a touch controller 14 coupled to a microprocessor 16 and to an analog capacitive sensor 12. In exemplary embodiments, controller 14 performs functions such as touch signal conditioning, data conversion, and real-time processing, while microprocessor 16 performs functions such as filtering and touch coordinate calculation. Controller 14 drives sensor 12 at the capacitance measurement locations using current sources 18a through 18d. When a conductive touch object is coupled to sensor 12, the resulting capacitance is measured at each corner, represented by lumped capacitances C_{x1} through C_{x4} . For ease of illustration, exemplary embodiments are described herein in terms of current drive circuits. However, one of skill in the art will recognize that the present invention is likewise applicable to voltage drive circuits such as those disclosed in commonly-assigned U.S. Ser. No. 11/612,790, filed on Dec. 19, 2006, which is hereby fully incorporated into this document.

[0023] As indicated, system 20 in FIG. 1B shows a matrix touch sensor embodiment, including a touch controller 24 coupled to a microprocessor 26 and to matrix capacitive sensor 30. In exemplary embodiments, controller 24 performs functions such as touch signal conditioning, data conversion, and real-time processing, while microprocessor 26 performs functions such as filtering and touch coordinate calculation. As shown in FIG. 1B for the purposes of illustration, controller 24 drives sensor 30 via nine current sources 28a through 28i, each current source coupled to a different sensing electrode. The electrodes are arranged as orthogonal sets of linear bars, including bottom electrodes 32 and top electrodes 36 through 39. A parasitic capacitance (not indicated) couples bottom electrodes 32 to ground and top electrodes 36 through 39 to ground. There can also be a mutual capacitance (not indicated) that couples each of bottom electrodes 32 to adjacent bottom electrodes, and each of bottom electrodes 32 to each of top electrodes 36 through 39. In certain embodiments, sensor 30 includes an electrically conductive shield 31 to mitigate currents that might otherwise flow due to parasitic capacitances. Shield 31 may be connected to a fixed voltage (not indicated) or it may be driven with an AC electrical signal V_s , which can for example be equal to the voltage signals applied to electrodes 32. Reducing the AC voltage difference between shield 31 and electrodes 32, and between shield 31 and electrodes 36 through 39, reduces capacitive currents that may flow through mutual (parasitic) capacitances. This is desirable because parasitic capacitance tends to reduce sensitivity to changes in touch capacitance.

[0024] For ease of illustration, and without loss of generality, various aspects of the present invention can be understood through discussions that focus on the case of four capacitance measurement channels, such as may exist when using a 4-wire analog capacitive sensor. With that in mind, FIG. 2 exemplifies a controller 60 having four timed-slope analog-to-digital converters 61 through 64 that are respectively used to measure capacitances C_{x1} through C_{x4} . Although only timed-slope converter 61 is shown in detail, it will be appreciated that each of timed-slope converters 62, 63 and 64

include corresponding components. In the general case, separate measurement channels are used for each capacitance measurement location, which in the case of a matrix touch sensor may be equivalent to the number of individual electrodes (e.g., sixteen measurement locations for an eight-by-eight electrode matrix).

[0025] The timed-slope converters are somewhat similar to dual-slope converters, each converter configured to generate forward (+) and reverse (−) ramp signals by alternately injecting forward direction and reverse direction currents from current sources into capacitances C_{x1} through C_{x4} . For example, timed-slope converter **61** includes current sources $IS1+$ and $IS1-$ (and, although not indicated, by consistent nomenclature, timed-slope converter **62** includes current sources $IS2+$ and $IS2-$, timed-slope converter **63** includes current sources $IS3+$ and $IS3-$, timed-slope converter **64** includes current sources $IS4+$ and $IS4-$, with $IS+$ and $IS-$ being used herein to indicate any or all of the current sources as indicated by context). In exemplary embodiments, the current sources are equal in magnitude so that $IS1+=IS1-=IS2+=IS2-=IS3+=IS3-=IS4+=IS4-$. Time-slope converter **61** also includes a comparator **A1** that provides a trigger $Trig1$ to control logic **79** when a high threshold is reached during a voltage ramp using $IS1+$, or when a low threshold is reached during a voltage ramp using $IS1-$. Similarly, timed-slope converter **62** includes a comparator **A2** that provides a trigger $Trig2$, and so forth.

[0026] Assuming that the measured capacitances are also equal, that is $C_{x1}=C_{x2}=C_{x3}=C_{x4}$, then the voltage signals $V1$, $V2$, $V3$, and $V4$ will have ramps of equal slope. For analog capacitive touch panel applications, C_{x1} through C_{x4} are typically close in value (for example, within about 30% of one another). A touch input to the sensor generally will have the effect of increasing one (or more) of the capacitances relative to the others, resulting in a slower ramp on the voltage signal of the channel having the greater capacitance. Differences in slopes result in differences in time required to ramp to a threshold voltage level (for example up from a low reference level such as $\frac{1}{2} V_{cc}$, or down from a high reference level such as $\frac{2}{3} V_{cc}$). The accumulated ramp times for the voltage signals $V1$ through $V4$ are measured concurrently over an integration period, and the measured differences between the accumulated ramp times are used to indicate the differences in capacitance among C_{x1} through C_{x4} . For time-slope converter **61**, the counter **71** (also denoted $Ctr1$) increments a count for every main clock cycle (MClk), thus accumulating the ramping time. The low and high voltage thresholds (denoted herein $-V_{th}$ and $+V_{th}$) are the switching points of hysteresis comparators (Schmitt triggers) **A1** through **A4** (only **A1** shown in FIG. 2).

[0027] Ramp signals $V1$ through $V4$ are generated by alternately turning on forward and reverse current generators, such as $IS1+$ and $IS1-$, at a desired rate. With reference to converter **61**, when $IS1+$ is on, a constant current flows into C_{x1} , generating an increasing voltage signal ramp. Unless prematurely terminated, the $V1$ signal will ramp up until comparator **A1** triggers at $+V_{th}$. At that point, $IS1+$ turns off. A voltage signal ramp down then occurs when source $IS1-$ turns on, and can continue until comparator **A1** is triggered at threshold $-V_{th}$. The ramp up, ramp down cycle is repeated a desired number of times depending on required measurement resolution, response times, and so forth. Each of the timed-slope converters is connected to circuitry **65** that can include the integration counter or other counters that control all of the

channels (such as a clip counter as exemplified in FIG. 4, or a period counter as exemplified in FIGS. 5 and 6), as well as serial I/O ports (SI/O) and an interrupt request port (IRQ) coupled to a microprocessor (not shown), for example.

[0028] FIG. 3 indicates a time sequence for an example circuit operation in the case where C_{x2} , C_{x3} , and C_{x4} are equal and C_{x1} is larger than C_{x2} , C_{x3} , and C_{x4} (the ramps in FIG. 3 could represent, for example, C_{x1} being about 15% larger). FIG. 3 indicates ramping of signals $V1$ through $V4$ between thresholds $-V_{th}$ and $+V_{th}$, when the comparator triggers $Trig1$ through $Trig4$ go high and low, when the $IS+$ and $IS-$ currents are turned on and off, the accumulated counts in the counters $Ctr1$ and $Ctr2$ through $Ctr4$, and the main clock MClk cycles. Also indicated in FIG. 3 are various times $t0$ through $t16$ at which various events take place. It should be noted that dashed lines are generally used to represent parameters associated with timed-slope converter **61** (measurement channel **1**), and contiguous lines are generally used to represent parameters associated with the timed-slope converters **62** through **64** (measurement channels **2** through **4**). The same conventions are used in FIGS. 4 through 6.

[0029] Because C_{x1} is larger than the other capacitances, the voltage signal ramp of $V1$ lags behind the voltage signal ramps of $V2$ through $V4$. The main clock MClk frequency can be any suitable frequency that provides multiple clock cycles over an expected range of ramping times, for example the MClk frequency may be about 10 MHz to 30 MHz. The periods of the ramp signals $V1$ through $V4$ (i.e., one full ramp up, ramp down cycle) have frequencies controlled by the magnitudes of currents from sources $IS+$ and $IS-$, and the capacitances C_{x} . In analog capacitive touch sensor examples, the frequencies of the voltage ramps might be in a range of about 20 KHz to about 200 KHz.

[0030] In exemplary embodiments, a measurement sequence starts on the rising edge of an MClk cycle, shown at $t0$ in FIG. 3. Four counters $Ctr1$ through $Ctr4$ increment counts at the end of each MClk cycle for each of the respective signals $V1$ through $V4$ as they ramp. The counter for each signal stops incrementing at the next rising edge of MClk that occurs after the respective signal reaches the voltage threshold ($+V_{th}$ for forward ramps and $-V_{th}$ for reverse ramps). For example, in FIG. 3, $Ctr2$ through $Ctr4$ stop at $t2$ with twelve increment counts. A stopped counter remains stopped until all the channels have reached the threshold. For example, at $t4$, $Ctr1$ is stopped at an increment count of fourteen, and since all four channels have reached the voltage threshold by time $t4$, all counters $Ctr1$ through $Ctr4$ are re-started and all voltage signals $V1$ through $V4$ begin reverse ramps (note that $Ctr1$ is stopped and immediately re-started at $t4$).

[0031] In certain embodiments, when the voltage threshold is reached on a signal channel, the ramping reverses direction (independent of other ramps and independent of MClk). For example, when the $+V_{th}$ threshold is reached at time $t1$ during a forward ramp of voltage signal $V2$, the output $Trig2$ of comparator **A2** switches to high, turning off the $IS2+$ current source and simultaneously turning on the $IS2-$ source. In FIG. 3, ramps $V2$ through $V4$ are shown to reverse at time $t1$, and ramp $V1$ is shown to reverse at time $t3$. Such ramp reversing terminates at the next rising edge of MClk, the same time that the respective channel's counter is stopped (e.g., at time $t2$ for ramps $V2$ through $V4$, and a time $t4$ for ramp $V1$). The $IS-$ source of the respective channel is turned off when its

counter is stopped, resulting in a zero slope, and effecting a delay as the channel waits for all the other channels to reach the threshold.

[0032] In FIG. 3, voltage signals V2 through V4 reverse at time t1 for the remainder of the current MClk cycle, which ends at time t2. At time t2, the counters for signal channels V2 through V4 are stopped, and the signal ramps are held at zero slope (i.e., delayed). At time t3, signal V1 reaches comparator A1's threshold (+Vth), and V1 reverses to a negative slope. By time t3, all the voltage signals have reached the threshold. Thus, in the embodiment shown in FIG. 3, all the voltage signals V1 through V4 are concurrently ramped down starting at time t4, which is the next rising edge of MClk. Note that the ramp down of voltage signal V1 that started at the reversal at time t3 need not be interrupted. It should be noted that, while ramp reversals upon reaching voltage thresholds is exemplified in FIG. 3 (as well as in FIGS. 4 through 6), the present invention is not limited to circuits or methods that implement such ramp reversals.

[0033] Continuing with the ramping cycles as shown in FIG. 3, each negative ramp stops when the -Vth threshold of its comparator is reached and the comparator output switches to low, turning off the IS- current source. As with the positive ramps, in certain embodiments the ramp can be reversed for the remainder of the MClk cycle during which the threshold was reached. For example, signal ramps V2 through V4 reverse at time t5, and signal ramp V1 reverses at time t7. After a channel reaches the threshold, the channel's counter stops at the next rising edge of MClk. For example, Ctr2, Ctr3, and Ctr4 stop at time t6 with total accumulated increment counts of twenty-four. A delay can then be effected on the channels of signal ramps V2 through V4, resulting in zero slope as the channels wait for signal V1 to reach the threshold -Vth. At time t7, voltage signal V1 reaches threshold -Vth (and in certain embodiments immediately reverses slope). At time t8, the counter Ctr1 is stopped at an increment count of twenty-eight, but since all four comparators A1 through A4 have been triggered by time t8, all counters Ctr1 through Ctr4 are re-started and voltage signals V1 through V4 ramp positive together.

[0034] This process (i.e., cycling the signal ramps between threshold levels and counting the clock cycles needed for each channel to complete a ramp) continues until all the channels have gone through N full cycles, called the integration period, which can be determined by an integration counter. The integration period can be a predetermined number of cycles, or can vary based on application and conditions (for example, capacitance measurement accuracy and resolution may be enhanced by increasing the integration period, and response time may place an upper limit on the integration period). In the example of FIG. 3, N=2 so that the integration period extends from time t0 to time t16, when all the channels have completed two full up and down voltage ramp cycles.

[0035] During the integration period, counter Ctr1 cumulatively increments fifty-six counts and counters Ctr2 through Ctr4 each cumulatively increment forty-eight counts. When the integration period is completed, an interrupt request (indicated by IRQ in FIG. 2, for example) is issued to a microprocessor, and the cumulative values held in the counters for each channel are transferred to the microprocessor. The cumulative number of counts for a channel relative to the other channels is proportionate to the capacitance of that channel relative to the others. In FIG. 3, counter Ctr1 has the highest number of cumulative counts, indicating that capacitance C_{x1}

has the largest magnitude. The ratios of the cumulative counts in one channel to the cumulative counts in the other channels indicate the ratios of the capacitances. In touch sensor embodiments, ratios of capacitances can be used to determine the touch location (calculations will depend on sensor configuration).

[0036] As discussed, if a channel reaches the voltage signal threshold before one or more of the other channels, the voltage level of that channel is held near the threshold level until one or more of the other channels also reach the threshold. As such, rather than starting a reverse direction ramp upon reaching the threshold, a delay is effected so that the reverse direction ramp can be started concurrently on multiple channels. Effecting delays on one or more channels so that the next ramp can be initiated concurrently on multiple channels allows the ramp cycles of the channels to be approximately in phase, assuming the capacitances being measured are similar in magnitude. Keeping the ramp cycles approximately in phase (i.e., all positive ramps occurring during the same time frame, and all negative ramps occurring during the same time frame) can have the effect of mitigating inter-channel currents (i.e., currents flowing between capacitance measurement locations) by keeping any differences between the voltage signals on the various channels at any given time relatively low. Reducing inter-channel currents can be particularly desirable when channels are connected to a 4-wire capacitive sensor where channels may be connected through a resistance. When individual channels are connected to electrodes in a matrix sensor, in-phase signal ramps may also be desired to minimize currents flowing through mutual capacitances of electrodes.

[0037] It will be appreciated that, although circuit operations are described and shown in FIGS. 3 through 6 in terms of bi-directional ramping (i.e., ramping up to a high threshold followed by ramping down to a low threshold), methods and circuits of the present invention can be implemented using unidirectional ramps such as used in the capacitance measurement circuits disclosed in U.S. Pat. No. 6,466,036, fully incorporated herein by reference. For example, in certain embodiments, the voltage signals are concurrently ramped up to a threshold, and after effecting a delay (e.g., to wait until all signal channels reach the threshold, to wait a predetermined amount of time, and so forth) the signal channels can be concurrently reset back to zero (e.g., in step function fashion) followed by re-starting the ramp ups. It will further be appreciated that, although circuit operations are described and shown in FIGS. 3 through 6 in terms of smooth ramping, for example due to application of a constant current, methods and circuits of the present invention can be implemented by applying a pulsed current or voltage, resulting in a stepped ramp. For example, U.S. Pat. No. 6,466,036 discloses a circuit that rapidly pulses current sources on and off to generate an incrementally stepped voltage ramp.

[0038] FIG. 4 shows an example of circuit operation similar to that shown in FIG. 3, except that each of the voltage signals V1 through V4 are delayed between ramp cycles thereby forming the clipped sawtooth patterns seen in FIG. 4. In certain embodiments, a clip counter (CCtr) and some logic can be added to the controller to generate the clipped sawtooth, which can result in generating fewer harmonics relative to a full sawtooth signal. The clip counter CCtr has the effect of adding a delay (for example, a predetermined number of MClk cycles) prior to the start of the next voltage ramp. In the example shown in FIG. 4, ramps V1 through V4 are stopped

at time t_4 , and all four signals are held at a constant value for M cycles of $MClk$, where in this case M equals two. All ramp downs are then re-started at time t_{4a} . The same delay is effected at times t_8 , t_{12} , and t_{16} , with respective next ramps starting at times t_{8a} , t_{12a} and t_{16a} . All other functions of the controller operate as described with respect to FIG. 3.

[0039] In addition to forming signals V_1 through V_4 into clipped sawtooths, signals V_1 through V_4 may also be held to a fixed frequency, for example as shown in FIG. 5. A period counter (PCtr) can be used to hold the signal ramps V_1 through V_4 to a fixed frequency determined by the period of the PCtr, regardless of capacitance changes (within a range). For the circuit operation exemplified by FIG. 5, the controller functions as described with respect to FIG. 3, with the following exceptions. Period counter PCtr is added to the controller (for example at logic block 65 of controller 60 shown in FIG. 2. Period counter PCtr can be clocked by the main clock, $MClk$, for example. In the embodiment shown, all channels are ramped down starting at time t_{4a} when PCtr goes low and all the comparator trigger signals Trig are high, and a new ramp up starts at time t_{8a} when all the comparator trigger signals Trig are low and the PCtr output goes high. When the ramp up is completed on all signal channels by time t_{12} , the voltage levels are held constant until the PCtr output goes low, at which point a new ramp down can be initiated at time t_{12a} (assuming all four comparator trigger signals are high).

[0040] As discussed, synchronizing the starts of the voltage signal ramps can be used to mitigate current flow between the measurement locations that can be caused by large voltage differences. Further refinement of current flow mitigation can be achieved in certain embodiments, as illustrated with respect to FIG. 6. Consider a rectangular 4-wire touch sensor where the measurement locations are at the four corners of a resistive plate. Any mismatch in signals V_1 through V_4 can generate accuracy-reducing currents flowing from corner to corner. The left half of FIG. 6 (first ramp up plus first ramp down) is the same as the left half of FIG. 5, and shows a V_1 waveform mismatched from waveforms V_2 , V_3 and V_4 , which ramp up as described previously. The degree of mismatch is indicated by the area between V_1 and V_2 through V_4 . In the example shown, the operation is the same as described for FIG. 5 except as indicated in the following.

[0041] Each ramp's duration is measured by respective counters Ctr1 through Ctr4, as with FIGS. 3 through 5. Differences between ramp durations are calculated periodically, and the start times of subsequent voltage ramp cycles on the respective channels are adjusted accordingly, for example in proportion to half the differences in ramp times. In FIG. 6, the ramp durations for voltage signals V_2 through V_4 are equal, ending at time t_2 , and the ramp duration for voltage signal V_1 is longer, ending at time t_4 . The difference in numbers of counts for signal V_1 to complete its ramp up versus the other signals is denoted by $\Delta Ct+$, which in the case illustrated by FIG. 6 is two $MClk$ cycles. For the subsequent negative ramps, which end at time t_6 for signals V_2 through V_4 and at time t_8 for signal V_1 , the differential count $\Delta Ct1-$ is shown to also equal two $MClk$ cycles, although in the general case they need not be the same. Taking into account the count differentials $\Delta Ct+$ and $\Delta Ct-$, the next ramp up cycle of V_1 starts at time t_{8a} , which is one $MClk$ count before starting the ramp ups of the V_2 , V_3 and V_4 voltage signals at time t_{6a} (i.e., half of the average count differential determined in the previous up and down ramps).

[0042] Adjusting the relative start times of the ramps in relation to measured ramp differentials can further mitigate the effects of corner to corner currents. As shown in FIG. 6, the adjusted start times results in the voltage signal ramp of V_1 matching the voltage signal ramps of V_2 through V_4 in the middle of the ramp up cycle so that the net corner to corner current flow adds to 0. This is illustrated by the areas between V_1 and V_2 through V_4 on the right side of FIG. 6. On both the ramp ups and ramp downs, voltage signal V_1 is greater than V_2 through V_4 for half the time and less than V_2 through V_4 for half the time, so that currents between them will equalize during each ramp cycle.

[0043] In certain embodiments, the process of measuring differential counts ΔCt and re-adjusting ramp start times is iterative and continuous, so that differentials measured during one ramp cycle are adjusted for in a subsequent ramp cycle, or alternatively, differentials measured during an integration cycle (for example over several ramp cycles) can be adjusted for in subsequent integration cycles. Refined phase alignment such as illustrated in FIG. 6 can be utilized in any of the operations illustrated in FIGS. 3 through 5.

[0044] The level of current required to generate voltage signal ramps as illustrated in FIGS. 3 through 6 is dependent on the magnitudes of the capacitances to be measured as well as the ramp durations. For example, assuming a 4-wire capacitive touch sensor implementation operated as described with respect to FIG. 3 where $V_{cc}=3V$, the difference between thresholds $+V_{th}$ and $-V_{th}$ is 1V (e.g., $+V_{th}$ at $\frac{2}{3} V_{cc}$ and $-V_{th}$ at $\frac{1}{3} V_{cc}$), and where the capacitances are on the order of 1000 pf. In such a case, $IS+$ and $IS-$ currents of 100 μA yield ramping periods of about 50 KHz.

[0045] In certain embodiments, some of the parameters may be programmable, for example the integration cycles (see FIGS. 3 and 4), the integration time (e.g., when a period counter is used, such as shown in FIG. 5, to indicate a fault if capacitance is overloaded so signal ramps do not reach V_{th} during a period), the period counter (if implemented), the clip counter (if implemented), the voltage signal period (variable as a percentage of $MClk$), the $IS+$ and $IS-$ current levels, and so forth.

[0046] FIG. 7 shows an exemplary drive circuit 100 that can be used in the timed-slope converters 61 through 64 as shown in FIG. 2. Circuit 100 includes a time-slope converter 104 that has a comparator A1 providing a trigger signal Trig1 to control logic 106 that regulates stopping and starting of a counter 108, much like the converter 61 shown in FIG. 2. Drive circuit 100 additionally includes a tri-state driver D1 and a resistor R1, which replace the current sources $IS1+$ and $IS1-$ shown in the converter 61 of FIG. 2, to generate currents into capacitor C_x1 . All of the operations illustrated in FIGS. 3 through 6 can be generated using circuit 100, although the voltage ramps may be less linear. Analog current sources are not required in a controller using drive circuit 100. As above, assuming a 4-wire capacitive touch sensor implementation operated as described with respect to FIG. 3 where $V_{cc}=3V$, the difference between thresholds $+V_{th}$ and $-V_{th}$ is 1V (e.g., $+V_{th}$ at $\frac{2}{3} V_{cc}$ and $-V_{th}$ at $\frac{1}{3} V_{cc}$), and where the capacitances are on the order of 1000 pf, using a 15K Ω resistor for R1 would source about 100 μA with an average voltage drop of 1.5V. While FIG. 7 indicates applying a voltage through a resistance, it will be recognized that a voltage can be applying through any impedance, such as resistor R1 in FIG. 7, a capacitor, and the like.

[0047] Certain embodiments of the present invention measure elapsed voltage signal ramp times using accumulators. Accumulators can be used in the embodiments described above to measure time in a digital counter, in an analog integrator, or in a combination of both. Analog integrators start and stop quickly, thus being capable of measuring with high resolution. Digital counters have higher dynamic range, but temporal resolution may be limited by the clock frequency (e.g., MClk). Thus, in certain embodiments the circuit shown in FIG. 8 may be a desirable accumulator circuit.

[0048] FIG. 8 shows an example of a sigma delta A-D converter 200 configured to measure time segments with high resolution. Capacitor C1 forms an analog integrator. A known reference current I1 feeds capacitor C1 when switch S1 is closed. Switch S1 is closed when the comparator trigger signals (e.g., +Trig and -Trig as in FIG. 3) are both high, that is when the voltage signal is ramping between low and high voltage thresholds. Sigma delta control logic 210 closes switch S2 for a fixed time when the input of A1 is above the $V_{cc}/2$ threshold, discharging integrator capacitor C1 incrementally. Each time switch S2 is closed, counter 220 is incremented. Counter 220 may be read periodically, and the incremental difference in counts between readings is proportionate to the total time that switch S1 is closed during the period.

[0049] As described in this document, current flow between capacitance measurement locations can be mitigated by controlling the phases of the drive signals. It will be appreciated that, for common capacitance-to-ground measurements systems such as the touch sensor systems shown in FIGS. 1A and 1B, driving the signals in phase can be used to desirably minimize mutual (inter-electrode) capacitance. In other systems, driving adjacent capacitance measurement locations out of phase can be used to enhance the measurement effect of inter-electrode mutual capacitance. For example, it can be desirable to measure, and therefore enhance, inter-electrode mutual capacitance in touch detection products that utilize shunt capacitance measurements, such as the AD7142, commercially available from Analog Devices, Inc. Phase control methods described herein may be used to adjust measurement channels to be in phase or out of phase.

[0050] The foregoing description of the various embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. For example, the detection methodologies described herein may be used in connection with a wide variety of touch implements, including tethered implements and implements that house a battery or other power source. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

1. For use in a touch sensor device that measures capacitances at a plurality of locations on a touch surface in response to a touch object coupling to the touch surface at a touch position, the capacitances being measured by applying electrical charge to the plurality of locations to ramp respective voltage signals between a first reference level and a second reference level, the method comprising:

controlling the phase of the voltage signal ramps to mitigate currents flowing between the locations.

2. The method of claim 1, wherein the voltage signal ramps are alternated between ramping up from the first reference

level to the second reference level and ramping down from the second reference level to the first reference level, and wherein controlling the phase comprises concurrently ramping up the voltage levels and concurrently ramping down the voltage levels.

3. The method of claim 1, wherein the voltage signals are ramped in the same direction, from the first reference level to the second reference level, with a reset back to the first reference level between each ramp, and wherein controlling the phase comprises concurrently ramping the voltage levels and concurrently resetting the voltage levels.

4. The method of claim 1, wherein applying electrical charge to the plurality of locations includes applying a continuous current, applying a pulsed current, or applying a voltage through an impedance.

5. The method of claim 1, wherein controlling the phase of the voltage signal ramps comprises concurrently starting the voltage signal ramps.

6. The method of claim 5, wherein concurrently starting the voltage signal ramps comprises effecting a delay on at least one voltage signal ramp that has reached a threshold level prior to other voltage signal ramps reaching the threshold level.

7. The method of claim 6, wherein the delay is a predetermined delay started upon the at least one voltage signal reaching the threshold level.

8. The method of claim 6, further comprising adjusting the delay to minimize average differences among the voltage signal ramps.

9. The method of claim 5, wherein the voltage signal ramps are regulated by a period timer that starts the voltage signal ramps at the same time according to a fixed frequency.

10. The method of claim 1, wherein controlling the phase of the voltage signal ramps comprises determining time differentials between when respective voltage signal ramps reach a threshold level, and using the determined time differentials to adjust subsequent ramp starting times.

11. The method of claim 1, further comprising measuring capacitances associated with each location by measuring ramp times for respective voltage signal ramps.

12. The method of claim 11, further comprising using the measured capacitances to determine the touch position.

13. A touch sensor device that measures capacitances at a plurality of locations on a touch surface in response to a touch object coupling to the touch surface at a touch position, the capacitances being measured by applying electrical charge to the plurality of locations to ramp respective voltage signals between a first reference level and a second reference level, the device comprising:

a signal control circuit that controls the phase of the voltage signal ramps to mitigate currents flowing between the locations.

14. The touch sensor device of claim 13, wherein the signal control circuit controls the phase by concurrently starting the voltage signal ramps.

15. The touch sensor device of claim 14, wherein the signal control circuit concurrently starts the voltage signal ramps by effecting a delay on at least one voltage signal ramp that has reached a threshold level prior to other voltage signal ramps reaching the threshold level.

16. The touch sensor device of claim 15, wherein the delay is a predetermined delay started upon the at least one voltage signal reaching the threshold level.

17. The touch sensor device of claim 15, wherein the signal control circuit adjusts the delay to minimize average differences among the voltage signal ramps.

18. The touch sensor device of claim 14, wherein the signal control circuit regulates the voltage signal ramps using a period timer that starts each voltage signal ramp at the same time according to a fixed frequency.

19. The touch sensor device of claim 13, wherein the signal control circuit controls the phase of the voltage signal ramps by determining time differentials between when respective voltage signal ramps reach a threshold level, and using the determined time differentials to adjust subsequent ramp starting times.

20. For use with a device that measures capacitances at a plurality of locations, each location associated with a capacitance measurement channel to ramp respective voltage signals on the respective capacitances, a method comprising:

- (a) concurrently initiating forward-direction voltage signal ramps on multiple channels; and
- (b) effecting a delay on the forward-direction voltage signal ramp of at least one channel in response to reaching a high voltage signal threshold.

21. The method of claim 20, further comprising:

- (c) concurrently initiating reverse-direction voltage signal ramps on the multiple channels; and
- (d) effecting a delay on the reverse-direction voltage signal ramp of at least one channel in response to reaching a low voltage signal threshold.

22. The method of claim 21, further comprising repeating steps (a) through (c) after step (d).

23. The method of claim 20, wherein the delay is adjusted to minimize differences among forward-direction and reverse direction voltages.

24. The method of claim 20, further comprising counting clock cycles for the multiple channels during the voltage signal ramps and correlating the number of clock cycles for a given channel with the capacitance being measured by the given channel.

25. The method of claim 24, wherein voltage signal ramp initiation steps are synchronized with a clock cycle.

26. The method of claim 20, wherein the delay ends upon all of the multiple channels having reached the high voltage signal threshold.

27. The method of claim 20, wherein the delay ends after a predetermined time.

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