

[54] **CHARACTER GENERATION SYSTEM
HAVING BOLD FONT CAPABILITY**

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[51] Int. Cl. **G06f 3/14**

[58] Field of Search 340/324 A; 178/15, 30; 355/20; 95/4.5

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ABSTRACT

In a character generation system a bold font is generated by causing the last dot of each horizontal line of dots from which a standard character is formed to be repeated. A loop-gated shift register converter arrangement determines from an interrogated character store output which dot is the last in each horizontal dot row of the selected character, and then presents the next following register stage.

18 Claims, 3 Drawing Figures

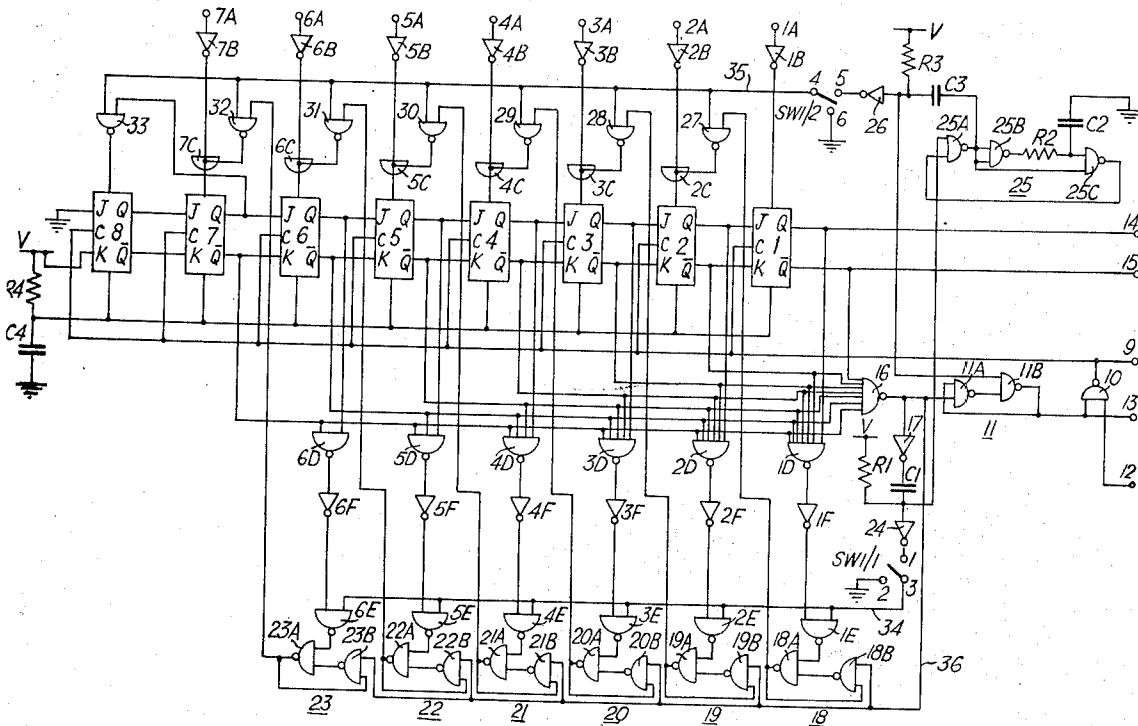


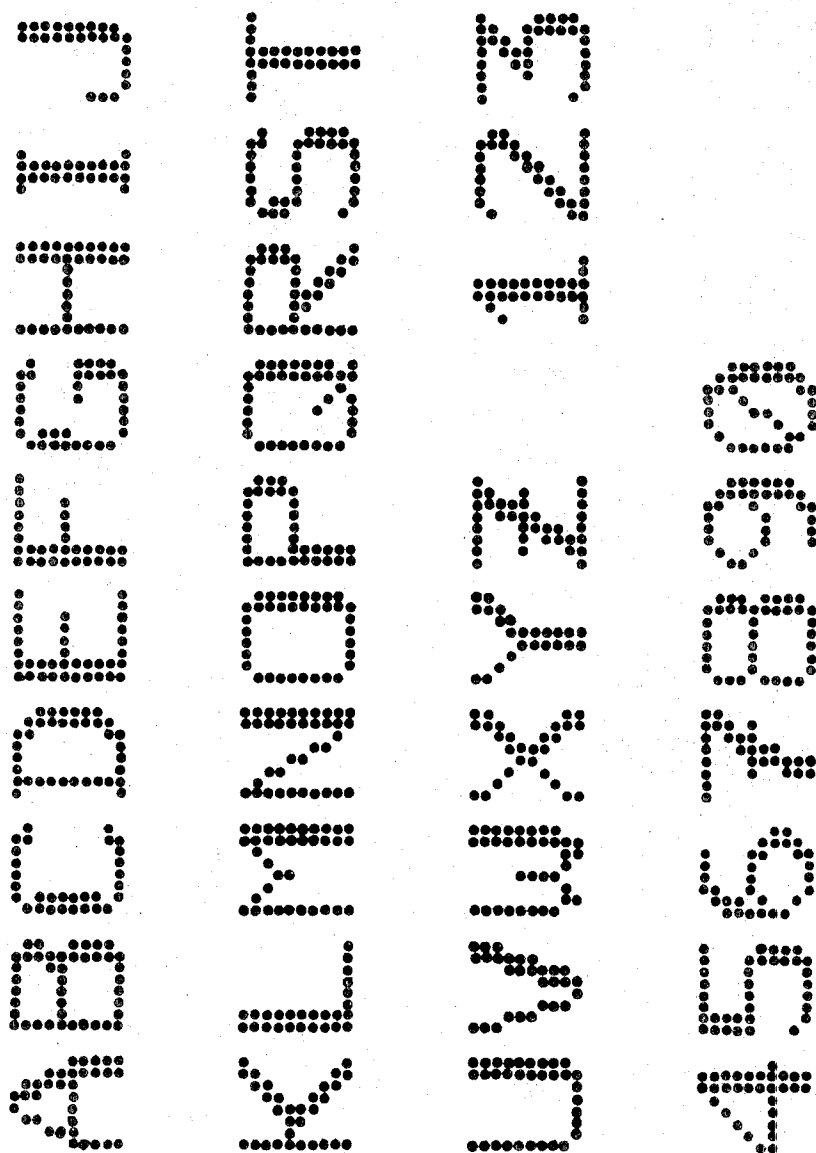
Fig. 1.



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Fig. 2.



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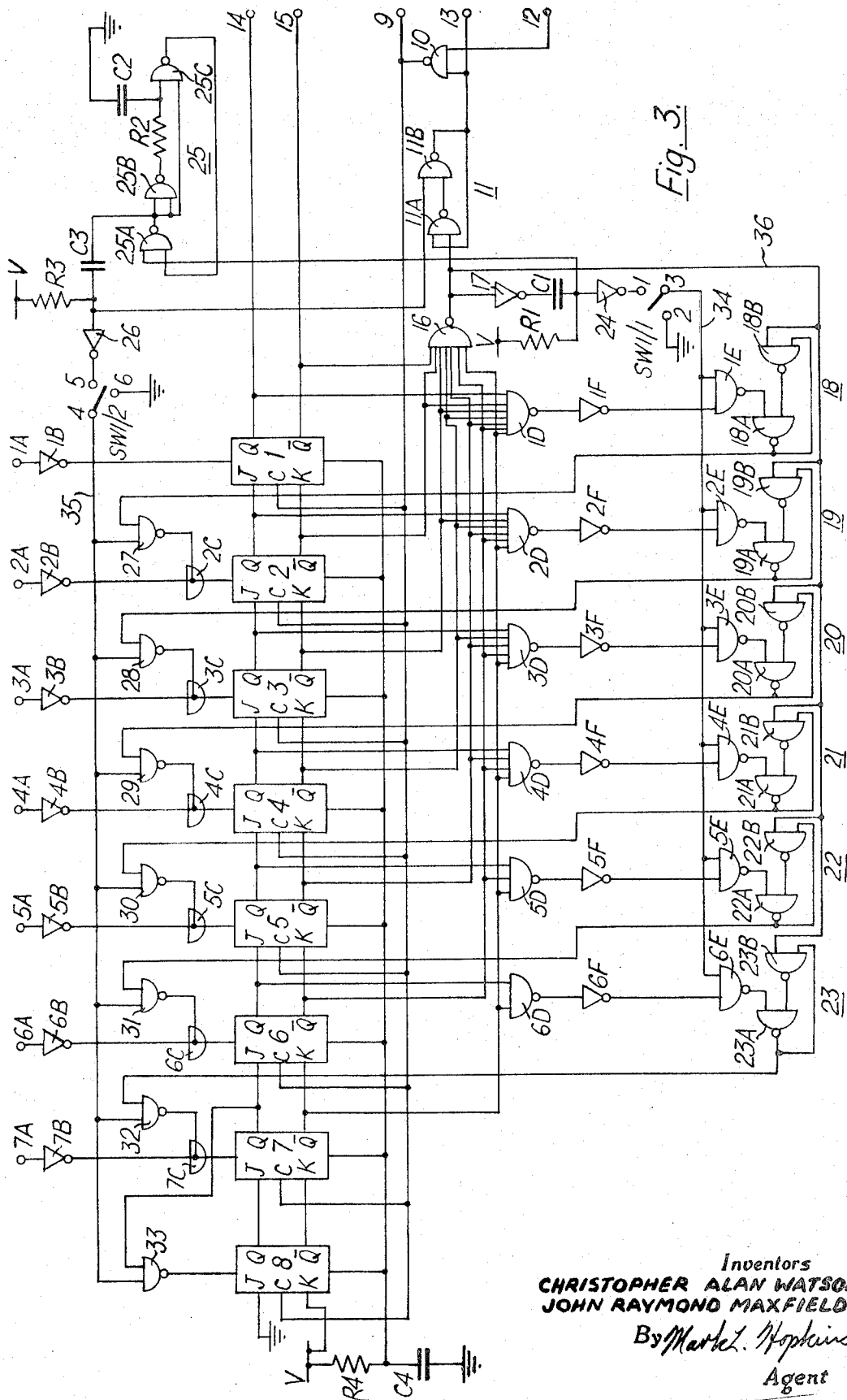


Fig. 3.

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CHARACTER GENERATION SYSTEM HAVING BOLD FONT CAPABILITY

BACKGROUND OF THE INVENTION

The invention relates to a character generation system having particular but not necessarily exclusive application to electrographic printing and/or display apparatus.

Such apparatus is defined as being of the kind wherein the recording surface of either a print drum or bank is selectively magnetized or electrostatically charged to form a pattern or latent image thereon representative of information contained in a signal applied to the apparatus, and wherein the print drum or band is passed through or relative to a powder applicator containing powder that is attracted to the latent image to develop same and to form a powder image which may be viewed at a display position and/or transferred to a permanent record by printing means which form part of the apparatus.

In general, character generation systems employed with electrographic printing and/or display apparatus of the kind as hereinbefore defined are of the type wherein coded characters which are representative of the characters to be generated by the system, are stored in at least one line store which is capable of storing a number of coded characters, wherein the coded characters are sequentially read from the line store and directed to a character store, wherein at least part of a selected one of the coded characters is interrogated in a character to cause a signal to be generated at the output thereof which is representative of at least part of the selected character and which is fed to means which direct the signal to character forming means whereat the selected character is formed from a dot matrix, and wherein the sequential reading of the contents of the line store is repeated until signals representative of the complete form of the number of coded characters have been directed to the character forming means. An example of this type of character generation system is outlined in co-pending U.S. Pat. application Ser. No. 762,455, filed Sept. 25, 1968.

In electrographic apparatus it is sometimes necessary, for the sake of emphasis or distinction, to produce two or more character fonts. However, the cost and possibly space availability would be prohibitive if the additional fonts required additional character stores.

For this reason it has previously been proposed, for example in co-pending U.S. Pat. application Ser. No. 809,896, filed Mar. 24, 1969, that a second character font, for example a simulated bold or italic character font, could be obtained by modifying the standard font. In the case of the bold font, all vertical lines of the character shape are thickened by electronically repeating dot positions in the horizontal lines of dots from which the character is formed. In applications where small character storage matrix sizes are necessary, the character shapes are made up of lines with a thickness of one dot width, and when the bold character font modification is introduced, the generated characters tend to be unsatisfactory in that the spaces between vertical lines of the standard character become filled, either completely or to an extent that the printed character may be illegible.

SUMMARY OF THE INVENTION

The invention provides a character generation system, of the type as hereinbefore referred to, including means for converting a standard font into a bold font, said means causing the last dot of each horizontal line of dots from which a standard character is formed to be repeated.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features according to the invention will be better understood from the following description when taken in conjunction with the accompanying drawings in which:

FIG. 1 illustrates character formats of a standard font;

FIG. 2 illustrates the character formats of a bold font which has been converted from the standard font of FIG. 1 by the character generation system according to the invention; and

FIG. 3 diagrammatically illustrates that part of the character generation system according to the invention for converting a standard font into a bold font.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Character generation systems of the type as hereinbefore referred to are, in general, arranged to generate an N-bit parallel signal representative of at least part of a selected character at a stage of the system which precedes the character forming means. This signal could in practice be generated at the interrogated character store when it is constituted by a storage matrix or at the means which direct the signal to the character forming means when they include for instance a switching matrix. This signal is representative of at least part of a standard character, for example any one of the characters illustrated in the drawing according to FIG. 1. In order to convert the standard character into a bold character, i.e. any one of the respective characters illustrated in the drawing according to FIG. 2, it is necessary to use a character generation system which includes the character font converting unit diagrammatically illustrated in the drawing according to FIG. 3.

It is assumed by way of example in the drawing according to FIG. 3 that the standard character (FIG. 1) is formed from a 7 (horizontal) by 10 (vertical) dot matrix and the N-bit parallel signal which is representative of at least part of a selected character is therefore a 7-bit parallel signal which is applied to the input terminals 1A to 7A of the character font converting unit.

The character font converting unit is basically a shift register which includes a number of stages 1 to 8 which are each formed by a flip-flop circuit. The flip-flops are connected in cascade i.e. the J and K inputs of each stage except stage 8 are respectively connected to the Q and $\bar{Q}$ outputs of the preceding stage, and one of the two signal inputs to each stage are connected together and to the junction of a resistance R4 and a capacitance C4 which are connected in series between earth potential and an electrical supply voltage V. Each of the other of the two signal inputs to each of the stage 1 to 7 is respectively connected to a separate one of the input terminals 1A to 7A respectively via an invert gate 1B to 7B. Each of the stages 2 to 7 have a wired-OR gate interposed between the invert gates 2B to 7B and the other of the two signal inputs of the stages i.e. the wired-OR gates 2C to 7C. The clock pulse input C of the stages 1 to 8 are connected to a terminal 9 and to the output of a NAND gate 10. One input to the gate 10 is connected to a terminal 12 and the other input is connected to a terminal 13 and to the output of a memory element indicated generally by the reference 11 and formed by NAND gates 11A and 11B. The output of the element 11 which is the output of the gate 11B, is connected to one of the inputs of the gate 11A whose output is connected to one of the inputs of the gate 11B. The two inputs to the element 11 are respectively connected to the other of the inputs of the gates 11A and 11B.

The Q and $\bar{Q}$ outputs of stage 1 are respectively connected to terminals 14 and 15 and the J and K inputs of stage 8 are respectively connected to earth potential and an electrical supply voltage V.

The Q outputs of the stages 1 to 6 are respectively connected to one input of NAND gates 1D to 6D. The other inputs of gate 1D are connected to the $\bar{Q}$ outputs of stages 2 to 7; the other inputs of gate 2D are connected to the $\bar{Q}$ outputs of stages 3 to 7; the other inputs of gate 3D are connected to the $\bar{Q}$ outputs of stages 4 to 7; the other inputs of gate 4D are connected to the $\bar{Q}$ outputs of stages 5 to 7; the other inputs of gate 5D are connected to the $\bar{Q}$ outputs of stages 6 and 7; and the other input of gate 6D is connected to the $\bar{Q}$ output of stage 7. The Q outputs of stages 1 to 7 are connected to the inputs of a NAND gate 16. The output of the gate 16 is connected to one output of the memory element 11, i.e. to the said other input of the gate 11A, to the input of an invert gate 17 and to one of the inputs of memory elements which are indicated generally by the references 18 to 23. The elements 18

to 23 are respectively formed by two NAND gates 18A, 18B to 23A, 23B.

The other of the inputs of the memory elements 18 to 23 are respectively connected to the outputs of NAND gates 1E to 6E. One of the inputs of the gates 1E to 6E are respectively connected to the outputs of the gates 1D to 6D respectively via invert gates 1F to 6F. The other of the inputs of the gates 1E to 6E are connected together and to the common terminal 3 of the pole SW1/1 of a two-pole, two-way, electrical switch SW1. Terminal 2 of the pole SW1/1 is connected to earth potential and terminal 1 is connected to the output of invert gate 17 via a capacitance C1 and an invert gate 24. The junction of the capacitance C1 and the gate 24 is connected to the electrical supply voltage V via a resistance R1 and to the input of a monostable circuit which is indicated generally by the reference 25.

The monostable circuit 25 comprises a NAND gate 25A having its output connected to the inputs of a NAND gate 25B and to one input of a NAND gate 25C. The output of the gate 25B is connected to the other input of the gate 25C via a resistance R2 and to earth potential via the resistance R2 and a capacitance C2 which are connected in series. The input of the circuit 25 is connected to one input of the gate 25A and the output is connected to the output of the gate 25A. The other input of the gate 25A is connected to the output of the gate 25C.

The output of the circuit 25 is connected to the electrical supply voltage V via a capacitance C3 and a resistance R3 which are connected in series. The junction of the resistance R3 and capacitance C3 is connected to a terminal 5 of the pole SW1/2 of the electrical switch SW1 via an invert gate 26 and to the other input of the memory element 11 i.e. to the said other input of the gate 11B. Terminal 6 of the pole SW1/2 is connected to earth potential and the common terminal 4 is connected to one of the inputs of NAND gates 27 to 33.

The other of the inputs of the gates 27 to 32 are respectively connected to the outputs of the memory elements 18 to 23 and the other of the input of the gate 33 is connected to the Q output of the stage 7.

The output of the gates 27 to 32 are respectively connected to one of the inputs of the gates 2C to 7C and the output of the gate 33 is connected to a signal input of the stage 8.

OPERATION

The font change is achieved by causing the last dot of each horizontal line of dots from which a standard character is formed to be repeated. This is effected by one of a number of loops of gates which are each associated with one of the stages of the shift register. The particular loop of gates determines the last dot of the horizontal line of dots and then presets the stage following the stage that holds this dot. During this period, the clock input is inhibited.

In some characters, for example the letters E, F and P, the last dot may be actually in the left-hand column of dots from which the character is formed, and in others for example the letters O, B and M, in the right-hand column of dots. Thus although the font change is essentially a bolding of part of a character, it is not always the same part of each character that is affected.

It should be noted that the $\bar{Q}$ output of a shift register stage is a logical 1 when the Q output is a logical 0 and vice versa.

In operation, the electrical switch SW1 is such that the common terminals 3 and 4 are respectively connected to terminals 1 and 5, and an oscillatory input which is used to drive the shift register is applied to the terminal 12 and therefore to an input of the gate 10. The clock rate for the shift register is gated by the gate 10 which is driven by the memory element 11.

In the quiescent condition the output of the gate 16 is at a logical 0 condition, signifying that the Q outputs of all the stages of the shift register are in the logical 0 condition. Under these conditions the signals on the lines 34 to 36 and the out-

put of the memory element 11 are representative of a logical 0.

It will be assumed by way of example that the code 1111000 which is representative of a horizontal line of dots is applied to the input terminals 1A to 7A in order to illustrate the functioning of the character font converting unit. Under these conditions, the Q outputs of the stages 1 to 4 will be changed to a logical 1 condition and therefore the $\bar{Q}$ outputs of these stages will be changed to a logical 0 condition. Since the gate 16 is such that its output is only a logical 0 when all the inputs are at a logical 1 condition, the output of gate 16 in the presence of this input signal changes to a logical 1 condition thereby releasing the reset line 36 of the memory elements 18 to 23 and the memory element 11.

The positive edge formed by the transition of the output of the gate 16 is inverted by the gate 17 and differentiated by the resistance R1 and the capacitance C1.

The differentiated pulse triggers the monostable circuit 25 and is also passed via the gate 24 and the pole SW1/1 to provide a positive pulse on the transfer line 34.

Simultaneously with this, the gates 1D to 6D are determining which of the stages 1 to 7 holds the last dot of the line i.e. which of the input terminals 1A to 7A has the last logical 1 input applied thereto.

With the quoted example, i.e. an input code of 1111000, the gate 1D has seven inputs, one of which goes to the Q output of stage 1 and the other six going to the $\bar{Q}$ outputs of the stages 2 to 7. The output of the gate 1D is normally a logical 1 and the output will only change to a logical 0 if all the inputs are at a logical 1 condition, i.e. if the Q output of the stage 1 is a logical 1 and the $\bar{Q}$ outputs of the stages 2 to 7 are at a logical 1 (the Q outputs are at a logical 0). Thus for the code 1111000, there are three logical 0 inputs and four logical 1 inputs to the gate 1D and therefore the output of this gate remains at a logical 1 condition. The same is the case for the gates 2D and 3D; however for the gate 4D which has four inputs (one to the Q output of stage 4 and three to the $\bar{Q}$ outputs of stages 5 to 7), all the inputs are at a logical 1 condition therefore the output of this gate changes from a logical 1 to a logical 0 condition.

The gates 5D and 6D also have inputs at both logical 0 and logical 1 conditions thus the output of each of these gates remains in a logical 1 condition.

Thus, for the cited example, the gate 4D is the only one whose output changes state and when the positive pulse occurs on the transfer line 34 the output of the gate 4E changes state i.e. from a logical 1 to a logical 0 causing the memory element 21 to be set in a manner such that the output of the gate 21A which is applied to one input of the gate 30 becomes a logical 1.

The trailing edge of the pulse produced by the monostable circuit 25 which is of sufficient duration to allow the foregoing to occur is differentiated by the resistance R3 and capacitance C3 and then the differentiated negative pulse is inverted by the gate 26 to provide a positive pulse on the transfer line 35. The delayed pulse on transfer line 35 changes the state of the gate 5C, since both inputs are at a logical 1 condition, and causes the presetting of stage 5 via the OR gate 5C. The differentiated pulse (negative) also triggers the memory element 11 thereby releasing the inhibit on the clock input to the shift register and allowing the "font-changed" character line to be shifted out at the terminals 14 and 15 to the following stage of the character generation system. Thus the last dot of the input code which is held at stage 4 has been repeated at stage 5.

The procedure outlined in preceding paragraphs holds for the repeating of all dot positions except the one associated with the input terminal 7A. For this dot position the repeated dot facility is achieved by the stage 8 and the gate 33. Stage 8 is set via the gate 33 only when the Q output of stage 7 is at a logical 1 condition i.e. when a logical 1 input signal appears at the input terminal 7A, and the delayed pulse appears on transfer line 35. Thus the dot position is repeated.

The gated oscillator signal is obtainable at the terminal 9 and it is used for the synchronization of subsequent stages of

the character generation system. An "inhibit and reset" control signal which is obtainable at the terminal 13 is utilized for alerting the recording head selection matrix each time a coded signal enters the character font converting unit.

Two transfer lines (34 and 35) are required because of the fact that, for the cited example, when stage 5 has been preset in order to repeat the last dot position, then gate 5D also changes state since its three inputs which are constituted by the Q output of stage 5 and the $\bar{Q}$ outputs of stages 6 and 7, are at a logical 1 condition. If only one transfer line were used, there would exist the possibility of the state of change of gate 5D being transferred thereby effecting the presetting of stage 6 and doubly-repeating the last dot position. However, the use of two transfer lines ensures that this cannot occur.

The "non-font-change" situation is selected by setting the electrical switch SW1 such that the common terminals 3 and 4 are respectively connected to terminals 2 and 6. This causes the transfer lines 34 and 35 to be connected to earth potential and the seven-bit code set in the shift register waits for the duration of the output pulse of the monostable circuit 25 before it is shifted out at the terminals 14 and 15 to the following stage of the character generation system.

In either position of the switch SW1 there is no necessity for further clock pulses to be generated when the final set 1 is taken out of the shift register (regardless of its position in the line of dots) since no information remains in the shift register. As this bit i.e. the final set 1, leaves the shift register, the gate 16 output returns to a logical 0 condition thereby causing all the font change memory elements to be reset and inhibited.

The input of each of the stages 1 to 8 which are connected together and to the junction of the resistance R4 and the capacitance C4 are the 'clear' inputs for the stages and they operate when the character font converting unit is switched-on, i.e. when the electrical supply is connected to the converting unit. At switch-on random setting of the stages 1 to 8 may occur.

It should be noted that while a serial output is obtained at the terminals 14 and 15, the character font converting unit may be adapted to provide a parallel output. This is effected by utilizing the stages 1 to 8 i.e. each of the flip-flops, as individual units and not as part of a shift register. Thus with this arrangement the Q outputs of each stage would be taken to a separate output terminal and the memory element 11, gate 10 and terminals 9 and 13 would be omitted since the clock pulses would not be required in the absence of the shift register mode of operation. The remainder of the converting unit would be operated in exactly the same manner to effect the repeating of the last dot position and provide an eight-bit parallel output signal to the following stage of the character generation system.

It is to be understood that the foregoing description of a specific example of this invention is made by way of example only and is not to be considered as a limitation on its scope.

What is claimed is:

1. In a character generation system including character pattern generation means of the Dot matrix type for generating signals representative of a standard font having a plurality of horizontal lines of dots each said dot being selectively controlled by a flip-flop, the improvement comprising;

selectively operable means for converting the standard font signal patterns generated by said pattern generation means into a bold font by repeating the last dot of each horizontal line of said standard font comprising N flip-flops, N-1 thereof each having a signal input thereof connected to a separate input terminal of the said converting means, first means for determining which of the N-1 flip-flops change their state when an (N-1)-bit parallel input signal is applied to said input terminals and for determining which one of the flip-flops of changed state is the last one to precede a flip-flop whose state is not changed, and second means for causing said flip-flop which is preceded by said last flip-flop of changed state to change its state.

2. The character generation system as claimed in claim 1 wherein the N flip-flops are connected in cascade to form a shift register, the J and K inputs of each flip-flop except the Nth one being respectively connected to the Q and $\bar{Q}$ outputs of a preceding flip-flop, wherein the J and K inputs of the Nth flip-flop are respectively connected to earth potential and an electrical supply voltage source, and wherein the output of said converting means is provided by the Q and $\bar{Q}$ outputs of the first one of said flip-flops.

3. The character generation system as claimed in claim 2 further including means for driving the shift register.

4. The character generation system as claimed in claim 1 wherein the Q output of each of the N flip-flops is connected to an output of said converting means.

5. The character generation system as claimed in claim 1 wherein said first means include a first NAND gate for each one of N-2 of said flip-flops, each one of said first NAND gates having one of its inputs connected to the Q output of the associated flip-flop and its other input(s) connected to the $\bar{Q}$ output of the following remaining one(s) of the N-1 flip-flops, and a second NAND gate having its output connected to one signal input of the Nth flip-flop and one of its two inputs connected to the Q output of the (N-1)th flip-flop.

6. The character generation system as claimed in claim 5 wherein a first invert gate is interposed between each one of the N-1 flip-flops and the associated input terminal.

7. The character generation system as claimed in claim 6 wherein said second means include a third NAND gate having its inputs connected to the $\bar{Q}$ outputs of the N-1 flip-flops and its output connected to the input of first pulse generating means and to one of two inputs of each one of N-2 memory elements, a fourth NAND gate for each of the N-2 memory elements, each of said fourth NAND gates having its output connected to the other input of the associated one of the N-2 memory elements and one of its two inputs connected to the output of a separate one of the first NAND gates via a third invert gate, the other input of each of the fourth NAND gates being connected together and to one output of the first pulse generating means, a fifth NAND gate for each one of the N-2 memory elements, each of the fifth NAND gates having one of its two inputs connected to the output of the associated one of the N-2 memory elements, the other of its inputs connected to one output of second pulse generating means and its output connected to one of the two inputs of an OR-gate, the input to the second pulse generating means being connected to another output of the first pulse generating means, and wherein each one of the OR-gates is interposed between the said one signal input of a separate one of the second to the (N-1)th flip-flops of the N-1 flip-flops and the associated one of the first invert gates, the other of the two inputs of each of the OR-gates being connected to the output of the associated first invert gate while the output of each of the OR-gates is connected to the said one signal input of the associated flip-flop.

8. The character generation system as claimed in claim 7 wherein the first pulse generating means include a first differentiating network, a second invert gate having its input connected to the input of the first generating means and its output connected to the input of the first differentiating network, and a fourth invert gate having its input connected to the output of the first differentiating network and to the said another output of the first generating means and its output connected to the said one output of the generating means.

9. The character generation system as claimed in claim 7 wherein the second pulse generating means include a second differentiating network having its output connected to one output of the second generating means via a fifth invert gate and to another output of the second generating means, and its input connected to the output of a monostable network, the input of the monostable network being connected to the input of the second generating means.

10. The character generation system as claimed in claim 8 wherein the other input of the second NAND gate is connected to the output of the second pulse generating means.

11. The character generation system as claimed in claim 1 further including switching means for selecting a standard font or bold font mode of operation.

12. The character generation system as claimed in claim 8 further including switching means for selecting a standard font or bold font mode of operation, said switching means being provided by a two-pole, two-way electrical switch, one pole being adapted to switch the output of the second pulse generating means either to the inputs of the second and fifth NAND gates or to earth potential while the other pole is adapted to switch the output of the first pulse generating means either to the inputs of the fourth NAND gates or to earth potential.

13. The character generation system as claimed in claim 7 further comprising means for driving the shift register, said means for driving the shift register including a memory element having one of its two inputs connected to the output of the third NAND gate and the other of its inputs connected to the said another output of the second pulse generating means, and a sixth NAND gate having its output connected to the drive input of each of the N flip-flops, one of its two inputs connected to the output of the memory element, and the other of its inputs adapted to be connected to an oscillatory input signal.

14. The character generation system as claimed in claim 13 wherein each of the memory elements include two NAND gates, wherein the output of one of the NAND gates is connected to the output of the respective memory element and to one of the two inputs of the other of the NAND gates, wherein the output of the said other of the NAND gates is connected to one of the two inputs of the said one of the NAND gates, and

wherein the two inputs of the memory element are each connected to the other of the inputs of a separate one of the two NAND gates.

15. The character generation system as claimed in claim 8 wherein each of the differentiating networks include a resistance and a capacitance connected in series between an electrical supply voltage source and the input of the network, the junction of the resistance and the capacitance being connected to the output of the network.

16. The character generation system as claimed in claim 9 wherein the monostable network includes three NAND gates, wherein the output of the network is connected to the output of one of the three gates, to the two inputs of another of the three gates, and to one of the two inputs of the other of the three gates, wherein the input of the network is connected to one of the two inputs of the said one of the three gates whose other input is connected to the output of the said other of the three gates, and wherein the other input of the said other of the three gates is connected to earth potential via a capacitance and to the output of the said another of the three gates via a resistance.

17. The character generation system as claimed in claim 2 wherein the N flip-flops each have another signal input thereof connected to an electrical bias network.

18. The character generation system as claimed in claim 17 wherein the electrical bias network includes a resistance and a capacitance connected in series between an electrical supply voltage source and earth potential, the junction of the resistance and capacitance being connected to the said another signal inputs of the N flip-flops.

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