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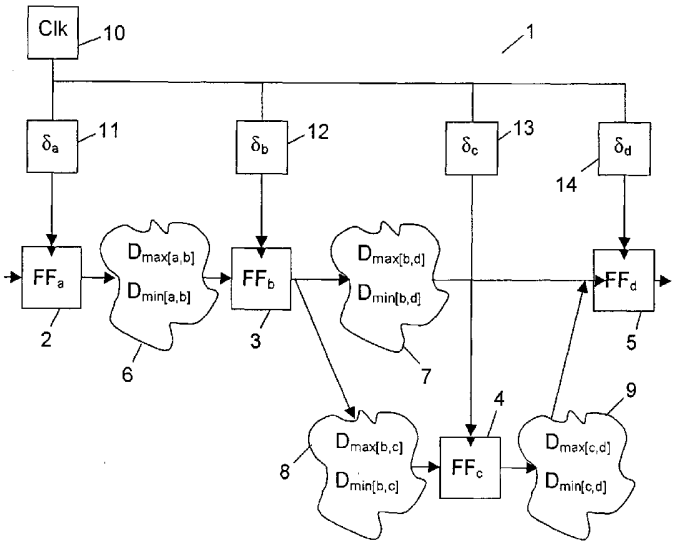
(54) Title: OPTIMIZATION OF THE DESIGN OF A SYNCHRONOUS DIGITAL CIRCUIT



(57) Abstract: The design of a synchronous digital circuit (1) can be modified. The circuit comprises a number of clocked storage devices (2, 3, 4, 5,) and a number of combinational logic elements defining combinational paths (6, 7, 8, 9,) between at least some of said clocked storage devices. Each combinational path from an output of one clocked storage device to an input of another has a minimum delay value (D_{min}) and a maximum delay value (D_{max}). The actual delay of the path assumes a value between the minimum and maximum delay values. The method comprises the steps of identifying the path (6; 7; 8; 9) having the greatest difference between the maximum delay value (D_{max}) and the minimum delay value (D_{MIN}), and reducing said difference by increasing the minimum delay value for the path having the greatest difference. With the method a higher clock frequency for the circuit can be achieved.

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2001/007144 A1 (TERAZAWA TOSHIHIRO) 5 July 2001 (2001-07-05) the whole document	1-11
A	US 5 764 528 A (NAKAMURA ATSUSHI) 9 June 1998 (1998-06-09) column 1, line 13 -column 3, line 63; figures 12-16	1-11
A	US 5 983 007 A (AGRAWAL VISHWANI DEO) 9 November 1999 (1999-11-09) column 5, line 29 - line 64; figure 4	1-11
A	US 2001/010092 A1 (KATO AKITOSHI) 26 July 2001 (2001-07-26) abstract	1,5,6,10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Jepsen, J

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	SOYATA T ET AL: "Synchronous performance and reliability improvement in pipelined ASICs" ASIC CONFERENCE AND EXHIBIT, 1994. PROCEEDINGS., SEVENTH ANNUAL IEEE INTERNATIONAL ROCHESTER, NY, USA 19-23 SEPT. 1994, NEW YORK, NY, USA,IEEE, 19 September 1994 (1994-09-19), pages 383-390, XP010140451 ISBN: 0-7803-2020-4 the whole document	1-11
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