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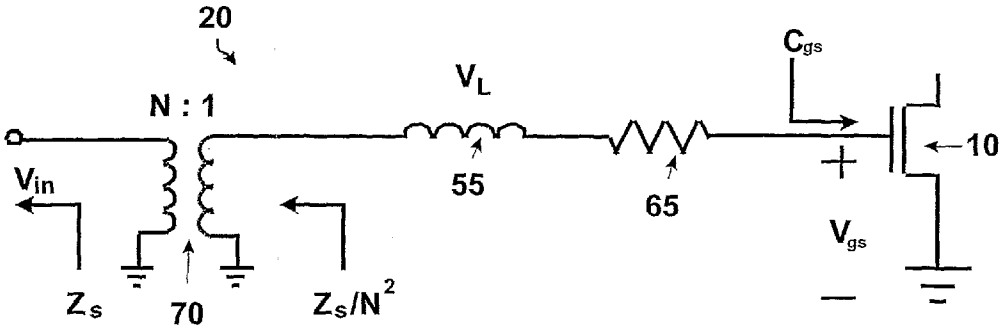
(54) **Title:** RESONANT TYPES OF COMMON-SOURCE/COMMON-EMITTER STRUCTURE FOR HIGH GAIN AMPLIFICATION



(57) **Abstract:** Radio frequency/millimeter wave integrated circuits (RF/MMICs) that employ a resonance mechanism between an input stage and a transistor are disclosed. The circuits contain an input stage, a transistor; and a transformer connected between either a gate or a base of the transistor and a voltage supply of the input stage. The methods disclosed maximize either a collector current or a drain current of a transistor by placing a transformer between the transistor and a voltage source.

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RESONANT TYPES OF COMMON-SOURCE/COMMON-EMITTER STRUCTURE FOR HIGH GAIN AMPLIFICATION

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. provisional patent application serial number 60/705,861, filed August 4, 2005 for a "Resonant Types of Common-Source/Common-Emitter Structure for High Gain Amplification " by Daquan Huang and Mau-Chung F. Chang, the disclosure of which is incorporated herein by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] The present invention was made with support from the United States Government under Grant number N66001-04-1-8934 awarded by the U.S. Navy. The United States Government has certain rights in the invention.

FIELD

[0003] The present invention relates to amplification circuits. More particularly, the present invention relates to radio frequency/millimiter wave integrated circuits (RF/MMICs) that employ a resonance mechanism between an input stage and a transistor.

BACKGROUND

[0004] Higher gain has always been desirable in amplification circuits, especially in radio frequency/millimeter wave integrated circuits (RF/MMICs).

[0005] In conventional radio frequency and millimeter wave circuit input stage designs, inductors are used such that they cancel the parasitic capacitances and match the input impedance to that of the signal source, aiming either to maximize the available power gain or to minimize the noise figure. However, in many analog and mixed-signal circuit designs, voltage gain is the only concern. Therefore, impedance matching is not the optimal design strategy.

[0006] To overcome this deficiency, the present disclosure presents a new design that employs a resonance mechanism to maximize a voltage gain.

SUMMARY

[0007] According to the present disclosure, amplification circuits are disclosed.

[0008] According to a first embodiment disclosed herein, a circuit is disclosed, comprising: an input stage; a transistor; and a transformer connected between a gate of the transistor and a voltage supply of the input stage.

[0009] According to a second embodiment disclosed herein, a circuit is disclosed, comprising: an input stage; a transistor; and a transformer disposed between a base of the transistor and a voltage supply of the input stage.

[0010] According to a third embodiment disclosed herein, a method for maximizing a drain current of a transistor is disclosed, comprising: selecting a transistor; selecting a transformer; and connecting the transformer between a gate of the transistor and a voltage source.

[0011] According to a fourth embodiment disclosed herein, a method for maximizing a collector current of a transistor is disclosed, comprising: selecting a transistor; selecting a transformer; connecting the transformer between a base of the transistor and a voltage source.

BRIEF DESCRIPTION OF THE FIGURES

[0012] Figure 1 depicts a series resonant common-source circuit as known in the Prior Art;

[0013] Fig. 2 depicts a parallel resonant common-source circuit as known in the Prior Art;

[0014] Fig. 3 depicts an electrically equivalent circuit of Fig. 1;

[0015] Fig. 4 depicts an electrically equivalent circuit of Fig. 2;

[0016] Fig. 5 depicts an embodiment of a series resonant common-source circuit according to the present disclosure;

[0017] Fig. 6 depicts an embodiment of a parallel resonant common-source circuit according to the present disclosure;

[0018] Figs. 7a-c depict other embodiments of a series resonant common-source circuit according to the present disclosure;

[0019] Figs. 8a-c depict other embodiments of a parallel resonant common-source circuit according to the present disclosure;

[0020] Fig. 9 depicts an embodiment of a parallel resonant common-emitter circuit according to the present disclosure;

[0021] Fig. 10 depicts an embodiment of a series resonant common-emitter circuit according to the present disclosure;

[0022] Figs. 11a-c depicts other embodiments of a parallel resonant common-emitter circuit according to the present disclosure; and

[0023] Figs. 12a-c depicts other embodiments of a series resonant common-emitter circuit according to the present disclosure.

[0024] In the following description, like reference numbers are used to identify like elements. Furthermore, the drawings are intended to illustrate major features of exemplary embodiments in a diagrammatic manner. The drawings are not intended to depict every feature of every implementation nor relative dimensions of the depicted elements, and are not drawn to scale.

DETAILED DESCRIPTION

[0025] According to prior art shown in **Figs. 1** and **2**, MOS transistors **10** in common-source circuits **20** and **30** convert the input voltage V_{gs} into the drain current I_D, wherein I_D for NMOS transistor is $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{gs} - V_{th})^2$; I_D for PMOS transistor is $I_D = \frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{gs} - V_{th})^2$; μ_n is the mobility of electrons; μ_p is the mobility of holes; C_{ox} is the gate oxide capacitance per unit area; W and L are the width and length of the gate; V_{th} is the threshold voltage; ω_o is resonant angular frequency determined by $\omega_o = \frac{1}{\sqrt{LC}}$; I_s is the inverse saturation current; and V_T is the threshold voltage. As known in the art, increasing V_{gs} increases the output current I_D that determines the output voltage by $V_{out} = I_D Z_o$, where Z_o is the output impedance of the circuit. Therefore, maximizing V_{gs} maximizes the voltage gain.

[0026] The series resonant input circuit **40** and the parallel resonant input circuit **50** shown in **Figs. 3** and **4** are electrically equivalent to common-source circuits **20** and **30**, respectively. As can be seen in **Figs. 3** and **4**, capacitors **60** represent the transistor gate capacitance of the transistors **10** in common-source circuits **20** and **30**.

[0027] In the series resonant input circuit **40**, driven by voltage source V_S, as shown in **Fig. 3**, the voltage (V_L or V_C) on the reactance elements (the inductor **55** and the capacitor **60**) is Q times higher than the input voltage V_{in}, where Q is the quality factor (Q-factor) defined by $Q = \omega_0 L/r = 1/r\omega_0 C$; $\omega_0 = \sqrt{\frac{1}{LC}}$; $V_L = jQV_{in}$; $V_C = -jQV_{in}$ and variables L, C and r are the series inductance of the inductor **55**, capacitance of the capacitor **60** and the parasitic resistance **65** respectively. Therefore, the input voltage V_{in} is amplified by Q times when it is applied to the series resonant input circuit **40**. However, the input voltage V_{in} may further be amplified by providing a smaller signal source impedance in the series resonant input circuit **40** as discussed below.

[0028] In the parallel resonant input circuit **50**, driven by a current source I_s as shown in **Fig. 4**, the current ($I_L$or I_C) of the reactance elements (the inductor **55** and the capacitor **60**) is Q times larger than the input current I_{in}, where $Q = R/\omega_0 L = R\omega_0 C$; $\omega_0 = \sqrt{\frac{1}{LC}}$; $I_L = -jQV_{in}$; $I_C = jQV_{in}$ and variables L, C and R are the parallel inductance of the inductor **55**, capacitance of the capacitor **60** and the parasitic resistance **65**. Therefore, I_L is Q times larger than the input current I_{in}.

[0029] In one exemplary embodiment, the present disclosure amplifies the input voltage V_{in} of the common-source circuit **20** by employing a resonance mechanism like a transformer **70**, for example, to reduce the signal source impedance Z_S by $1/N^2$ in the common-source circuit **20**, as shown in **Fig. 5**. By reducing the signal source impedance Z_S using the transformer **70**, a higher Q-factor, $Q = \omega_0 L/real(Z_s/N^2) = 1/real(Z_s/N^2)\omega_0 C$, is obtained.

[0030] In another exemplary embodiment, the present disclosure amplifies the transistor **10**'s input voltage V_{gs} of the common-source circuit **30** by employing a resonance mechanism like a transformer **80**, for example, with the primary to secondary coil turn ratio $N_1:N_2>1$ in the common-source circuit **30**, as shown in **Fig. 6**.

[0031] In another exemplary embodiment, a variable capacitor device **90** like, for example, a varactor, disposed between the transformer **70** and the transistor **10** may be used to adjust the resonant frequency of the common-source circuit **20**, as shown in **Fig. 7a**. The resonant frequency may be determined by $f_o = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}$, where C includes capacitance of variable capacitor device **90** and inductor/transformer parasitic capacitance.

[0032] Similarly, a variable capacitor device **91** like, for example, a varactor, disposed between the transformer **70** and V_{in} may be used to adjust the resonant frequency of the common-source circuit **20**, as shown in **Fig. 7b**.

[0033] Also, variable capacitor device **92**, disposed between the transformer **70** and V_{in}, together with a variable capacitor devices **93**, disposed between the transformer **70** and the transistor **10** may also be used to adjust the resonant frequency of the common-source circuit **20**, as shown in **Fig. 7c.**

[0034] In another exemplary embodiment, a variable capacitor device **95** like, for example, a varactor, disposed between the transformer **80** and the input voltage V_{in} may be used to adjust the resonant frequency of the common -source circuit **30**, as shown in **Fig. 8a.**

[0035] Similarly, a variable capacitor device **96** like, for example, a varactor, disposed between the transformer **80** and the transistor **10** may be used to adjust the resonant frequency of the common -source circuit **30**, as shown in **Fig. 8b.**

[0036] Also, variable capacitor device **97**, disposed between the transformer **80** and V_{in}, together with a variable capacitor devices **98**, disposed between the transformer **80** and the transistor **10** may also be used to adjust the resonant frequency of the common-source circuit **30**, as shown in **Fig. 8c.**

[0037] In another exemplary embodiment, teachings of the present disclosure may be applied to common-emitter circuit **140** using bipolar technology as shown in **Figs. 9** and **10.**

[0038] A bipolar transistor **110** in the common-emitter circuit **140** converts the input voltage V_{be} into the collector current I_C, wherein $I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$. As known in the art, increasing V_{be} increases the output current I_C that in turn yields higher voltage gain. Therefore, employing a resonance mechanism like a transformer **100**, for example, with the primary to secondary coil turn ratio $N_1:N_2>1$ in the common-emitter circuit **140**, as shown in **Fig. 9** amplifies the transistor **110**'s input voltage V_{be} of the common-emitter circuit **140.**

[0039] Similarly, employing a resonance mechanism like a transformer **165**, for example, in the common-emitter circuit **160**, as shown in **Fig. 10** also amplifies the transistor **110**'s input voltage V_{be} of the common-emitter circuit **160**.

[0040] In another exemplary embodiment, a variable capacitor device **101** like, for example, a varactor, disposed between the transformer **100** and the input voltage V_{in} may be used to adjust the resonant frequency of the common–emitter circuit **140**, as shown in **Fig. 10a.**

[0041] Similarly, a variable capacitor device **102** like, for example, a varactor, disposed between the transformer **100** and the transistor **110** may be used to adjust the resonant frequency of the common-emitter circuit **140**, as shown in **Fig. 10b.**

[0042] Also, variable capacitor device **103**, disposed between the transformer **100** and V_{in}, together with a variable capacitor devices **104**, disposed between the transformer **100** and the transistor **110** may also be used to adjust the resonant frequency of the common-emitter circuit **140**, as shown in **Fig. 10c.**

[0043] In another exemplary embodiment, a variable capacitor device **180** like, for example, a varactor, disposed between the transformer **165** and the transistor **110** may be used to adjust the resonant frequency of the common-emitter circuit **160**, as shown in **Fig. 11a.**

[0044] Similarly, a variable capacitor device **181** like, for example, a varactor, disposed between the transformer **165** and V_{in} may be used to adjust the resonant frequency of the common-emitter circuit **160**, as shown in **Fig. 11b.**

[0045] Also, variable capacitor device **182**, disposed between the transformer **165** and V_{in}, together with a variable capacitor devices **183**, disposed between the transformer **165** and the transistor **110** may also be used to adjust the resonant frequency of the common-emitter circuit **160**, as shown in **Fig. 11c.**

[0046] The foregoing detailed description of exemplary and preferred embodiments is presented for purposes of illustration and disclosure in accordance with the requirements of the law. It is not intended to be exhaustive nor to limit the invention to the precise form(s) described, but only to enable others skilled in the art to understand how the invention may be suited for a particular use or implementation. The possibility of modifications and variations will be apparent to practitioners skilled in the art. No limitation is intended by the description of exemplary embodiments which may have included tolerances, feature dimensions, specific operating conditions, engineering specifications, or the like, and which may vary between implementations or with changes to the state of the art, and no limitation should be implied therefrom. Applicant has made this disclosure with respect to the current state of the art, but also contemplates advancements and that adaptations in the future may take into consideration of those advancements, namely in accordance with the then current state of the art. It is intended that the scope of the invention be defined by the Claims as written and equivalents as applicable. Reference to a claim element in the singular is not intended to mean "one and only one" unless explicitly so stated. Moreover, no element, component, nor method or process step in this disclosure is intended to be dedicated to the public regardless of whether the element, component, or step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for. . ." and no method or process step herein is to be construed under those provisions unless the step, or steps, are expressly recited using the phrase "step(s) for. . .."

What is claimed is:

1. A circuit comprising:
an input stage;
a transistor; and
a transformer connected between a gate of the transistor and a voltage supply of the input stage.

2. The circuit of Claim 1, wherein the transistor is a MOS transistor.

3. The circuit of Claim 1, the input stage is a series resonant circuit.

4. The circuit of Claim 1, the input stage is a parallel resonant circuit.

5. The circuit of Claim 4, wherein the transformer has a primary to secondary coil turn ratio $N_1:N_2>1$.

6. The circuit of Claim 1, further comprising a variable capacitance device connected to the circuit for controlling an operating frequency of the circuit.

7. The circuit of Claim 6, wherein the variable capacitance device is a varactor.

8. A circuit comprising:
an input stage;
a transistor; and
a transformer disposed between a base of the transistor and a voltage supply of the input stage.

9. The circuit of Claim 8, wherein the transistor is a MOS transistor.

10. The circuit of Claim 8, wherein the transistor is a bipolar transistor.

11. The circuit of Claim 8, the input stage is a series resonant circuit.

12. The circuit of Claim 8, the input stage is a parallel resonant circuit.

13. The circuit of Claim 12, wherein the transformer has a primary to secondary coil turn ratio N_1:N_2>1.

14. The circuit of Claim 8, further comprising a variable capacitance device connected to the circuit for controlling an operating frequency of the common-emitter structure.

15. The circuit of Claim 14, wherein the variable capacitance device is a varactor.

16. A method for maximizing a drain current of a transistor comprising:

selecting a transistor;

selecting a transformer; and

connecting the transformer between a gate of the transistor and a voltage source.

17. The method of Claim 16, wherein the transistor is a MOS transistor.

18. The method of Claim 16, further comprising adjusting an operating frequency of a transistor with a variable capacitance device.

19. The method of Claim 18, wherein the variable capacitance device is a varactor.

20. A method for maximizing a collector current of a transistor comprising:

selecting a transistor;

selecting a transformer;

connecting the transformer between a base of the transistor and a voltage source.

21. The method of Claim 20, wherein the transistor is a bipolar transistor.

22. The method of Claim 20, wherein the transformer has a primary to secondary coil turn ratio $N_1:N_2>1$.

23. The method of Claim 20, further comprising adjusting an operating frequency of the transistor with a variable capacitance device.

24. The method of Claim 23, wherein the variable capacitance device is a varactor.

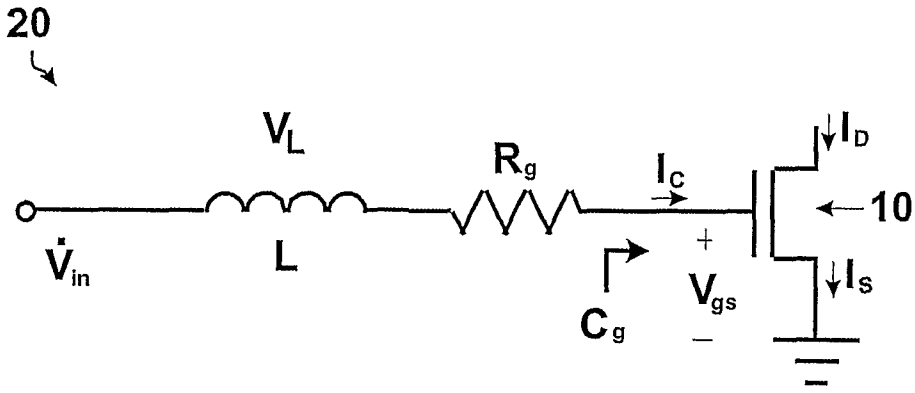

Fig. 1 Prior art

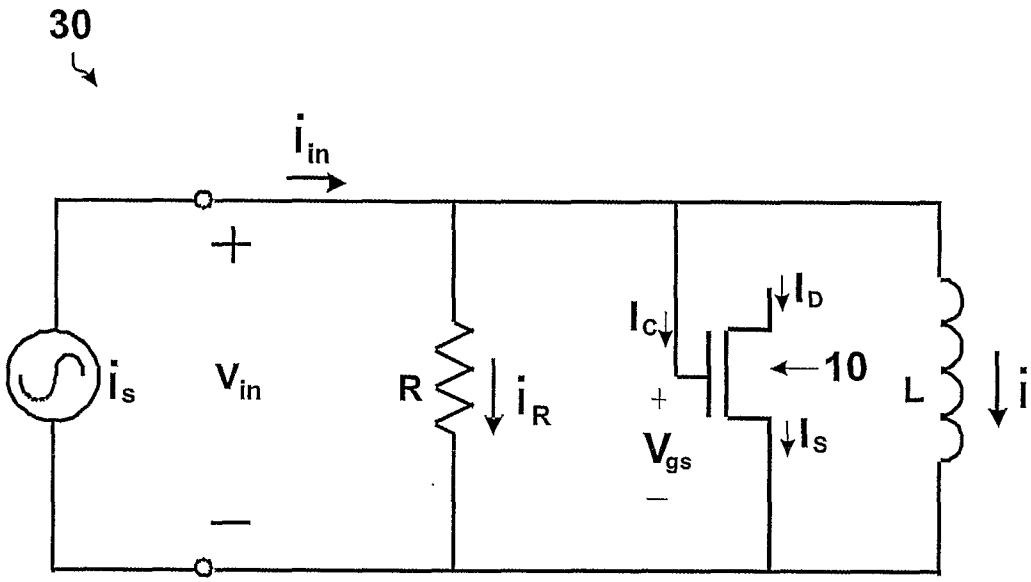

Fig. 2 Prior art

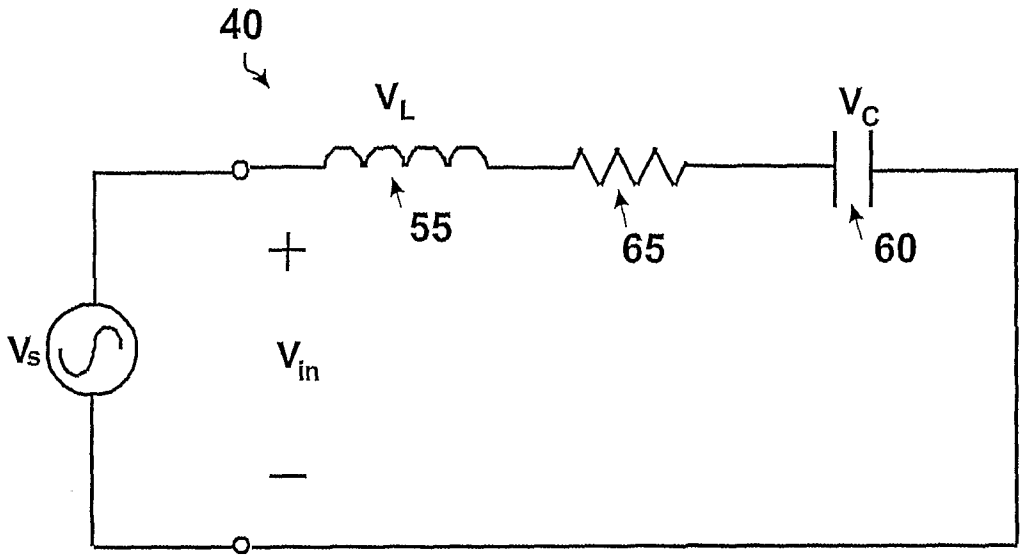

Fig. 3 Prior art

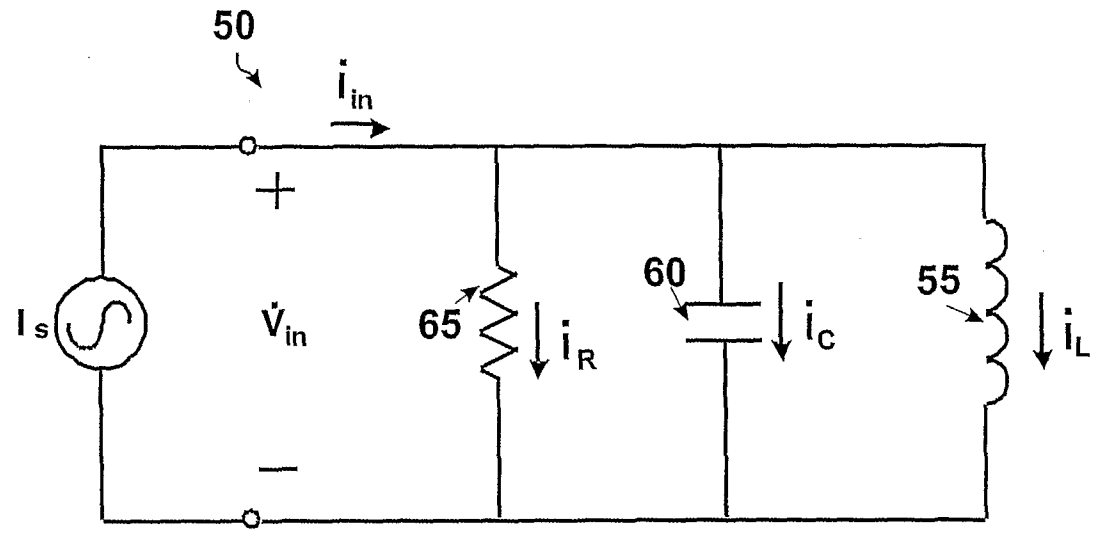

Fig. 4 Prior art

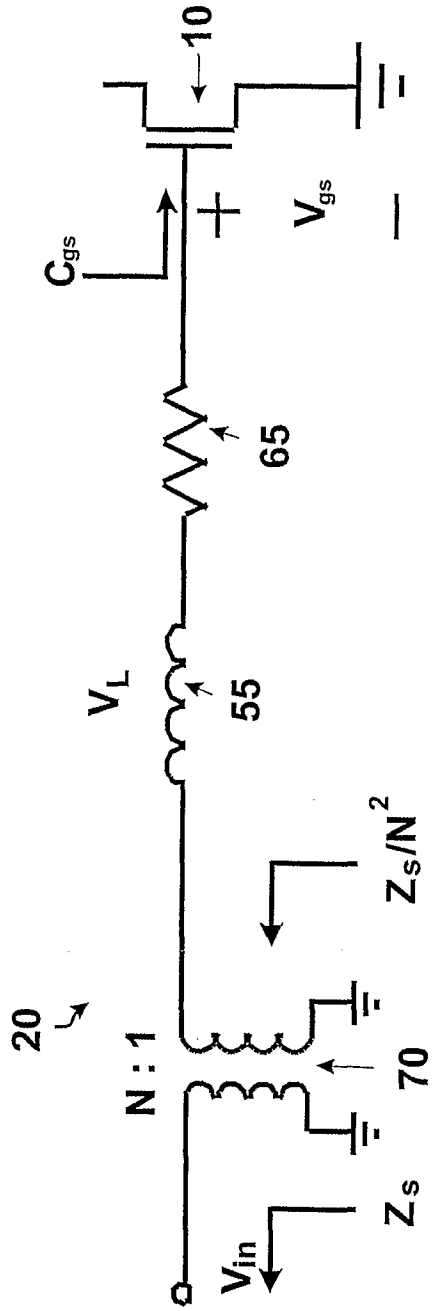
10
C_{gs}
V_{gs}
65
V_L
55
Z_s/N^2
20
N : 1
70
Z_s
V_{in}

Fig. 5

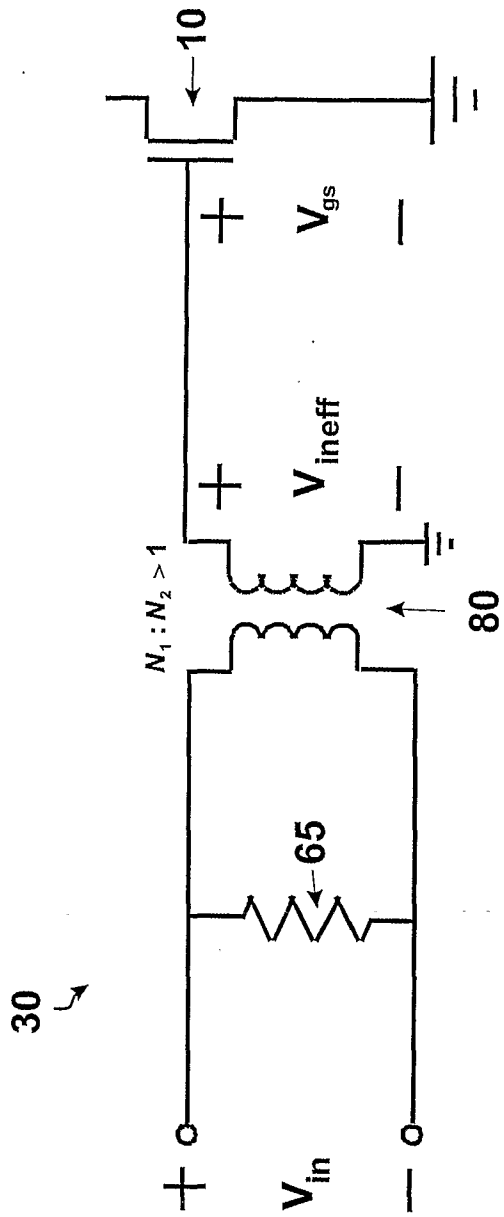
10
V_{gs}
V_{ineff}
$N_1 : N_2 > 1$
80
65
30
V_{in}

Fig. 6

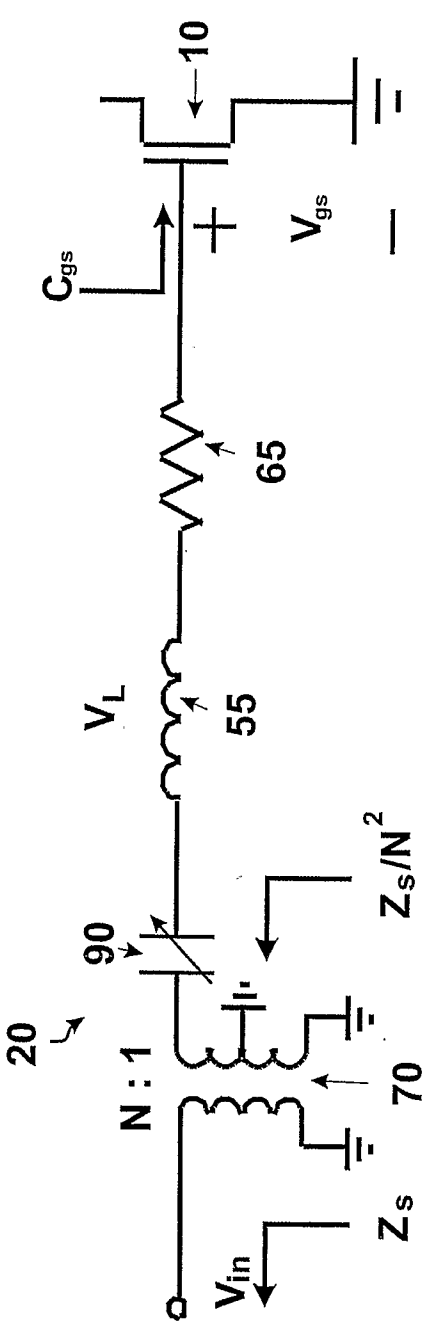
10
C_{gs}
V_{gs}
65
V_L
55
Z_S/N^2
90
20
N : 1
70
Z_S
V_{in}

Fig. 7a

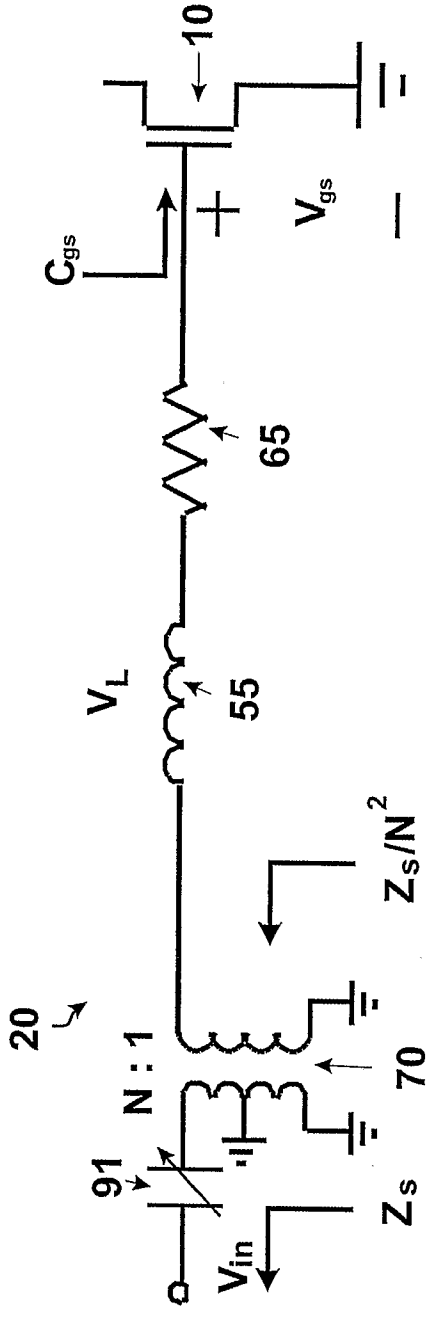
10
C_{gs}
V_{gs}
65
V_L
55
Z_S/N^2
20
N : 1
70
91
Z_S
V_{in}

Fig. 7b

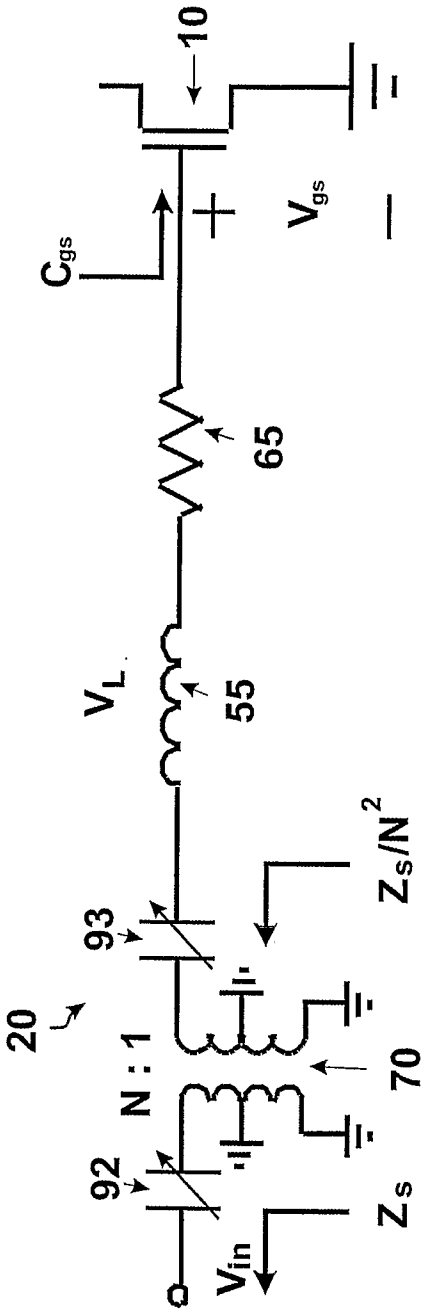

Fig. 7c

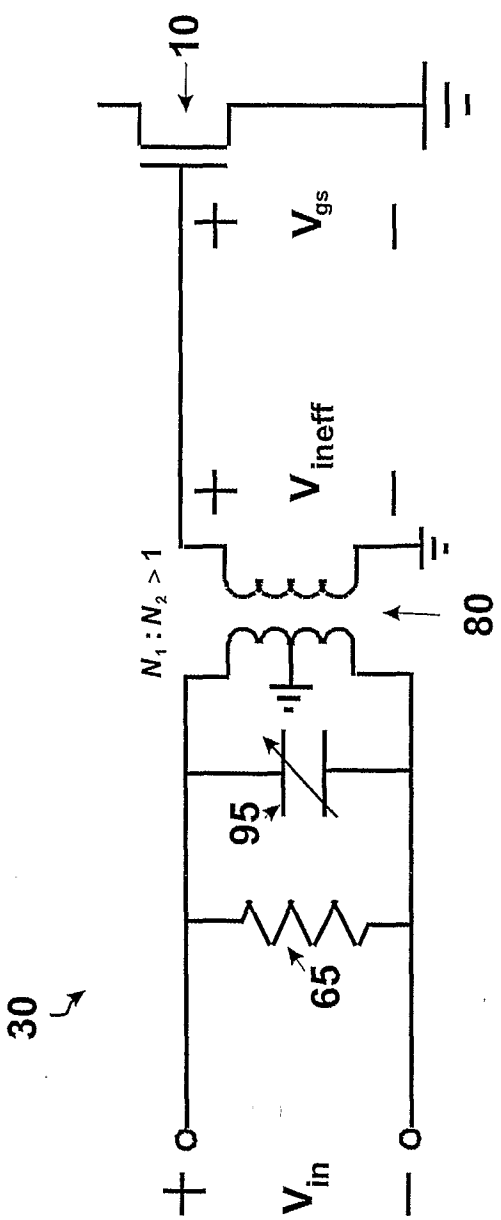
10
V_{gs}
V_{ineff}
$N_1 : N_2 > 1$
80
95
65
30
V_{in}

Fig. 8a

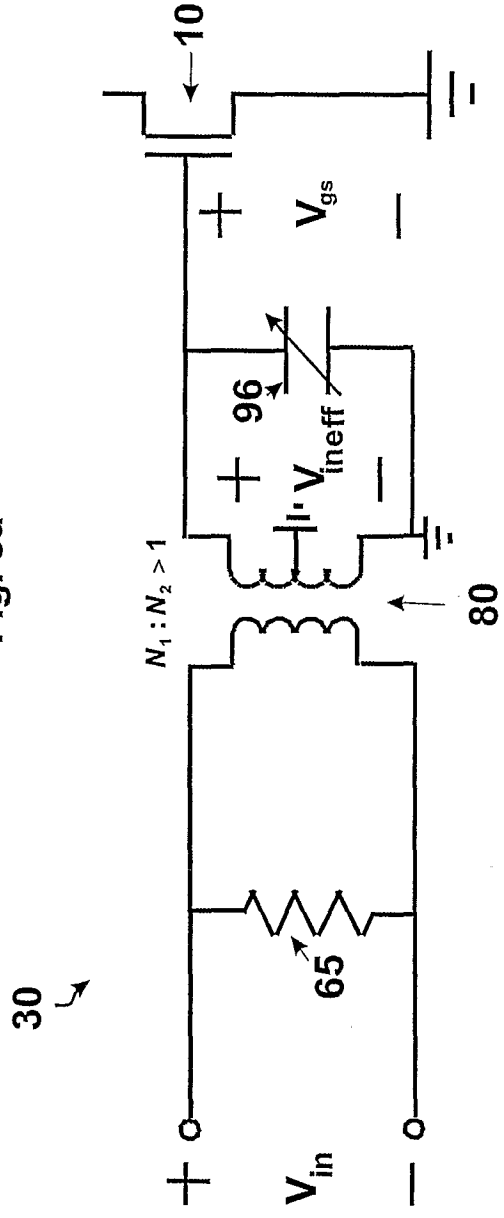
10
V_{gs}
96
V_{ineff}
$N_1 : N_2 > 1$
80
65
30
V_{in}

Fig. 8b

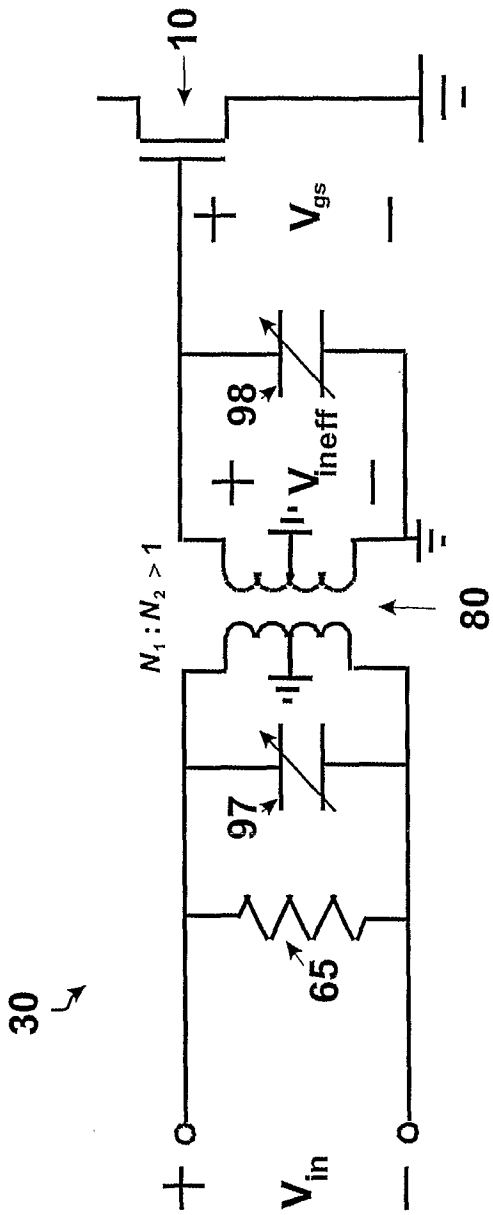

Fig. 8c

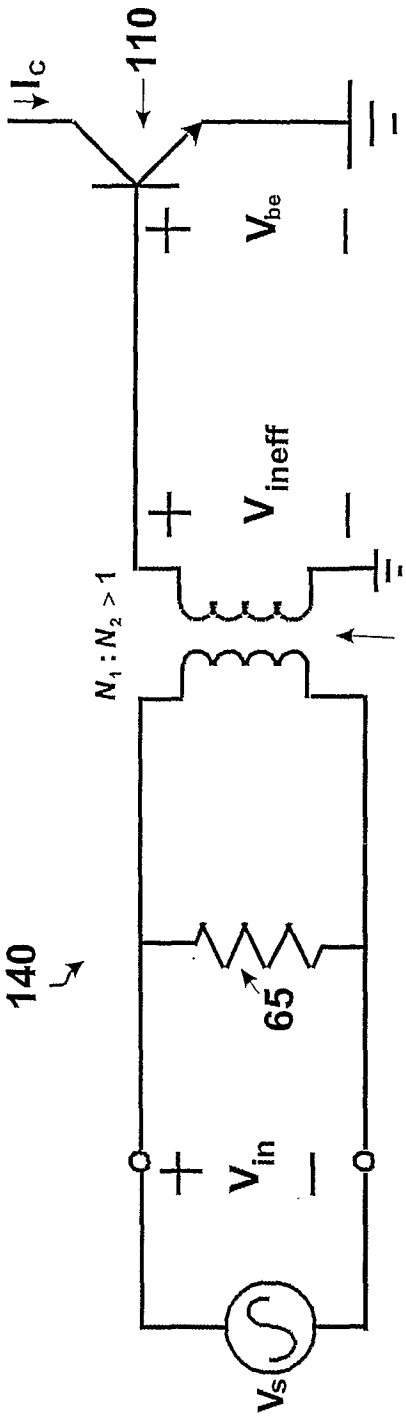
I_C
110
V_{be}
V_{ineff}
$N_1 : N_2 > 1$
100
140
65
V_{in}
V_S

Fig. 9

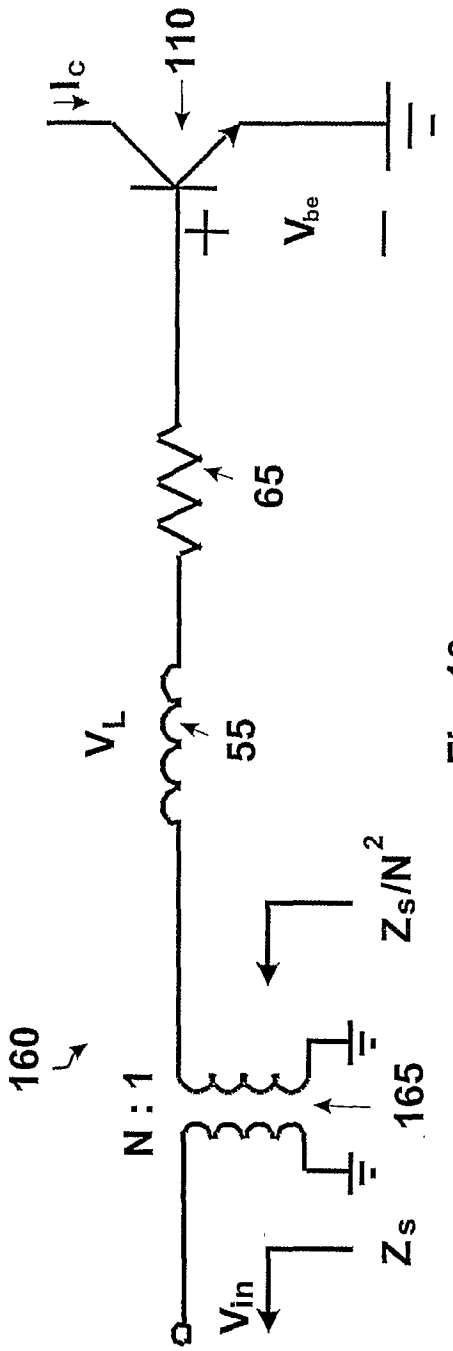
I_C
110
V_{be}
65
V_L
55
Z_S/N^2
160
N : 1
165
Z_S
V_{in}

Fig. 10

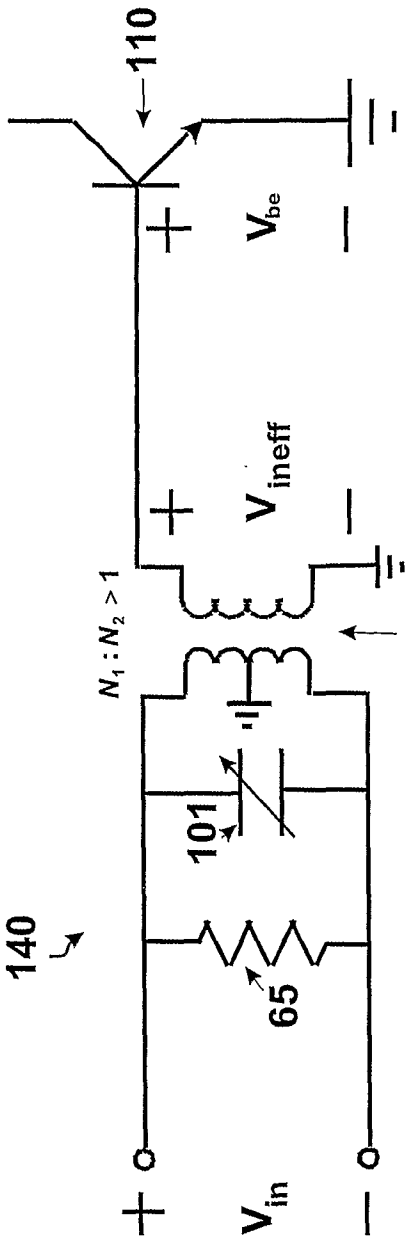

Fig. 11a

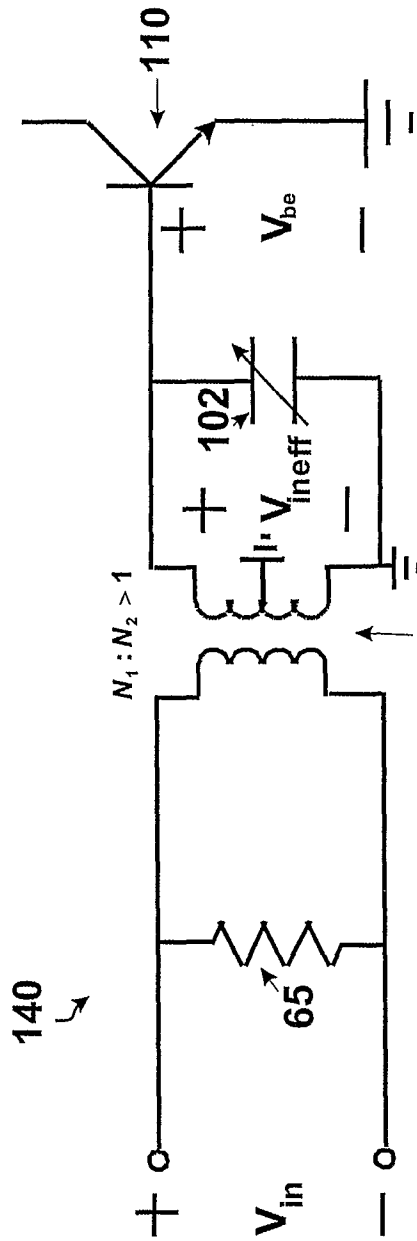

Fig. 11b

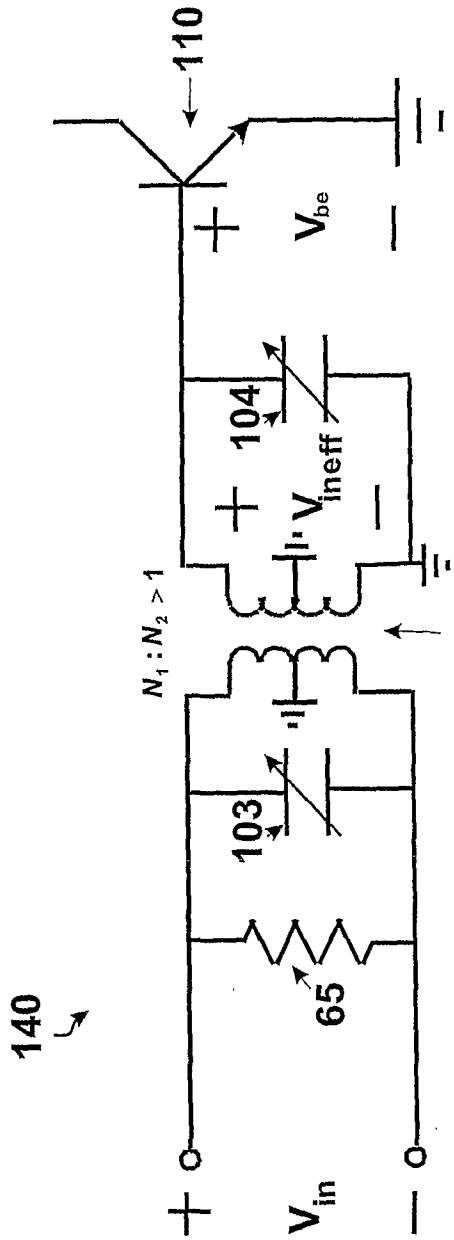

Fig. 11c

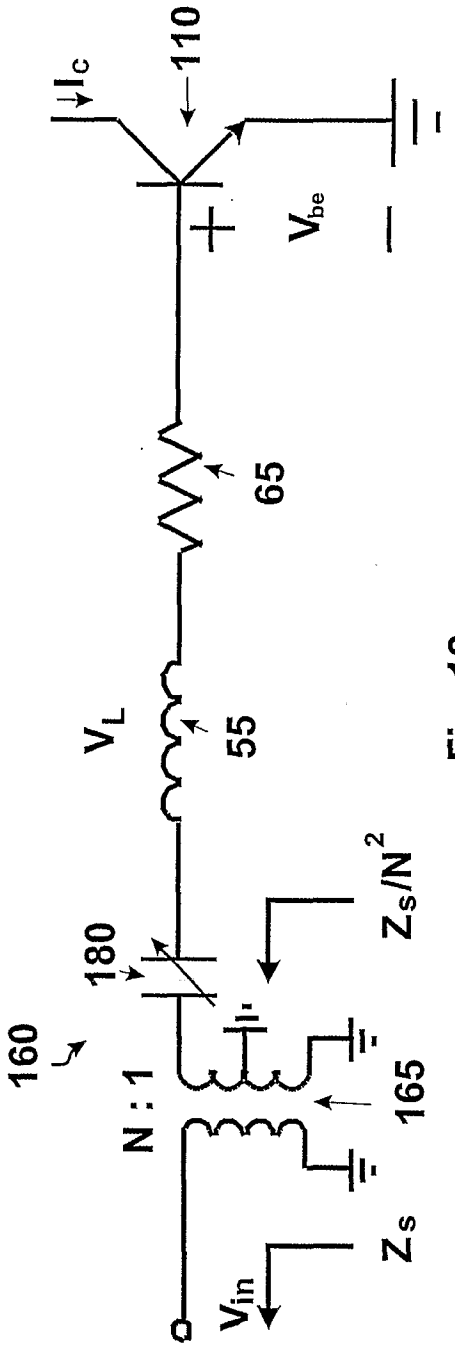

Fig. 12a

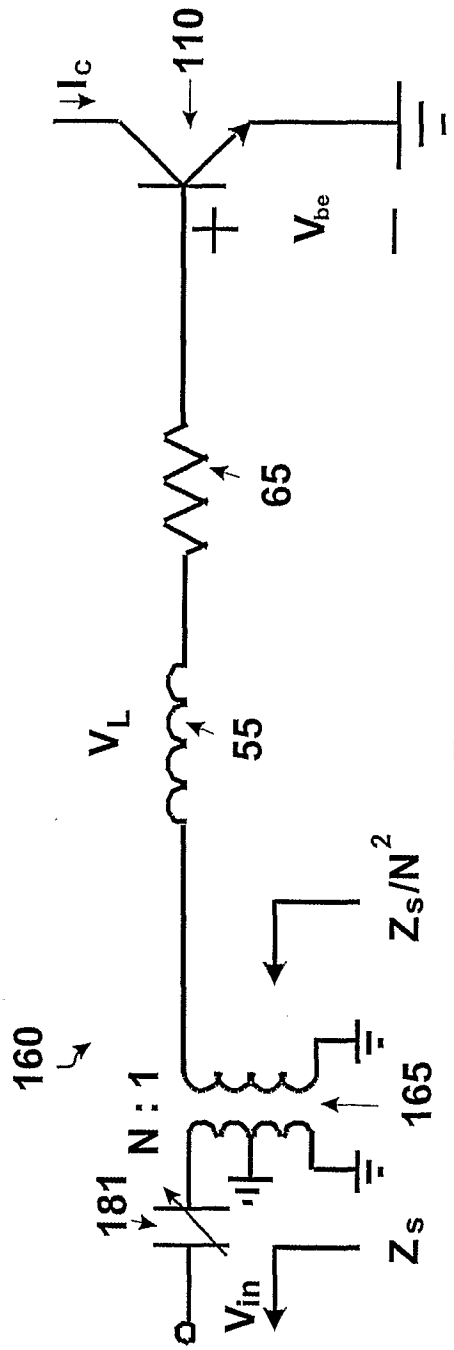

Fig. 12b

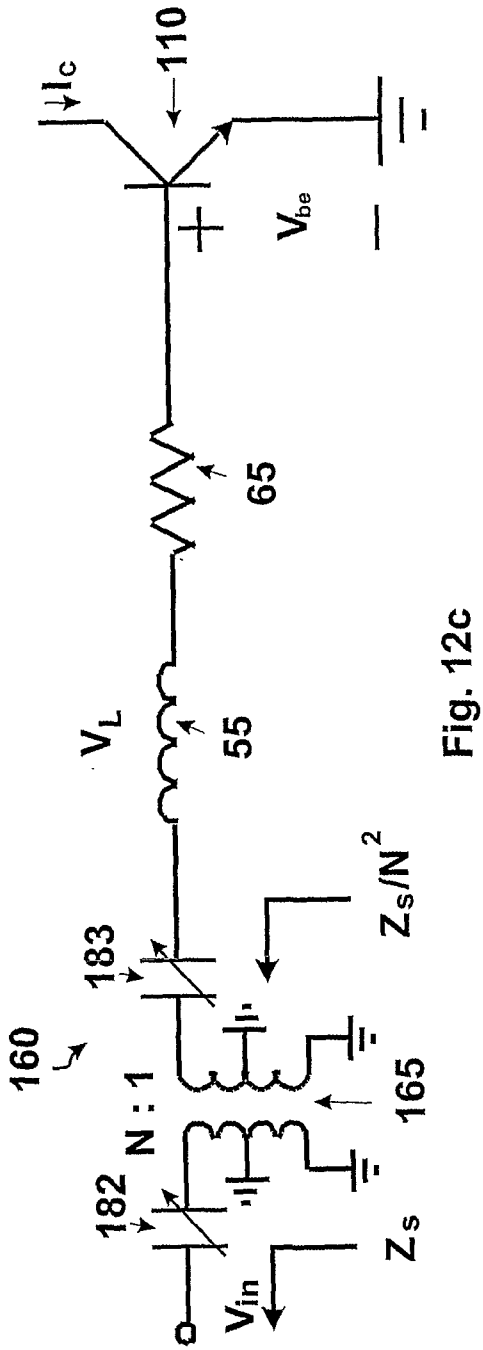

Fig. 12c