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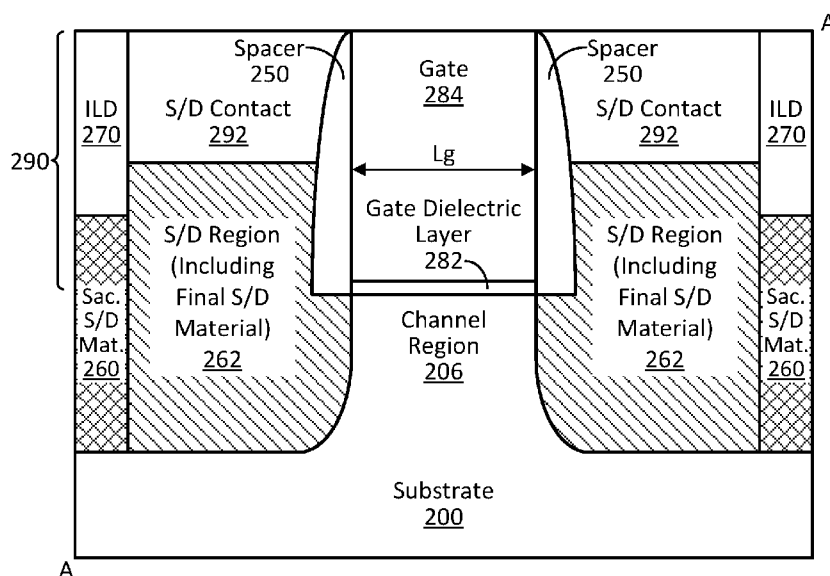
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(54) Title: TRANSISTORS INCLUDING FINAL SOURCE/DRAIN MATERIAL PROCESSED AFTER REPLACEMENT GATE PROCESSING

**FIG. 3**

(57) **Abstract:** Techniques are disclosed for forming transistors including final source/drain (S/D) material processed after replacement gate processing. In some cases, at least one of the S/D regions of a transistor may initially be formed with sacrificial S/D material that is intended to be removed and replaced later in the process flow with final S/D material. The sacrificial S/D material may be formed during the typical S/D region formation (e.g., after the dummy gate stack and gate spacers have been formed). Then, the sacrificial S/D material may be removed and replaced with final S/D material through a corresponding S/D contact trench, such that the final S/D material is not formed until near the end of the front-end-of line (FEOL) processing. This allows delaying formation of the final S/D material until after replacement gate processing has occurred, thereby addressing the problem of dopant diffusion from the S/D regions into the channel.



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TRANSISTORS INCLUDING FINAL SOURCE/DRAIN MATERIAL PROCESSED AFTER REPLACEMENT GATE PROCESSING

5 BACKGROUND

Semiconductor devices are electronic components that exploit the electronic properties of semiconductor materials, such as silicon (Si), germanium (Ge), and gallium arsenide (GaAs). A field-effect transistor (FET) is a semiconductor device that includes three terminals: a gate, a source, and a drain. A FET uses an electric field applied by the gate to control the electrical conductivity of a channel through which charge carriers (e.g., electrons or holes) flow from the source to the drain. In instances where the charge carriers are electrons, the FET is referred to as an n-channel device, and in instances where the charge carriers are holes, the FET is referred to as a p-channel device. Some FETs have a fourth terminal called the body or substrate, which can be used to bias the transistor. In addition, metal-oxide-semiconductor FETs (MOSFETs) include a gate dielectric layer between the gate and the channel. MOSFETs may also be known, more generally, as metal-insulator-semiconductor FETs (MISFETs) or insulated-gate FETs (IGFETs). Complementary MOS (CMOS) structures use a combination of p-channel MOSFET (p-MOS) and n-channel MOSFET (n-MOS) to implement logic gates and other digital circuits.

A FinFET is a MOSFET transistor built around a thin strip of semiconductor material (generally referred to as a fin). The conductive channel of the FinFET device resides on the outer portions of the fin adjacent to the gate dielectric. Specifically, current runs along/within both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate transistor. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin). A nanowire transistor (sometimes referred to as a gate-all-around (GAA) or nanoribbon transistor) is configured similarly to a fin-based transistor, but instead of a finned channel region where the gate is on three portions (and thus, there are three effective gates), one or more nanowires are used for the channel region and the gate material generally surrounds each nanowire.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a method of forming an integrated circuit (IC) including at least one source/drain (S/D) region processed after replacement gate processing, in accordance with some embodiments of the present disclosure.

5 Figures 2A-J illustrate example integrated circuit structures that are formed when carrying out the method of Figure 1, in accordance with some embodiments.

Figure 3 illustrates an example cross-sectional view taken along plane A-A of the IC structure of Figure 2J, in accordance with some embodiments.

10 Figure 4 illustrates a computing system implemented with integrated circuit structures and/or transistor devices formed using the techniques disclosed herein, in accordance with some embodiments of the present disclosure.

These and other features of the present embodiments will be understood better by reading the following detailed description, taken together with the figures herein described. In the drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of the disclosed techniques may have less than perfect straight lines and right angles, and some features may have surface topography or otherwise be non-smooth, given real-world limitations of fabrication processes. Further still, some of the features in the drawings may include a patterned and/or shaded fill, which is primarily provided to assist in visually differentiating the different features. In short, the figures are provided merely to show example structures.

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DETAILED DESCRIPTION

25 As transistors are scaled to include smaller critical dimensions and technology nodes proceed to smaller resolutions, various non-trivial issues occur. For example, as transistor dimensions scale down, problems encountered include increased threshold voltage, reduced drive current, and increased dopant diffusion (e.g., into the channel from the source/drain), thereby adversely affecting transistor performance. Such problems are enhanced when fabricating transistors with sub-30 nm gate lengths. Further, such problems are particularly significant for transistors fabricated via a gate

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last process (such as a replacement metal gate (RMG) process). For instance, dopant from one or both adjacent source/drain regions may undesirably diffuse into the channel region during the gate last/replacement gate process, such as during the high temperature anneal processes used to form the final gate stack (e.g., when depositing the replacement gate metal). Techniques for addressing these problems include complicated schemes aimed at controlling: dopant material via implantation; annealing process conditions; dopant material choices; and epitaxial deposition process conditions. While such techniques are intended to improve the short channel performance of transistors as gate lengths are scaled down, the techniques suffer from being ineffective and/or difficult to manufacture in a practical/efficient/cost-effective manner.

Thus, and in accordance with one or more embodiments of the present disclosure, techniques are provided for forming transistors including final source/drain (S/D) material processed after replacement gate processing. In some embodiments, at least one of the S/D regions may initially be formed with sacrificial S/D material that is intended to be removed and replaced later in the process flow with final S/D material. In some such embodiments, the sacrificial S/D material may be formed during the typical S/D region formation (e.g., after the dummy gate stack and gate spacers have been formed). Then, in some such embodiments, the sacrificial S/D material may be removed and replaced with final S/D material through a corresponding S/D contact trench, such that the final S/D material is not formed until near the end of the front-end-of line (FEOL) processing (e.g., almost to back-end-of-line (BEOL) processing), thereby delaying formation of the final S/D material until after replacement gate processing has occurred. Alternatively, in some embodiments, the insulator material (e.g., interlayer dielectric (ILD) material) over the sacrificial S/D material that was formed to assist with the replacement gate processing may be removed (as opposed to merely forming S/D contact trenches therein) to allow for the removal and replacement of the sacrificial S/D material with final S/D material.

As can be understood based on this disclosure, by delaying the formation of final S/D material in at least one of the S/D regions, undesired doping of the adjacent channel region can be minimized or completely avoided, as the high temperature processing (e.g., processing that exceeds 400, 450, 500, 550, or 600 degrees Celsius, such as high temperature anneals used in replacement gate metal deposition processing) can be completed (entirely or at least in part) prior to the formation of the final S/D material. In other words, by delaying the formation of final S/D material (e.g., via through-contact trench S/D processing to remove and replace sacrificial S/D material with final S/D

material), the techniques described herein can help address thermal budget constraints that may accompany the transistor fabrication process flow. In some embodiments, the temperature or thermal budget for forming the final S/D material may be kept relatively low to, for example, prevent gate stack issues (e.g., to prevent deterioration of the gate metal and also to enable keeping the gate dielectric thickness relative low, such as less than 1-2 nm), as well as providing better short channel control from reduced dopant diffusion from the final S/D material near/at the S/D-channel interface (e.g., the final S/D material in S/D tips under the gate spacers). Thus, the techniques described herein enable more effective and manufacturable methods for achieving enhanced short channel control when fabricating transistors having relatively small gate lengths (e.g., gate lengths less than 50, 45, 40, 35, 30, 25, 20, 15, 10 or 5 nm).

As can be understood based on this disclosure, the techniques can be implemented for transistors including group IV semiconductor material, group III-V semiconductor material, and/or any other suitable semiconductor material. The use of “group IV semiconductor material” (or “group IV material” or generally, “IV”) herein includes at least one group IV element (e.g., silicon, germanium, carbon, tin), such as silicon (Si), germanium (Ge), silicon germanium (SiGe), and so forth. The use of “group III-V semiconductor material” (or “group III-V material” or generally, “III-V”) herein includes at least one group III element (e.g., aluminum, gallium, indium) and at least one group V element (e.g., nitrogen, phosphorus, arsenic, antimony, bismuth), such as gallium arsenide (GaAs), indium gallium arsenide (InGaAs), indium aluminum arsenide (InAlAs), gallium phosphide (GaP), gallium antimonide (GaSb), indium phosphide (InP), and so forth. Note that group III may also be known as the boron group or IUPAC group 13, group IV may also be known as the carbon group or IUPAC group 14, and group V may also be known as the nitrogen family or IUPAC group 15, for example. For instance, in some embodiments, the techniques can be used to benefit transistors including channel material that includes Si, Ge, tin (Sn), indium (In), gallium (Ga), arsenic (As), and/or aluminum (Al).

The sacrificial S/D material may include any suitable material as will be apparent in light of this disclosure. In some embodiments, the sacrificial S/D material may be selected such that it can be selectively removed relative to the channel region material. For instance, in some such embodiments, the sacrificial S/D material may be selected such that it can be selectively etched relative to the channel region material using a wet etch process that includes a given etchant, where the given etchant removes the sacrificial S/D material without removing the channel region material

or the given etchant removes the sacrificial S/D material at a rate that is relatively faster than the removal of the channel region material (e.g., at least 1.5, 2, 3, 4, 5, 10, 20, 30, 40, 50, or 100 times faster, for a given etchant). In some embodiments, the sacrificial S/D material may include semiconductor material (e.g., group IV and/or group III-V semiconductor material); however, the present disclosure is not intended to be so limited unless otherwise stated. In some embodiments, the sacrificial S/D material may include undoped/intrinsic semiconductor material or minimally doped semiconductor material (e.g., with dopant concentrations of less than 1×10^{17} atoms per cubic centimeter (cm) of either n-type or p-type dopant). In some such embodiments, where the sacrificial S/D material is undoped (or minimally doped), the processing avoids dopants that would otherwise be included in the S/D material from undesirably diffusing into the material of the adjacent channel region (such as during high temperature anneals during replacement metal gate processing). To provide an example sacrificial S/D material, SiGe (e.g., intrinsic/undoped SiGe) may be used as a sacrificial S/D material, in some embodiments (e.g., for embodiments including a Si channel). In some such embodiments, the sacrificial SiGe may include a Ge concentration (by atomic percentage) in the range of 5-100% (e.g., in the subrange of 5-10, 5-20, 5-30, 5-50, 5-75, 10-20, 10-30, 10-50, 10-75, 10-100, 20-30, 20-50, 20-75, 20-100, 30-50, 30-75, 30-100, 50-75, 50-100, or 75-100%, or approximately 5, 10, 15, 20, 25, 30, 35, 40, 45, 50, 55, 60, 65, 70, 75, 80, 85, 90, 95, or 100%), or any other suitable value or range as will be apparent in light of this disclosure. Note that where SiGe includes a Ge concentration of 100%, it may just be considered Ge. To provide another example sacrificial S/D material, InP (e.g., intrinsic/undoped InP) may be used as a sacrificial S/D material, in some embodiments (e.g., for embodiments including a GaAs or InGaAs channel). Numerous material variations and configurations will be apparent in light of this disclosure.

In some embodiments, the techniques described herein can be used to benefit n-channel devices (e.g., n-MOS) and/or p-channel devices (e.g., p-MOS). Further, in some embodiments, the techniques described herein can be used to benefit MOSFET devices, tunnel FET (TFET) devices, high-electron-mobility transistor (HEMT) devices, and any other suitable devices as will be apparent in light of this disclosure. Further still, in some embodiments, the techniques described herein can be used to form complementary transistor circuits (such as CMOS circuits), where the techniques can be used to benefit one or more of the included n-type and p-type transistors making up the CMOS circuit. Further yet, in some embodiments, the techniques described herein can be used to benefit a multitude of transistor configurations, such as planar and non-planar configurations, where

the non-planar configurations may include finned or FinFET configurations (e.g., dual-gate or tri-gate), gate-all-around (GAA) configurations (e.g., nanowire or nanoribbon), or some combination thereof (e.g., a beaded-fin configurations), to provide a few examples. As previously stated, the techniques may be used to form only one of an S/D pair (i.e., either the source or the drain) for a given transistor, such that only one of S/D regions includes final material processed after replacement gate processing, in accordance with some embodiments. For instance, in some such embodiments, the final S/D material of one of the S/D regions may be formed when sacrificial S/D material of the other S/D regions is formed, where only that other S/D region has the S/D material (i.e., the sacrificial S/D material) removed and replaced after replacement gate processing. However, in other embodiments, both of the S/D regions (i.e., both the source and the drain) for a given transistor may be processed using the techniques described herein. Therefore, the techniques for forming transistors including final S/D material processed after replacement gate processing as described herein can benefit a multitude of transistor devices, as will be apparent in light of this disclosure.

Use of the techniques and structures provided herein may be detectable using tools such as: electron microscopy including scanning/transmission electron microscopy (SEM/TEM), scanning transmission electron microscopy (STEM), nano-beam electron diffraction (NBD or NBED), and reflection electron microscopy (REM); composition mapping; x-ray crystallography or diffraction (XRD); energy-dispersive x-ray spectroscopy (EDS); secondary ion mass spectrometry (SIMS); time-of-flight SIMS (ToF-SIMS); atom probe imaging or tomography; local electrode atom probe (LEAP) techniques; 3D tomography; or high resolution physical or chemical analysis, to name a few suitable example analytical tools. In particular, in some embodiments, such tools may indicate an integrated circuit (IC) including at least one transistor including final S/D material processed after replacement gate processing. In some such embodiments, the techniques may be detected based on the final S/D material extending into an overlying S/D contact trench, due to the material being deposited after the overlying S/D contact trench has been formed (as the processing may be performed through that S/D contact trench, prior to forming the S/D contact). In some embodiments, the techniques may be detected based on sacrificial S/D material still being present elsewhere on the IC. For instance, in some such embodiments, the techniques may be detected based on at least a portion of the sacrificial S/D material remaining near the transistor, such as the sacrificial S/D material being adjacent to the final S/D material that replaced the sacrificial S/D

material. Further, in some embodiments, the sacrificial S/D material formed when replacing a given fin may never be removed at all, where such non-removed sacrificial S/D material may be a dummy structure that was never processed into a transistor (and thus, a portion of the sacrificial S/D material feature was removed and replaced with final S/D material).

5 In some embodiments, the techniques and structures described herein may be detected based on the benefits derived therefrom, such as the reduction or elimination of undesired/unintentional doping of the channel region via diffusion from adjacent S/D material (which can be achieved using through-contact S/D processing). For instance, elemental mapping via, e.g., secondary ion mass spectrometry, transmission electron microscopy, or atom probe tomography can be used look at
10 composition profiles across the S/D-channel interfaces and identify very sharp dopant profiles that can be achieved using the techniques described herein. Further, in some embodiments, the techniques described herein may enable forming transistor devices with sub-30 nm gate lengths (or gate lengths below some other suitable threshold as will be apparent in light of this disclosure), which can also be detected and measured. In some embodiments, the techniques enable transistor
15 scaling (particularly for non-planar transistors) to future nodes (with relatively smaller gate lengths and novel material schemes) to ensure low operating voltage, higher drive currents, faster switching speeds, and thereby an overall improved performance. Numerous configurations and variations will be apparent in light of this disclosure.

Architecture and Methodology

20 Figure 1 illustrates a method 100 of forming an integrated circuit (IC) including final source/drain (S/D) material processed after replacement gate processing, in accordance with some embodiments of the present disclosure. Figures 2A-J illustrate example integrated circuit structures that are formed when carrying out method 100 of Figure 1, in accordance with some embodiments. The structures of Figures 2A-J are primarily depicted and described herein in the context of forming
25 transistor devices having finned configurations (e.g., FinFET or tri-gate), for ease of illustration and description. However, in some embodiments, the techniques can be used to form transistors of any suitable any suitable geometry or configuration, as can be understood based on this disclosure. For example, Figure 2G illustrates an example integrated circuit structure including transistors having nanowire configurations, as will be described in more detail below. Note that method 100 can be
30 used to benefit a multitude of different transistor types, such as MOSFET devices, TFET devices, HEMT devices, and/or any other suitable devices as will be apparent in light of this disclosure. In

some embodiments, method 100 can be used to benefit n-channel devices (e.g., n-MOS) and/or p-channel devices (e.g., p-MOS). Further still, in some embodiments, method 100 can be used to benefit complementary transistor circuits (such as CMOS circuits), where either one or both of included n-type and p-type transistors making up the CMOS circuit are formed using the techniques described herein. Other example transistor devices can include few to single electron quantum transistor devices and some devices may employ semiconductor materials that are three dimensional crystals as well as two dimensional crystals or nanotubes, in accordance with some embodiments. In some embodiments, the techniques may be used to benefit devices of varying scales, such as IC devices having critical dimensions in the micrometer (micron) range and/or in the nanometer (nm) range (e.g., formed at the 22, 14, 10, 7, 5, or 3 nm process nodes, or beyond).

Method 100 of Figure 1 includes patterning 102 substrate 200 (which is intended to at least partially be used as transistor channel region material) into fins 202 to form the example resulting structure shown in Figure 2B, in accordance with some embodiments. As can be understood based on this disclosure, in some embodiments, at least a portion of substrate 200 may be used for the channel region material for one or more transistors formed therefrom. However, the present disclosure is not intended to be so limited. For example, layer 200 may be a channel region material layer from which the channel region of one or more transistors are formed, but it need not be the bottom-most layer of an IC structure (which is commonly referred to as a substrate), in accordance with some embodiments. For instance, layer 200 may include one or more underlying layers (e.g., a bulk wafer layer), in some embodiments. However, for ease of illustration, the following description will treat layer 200 as both the substrate and the channel region material layer, as will be apparent in light of this disclosure.

As shown in the example structure of Figure 2A, and to form the structure of Figure 2B, hardmask 210 was patterned on substrate 200 to assist with forming substrate 200 into fins 202, in this example embodiment. Hardmask 210 may be formed or deposited on substrate 200 using any suitable technique, as will be apparent in light of this disclosure. For example, hardmask 210 may be blanket deposited or otherwise grown on substrate 200 using chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), spin-on processing, and/or any other suitable process to form hardmask 210 on substrate 200. In some instances, the top surface of substrate 200 on which hardmask 210 is to be deposited may be treated (e.g., chemical treatment, thermal treatment, etc.) prior to deposition of the hardmask 210 material. Hardmask 210 can be

patterned 102 using any suitable techniques, such as one or more lithography and etch processes, for example. Hardmask 210 may include any suitable material, such as oxide material, nitride material, and/or any other suitable dielectric material, for example. Specific oxide and nitride materials may include silicon oxide, titanium oxide, hafnium oxide, aluminum oxide, silicon nitride, and titanium nitride, just to name a few examples. In some cases, the material of hardmask 210 may be selected based on the material of substrate 200, for example.

Substrate 200, in some embodiments, may include: a bulk substrate including group IV semiconductor material, such as silicon (Si), germanium (Ge), silicon germanium (SiGe), or silicon carbide (SiC), and/or group III-V material and/or any other suitable material(s) as will be apparent in light of this disclosure; an X on insulator (XOI) structure where X is one of the aforementioned materials (e.g., group IV and/or group III-V semiconductor material) and the insulator material is an oxide material or dielectric material or some other electrically insulating material; or some other suitable multilayer structure where the top layer includes one of the aforementioned materials (e.g., group IV and/or group III-V semiconductor material). As previously described, the use of “group IV semiconductor material” (or “group IV material” or generally, “IV”) herein includes at least one group IV element (e.g., silicon, germanium, carbon, tin), such as silicon (Si), germanium (Ge), silicon germanium (SiGe), and so forth. The use of “group III-V semiconductor material” (or “group III-V material” or generally, “III-V”) herein includes at least one group III element (e.g., aluminum, gallium, indium) and at least one group V element (e.g., nitrogen, phosphorus, arsenic, antimony, bismuth), such as gallium arsenide (GaAs), indium gallium arsenide (InGaAs), indium aluminum arsenide (InAlAs), gallium phosphide (GaP), gallium antimonide (GaSb), indium phosphide (InP), and so forth. Note that group III may also be known as the boron group or IUPAC group 13, group IV may also be known as the carbon group or IUPAC group 14, and group V may also be known as the nitrogen family or IUPAC group 15, for example. In some embodiments, substrate 200 may be doped with any suitable n-type and/or p-type dopant. For instance, in the case, of a Si substrate, the Si may be p-type doped using a suitable acceptor (e.g., boron) or n-type doped using a suitable donor (e.g., phosphorous, arsenic), to provide some example cases. However, in some embodiments, substrate 200 may be undoped/intrinsic or relatively minimally doped (such as including a dopant concentration of less than 1×10^{17} atoms per cubic centimeter (cm)), for example.

In some embodiments, substrate 200 may include a surface crystalline orientation described by a Miller Index of $\langle 100 \rangle$, $\langle 110 \rangle$, or $\langle 111 \rangle$, or its equivalents, as will be apparent in light of this

disclosure. Although substrate 200, in this example embodiment, is shown as having a thickness (dimension in the Y-axis direction) similar to other layers shown in subsequent structures for ease of illustration, in some instances, substrate 200 may be much thicker than the other layers, such as having a thickness in the range of 50 to 950 microns, for example, or any other suitable thickness as will be apparent in light of this disclosure. In some embodiments, substrate 200 may be used for one or more other IC devices, such as various diodes (e.g., light-emitting diodes (LEDs) or laser diodes), various transistors (e.g., MOSFETs or TFETs), various capacitors (e.g., MOSCAPs), various microelectromechanical systems (MEMS), various nanoelectromechanical systems (NEMS), various radio frequency (RF) devices, various sensors, or any other suitable semiconductor or IC devices, depending on the end use or target application. Accordingly, in some embodiments, the structures described herein may be included in a system-on-chip (SoC) application, as will be apparent in light of this disclosure.

Continuing with process 102 to form at least a portion of substrate 200 into fins, any suitable techniques may be used to form the example resulting structure of Figure 2B, such as performing a shallow trench recess (STR) etch, in accordance with an embodiment. The STR etch used to form trenches 215 and fins 202 may include any suitable techniques, such as any suitable wet and/or dry etching processes, for example. In some such cases, the STR etch may be performed in-situ/without air break, while in other cases, the STR etch may be performed ex-situ, for example. Trenches 215 may be formed with varying widths (dimension in the X-axis direction) and depths (dimension in the Y-axis direction) as can be understood based on this disclosure. For example, multiple hardmask patterning and STR etch processes may be performed to achieve varying depths in the trenches 215 between fins 202. Fins 202 may be formed to have varying widths F_w (dimension in the X-axis direction) and heights F_h (dimension in the Y-axis direction). For example, in embodiments employing an aspect ratio trapping (ART) integration scheme, the fins may be formed to have particular height to width ratios such that if they are later removed or recessed, the resulting fin-shaped trenches formed allow for defects in the replacement material deposited to terminate on a side surface as the material grows vertically, such as non-crystalline/dielectric sidewalls, where the sidewalls are sufficiently high relative to the size of the growth area so as to trap most, if not all, of the defects, if such an ART scheme is used. As can be understood in some such embodiments, the channel region material need not be native to substrate 200 (as opposed to the structures formed using method 100, as will be apparent in light of this disclosure).

In some embodiments, the fin widths Fw may be in the range of 4-400 nm (e.g., in the subrange of 4-10, 4-20, 4-50, 4-100, 4-200, 10-20, 10-50, 10-100, 10-200, 10-400, 50-100, 50-200, 50-400, or 100-400 nm), for example, or any other suitable value or range, as will be apparent in light of this disclosure. In some embodiments, the fin heights Fh may be in the range of 4-800 nm (e.g., in the subrange of 4-10, 4-20, 4-50, 4-100, 4-200, 4-400, 10-20, 10-50, 10-100, 10-200, 10-400, 10-800, 50-100, 50-200, 50-400, 50-800, 100-400, 100-800, or 400-800 nm), for example, or any other suitable value or range, as will be apparent in light of this disclosure. In embodiments employing an aspect ratio trapping (ART) scheme, the fins may be formed to have particular height to width ratios such that when they are later recessed and/or removed, the resulting fin trenches formed allow for defects in the replacement material deposited to terminate on a side surface as the material grows vertically, such as non-crystalline/dielectric sidewalls, where the sidewalls are sufficiently high relative to the size of the growth area so as to trap most, if not all, of the defects. In some such embodiments, the height to width ratio of the fins (Fh:Fw) may be greater than 1, such as greater than 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, 9, or 10, or any other suitable threshold ratio, as will be apparent in light of this disclosure. Note that the trenches 215 and fins 202 are each shown in Figure 2B as having the same relative sizes and shapes in this example structure for ease of illustration; however, the present disclosure is not intended to be so limited. For example, in some embodiments, the fins 202 may be formed to have varying heights Fh and/or varying widths Fw. Moreover, in some embodiments, the trenches 215 between fins 202 may be formed to have varying depths and/or varying widths. Further note that although four fins 202 are shown in the example structure of Figure 2B, any number of fins may be formed, such as one, two, three, five, ten, hundreds, thousands, millions, and so forth, as can be understood based on this disclosure.

Method 100 of Figure 1 continues with filling 104 trenches 215 with shallow trench isolation (STI) material 220 and polishing/planarizing to form the resulting example structure shown in Figure 2C, in accordance with some embodiments. In some embodiments, filling process 104 may include any suitable deposition/growth process described herein (e.g., CVD, ALD, PVD), or any other suitable deposition process. In some embodiments, STI material 220 may include any suitable insulating material, such as one or more dielectric, oxide (e.g., silicon dioxide), and/or nitride (e.g., silicon nitride) materials. In some embodiments, STI material 220 may be selected based on the material of substrate 200. For instance, in the case of a Si substrate, STI material may be silicon dioxide or silicon nitride, to provide some examples.

Method 100 of Figure 1 continues with recessing 106 the STI material 220 to cause at least a portion 204 of fins 202 to exude from the STI plane, thereby forming the resulting example structure shown in Figure 2D, in accordance with some embodiments. As can be understood based on this disclosure, fin portions 204 may be used in the active channel region of one or more transistors, such that fin portions 204 (the portions of fins 202 above the top plane of STI layer 220) may be referred to as active fin portions herein, for example. Moreover, the remaining portions of fins 202 below the top plane of STI layer 220 are indicated as portions 203, where such portions may be referred to as sub-fin and/or sub-channel portions, for example. As shown in Figure 2D, the portions 204 of fins 202 exuding above the top plane of STI layer 220 have an active fin height indicated as F_{ah} , which may be in the range of 4-800 nm (e.g., in the subrange of 4-10, 4-20, 4-50, 4-100, 4-200, 4-400, 10-20, 10-50, 10-100, 10-200, 10-400, 10-800, 50-100, 50-200, 50-400, 50-800, 100-400, 100-800, or 400-800 nm), for example, or any other suitable value or range, as will be apparent in light of this disclosure.

Recall that in the example embodiment of Figure 2D, fins portions 203 and 204 (from fins 202) are native to substrate 200. In other words, fins 202 were formed from substrate 200 in this example embodiment and thus both of features 200 and 202 include the same material in the structure of Figure 2D, such that fins 202 (including portions 203 and 204) and substrate 200 are one homogenous structure. However, as previously described, in other embodiments, some or all of fins 202 may be removed and replaced with replacement fins, for example. In some such embodiments, the processing may continue from the structure of Figure 2C and include etching the fins 202 (e.g., using any suitable wet and/or dry etch processes) to form fin-shaped trenches between STI layer 220, where the etching either completely or partially removes fins 202 (e.g., either goes all the way to/past the bottom plane of STI layer 220 or does not, respectively). In such embodiments, the fin trenches can be used for the deposition of a replacement material, and continuing with recess process 106 would result in the fins of Figure 2D being replacement fins (which may include different material than what is included in substrate 200). In some such embodiments, the replacement material may include group IV semiconductor material and/or group III-V semiconductor material, and/or any other suitable material as will be apparent in light of this disclosure. For instance, replacement fins including SiGe may be formed by removing native Si fins during such processing and replacing them with the SiGe material, to provide an example. Note that in some such embodiments where the fins are removed and replaced (and thus, are not native fins),

an ART processing scheme may be employed, where the fin trenches have a high aspect ratio (e.g., height:width ratio of greater than 1, 1.5, 2, 3, 4, 5, or a higher value). Such an ART processing scheme may be employed, for example to trap dislocations, thereby preventing the dislocations from reaching the epitaxial film surface and greatly reducing the surface dislocation density within the trenches.

Regardless of whether active fin portions 204 are native to substrate 200 or not, method 100 of Figure 1 continues with forming 108 a dummy gate stack, including dummy gate dielectric 242 and dummy gate 244, thereby forming the example resulting structure of Figure 2E, in accordance with some embodiments. In this example embodiment, dummy gate dielectric 242 (e.g., dummy oxide material) and dummy gate or dummy gate electrode 244 (e.g., dummy poly-silicon material) may be used for a replacement gate process. Note that side-wall spacers 250, referred to generally as gate spacers (or simply, spacers), on either side of the dummy gate stack were also formed, and such spacers 250 can help determine the channel length and can help with the replacement gate processes, for example. As can be understood based on this disclosure, the dummy gate stack (and spacers 250) can help define the channel region and source/drain (S/D) regions of each fin, where the channel region is below the dummy gate stack (as it will be located below the final gate stack), and the S/D regions are on either side of the channel region. Note that because the IC structures are being primarily described in the context of forming finned transistors, the final gate stack will also be adjacent to either side of the fin, as the gate stack will reside along three walls of the finned channel regions, in some embodiments. Formation of the dummy gate stack may include depositing the dummy gate dielectric material 242 and dummy gate electrode material 244, patterning the dummy gate stack, depositing gate spacer material 250, and performing a spacer etch to form the structure shown in Figure 2E, for example. Spacers 250 may include any suitable material, such as any suitable electrical insulator, dielectric, oxide (e.g., silicon oxide), and/or nitride (e.g., silicon nitride) material, as will be apparent in light of this disclosure. Note that in some embodiments, a hardmask (not shown) may be formed over the dummy gate stack (which may also be formed over spacers 250) to protect the dummy gate stack during subsequent processing, for example.

Method 100 of Figure 1 continues with forming 110 sacrificial S/D material 260 to form the example resulting structure of Figure 2F, in accordance with some embodiments. Note that in addition to sacrificial S/D material 260 being formed during the S/D region processing, final S/D material 261 was also formed in this example embodiment, which will be described in more detail

herein. In some embodiments, the sacrificial S/D material 260 may be formed using any suitable techniques, such as masking regions outside of the S/D regions to be processed, etching portions of the fins from the structure of Figure 2E (in this example case, active portions 204 were etched and removed, leaving only sub-fin portions 203 upon which replacement S/D material was formed, as shown), and forming/depositing/growing the sacrificial S/D material (e.g., using any suitable techniques, such as CVD, metal-organic CVD (MOCVD), ALD, molecular beam epitaxy (MBE), PVD), for example. In some embodiments, the source regions may be processed separately from the drain regions, as they may include different sacrificial material or only one of the S/D regions may include sacrificial material. Further, in some embodiments, post-gate replacement (e.g., through-contact trench) S/D processing need not be performed for both of the S/D regions of a given transistor. Further still, different S/D regions on a given IC structure may be processed than other S/D regions, thereby allowing for any combination of replacement material S/D regions at this stage, where the replacement material may include final S/D material or sacrificial S/D material to be later removed and replaced with final S/D material (e.g., via through-S/D contact processing).

Thus, in some embodiments, an S/D region not including sacrificial S/D material 260 may be formed with final S/D material at this stage of the process flow, as can be understood based on this disclosure (such as is shown in Figure 2F with the second left-most S/D set, where the front-most fin portion was replaced with sacrificial S/D material 260 and the back-most fin portion was replaced with final S/D material 261). In some such embodiments, one of the S/D regions (either the source region or drain region) may be masked off while processing occurs in the other S/D region, and then the masking and processing can be switched, for example. This can be repeated as many times as desired to form any combination of desired replacement material S/D regions, whether the replacement material is final S/D material or sacrificial S/D material. For instance, in the example structure of Figure 2F, the left-most S/D regions were also processed to include final S/D material 261. As can be understood based on this disclosure, such a combination of final and sacrificial S/D material may be utilized when forming different transistor types on the same IC. For instance, the left-most fin that includes final S/D material 261 may be formed into one of an n-MOS device or a p-MOS device, where it may be desired to process the final S/D material (e.g., n-type doped semiconductor material or p-type doped semiconductor material, respectively) at this stage, whereas the right-most fin that includes sacrificial S/D material 260 may be formed into the other of an n-MOS device or a p-MOS device, where it may be desired to process the final S/D material after

replacement gate processing (e.g., through-S/D contact trenches). In other words, the techniques described herein enable final p-type doped S/D regions to be processed at a different stage in the process flow than final n-type doped S/D regions. Numerous different techniques for processing the S/D regions will be apparent in light of this disclosure.

5 The sacrificial S/D material may include any suitable material as will be apparent in light of this disclosure. In some embodiments, the sacrificial S/D material may be selected such that it can be selectively removed relative to the channel region material. For instance, in some such embodiments, the sacrificial S/D material may be selected such that it can be selectively etched relative to the channel region material using a wet etch process that includes a given etchant, where
10 the given etchant removes the sacrificial S/D material without removing the channel region material or the given etchant removes the sacrificial S/D material at a rate that is relatively faster than the removal of the channel region material (e.g., at least 1.5, 2, 3, 4, 5, 10, 20, 30, 40, 50, or 100 times faster, for a given etchant). In some embodiments, the sacrificial S/D material may also be selected such that it can be selectively removed relative to the material of ILD layer 270 (which is described
15 in more detail below) and/or the material underlying the sacrificial S/D material (the material of sub-fin portion 203, in this example case), such that the sacrificial S/D material can be removed later in the process flow without significantly/critically affecting the material of ILD layer 270 and/or the underlying material. For instance, in some such embodiments, the sacrificial S/D material may be selected such that it can be selectively etched relative to the material of ILD layer 270 and/or the
20 underlying material using a wet etch process that includes a given etchant, where the given etchant removes the sacrificial S/D material without removing the channel region material or the given etchant removes the sacrificial S/D material at a rate that is relatively faster than the removal of the channel region material (e.g., at least 1.5, 2, 3, 4, 5, 10, 20, 30, 40, 50, or 100 times faster, for a given etchant).

25 In some embodiments, the sacrificial S/D material may include semiconductor material (e.g., group IV and/or group III-V semiconductor material); however, the present disclosure is not intended to be so limited unless otherwise stated. For instance, in some embodiments, sacrificial S/D material 260 may include SiGe, where the Ge concentration (by atomic percentage) in the sacrificial SiGe may be in the range of 5-100% (e.g., in the subrange of 5-10, 5-20, 5-30, 5-50, 5-75,
30 10-20, 10-30, 10-50, 10-75, 10-100, 20-30, 20-50, 20-75, 20-100, 30-50, 30-75, 30-100, 50-75, 50-100, or 75-100%, or approximately 5, 10, 15, 20, 25, 30, 35, 40, 45, 50, 55, 60, 65, 70, 75, 80, 85,

90, 95, or 100%), or any other suitable value or range as will be apparent in light of this disclosure. Note that where SiGe includes a Ge concentration of 100%, it may just be considered Ge. Generally, in some embodiments, sacrificial S/D material 260 may include any suitable group IV semiconductor material, such as Si, SiGe, and/or Ge, for example. In addition, in some
5 embodiments, sacrificial S/D material 260 may include InGaAs, where the In concentration (by atomic percentage of the included group III materials) in the sacrificial InGaAs may be in the range of 5-60% (e.g., in the subrange of 5-10, 5-20, 5-40, 10-20, 10-40, 10-60, 20-40, 20-60, or 40-60%), or some other suitable concentration as will be apparent in light of this disclosure. Generally, in some embodiments, sacrificial S/D material 260 may include any suitable group III-V
10 semiconductor material, such as GaAs, InGaAs, InAs, and/or InP, for example. In some embodiments, sacrificial S/D material 260 may include impurity dopants, such as to assist with selectively removing the sacrificial material 260 through contact trench processing, for example. However, in other embodiments, the sacrificial S/D material 260 may be intrinsic/undoped or relatively minimally doped (e.g., with dopant concentration of less than $1E17$ atoms per cubic cm),
15 to prevent any included dopant from diffusing into the adjacent channel region during subsequent processing (e.g., during high temperature replacement gate anneal processing), as can be understood based on this disclosure. Thus, the use of sacrificial S/D material can help prevent the adjacent channel region from being doped in an unintentional/undesired manner, thereby improving transistor performance, as can be understood based on this disclosure.

20 Method 100 of Figure 1 continues with depositing 112 isolation material 270 and patterning/recessing to expose the dummy gate stack, followed by performing 114 the final gate stack processing to form the example resulting structure of Figure 2G, in accordance with some embodiments. As shown in Figure 2G, the processing in this example embodiment included depositing interlayer dielectric (ILD) layer 270 on the structure of Figure 2F, followed by
25 planarization and/or polishing to reveal the dummy gate stack. Note that ILD layer 270 is shown as transparent in the example structure of Figure 2G to allow for the underlying features to be seen; however, the present disclosure is not intended to be so limited. In some embodiments, the ILD layer 270 may include any suitable electrical insulator, dielectric, oxide (e.g., silicon oxide), and/or nitride (e.g., silicon nitride) material, as will be apparent in light of this disclosure. Recall that in
30 this example embodiment, the gate stack is formed using a gate last flow (also called a replacement gate or replacement metal gate (RMG) process). The gate stack processing, in this example

embodiment, continued with removing the dummy gate stack (including dummy gate 244 and dummy gate dielectric 242) to allow for the final gate stack to be formed.

Note that when the dummy gate is removed, the finned channel regions (from active fin portions 204 that were covered by the dummy gate) are exposed to allow for any desired processing of those channel regions. Such processing of a given channel region may include various different techniques, such as removing and replacing a given channel region with replacement material, doping a given channel region as desired, forming a given channel region into one or more nanowires (or nanoribbons) for a gate-all-around (GAA) transistor configuration, cleaning/polishing a given channel region, and/or any other suitable processing as will be apparent in light of this disclosure. For instance, finned channel region 206 is illustrated (which is the channel region of the right-most of the four original finned structures), which may have been formed by doping the native fin 204 with a desired suitable n-type or p-type dopant, for example. However, in other embodiments, finned channel region 206 may include the exact same material as active fin portions 204 previously formed, and such material may be intrinsic/undoped semiconductor material, for example. To provide another example, nanowire channel region 208 (which is the channel region of the left-most of the four original finned structures) may have been formed after the dummy gate was removed and the channel regions of the fins were exposed, by converting the finned structure at that location into the nanowires 208 shown using any suitable techniques, for example. For instance, the original finned channel region may have included a multilayer structure, where one or more of the layers are sacrificial and can be selectively etched to remove those sacrificial layers and release the nanowires 208. As shown in Figure 2G, nanowire channel region 208 includes 2 nanowires (or nanoribbons) in this example case. However, a nanowire (or nanoribbon or GAA) transistor formed using the techniques disclosed herein may include any number of nanowires (or nanoribbons) such as 1, 3, 4, 5, 6, 7, 8, 9, 10, or more, depending on the desired configuration.

As can be understood based on this disclosure, the channel region is at least below the gate stack, in this example embodiment. For instance, in the case of a finned transistor configuration, the channel region may be below and between the gate stack, as the stack is formed on three sides as is known in the art. However, if the transistor device were inverted and bonded to what will be the end substrate, then the channel region may be above the gate. Therefore, in general, the gate and channel relationship may include a proximate relationship (which may or may not include intervening gate dielectric layer and/or other suitable layers), where the gate is near the channel

region such that it can exert control over the channel region in some manner (e.g., in an electrical manner), in accordance with some embodiments. Further, in the case of a nanowire (or nanoribbon or GAA) transistor configuration, the gate stack may completely surround each nanowire/nanoribbon in the channel region (or at least substantially surround each nanowire, such as surrounding at least 70, 80, or 90% of each nanowire). Further still, in the case of a planar transistor configuration, the gate stack may simply be above the channel region. In some embodiments, the channel region may include group IV semiconductor material (e.g., Si, SiGe, Ge), group III-V semiconductor material (e.g., GaAs, InGaAs, InAs), and/or any other suitable material as will be apparent in light of this disclosure. In some embodiments, semiconductor material included in the channel region may be native to substrate 200 and/or semiconductor material included in the channel region may not be native to substrate 200 (e.g., such that it is replacement material or material formed above substrate 200). Recall that in some embodiments, the channel region may be doped (e.g., with any suitable n-type and/or p-type dopant) or intrinsic/undoped (or relatively minimally doped), depending on the particular configuration.

Note that S/D regions are adjacent to either side of a corresponding channel region, as can be seen in Figures 2G and 3, for example. More specifically, S/D regions are directly adjacent to a corresponding channel region, such that there are no intervening layers between either of the S/D regions and the channel region, in the example embodiments. However, the present disclosure is not intended to be so limited. Also note that the configuration/geometry of a transistor formed using the techniques described herein may primarily be described based on the shape/configuration of the respective channel region of that transistor, for example. For instance, a nanowire (or nanoribbon or GAA) transistor may be referred to as such because it includes one or more nanowires (or nanoribbons) in the channel region of that transistor. However, the transistor type (e.g., MOSFET, TFET, HEMT, or other suitable type) may be described based on the doping and/or operating scheme of the source, channel, and drain regions, and thus those respective regions may be used to determine the type or classification of a given transistor, for example. This is especially true for MOSFET versus TFET transistors, as they may structurally be very similar (or the same), but include different doping schemes (e.g., source-drain doping schemes for MOSFET of p-p or n-n versus p-n or n-p for TFET).

Continuing with performing 114 final gate stack processing, after the dummy gate has been removed and any desired channel region processing has been performed, the final gate stack can

then be formed, in accordance with some embodiments. In this example embodiment, the final gate stack includes gate dielectric layer 282 and gate 284, as shown in Figure 2G. The gate dielectric layer 282 may include, for example, any suitable oxide (such as silicon dioxide), high-k gate dielectric material, and/or any other suitable material as will be apparent in light of this disclosure.

5 Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate, to provide some examples. In some embodiments, an annealing process may be carried out

10 on the gate dielectric layer 282 to improve its quality when high-k material is used. The gate 284 (or gate electrode) may include a wide range of materials, such as polysilicon, silicon nitride, silicon carbide, or various suitable metals or metal alloys, such as aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), copper (Cu), titanium nitride (TiN), or tantalum nitride (TaN), for example. In some embodiments, gate dielectric layer 282 and/or gate 284 may include a multilayer structure of

15 two or more material layers, for example. In some embodiments, gate dielectric layer 282 and/or gate 284 may include grading (e.g., increasing and/or decreasing) the content/concentration of one or more materials in at least a portion of the feature(s). Additional layers may be present in the final gate stack, in some embodiments, such as one or more work function layers or other suitable layers, for example. Note that although gate dielectric layer 282 is only shown below gate 284 in the

20 example embodiment of Figure 2G, in other embodiments, the gate dielectric layer 282 may also be present on one or both sides of gate 284, such that the gate dielectric layer 282 may also be between gate 284 and one or both of spacers 250, for example. Numerous different gate stack configurations will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with forming 116 S/D contact trenches 290 in the isolation

25 material (e.g., ILD layer 270) to form the example resulting structure of Figure 2H, in accordance with some embodiments. Such processing may include any suitable techniques, such as one or more wet and/or dry etch processes, to form contact trenches 290 in ILD layer 270 over one or more of the S/D regions. Note that, in this example embodiment, S/D contact trenches were only formed over S/D regions to be processed through those contacts (e.g., by removing and replacing sacrificial S/D

30 material 260), and thus, S/D contact trenches were not formed over the other S/D regions. Specifically, S/D contact trenches were not formed over final S/D material regions 261 in this

example embodiment, as contact to those S/D regions will be made at a later stage in the process flow. However, in some embodiments, S/D contact trenches may also be formed in such areas (e.g., over final S/D material regions 261), such as where the removal and replacement of sacrificial S/D material 260 will not affect those areas or those areas may be masked off prior to performing the removal and replacement process (so those areas are not affected).

In addition, not all sacrificial S/D material regions 260 may be used in transistor devices, and thus, not all of the sacrificial S/D material regions 260 may be further processed (e.g., removed and replaced with final S/D material). For instance, the second right-most set of sacrificial S/D material regions 260 are not to be processed further and thus may be dummy sacrificial S/D material regions that remain in the final IC structure. Such dummy sacrificial S/D material structures can be utilized to detect use of the techniques described herein, for example. Generally, formation of contact trenches 290 allows for processing of the underlying S/D regions therethrough, as can be understood based on this disclosure. Note that the contact trenches 290 are all shown as discrete trenches in this example embodiment (e.g., one trench per single S/D region); however, the present disclosure is not intended to be so limited, such that a single trench may access multiple S/D regions (e.g., multiple adjacent source regions or multiple adjacent drain regions), in some embodiments.

Method 100 of Figure 1 continues with processing 118 one or more S/D regions through contact trenches 290 to form the example resulting structure of Figure 2I, in accordance with some embodiments. In some embodiments, the through-contact trench processing may include any suitable techniques, such as performing one or more wet and/or dry etch processes (e.g., one or more selective etch processes) to remove sacrificial S/D material 260 from portions below the trenches 290 and then forming the final S/D material 262 using any suitable techniques (e.g., via CVD, MOCVD, ALD, MBE, or PVD). In some such embodiments, selective etch processing used to remove sacrificial S/D material 260 may be performed without adversely affecting other exposed material (such as the material of ILD layer 270, and the material of the eventually exposed sub-fin portions 203 and channel regions). In some such embodiments, one or more features may be masked off to assist with preventing adversely affecting the feature(s). In this example embodiment, it can be seen that the three S/D regions that included overlying contact trenches 290 were processed to remove sacrificial S/D material regions 260 and replace them with final S/D material 262. As can also be seen in Figure 2I, the final material 262 of the S/D regions that were processed through contact trenches 290 extends into each corresponding contact trench 290; however, the present

disclosure is not intended to be so limited unless otherwise stated. Moreover, in this example embodiment, sacrificial S/D material 260 remains in portions where contact trenches 290 did not provide access thereto and thus such unexposed sacrificial S/D material was not removed, such as in portions adjacent to the processed S/D regions that were not below the contact trenches 290 (e.g., the portions adjacent the S/D regions opposite the side of those regions that are adjacent to the channel region).

In some embodiments, the source region of a given transistor may be processed separately from the drain region of the given transistor, as the S/D regions may include different material and/or different doping types, as can be understood based on this disclosure. In some such embodiments, one of the S/D regions (either the source region or drain region) may be masked off or still include ILD layer 270 (while the other has it removed) while processing occurs for the other of the S/D regions, and then the process can be repeated in reverse order to process the originally masked off (or otherwise non-processed) S/D region. However, processing may occur to both S/D regions for a given transistor simultaneously. In some embodiments, the native fin 204 material (i.e., native to substrate 200) may remain in one or both of the S/D regions, where such native material can be doped to form final S/D region material (which may occur earlier in the process flow, for example). Thus, the material of the S/D regions may include native and/or replacement material, such that there may or may not be a distinct interface between the sub-fin portions 203 and the S/D regions. Note that even in embodiments where material native to substrate 200 is used in an S/D region, there may still be a distinct interface between that S/D region and the sub-fin 203, because of impurity dopants introduced into the S/D region, for example.

In some embodiments, when forming final S/D material (such as final S/D material 262) through S/D contact trenches, the deposition processing may be performed using relatively low temperatures, such as temperatures of less than 600, 550, 500, 450, or 400 degrees Celsius, or any other suitable threshold temperature as will be apparent in light of this disclosure. In some such embodiments, such processing can be beneficial from a dopant diffusion into the channel region standpoint, as final gate stack processing may include temperatures over those thresholds, such as temperatures over 600, 650, or 700 degrees Celsius, for example. Thus, by using relatively lower temperatures to deposit the final S/D material, in some embodiments, the techniques described herein can prevent deterioration of the final gate stack (e.g., that may include a metal gate) and also enables keeping the gate dielectric thickness (dimension between the gate and the channel) relatively

low (e.g., less than 3, 2, or 1 nm), as well as providing better short channel control from reduced dopant diffusion from the S/D regions into the adjacent channel region. Note that features 260, 261, and 262 are illustrated with patterning/shading to merely assist with visually identifying those features; however, the patterning/shading is not intended to limit the present disclosure in any manner. Also note that the structure of the S/D regions is also shown in Figure 3, which illustrates an example cross-sectional view taken along plane A-A of the IC structure of Figure 2J, which will be described in more detail below. Thus, the cross-sectional view of Figure 3 helps to illustrate such S/D regions and the transistor structure in general, for instance. Numerous different techniques for processing the S/D regions will be apparent in light of this disclosure.

In some embodiments, the S/D regions may include any suitable material, such as group IV semiconductor material (e.g., Si, SiGe, Ge), group III-V semiconductor material (e.g., GaAs, InGaAs, InAs), and/or any other suitable semiconductor material, and may also include any suitable doping scheme, as will be apparent in light of this disclosure. When impurity dopants are included in semiconductor material of a layer/region/feature, the impurity dopants can convert the semiconductor material to extrinsic semiconductor material (as opposed to intrinsic semiconductor material), as can be understood based on this disclosure. Such doping intentionally introduces the impurities in semiconductor material to, for example, modulate the electrical properties of the semiconductor material. Therefore, such impurity doping may be used to change the electrical properties of included group IV and/or group III-V semiconductor material, for instance. In some embodiments, doping semiconductor material may be achieved using any suitable techniques, such as via diffusion, ion implantation, depositing/growing the dopants with the primary semiconductor material, and/or any other suitable techniques as will be apparent in light of this disclosure. In some embodiments, the dopants may be introduced into native semiconductor material (native to the substrate) and/or replacement semiconductor material (e.g., that is epitaxially formed), for instance. Further, in embodiments where implantation is used, the impurity dopants may be implanted with or without preamorphizing treatments, for example. Any number of doping processes may be performed as desired to introduce suitable n-type and/or p-type dopant into the semiconductor material of the source, drain, and/or channel regions, as will be apparent in light of this disclosure.

In some embodiments, semiconductor material included in at least one of the layers/regions/features (e.g., in the channel region) may not be intentionally doped, such that the semiconductor material is intrinsic or nominally undoped. Such nominal doping may occur as a

result of undesired diffusion, for example, and thus, the use of “nominally undoped” with reference to semiconductor material or a layer/region/feature including semiconductor material includes having an impurity dopant concentration of less than $1\text{E}15$, $1\text{E}16$, $1\text{E}17$, or $1\text{E}18$ atoms per cubic centimeter (cm), or less than some other suitable threshold amount, as will be apparent in light of this disclosure. Note that when dopants are present in the semiconductor material of any layer/region feature of a transistor device, the dopants may be present in any suitable concentration, such as in a concentration in the range of $1\text{E}15$ to $5\text{E}22$ atoms per cubic centimeter (cm), or any other suitable concentration as will be apparent in light of this disclosure. Relatively high dopant concentrations (e.g., greater than $1\text{E}19$, $1\text{E}20$, or $1\text{E}21$) may be considered degenerate doping, where the semiconductor material starts to act more like a conductor (or actually does exhibit electrical properties similar to a conductor), as is known in the art. Conventional dopants for group IV semiconductor material (e.g., Si, SiGe, Ge) includes phosphorous (P) and/or arsenic (As) for n-type dopant (donors) and boron (B) for p-type dopant (acceptors), to provide some examples. In addition, conventional dopants for group III-V semiconductor material (e.g., GaAs, InGaAs, InAs) includes Si for n-type dopant (donors) and beryllium (Be) and carbon (C) for p-type dopant, to provide some examples.

In some embodiments, final S/D material (e.g., final S/D material 261 and/or 262) may include relatively more doping than sacrificial S/D material (e.g., sacrificial S/D material 260), such as including relatively greater doping concentrations of at least $1\text{E}16$, $5\text{E}16$, $1\text{E}17$, $5\text{E}17$, or $1\text{E}18$ atoms per cubic cm, or any other suitable threshold value as will be apparent in light of this disclosure. As can be understood based on this disclosure, including relatively lower dopant concentrations in the sacrificial S/D material (such as having the sacrificial S/D material be intrinsic/undoped) and performing the techniques described herein (e.g., through-contact S/D processing) allows for the end transistor device to include final S/D material including a desired dopant concentration while also preventing dopant from the at least one of the S/D regions from undesirably diffusing into the adjacent channel region (which would shorten the effective channel length between the corresponding S/D regions). Thus, the techniques are particularly beneficial when transistor devices are scaled down to include gate lengths of less than 50, 45, 40, 35, 30, 25, 20, 15, or 10 nm, or some other suitable threshold length as will be apparent in light of this disclosure.

Recall that the techniques described herein may be used for various different transistor types. For example, where S/D regions on either side of a corresponding channel region are to be used for a MOSFET device, the S/D regions may each include the same type of dopant in a source-channel-drain doping scheme of either p-n-p or p-i-p (e.g., for p-MOS), or n-p-n or n-i-n (e.g., for n-MOS),
5 for example, where 'p' represents being p-type doped, 'n' represented being n-type doped, and 'i' represented being intrinsic/undoped (or nominally undoped). For instance, the right-most structure in Figure 2J that includes S/D regions 262 may be one of an n-MOS and p-MOS device and the left-most structure in Figure 2J that includes S/D regions 261 may be the other of an n-MOS and p-MOS device, to provide an example. To provide another example, for TFET devices, the source-channel-
10 drain doping scheme may be either p-i-n or n-i-p (e.g., the second left-most structure in Figure 2J that includes S/D region 261 and S/D region 262 may be a TFET device). Thus, the techniques described herein can be used to form S/D regions of a given transistor device with various different doping and material schemes, where one or both of the S/D regions is processed with the final material after a replacement gate process has been performed in a gate last process flow.

15 In some embodiments, one or both S/D regions of a given transistor formed using the techniques described herein may include a multilayer structure of two or more material layers, for example. In some embodiments, one or both S/D regions of a given transistor formed using the techniques described herein may include grading (e.g., increasing and/or decreasing) the content/concentration of one or more materials in at least a portion of the region(s), where the
20 material graded may relate to the concentration of included semiconductor material (e.g., the concentration of Ge throughout a SiGe S/D region) and/or included dopant, for example. Thus, in accordance with some embodiments, a multitude of transistor types, and thus, S/D configurations and doping schemes, may be employed, as can be understood based on this disclosure. Further, the configurations and/or properties (e.g., included semiconductor material, doping, bandgap properties,
25 relative location, and so forth) of at least two layers/regions/features of the IC structures described herein may be defined in any suitable relative manner, as will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with forming 120 S/D contacts to form the example resulting structure of Figure 2J, in accordance with an embodiment. In some embodiments, S/D contacts 292 may be formed using any suitable techniques, such as depositing metal or metal alloy
30 (or other suitable electrically conductive material) in the contact trenches 290. Note that for S/D contacts formed over the S/D regions including final S/D material 261, contact trenches were first

formed prior to forming the S/D contacts 292 shown. In some embodiments, S/D contact 292 formation may include silicidation, germinidation, III-V-ization (e.g., intermetallic relatively high conductivity compound via metal and III-V material reaction), and/or annealing processes, for example. In some embodiments, S/D contacts 292 may include aluminum or tungsten, although any
5 suitable conductive metal or alloy can be used, such as silver, nickel-platinum, or nickel-aluminum, for example. In some embodiments, one or more of the S/D contacts 292 may include a resistance reducing metal and a contact plug metal, or just a contact plug, for instance. Example contact resistance reducing metals include, for instance, nickel, aluminum, titanium, gold, gold-germanium, nickel-platinum, or nickel aluminum, and/or other such resistance reducing metals or alloys.
10 Example contact plug metals include, for instance, aluminum, copper, nickel, platinum, titanium, or tungsten, or alloys thereof, although any suitably conductive contact metal or alloy may be used. In some embodiments, additional layers may be present in the S/D contact 292 regions, such as adhesion layers (e.g., titanium nitride) and/or liner or barrier layers (e.g., tantalum nitride), if so desired. As can be seen in Figures 2J and 3, at least a portion of the S/D regions 262 that were
15 processed through the contact trenches 290 is in those corresponding contact trenches 290, in this example embodiment.

Method 100 of Figure 1 continues with completing 122 integrated circuit (IC) processing, as desired, in accordance with some embodiments. Such additional processing to complete the IC may include back-end or back-end-of-line (BEOL) processing to form one or more metallization layers
20 and/or to interconnect the transistor devices formed, for example. Any other suitable processing may be performed, as will be apparent in light of this disclosure. Note that the processes 102-122 of method 100 are shown in a particular order in Figure 1 for ease of description. However, one or more of the processes 102-122 may be performed in a different order or may not be performed at all. Further, additional processes may be performed in addition to or instead of processes 102-122 in
25 variations of method 100, in accordance with some embodiments. Numerous variations on method 100 and the techniques described herein will be apparent in light of this disclosure.

Figure 3 illustrates an example cross-sectional view taken along plane A-A of the IC structure of Figure 2J, in accordance with some embodiments of the present disclosure. Figure 3 is provided to assist in illustrating different components of the structure of Figure 2J. Therefore, the previous
30 relevant description with respect to each similarly numbered feature is equally applicable to Figure 3. However, note that the dimensions of the features shown in Figures 2J and 3 may differ, for ease

of illustration. Also note that some variations occur between the structures, such as the shape of spacers 250, for example, as is shown in Figure 3. Further note that the portion of the structure where S/D contact trenches 290 were formed is indicated in Figure 3, and as can be understood based on the structure, both of the S/D regions 262 extend into the contact trenches 290 in which S/D contacts 292 were formed. In addition, sacrificial S/D material 260 remains adjacent to both of the S/D regions 262, as shown. As can be understood based on this disclosure, by using the techniques described herein (e.g., delaying formation of the highly-doped final S/D material until after gate replacement processing, such that dopant diffusion from one or both S/D regions into the adjacent channel region is reduced or eliminated), very sharp dopant profiles will be present in the end device, in accordance with some embodiments. For example, in some embodiments, the dopant profile at the source-channel and/or drain-channel interfaces will be very distinct, as dopant from the source and/or drain regions does not diffuse into the adjacent channel region.

In some embodiments, the length of gate 284 (e.g., the dimension between spacers 250 in the Z-axis direction), which is indicated as L_g , may be any suitable length as will be apparent in light of this disclosure. For instance, in some embodiments, the gate length may be in the range of 3-100 nm (e.g., 3-10, 3-20, 3-30, 3-50, 5-10, 5-20, 5-30, 5-50, 5-100, 10-20, 10-30, 10-50, 10-100, 20-30, 20-50, 20-100, or 50-100 nm), or any other suitable value or range as will be apparent in light of this disclosure. In some embodiments, the gate length may be less than a given threshold, such as less than 100, 50, 45, 40, 35, 30, 25, 20, 15, 10, 8, or 5 nm, or less than some other suitable threshold as will be apparent in light of this disclosure. In some embodiments, the techniques enable maintaining a desired device performance when scaling to such low thresholds, such as sub-50, sub-40, sub-30, or sub-20 nm thresholds, as can be understood based on this disclosure. Further, in some embodiments, the techniques described herein allow the gate length and the effective channel length (dimension between the S/D regions in the Z-axis direction) to be the same or approximately the same, due to the lack of dopant diffusion from the adjacent S/D regions that would have occurred if the techniques described herein were not used (thereby causing undesired short channel effects). Thus, the gate length may approximate the effective channel length, and the techniques described herein can prevent that effective channel length from undesirably shortening due to undesirable S/D dopant diffusion that would otherwise occur during gate last transistor processing (if the techniques described herein are not employed). Numerous variations and configurations will be apparent in light of the present disclosure.

Example System

Figure 4 illustrates a computing system 1000 implemented with integrated circuit structures and/or transistor devices formed using the techniques disclosed herein, in accordance with some embodiments of the present disclosure. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including, but not limited to, a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 1000, etc.

Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The

computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

5 The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from
10 registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also may include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices
15 formed using the disclosed techniques as variously described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication
20 chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing system 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment
25 control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device or system that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. Note that reference to a computing system is intended to include computing devices, apparatuses, and other structures configured for computing or processing information.

Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is an integrated circuit (IC) including: a substrate; and a transistor at least one of
5 above and in the substrate, the transistor including a gate, a channel region below the gate, source and drain (S/D) regions adjacent the channel region, and a contact above one of the S/D regions, wherein the contact is in a trench and wherein material of the one of the S/D regions extends into the trench.

Example 2 includes the subject matter of Example 1, wherein semiconductor material distinct
10 from the substrate is directly adjacent to the one of the S/D regions on a side opposite the channel region, wherein the semiconductor material is undoped or nominally doped with a dopant concentration of less than $1E16$ atoms per cubic centimeter (cm).

Example 3 includes the subject matter of Example 2, wherein the semiconductor material includes silicon germanium (SiGe).

Example 4 includes the subject matter of Example 3, wherein the channel region includes
15 silicon (Si).

Example 5 includes the subject matter of Example 3, wherein the channel region includes germanium (Ge).

Example 6 includes the subject matter of Example 2, wherein the semiconductor material
20 includes indium phosphide (InP).

Example 7 includes the subject matter of Example 6, wherein the channel region includes at least one of gallium arsenide (GaAs) and indium gallium arsenide (InGaAs).

Example 8 includes the subject matter of any of Examples 1-7, wherein the gate includes a length between two adjacent spacers of less than 30 nanometers (nm).

Example 9 includes the subject matter of any of Examples 1-8, further including a contact
25 above both of the S/D regions, wherein each contact is in a corresponding trench and wherein material of the S/D regions extends into the corresponding trench.

Example 10 includes the subject matter of any of Examples 1-9, wherein the S/D regions each include one of n-type and p-type dopant.

Example 11 includes the subject matter of any of Examples 1-9, wherein one of the S/D regions includes n-type dopant and the other of the S/D regions includes p-type dopant.

Example 12 includes the subject matter of any of Examples 1-11, wherein the transistor is one of an n-channel and p-channel device.

5 Example 13 includes the subject matter of any of Examples 1-12, wherein the transistor includes a configuration that is at least one of a planar, finned, double-gate, tri-gate, finned field-effect transistor (FinFET), nanowire, nanoribbon, and gate-all-around (GAA) configuration.

10 Example 14 includes the subject matter of any of Examples 1-13, wherein the transistor is at least one of a metal-oxide-semiconductor field-effect transistor (MOSFET) and a tunnel FET (TFET) device.

Example 15 includes the subject matter of any of Examples 1-14, wherein the transistor is a p-channel metal-oxide-semiconductor field-effect transistor (p-MOS) device.

15 Example 16 includes the subject matter of any of Examples 1-15, further including a complementary metal-oxide-semiconductor (CMOS) device at least one of above and in the substrate, wherein the CMOS device includes the transistor.

Example 17 is a computing system including the subject matter of any of Examples 1-16.

20 Example 18 is an integrated circuit (IC) including: a substrate; a transistor at least one of above and in the substrate, the transistor including a gate including at least one metal material, a channel region below the gate, and source and drain (S/D) regions adjacent the channel region; and semiconductor material distinct from the substrate and adjacent one of the S/D regions on a side opposite the channel region, wherein the semiconductor material is undoped or nominally doped with a dopant concentration of less than $1E16$ atoms per cubic centimeter (cm).

25 Example 19 includes the subject matter of Example 18, further including a contact above the one of the S/D regions, wherein the contact is in a trench and wherein material of the one of the S/D regions extends into the trench.

Example 20 includes the subject matter of Example 18 or 19, wherein the semiconductor material includes silicon germanium (SiGe).

Example 21 includes the subject matter of Example 20, wherein the channel region includes silicon (Si).

Example 22 includes the subject matter of Example 20, wherein the channel region includes germanium (Ge).

Example 23 includes the subject matter of Example 18 or 19, wherein the semiconductor material includes indium phosphide (InP).

5 Example 24 includes the subject matter of Example 23, wherein the channel region includes at least one of gallium arsenide (GaAs) and indium gallium arsenide (InGaAs).

Example 25 includes the subject matter of any of Examples 18-24, wherein the gate includes a length between two adjacent spacers of less than 30 nanometers (nm).

10 Example 26 includes the subject matter of any of Examples 18-25, further including a contact above both of the S/D regions, wherein each contact is in a corresponding trench and wherein material of the S/D regions extends into the corresponding trench.

Example 27 includes the subject matter of any of Examples 18-26, wherein the S/D regions each include one of n-type and p-type dopant.

15 Example 28 includes the subject matter of any of Examples 18-26, wherein one of the S/D regions includes n-type dopant and the other of the S/D regions includes p-type dopant.

Example 29 includes the subject matter of any of Examples 18-28, wherein the transistor is one of an n-channel and p-channel device.

20 Example 30 includes the subject matter of any of Examples 18-29, wherein the transistor includes a configuration that is at least one of a planar, finned, double-gate, tri-gate, finned field-effect transistor (FinFET), nanowire, nanoribbon, and gate-all-around (GAA) configuration.

Example 31 includes the subject matter of any of Examples 18-30, wherein the transistor is at least one of a metal-oxide-semiconductor field-effect transistor (MOSFET) and a tunnel FET (TFET) device.

25 Example 32 includes the subject matter of any of Examples 18-31, wherein the transistor is a p-channel metal-oxide-semiconductor field-effect transistor (p-MOS) device.

Example 33 includes the subject matter of any of Examples 18-32, further including a complementary metal-oxide-semiconductor (CMOS) device at least one of above and in the substrate, wherein the CMOS device includes the transistor.

Example 34 is a computing system including the subject matter of any of Examples 18-33.

Example 35 is a method of forming an integrated circuit (IC), the method including: removing at least a portion of sacrificial semiconductor material through a trench in an insulator layer, the sacrificial semiconductor material in one of a source region and a drain region of a transistor, the transistor at least one of above and in a substrate, and the sacrificial semiconductor material being
5 distinct from the substrate; and replacing the removed sacrificial material with doped semiconductor material.

Example 36 includes the subject matter of Example 35, wherein the substrate is a silicon (Si) substrate.

Example 37 includes the subject matter of Example 36, wherein the doped semiconductor
10 material includes a dopant concentration that is at least $1E17$ atoms per cubic centimeter (cm) greater than a dopant concentration included in the sacrificial semiconductor material.

Example 38 includes the subject matter of any of Examples 35-37, wherein at least a portion of the sacrificial semiconductor material remains adjacent to the doped semiconductor material on a side opposite a channel region of the transistor.

Example 39 includes the subject matter of any of Examples 35-38, further including forming
15 the sacrificial semiconductor material prior to performing replacement gate processing.

Example 40 includes the subject matter of any of Examples 35-39, wherein replacing the removed sacrificial semiconductor material with doped semiconductor material includes processing that does not exceed a temperature of 600 degrees Celsius.

Example 41 includes the subject matter of any of Examples 35-40, wherein the doped
20 semiconductor material includes p-type dopant.

Example 42 includes the subject matter of any of Examples 35-40, wherein the doped semiconductor material includes n-type dopant.

The foregoing description of example embodiments has been presented for the purposes of
25 illustration and description. It is not intended to be exhaustive or to limit the present disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the present disclosure be limited not by this detailed description, but rather by the claims appended hereto. Future filed applications claiming priority to this application may claim the disclosed subject matter in a different manner, and may generally
30 include any set of one or more limitations as variously disclosed or otherwise demonstrated herein.

CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:
a substrate; and
5 a transistor at least one of above and in the substrate, the transistor including
a gate,
a channel region below the gate,
source and drain (S/D) regions adjacent the channel region, and
a contact above one of the S/D regions, wherein the contact is in a trench and wherein
10 material of the one of the S/D regions extends into the trench.
2. The IC of claim 1, wherein semiconductor material distinct from the substrate is
directly adjacent to the one of the S/D regions on a side opposite the channel region, wherein the
semiconductor material is undoped or nominally doped with a dopant concentration of less than
1E16 atoms per cubic centimeter (cm).
- 15 3. The IC of claim 2, wherein the semiconductor material includes silicon germanium
(SiGe).
4. The IC of claim 3, wherein the channel region includes silicon (Si).
5. The IC of claim 3, wherein the channel region includes germanium (Ge).
6. The IC of claim 2, wherein the semiconductor material includes indium phosphide
20 (InP).
7. The IC of claim 6, wherein the channel region includes at least one of gallium
arsenide (GaAs) and indium gallium arsenide (InGaAs).
8. The IC of claim 1, wherein the gate includes a length between two adjacent spacers
of less than 30 nanometers (nm).

9. The IC of claim 1, further comprising a contact above both of the S/D regions, wherein each contact is in a corresponding trench and wherein material of the S/D regions extends into the corresponding trench.

10. The IC of claim 1, wherein the S/D regions each include one of n-type and p-type dopant.

11. The IC of claim 1, wherein one of the S/D regions includes n-type dopant and the other of the S/D regions includes p-type dopant.

12. The IC of claim 1, wherein the transistor is one of an n-channel and p-channel device.

13. The IC of claim 1, wherein the transistor includes a configuration that is at least one of a planar, finned, double-gate, tri-gate, finned field-effect transistor (FinFET), nanowire, nanoribbon, and gate-all-around (GAA) configuration.

14. The IC of claim 1, wherein the transistor is at least one of a metal-oxide-semiconductor field-effect transistor (MOSFET) and a tunnel FET (TFET) device.

15. The IC of claim 1, wherein the transistor is a p-channel metal-oxide-semiconductor field-effect transistor (p-MOS) device.

16. The IC of claim 1, further comprising a complementary metal-oxide-semiconductor (CMOS) device at least one of above and in the substrate, wherein the CMOS device includes the transistor.

17. A computing system comprising the IC of any of claims 1-16.

20 18. An integrated circuit (IC) comprising:
a substrate;
a transistor at least one of above and in the substrate, the transistor including
a gate including at least one metal material,
a channel region below the gate, and
25 source and drain (S/D) regions adjacent the channel region; and

semiconductor material distinct from the substrate and adjacent one of the S/D regions on a side opposite the channel region, wherein the semiconductor material is undoped or nominally doped with a dopant concentration of less than 1×10^{16} atoms per cubic centimeter (cm).

5 19. The IC of claim 18, further comprising a contact above the one of the S/D regions, wherein the contact is in a trench and wherein material of the one of the S/D regions extends into the trench.

 20. The IC of claim 18, further comprising a contact above both of the S/D regions, wherein each contact is in a corresponding trench and wherein material of the S/D regions extends
10 into the corresponding trench.

 21. The IC of claim 18, wherein the gate includes a length between two adjacent spacers of less than 30 nanometers (nm).

 22. The IC of any of claims 18-21, wherein the transistor is a p-channel metal-oxide-semiconductor field-effect transistor (p-MOS) device.

15 23. A method of forming an integrated circuit (IC), the method comprising:
removing at least a portion of sacrificial semiconductor material through a trench in an insulator layer, the sacrificial semiconductor material in one of a source region and a drain region of a transistor, the transistor at least one of above and in a substrate, and the sacrificial semiconductor material being distinct from the substrate; and
20 replacing the removed sacrificial material with doped semiconductor material.

 24. The method of claim 23, further comprising forming the sacrificial semiconductor material prior to performing replacement gate processing.

 25. The method of claim 23 or 24, wherein replacing the removed sacrificial semiconductor material with doped semiconductor material includes processing that does not exceed
25 a temperature of 600 degrees Celsius.

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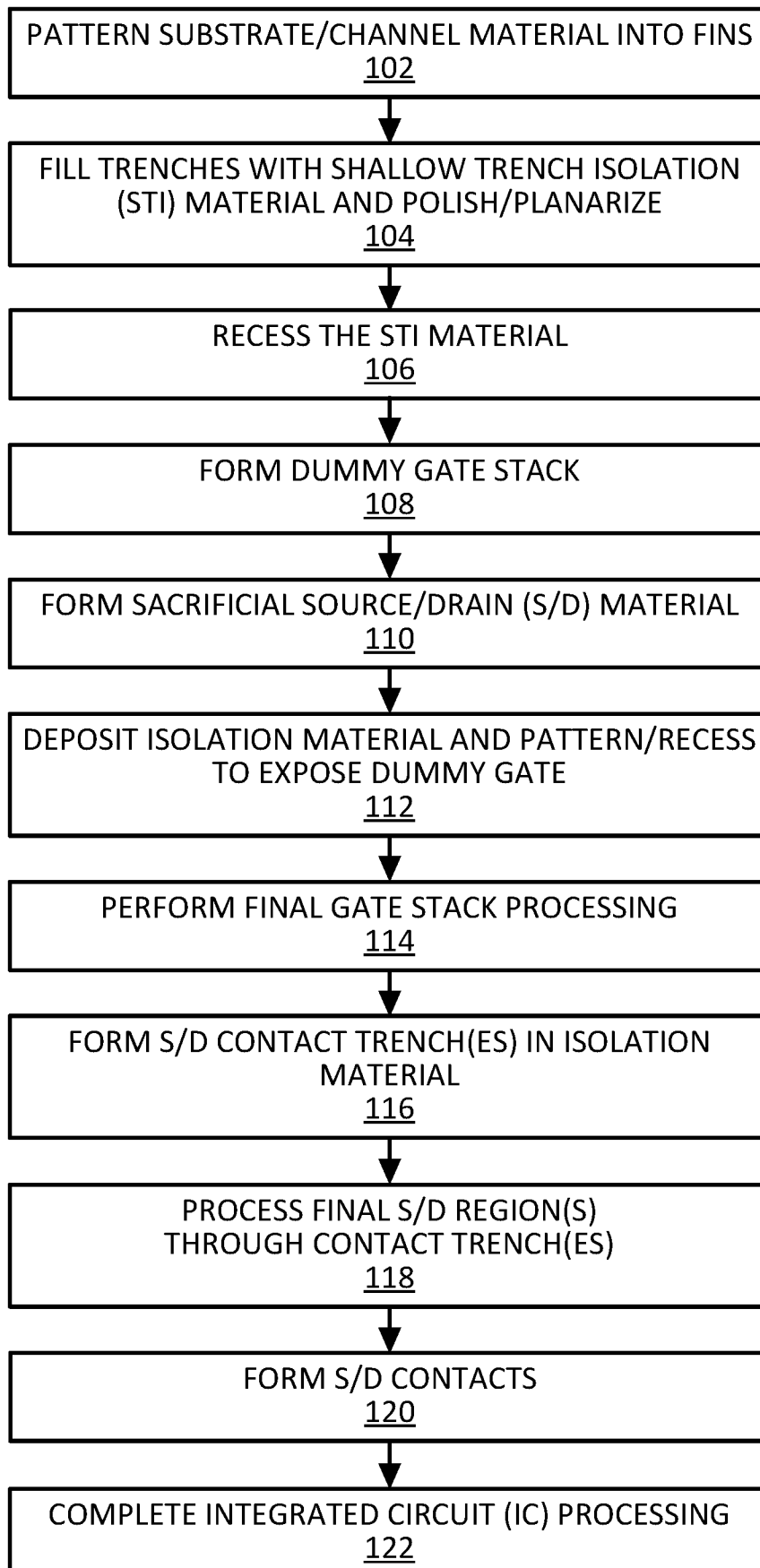
METHOD
100 →

FIG. 1

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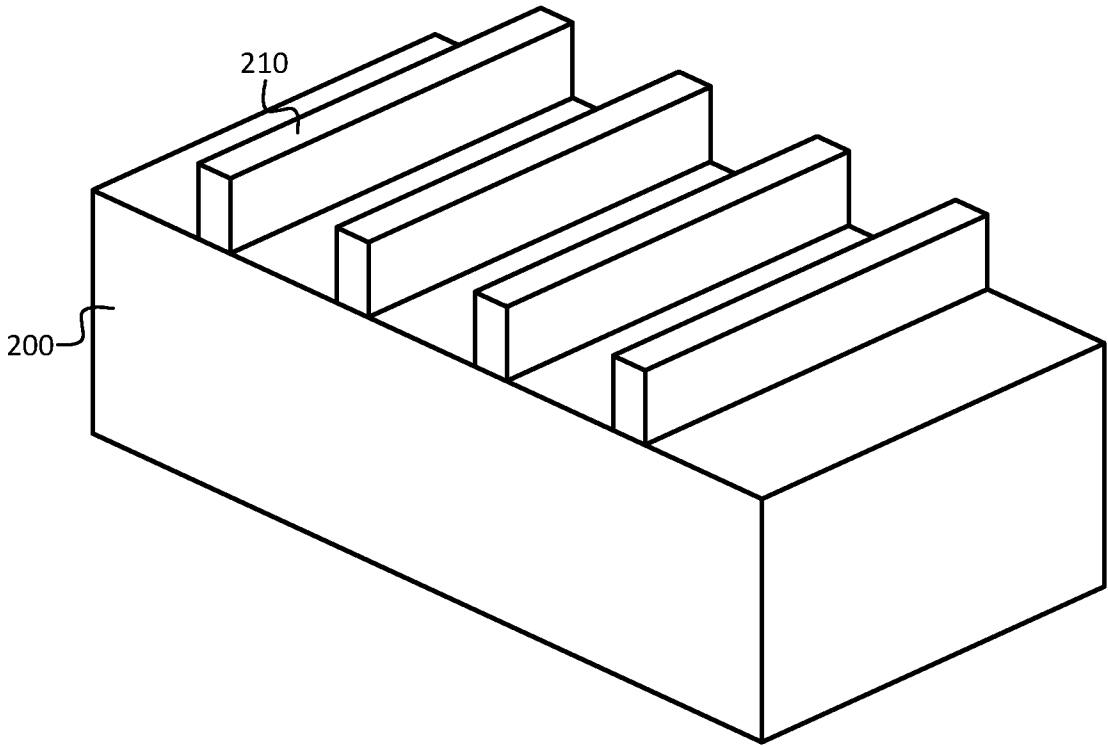


FIG. 2A

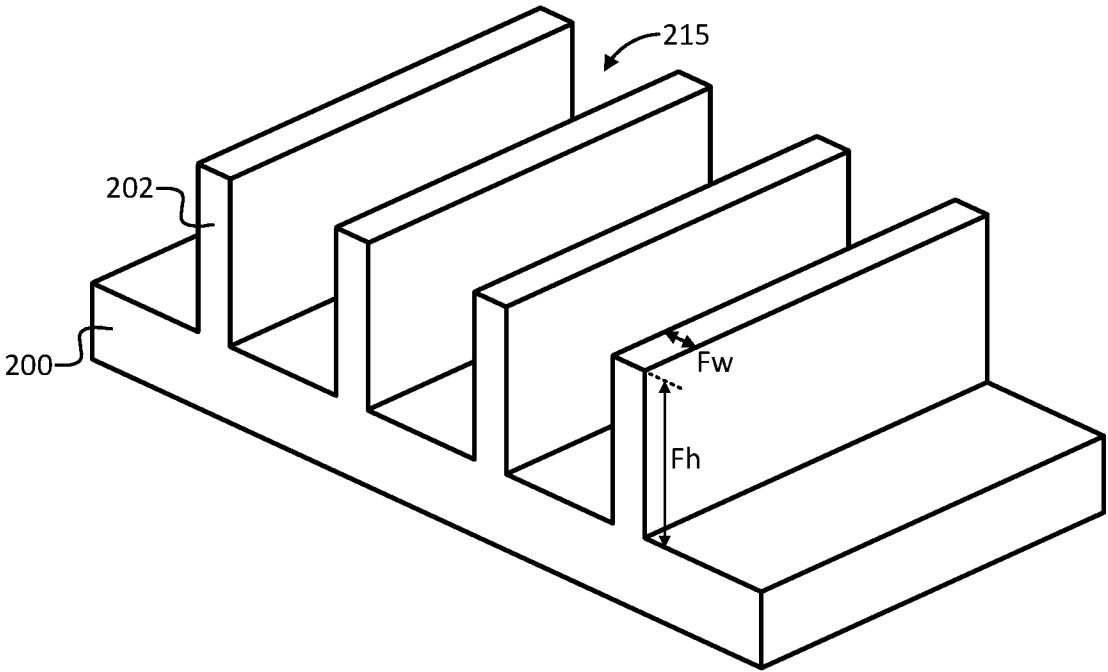
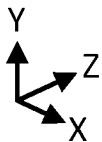


FIG. 2B



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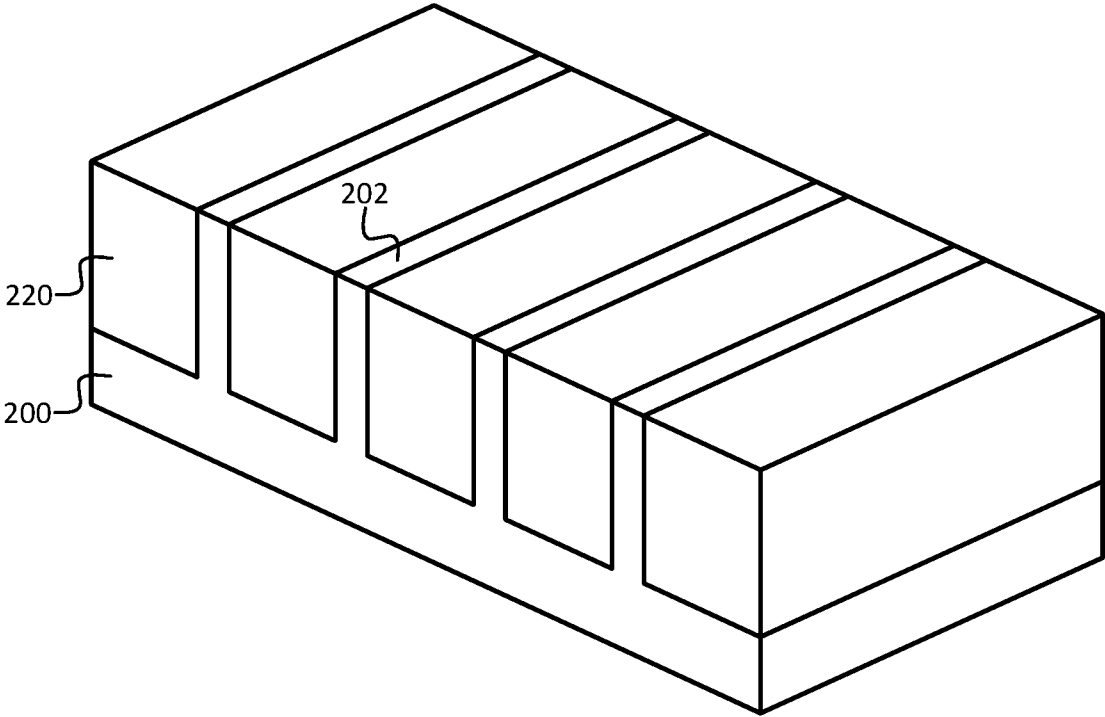


FIG. 2C

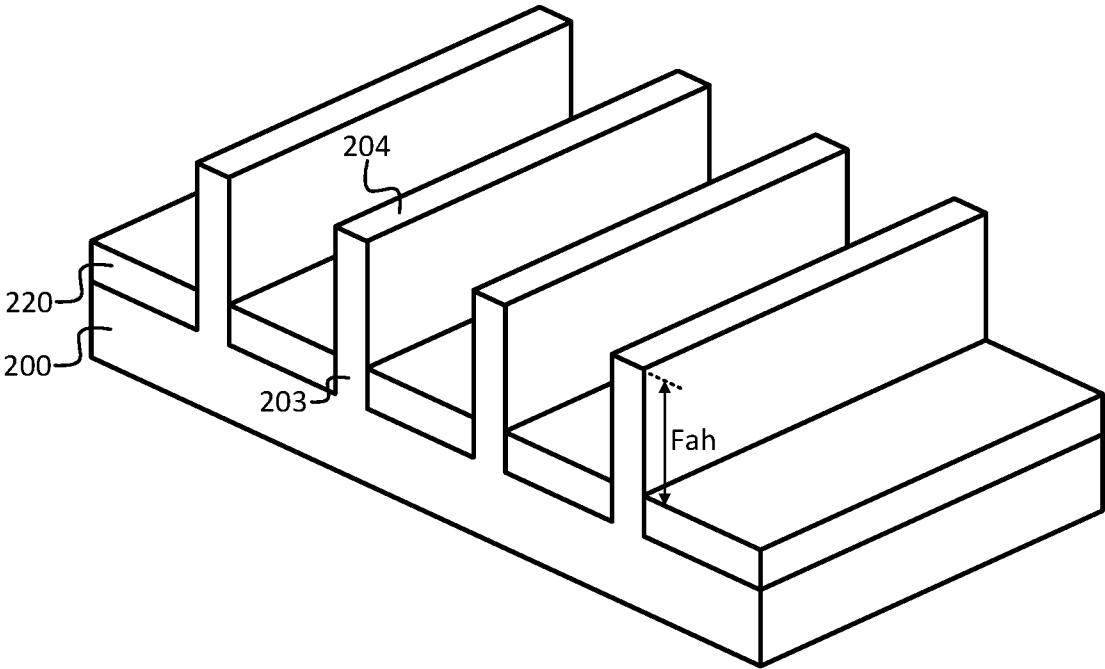


FIG. 2D



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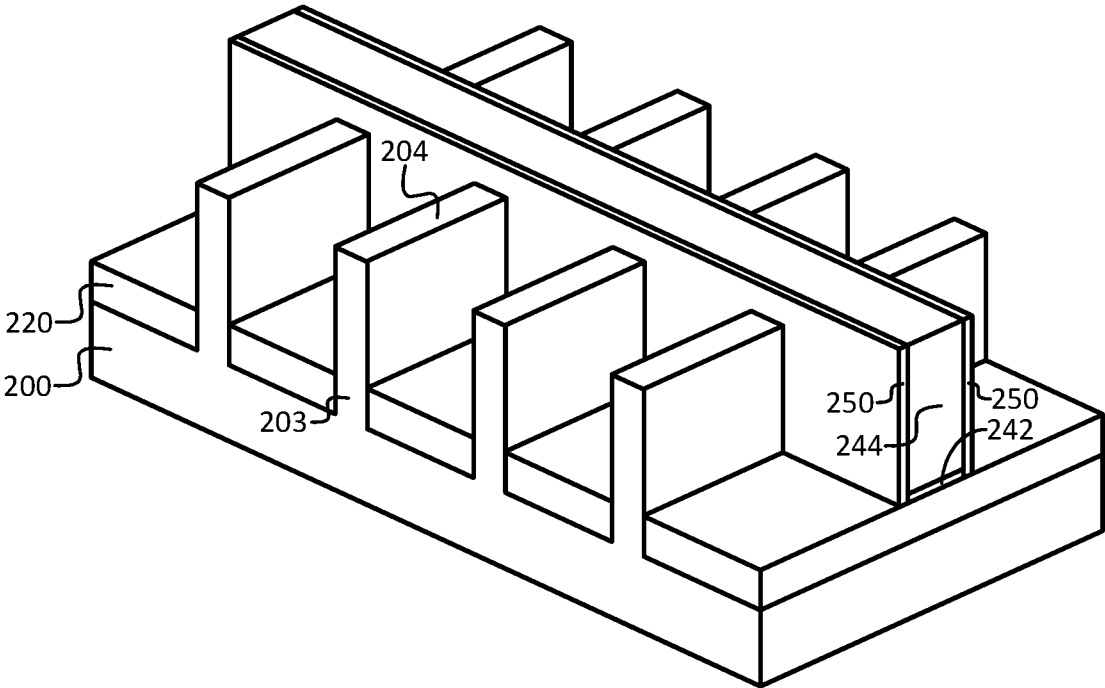


FIG. 2E

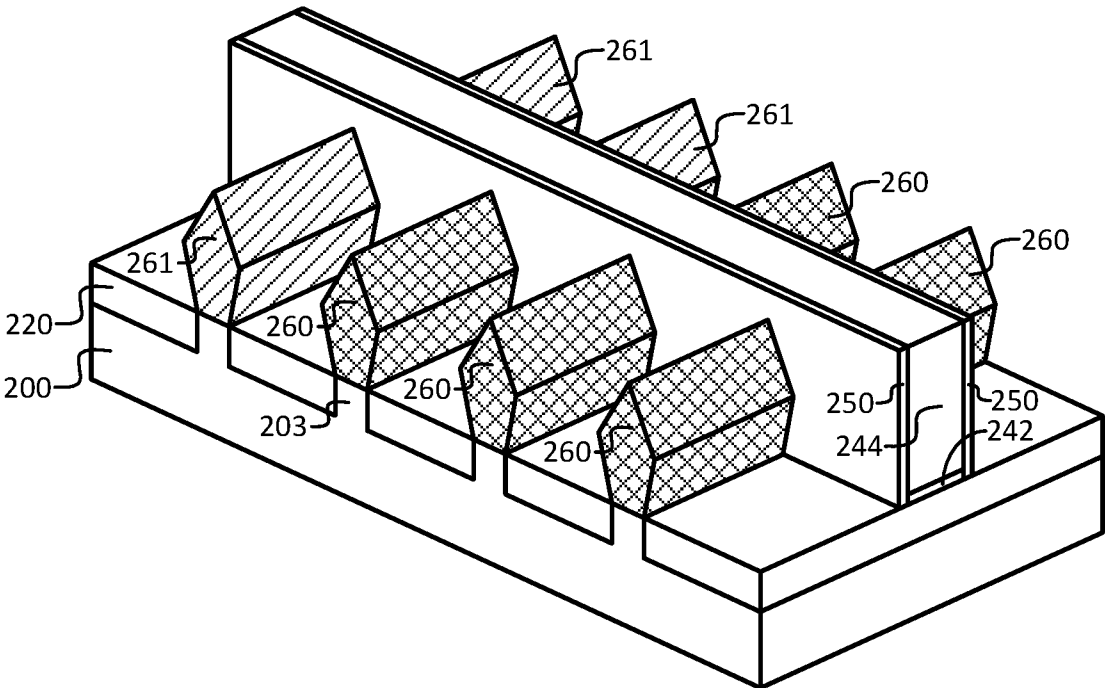


FIG. 2F



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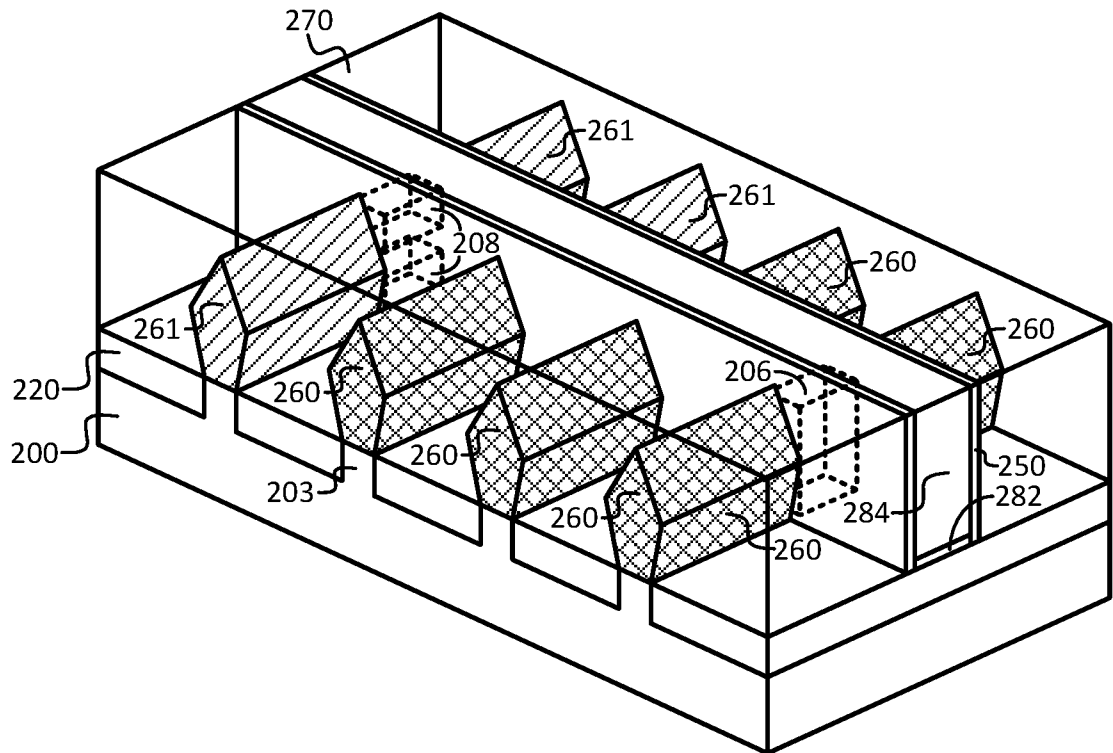


FIG. 2G

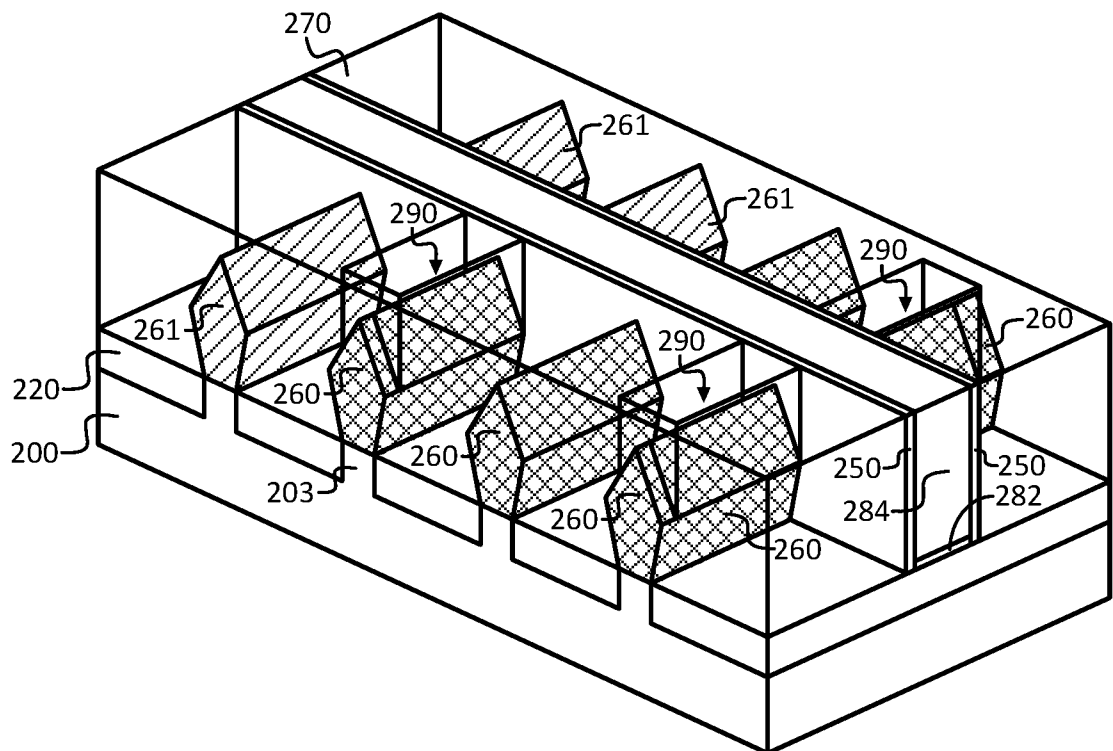
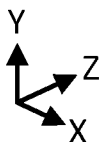


FIG. 2H



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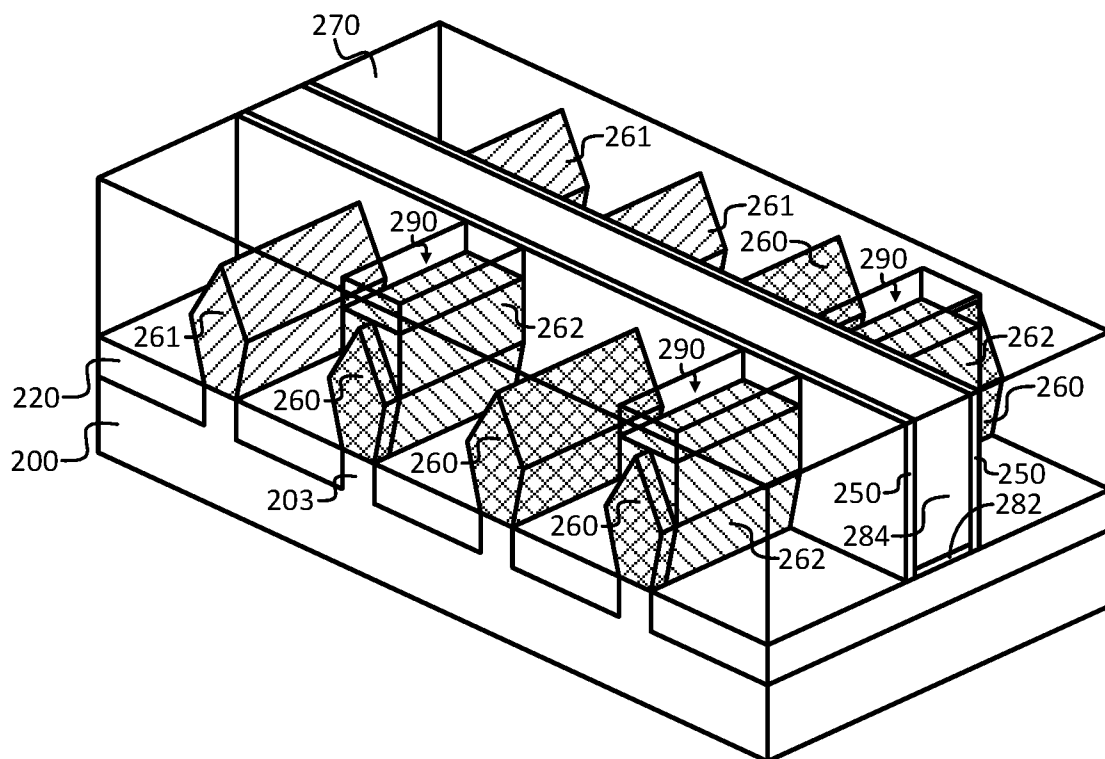


FIG. 2I

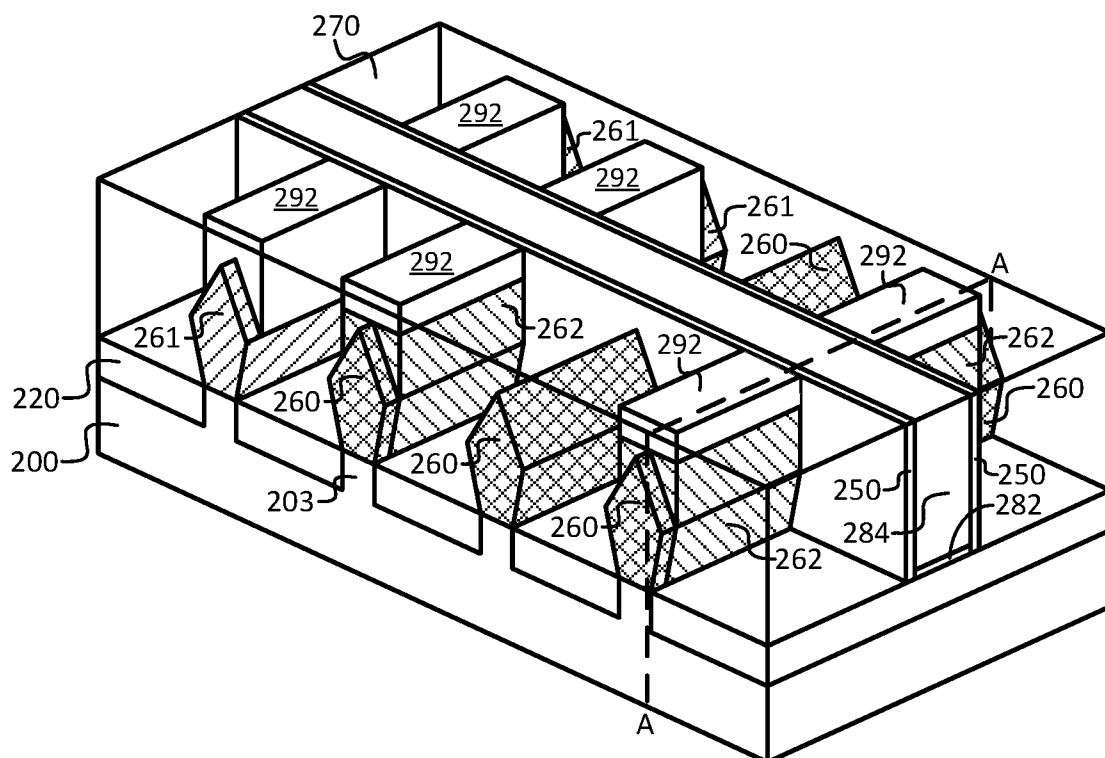
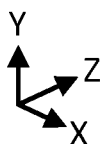


FIG. 2J



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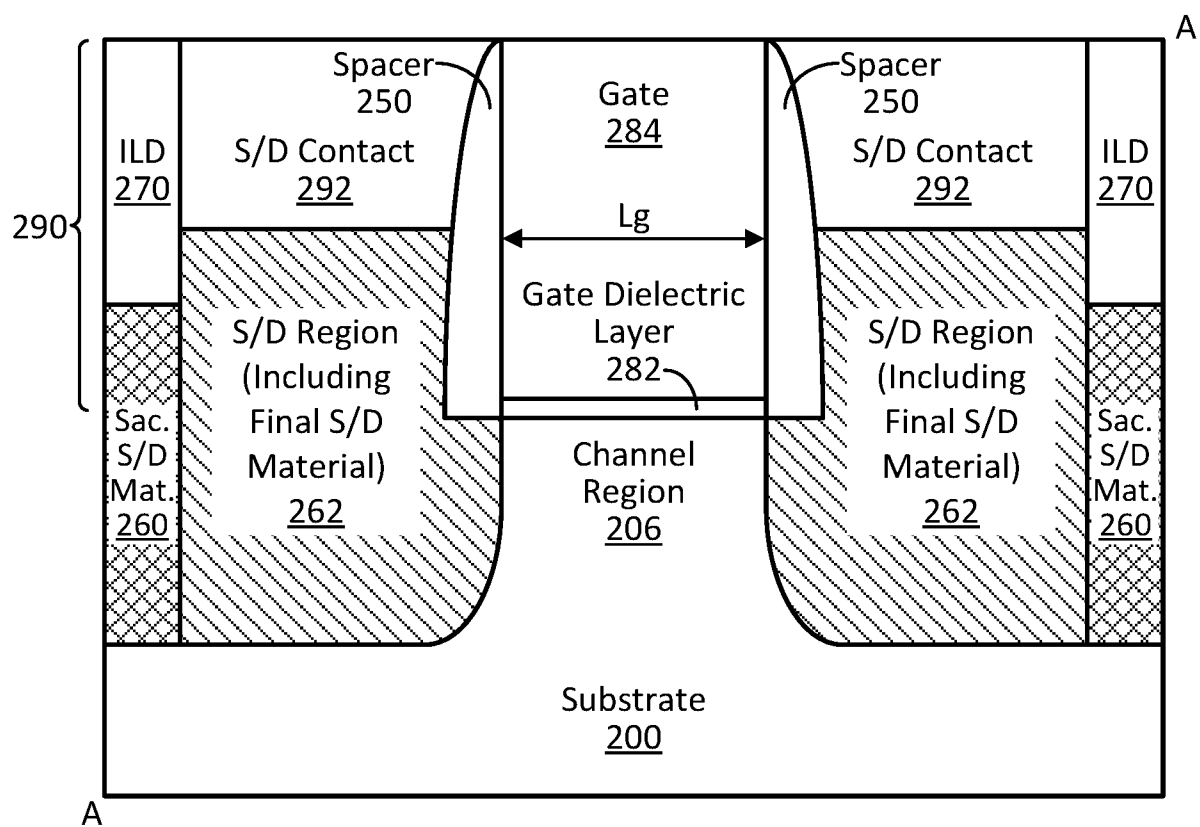
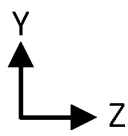


FIG. 3



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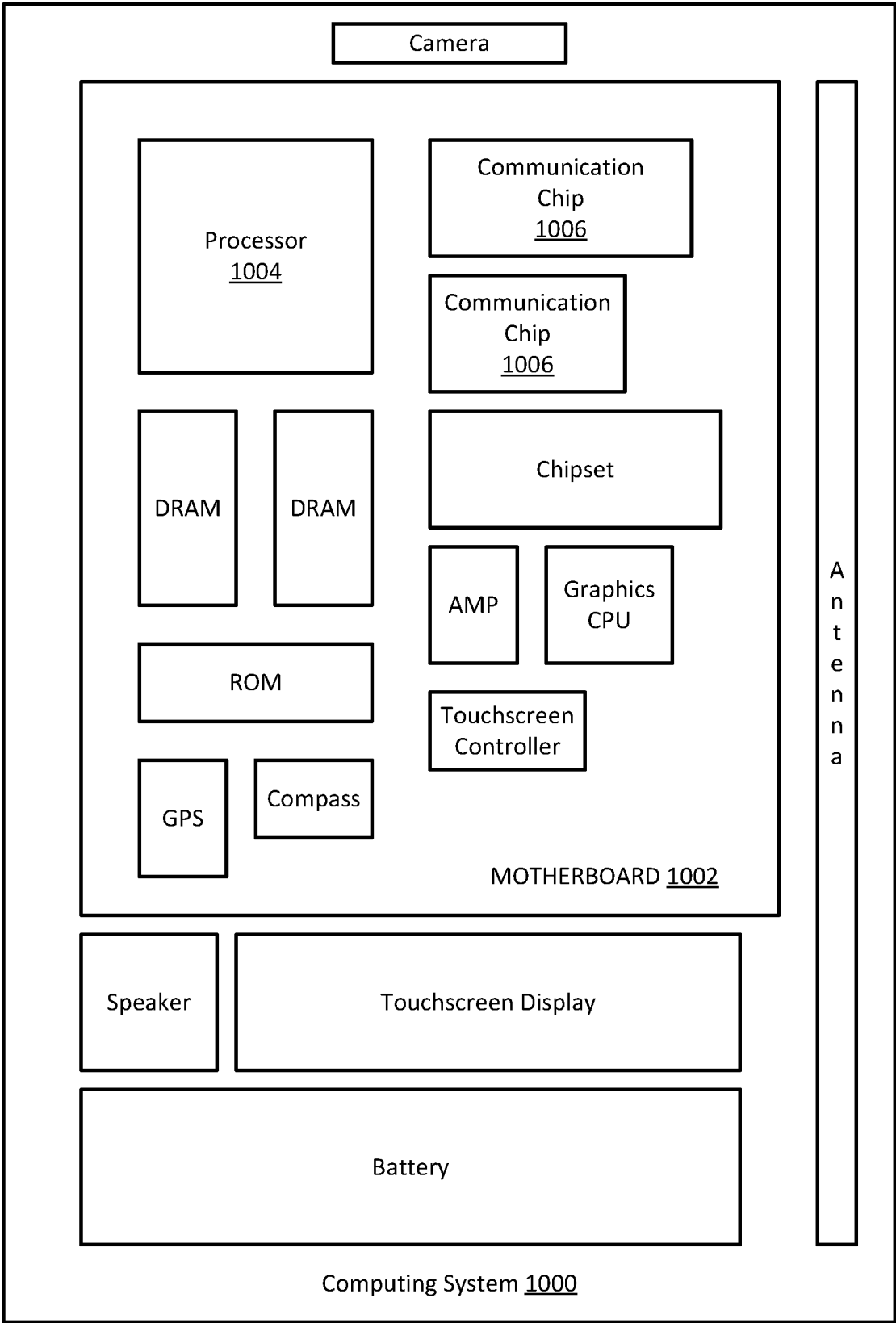


FIG. 4

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A. CLASSIFICATION OF SUBJECT MATTER**H01L 29/78(2006.01)i, H01L 29/66(2006.01)i, H01L 21/8238(2006.01)i, H01L 29/423(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 29/08; H01L 21/306; H01L 21/336; H01L 21/02; H01L 29/66; H01L 29/423; H01L 21/8238

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: IC, source, drain, gate, trench, doped

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2015-0069473 A1 (GLASS et al.) 12 March 2015 See paragraphs [10]-[66], claims 1,2,17 and figure 3E.	1-25
Y	WO 2015-142357 A1 (INTEL CORPORATION) 24 September 2015 See page 9, line 11-page 16, line 16, claims 16-20 and figures 1-4.	1-25
A	US 2015-0279935 A1 (GLOBALFOUNDRIES INC.) 01 October 2015 See paragraph [58], claims 1-11 and figure 3C.	1-25
A	US 2016-0359046 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 08 December 2016 See paragraphs [46],[60] and figures 18,19.	1-25
A	US 2014-0011330 A1 (INSTITUTE OF MICROELECTRONICS, CHINESE ACADEMY OF SCIENCES) 09 January 2014 See paragraph [88] and figure 22B.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

25 August 2017 (25.08.2017)

Date of mailing of the international search report

28 August 2017 (28.08.2017)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/068660

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015-0069473 A1	12/03/2015	US 9633835 B2	25/04/2017
WO 2015-142357 A1	24/09/2015	CN 106062962 A	26/10/2016
		EP 3120388 A1	25/01/2017
		KR 10-2016-0136285 A	29/11/2016
		TW 201543676 A	16/11/2015
		US 2017-0012124 A1	12/01/2017
US 2015-0279935 A1	01/10/2015	CN 104979347 A	14/10/2015
		TW 201541611 A	01/11/2015
		TW I563632 B	21/12/2016
		US 9299781 B2	29/03/2016
US 2016-0359046 A1	08/12/2016	US 2016-0013313 A1	14/01/2016
		US 9472628 B2	18/10/2016
US 2014-0011330 A1	09/01/2014	CN 102034865 A	27/04/2011
		CN 102034865 B	04/07/2012
		US 2011-0193164 A1	11/08/2011
		US 8552477 B2	08/10/2013
		US 8741703 B2	03/06/2014
		WO 2011-038598 A1	07/04/2011