

(43) International Publication Date
26 November 2015 (26.11.2015)

- (51) **International Patent Classification:**
H01L 51/05 (2006.01) *H01L 51/30* (2006.01)
- (21) **International Application Number:**
PCT/GB2015/051478
- (22) **International Filing Date:**
20 May 2015 (20.05.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
1408946.0 20 May 2014 (20.05.2014) GB
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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

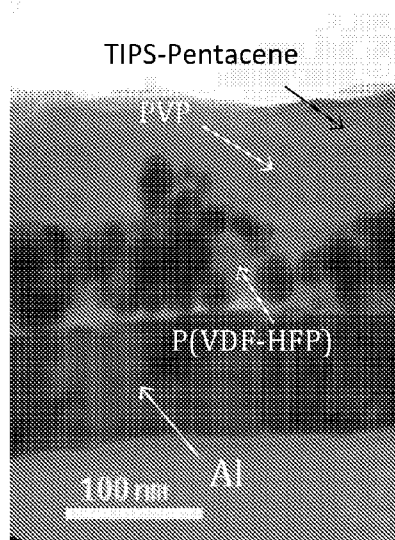
— of inventorship (Rule 4.17(iv))

Published:

— with international search report (Art. 21(3))

(54) **Title:** DIELECTRIC MATERIALS FOR LOW VOLTAGE OFET OPERATION

FIG. 2



(57) **Abstract:** Organic thin film transistors are disclosed, as well as processes for their manufacture and their use in electronic devices. The organic thin film transistors comprise a bilayer gate dielectric formed from a nanocomposite layer and an intermediate capping layer. The organic thin film transistors operate at very low voltages, allowing their incorporation into portable and wearable devices, as well as apparatuses used in water-sensing applications.

DIELECTRIC MATERIALS FOR LOW VOLTAGE OFET OPERATION

INTRODUCTION

[0001] The present invention relates to organic thin film transistors (OTFTs), as well as to their methods of manufacture and their uses.

BACKGROUND OF THE INVENTION

[0002] Over the past 25 years, organic field-effect transistors (OFETs) have undergone outstanding improvements in both performance and reliability with field-effect mobilities (μ) surpassing that of benchmark amorphous silicon-based devices ($0.5\text{--}1\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$).^[1] In particular, organic thin film transistors (OTFTs) have gained substantial interest due to their promising advantages of low-cost, lightweight and large-area processing compatible with flexible, plastic substrates, suitable for applications such as flexible displays,^[2] radio-frequency identification (RFID) tags,^[3] non-volatile memories,^[4] and sensors^[5].

[0003] Nonetheless, the key challenge in ubiquitous practicality of OTFTs, particularly in low-power electronics, portable and wearable electronics and aqueous sensing applications, is their relatively high operating voltage ($>20\text{ V}$) and subsequent high power consumption due to the low carrier mobilities of organic semiconductors. Lowering the operational voltage of OTFTs is achieved by reducing threshold voltage (V_T) and subthreshold swing (SS).^[6] Since both parameters are strongly controlled by the gate dielectric and density of charge traps at dielectric-semiconductor interface, a high-capacitance gate dielectric with superior interface properties, solution-processable at low-temperature and compatible with flexible substrates is the optimal choice for low-voltage OTFTs.^[6,7]

[0004] As given by Equation 1 shown below:

$$C_i = \frac{\epsilon_0 k}{d} \quad (1)$$

where ϵ_0 is vacuum permittivity, high capacitance per unit area (C_i) can be achieved by either decreasing gate dielectric thickness (d) or increasing dielectric constant (k). Most common solution-processable polymers have relatively low dielectric constants ($k \sim 2\text{--}4$),^[8] as a result of which ultrathin layers ($<20\text{ nm}$) are necessary to obtain large capacitance. Nonetheless, thin polymeric dielectric films often suffer from structural heterogeneities, such as pinholes, and thus large leakage currents.^[9]

[0005] A new approach to obtain solution-processable high capacitance dielectric layers with improved electrical and mechanical properties is incorporation of inorganic high-k nanoparticles into a polymer matrix. The so-called nanocomposite dielectric manifests a combination of desirable properties offered by the two constituents; low-temperature, large-area, solution-processability and flexibility of polymer on one hand and high dielectric constant and breakdown strength of nanoparticles on the other hand. Hence, nanocomposites are a promising alternative class of materials to obtain high-capacitance dielectrics essential to realise flexible, low-voltage OTFTs.

[0006] However, higher nanoparticle concentration leads to increased thickness and surface roughness, and hence degraded device performance consequently. In OTFTs, dielectric surface roughness is understood to play a crucial role in the formation of dielectric-semiconductor interface and device overall performance. Charge carriers accumulated at dielectric-semiconductor interface upon gate voltage application only move by drift, horizontally along the surface by modulating drain voltage. The topographic features in a rough nanocomposite surface act as charge traps and transport barriers, necessitating higher gate voltage to modulate channel current and hampering charge carrier mobility.^[10] Steudel *et al.*^[11] reported on a pronounced drop from $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ to $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in mobility of pentacene FETs fabricated on dielectric with increasing root-mean-square (RMS) surface roughness from 0.17 nm to 9.2 nm. They attributed hindered charge mobility to trapping of charges (holes) in the roughness minima unable to move out to the surface by source-drain voltage, but only by diffusion or drift along a local horizontal potential gradient.^[11]

[0007] The drawbacks of nanocomposite dielectrics were reported by Yang *et al.*^[12], who documented that when low-k polymer matrix (e.g. poly(4-vinylphenol) (PVP), $k \sim 3.9$) is used, considerably higher concentrations of higher-k nanoparticles are required to obtain a high-capacitance dielectric, meaning that whilst relatively high-capacitance dielectrics using a low-k nanocomposite could be achieved, corresponding OTFTs were operated at a high range of voltage ($>20 \text{ V}$), with the field effect mobility being adversely affected by the increased surface roughness.

[0008] Dang *et al.*^[13], Almadhoun *et al.*^[14], Kim *et al.*^[15], and Noh *et al.*^[16], have also underlined the difficulties involved in obtained homogeneous and stable nanocomposite dispersions. The high surface energy and surface-to-volume ratio of nanoparticles often gives rise to agglomeration and phase separation from the polymer matrix, particularly at higher loadings, and hence an inhomogeneous mixture with poor processability, increased porosity and defect density. Consequently, percolative pathways are created

through the aggregated nanoparticles, which leads to increased leakage current density, reduced dielectric breakdown strength and dielectric constant.

[0009] There therefore remains a need for OTFT dielectrics exhibiting improved performance characteristics, as well as the ability to be more easily manufactured.

[0010] The present invention was devised with the foregoing in mind.

SUMMARY OF THE INVENTION

[0011] According to a first aspect of the present invention there is provided an organic thin film transistor comprising a semiconductor layer and a gate dielectric layer, and a continuous intermediate layer disposed therebetween, wherein

- a) the gate dielectric layer has a thickness of 50 nm – 1 μ m and comprises 2 – 11 wt.% of nanoparticles dispersed in a polymer matrix, the nanoparticles having an average particle size of 20 – 200 nm and a high dielectric constant, and the polymer matrix having a high dielectric constant; and
- b) the intermediate layer has a thickness of 10 – 55 nm and comprises a polymeric material having a low dielectric constant

[0012] According to a second aspect of the present invention there is provided a process for the preparation of an organic thin film transistor as defined herein, the process comprising the steps of:

- a) providing a gate electrode,
- b) applying the dielectric layer to an exposed surface of the gate electrode,
- c) applying the intermediate layer to the exposed surface of the dielectric layer, and
- d) applying the semiconductor layer to the exposed surface of the intermediate layer.

[0013] According to a third aspect of the present invention there is provided an electronic device comprising an organic thin film transistor as defined herein.

[0014] According to a fourth aspect of the present invention there is provided a use of an organic thin film transistor as defined herein for water sensing applications.

[0015] According to a fifth aspect of the present invention there is provided an organic thin film transistor obtainable, obtained, or directly obtained, by a process defined herein.

DETAILED DESCRIPTION OF THE INVENTION

Organic thin film transistors

[0016] As discussed hereinbefore, the present invention provides an organic thin film transistor comprising a semiconductor layer and a gate dielectric layer, and a continuous intermediate layer disposed therebetween, wherein

- a) the gate dielectric layer has a thickness of 50 nm – 1 μ m and comprises 2 – 11 wt.% of nanoparticles dispersed in a polymer matrix, the nanoparticles having an average particle size of 20 – 200 nm and a high dielectric constant, and the polymer matrix having a high dielectric constant; and
- b) the intermediate layer has a thickness of 10 – 55 nm and comprises a polymeric material having a low dielectric constant.

[0017] The OTFTs of the present invention provide a number of advantages over the prior art. Most significantly, the present OTFTs exhibit strikingly low operational voltage characteristics, whilst at the same time lending themselves to simple, inexpensive manufacturing techniques.

[0018] The gate dielectric layer forming part of the present OTFTs exhibits a high capacitance attributable in part to the combination of high k nanoparticles (i.e. a dielectric constant, when in bulk, of greater than 4) and high k polymer matrix (i.e. a dielectric constant of greater than 4). The use of a high k polymer matrix eliminates the need for high concentrations of high k nanoparticle fillers, thereby advantageously allowing for a comparatively thin dielectric layer having reduced surface roughness that is still able to yield high carrier mobility and low OTFT operating voltages. The use of nanoparticles having an average particle size of less than 500 nm further contributes to affording a comparatively thinner and smoother dielectric layer. Moreover, the nanocomposite material forming the dielectric layer is solution processable as a homogeneous and stable suspension, meaning that a uniform layer can be deposited via solution-based processes (such as spin-coating), without subsequent phase separation.

[0019] The intermediate layer forming part of the present OTFTs simultaneously allows for improved device performance characteristics, whilst at the same time greatly facilitating the manufacturing process. The thin, low k (i.e. a dielectric constant of less than 5), not only contributes to having a smoother dielectric surface, but also advantageously reduces the interfacial energy between the dielectric layer and the semiconductor layer, thereby markedly simplifying the deposition process of the latter. Moreover, the intermediate layer exhibits a high degree of insolubility in those solvents

commonly used for solution deposition of semiconductors, meaning that little to no interfacial mixing is observed at the intermediate layer/semiconductor layer interface. Furthermore, in spite of its thinness, the solution-processable continuous intermediate can be deposited with few or no pinholes, meaning that leakage current between the source/drain and gate contacts is markedly reduced.

[0020] The present OTFTs can be operated at voltages of less than 1 V, which makes them highly suitable for incorporation into portable or wearable electronic devices, or those intended for use in water sensing applications.

[0021] In an embodiment, the organic thin film transistor comprises a semiconductor layer and a gate dielectric layer, and a continuous intermediate layer disposed therebetween, wherein

- a) the gate dielectric layer has a thickness of 50 nm – 1 μ m and comprises 2 – 11 wt.% of nanoparticles dispersed in a polymer matrix, the nanoparticles having an average particle size of 20 – 200 nm and a high dielectric constant, and the polymer matrix having a high dielectric constant; and
- b) the intermediate layer has a thickness of 10 – 40 nm and comprises a polymeric material having a low dielectric constant.

[0022] In another embodiment, the gate dielectric layer has a thickness of 50 – 300 nm. Suitably, the gate dielectric layer has a thickness of 100 – 200 nm. Thinner dielectrics are desirable since they result in greater capacitance according to Equation 1.

[0023] In another embodiment, the gate dielectric layer comprises 3 – 8 wt.% of nanoparticles dispersed in a polymer matrix. Suitably, the gate dielectric layer comprises 4 – 7 wt.% of nanoparticles dispersed in a polymer matrix. More suitably, the gate dielectric layer comprises 5 wt.% of nanoparticles dispersed in a polymer matrix. A relatively low concentration of nanoparticles allows for a thinner, more homogenous dielectric layer.

[0024] In another embodiment, the gate dielectric layer comprises nanoparticles dispersed in a polymer matrix in a volume ratio of 1:1 – 8:1. Suitably, the gate dielectric layer comprises nanoparticles dispersed in a polymer matrix in a volume ratio of 2:1 – 4:1. More suitably, the gate dielectric layer comprises nanoparticles dispersed in a polymer matrix in a volume ratio of 3:1.

[0025] In another embodiment, the dielectric layer comprises only one type of nanoparticles. In another embodiment, the dielectric layer comprises a mixture of two or more different types of nanoparticles.

[0026] In another embodiment, the dielectric layer comprises a surfactant, so as to limit any nanoparticle agglomeration, if present.

[0027] In another embodiment, the nanoparticles, when in bulk, have a dielectric constant of greater than 10. Suitably, the nanoparticles, when in bulk, have a dielectric constant of greater than 15. The high dielectric constant nanoparticles forming part of the present invention afford a highly capacitive dielectric layer without causing significant surface roughening.

[0028] In another embodiment, the nanoparticles are formed from inorganic material. Suitably, the nanoparticles are formed from one or more ABO_3 -type perovskites. More suitably, the nanoparticles are formed from one or more ABO_3 -type perovskites selected from the group consisting of barium strontium titanate, barium zirconate, calcium titanate, calcium zirconate, and barium titanate. More suitably, the nanoparticles are formed from barium strontium titanate, barium zirconate or a mixture thereof. Most suitably, the nanoparticles are formed from barium strontium titanate.

[0029] In another embodiment, the nanoparticles have an average particle size of 20 – 100 nm. Suitably, the nanoparticles have an average particle size of 20 – 50 nm.

[0030] In another embodiment, the polymer matrix has a dielectric constant of greater than 5. Suitably, the polymer matrix has a dielectric constant of greater than 7. More suitably, the polymer matrix has a dielectric constant of greater than 9.

[0031] In another embodiment, the polymer matrix is formed from one or more homopolymers or copolymers. Optionally, the one or more homopolymers or copolymers is cross-linked. In one embodiment, the polymer matrix is formed from one or more ferroelectric polymers. In another embodiment, the polymer matrix is formed from one or more fluorinated polymers. Exemplary materials suitable for incorporation into the polymer matrix include poly(vinylidene fluoride) (PVDF), poly(vinylidene fluoride-co-trifluoroethylene) [P(VDF-TrFE)], poly(vinylidene fluoride-co-hexafluoropropylene) [P(VDF-HFP)], poly(vinylidene fluoride-co-trifluoroethylene-co-chlorofluoroethylene) [P(VDF-TrFE-CFE)], poly(trifluoroethylene) (PTFE), cyanoethyl pullulan (CEP), cyanoethylated cellulose, and trimethylolpropane triglycidyl ether cross-linked cyanoethyl pullulan (TTE/CEP). Suitably, the polymer matrix is formed from poly(vinylidene fluoride-co-hexafluoropropylene) [P(VDF-HFP)].

[0032] In another embodiment, the intermediate layer has a thickness of 10 – 50 nm. Suitably, the intermediate layer has a thickness of 10 – 45 nm. More suitably, the intermediate layer has a thickness of 10 – 40 nm. Even more suitably, the intermediate layer has a thickness of 15 – 35 nm. Most suitably, the intermediate layer has a

thickness of 20 – 30 nm. It will be understood that the thickness of the intermediate layer is provided as an average value calculated from the observed thickness at numerous points across the layer.

[0033] In another embodiment, the intermediate layer has a dielectric constant of less than 5. Suitably, the intermediate layer has a dielectric constant of less than 4.5. More suitably, the intermediate layer has a dielectric constant of less than 4.

[0034] In another embodiment, the intermediate layer is formed from one or more homopolymers or copolymers. Suitably, the one or more homopolymers or copolymers is cross-linked, such that the intermediate layer exhibits a high degree of insolubility in those solvents commonly used for solution deposition of semiconductors. In one embodiment, the intermediate layer is formed from one or more polymers selected from the group consisting of poly(α -methylstyrene), cross-linked poly(4-vinylphenol), polystyrene, poly(methyl methacrylate), or copolymers thereof (such as poly(4-vinylphenol-co- methyl methacrylate)). In another embodiment, the intermediate layer is formed from one or more of the aforementioned polymers in combination with one or more self-assembled monolayers (SAMs) (e.g. Hexamethyldisilazane (HMDS), Octyltrichlorosilane (OTS), Octylphosphonic acid (OPA), Octadecylphosphonic acid (ODPA), and Octadecyltrichlorosilane (ODTS)). Suitably, the intermediate layer is formed from poly(4-vinylphenol) cross-linked with poly(melamine-co-formaldehyde).

[0035] In another embodiment, the intermediate layer is formed from a 2 – 10 wt% poly(4-vinylphenol) solution with poly(melamine-co-formaldehyde) cross-linker. Suitably, intermediate layer is formed from a 2 wt% poly(4-vinylphenol) solution with poly(melamine-co-formaldehyde) cross-linker. In an embodiment, the weight ratio of poly(4-vinylphenol) to poly(melamine-co-formaldehyde) is 1.5:1 – 2.5:1.

[0036] The semiconductor layer forming part of the present OTFTs may be formed from any suitable material, as will be appreciated by the skilled reader. For example, the semiconductor layer may comprise one or more suitable materials selected from small molecules (e.g. 6,13-bis(triisopropylsilyl)ethynyl)pentacene (TIPS-Pentacene), dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT)), polycrystalline polymers (e.g. poly(3,6-di(2-thien-5-yl)-2,5-di(2-octyldodecyl)-pyrrolo[3,4-c]pyrrole-1,4-dione)thieno[3,2-b]thiophene (PDPPTT), poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTtT)), amorphous polymers (e.g. poly(triarylamine) (PTAA), indenofluorene poly(triarylamine) (IF-PTAA)) and small molecule/polymer blends (e.g. a blend of 6,13-bis(triisopropylsilyl)ethynyl)pentacene and poly(α -methylstyrene), or a blend of PBTtT and PMMA). Suitably, the semiconductor layer comprises a blend of 6,13-

bis(triisopropylsilylethynyl)pentacene and poly(α -methylstyrene). More suitably, the semiconductor layer comprises PDPPTT, DNTT, 6,13-bis(triisopropylsilylethynyl)pentacene, or a blend of 6,13-Bis(triisopropylsilylethynyl)pentacene and poly(α -methylstyrene).

[0037] In another embodiment, the configuration of the transistor is selected from the group consisting of bottom-gate bottom-contact, bottom-gate top-contact, top-gate bottom-contact and top-gate top-contact. Suitably, the OTFT has a bottom-gate bottom-contact configuration. Suitably, the configuration of the transistor is bottom-gate bottom-contact.

Organic thin film transistor preparation

[0038] As discussed hereinbefore, the present invention also provides a process for the preparation of an organic thin film transistor as defined herein, the process comprising the steps of:

- a) providing a gate electrode,
- b) applying the dielectric layer to an exposed surface of the gate electrode,
- c) applying the intermediate layer to the exposed surface of the dielectric layer, and
- d) applying the semiconductor layer to the exposed surface of the intermediate layer.

[0039] The processes of the present invention present a number of advantages over prior art approaches. Owing to the specific materials they incorporate, many prior art OTFTs require highly-sophisticated and expensive high-vacuum and high-temperature deposition techniques in order to deposit the gate dielectric layer. In comparison, the gate dielectric layer and intermediate layer forming part of the present OTFTs lend themselves to comparatively facile and inexpensive low-temperature solution-based manufacturing techniques, such as spin coating.

[0040] It will be understood that the present OTFTs are prepared by sequentially depositing the various layers specified in steps b), c) and d) one on-top of the other. Hence, in step c), *the exposed surface* of the dielectric layer will be understood to be the surface that lies opposite the dielectric layer/gate electrode interface. Likewise, in step d), *the exposed surface* of the intermediate layer will be understood to be the surface that lies opposite the intermediate layer/dielectric layer interface.

[0041] In an embodiment, the dielectric layer is applied to the gate electrode as a dispersion. Suitably, the dispersion comprises at least one organic solvent. In an embodiment, the dispersion comprises the polymer matrix dissolved in DMF, into which the nanoparticles are dispersed. Suitably, the dispersion has a volume ratio of polymer matrix to nanoparticles of 1:1 – 8:1. More suitably, the dispersion has a volume ratio of nanoparticles to polymer matrix of 1.25:1 – 7:1. Even more suitably, the dispersion has a volume ratio of polymer matrix to nanoparticles of 2:1 – 4:1. Most suitably, the dispersion has a volume ratio of polymer matrix to nanoparticles of 3:1

[0042] In another embodiment, step b) comprises spin coating an exposed surface of the gate electrode with the dielectric layer. In one embodiment, the spin coating is carried out at 1500 – 3000 rpm. In another embodiment, step b) further comprises the step of heating the spin coated dielectric layer at a temperature of 70 – 110°C, or more suitably at 90°C.

[0043] In another embodiment, the intermediate layer is applied to the dielectric layer as a solution. Suitably, the intermediate layer solution comprises at least one organic solvent. In one embodiment, the intermediate layer solution comprises propylene glycol monomethyl ether acetate (PGMEA).

[0044] In another embodiment, step c) comprises spin coating the exposed surface of the dielectric layer with the intermediate layer. In one embodiment, the spin coating is carried out at 4000 – 6000 rpm. In another embodiment, step c) further comprises the step of heating the spin coated intermediate layer at a temperature of 110 – 150°C, or more suitably at 130°C.

[0045] In another embodiment, the semiconductor layer is applied to the intermediate layer as a solution.

[0046] In another embodiment, step d) comprises spin coating the exposed surface of the intermediate layer with the semiconductor layer. In an embodiment, the spin coating is carried out at 500 – 2000 rpm. In another embodiment, step d) further comprises heating the spin coated semiconductor layer at a temperature of 40 – 120°C, depending on the particular semiconductor material. In one embodiment, the heating is carried out at a temperature of 50 – 80°C. In another embodiment, the heating is carried out at a temperature of 100 – 130°C.

[0047] In another embodiment, one or more of steps b), c) and d) is performed by vacuum deposition.

[0048] In another embodiment, the process further comprises the step of providing source and drain electrodes. The skilled person will appreciate that the source and drain electrodes can be deposited at any suitable instance in order to arrive at any one particular configuration or geometry of OTFT.

Applications of organic thin film transistors

[0049] As discussed hereinbefore, the present invention also provides an electronic device comprising an organic thin film transistor as defined herein.

[0050] The low-voltage OTFTs of the invention are promising candidates for wearable and portable electronics (e.g. personal medical devices), since they are simply battery-driven (<1.5 V for AAA batteries and <0.9 V for button cell batteries), in addition to their low power consumption and lightweight which allow them to be wearable and portable with longer lifetime without the need to carry a step-up conversion to charge them up. Moreover, the present OTFTs can be successfully fabricated on flexible substrates and hence offers flexibility required for wearable textiles as well as its solution-processability which provides large-area production.

[0051] In an embodiment, the electronic device is portable or wearable.

[0052] As discussed hereinbefore, the present invention also provides a use of an organic thin film transistor as defined herein for water sensing applications.

[0053] Low-voltage transistor operation is critical to stable operation in aqueous media to avoid electrolytic hydrolysis of water (which occurs below approximately 1.4V) and high ionic conduction through the analyte solution.

EXAMPLES

[0054] Examples of the invention will now be described, by way of example only, with reference to the accompanying figures, in which:

Fig. 1 shows a schematic of bottom-gate, bottom-contact (BGBC) OTFTs prepared in accordance with the present invention.

Fig. 2 shows a Transmission Electron Microscopy (TEM) image of stack structure of PVP-capped BST-P(VDF-HFP) nanocomposite layer spin-coated on an Al-coated substrate.

Fig. 3 shows the contact angle of a water drop on (a) an uncapped: $89^\circ \pm 0.7$ BST-P(VDF-HFP), and (b) on PVP-capped: $77^\circ \pm 0.5$, BST-P(VDF-HFP) nanocomposite layer; γ_{lv} , γ_{sv} , and γ_{sl} represent the liquid-vapour, solid-vapour, and solid-liquid interfacial tensions, respectively, and θ is the contact angle.

Fig. 4 shows tapping mode atomic force microscopy (AFM) images of adhesion profile of (a) uncapped and (b) PVP-capped BST-P(VDF-HFP) and (c) uncapped and (d) PVP-capped BZ-P(VDF-HFP).

Fig. 5 shows leakage current density of (a) BST-P(VDF-HFP) and (b) BZ-P(VDF-HFP) nanocomposite dielectric films.

Fig. 6 shows (a) leakage current density and (b) capacitance density for various concentrations of PVP intermediate layer.

Fig. 7 shows transfer characteristics including leakage current (dotted line) and output characteristic of (a) and (b) PDDTTTT and DNTT (c) and (d) OTFTs using PVP-capped BST-P(VDF-HFP) gate dielectric layer, $V_{SD} = -1$ V, channel length (L) = 2000 μm and channel width (W) = 40 μm .

Fig. 8 shows transfer characteristics including leakage current (dotted line) and output characteristic of TIPS-Pentacene/PaMS OTFTs using PVP-capped (a) and (b) BST-P(VDF-HFP) and (c) and (d) BZ-P(VDF-HFP) gate dielectric layer, $V_{SD} = -1$ V, channel length (L) = 2000 μm and channel width (W) = 50 μm .

Fig. 9 shows (a) transfer and (b) output characteristics of IDT-BT, OFET using PVP-capped, BST-P(VDF-HFP) nanocomposite dielectric layer. $V_{SD} = -3$ V, channel length (L) = 2000 μm and channel width (W) = 60 μm .

Fig. 10 shows (a) leakage current densities of uncapped and PVP-capped, CT-P(VDF-HFP) nanocomposite dielectric films; (b) transfer and (c) output characteristics of PDPPTT OFET using PVP-capped, CT-P(VDF-HFP) nanocomposite dielectric layer. $V_{SD} = -1.5$ V, channel length (L) = 2000 μm and channel width (W) = 60 μm .

Fig. 11 shows (a) areal capacitance of pristine and nanocomposites of cellulose; and (b) leakage current densities of uncapped and PVP-capped, BST-Cellulose nanocomposite dielectric films.

Fig. 12 shows tapping mode AFM images of peak force profile of (a) uncapped and (b) PVP-capped BST-Cellulose nanocomposite layers.

Fig. 13 shows (a) transfer and (b) output characteristics of PDPPTT OFET using uncoated BST-cellulose nanocomposite dielectric layer. $V_{SD} = -3$ V, channel length (L) = 2000 μm and channel width (W) = 80 μm .

Fig. 14 shows (a) transfer and (b) output characteristics of PDPPTT OFET using PVP-BST-cellulose nanocomposite dielectric layer. $V_{SD} = -1.5$ V, channel length (L) = 2000 μm and channel width (W) = 70 μm .

Fig. 15 shows (a) transfer and (b) output characteristics of PDPPTT OFET using PVP-BZ-cellulose nanocomposite dielectric layer. $V_{SD} = -1.5$ V, channel length (L) = 2000 μm and channel width (W) = 70 μm .

Materials

[0055] Pre-synthesised barium strontium titanate nanoparticles (BST, average particle size <100 nm), barium zirconate nanoparticles (BZ, average particle size <50 nm), calcium titanate nanoparticles (CT, average particle size = 100 nm), poly(4-vinylphenol) (PVP, average $M_w \sim 25,000$), poly (melamine-co-formaldehyde) (PMF, $M_n \sim 432$, 84 wt% in 1-butanol), propylene glycol monomethyl ether acetate (PGMEA, $\geq 99.5\%$), poly (vinylidene fluoride-co-hexafluoropropylene) (PVDF-HFP), cyanoethylated cellulose, N,N-dimethylformamide (DMF, 99.8%), 6, 13-bis (triisopropylsilylethynyl) pentacene (TIPS-Pentacene), poly (α -methylstyrene) (PaMS, $M_w \sim 300,000$) and 2,3,4,5,6-pentafluorothiophenol (PFBT) are purchased from Sigma-Aldrich. All chemicals and solvents were used as received without further purification. PDPPTT and indacenodithiophene-benzothiadiazole (IDT-BT) were synthesised in-house.

Example 1 – Preparation of nanocomposite suspension

[0056] P(VDF-HFP) pellets (50 mg ml^{-1}) are dissolved in DMF and stirred for minimum 6 hours. Various volume ratios (7:1 to 1.25:1) of BST or BZ nanoparticles are dispersed in P(VDF-HFP) solution, followed by a 2-hour ultrasonication and thereafter stirring for minimum 12 hours to further promote uniform dispersion of nanoparticles. The nanocomposite suspension is then centrifuged at 6000 rpm for 5 min to separate any possible larger particles and agglomerates to obtain a homogeneous suspension. The resultant nanocomposite suspension is stable and no apparent precipitation is observed for weeks.

Example 2 – Fabrication of thin film transistors

[0057] Fig. 1 shows a schematic of bottom-gate, bottom-contact (BGBC) OTFTs.

[0058] BGBC transistors are fabricated on Corning® glass substrates on which a 100 nm aluminium (Al) layer is thermally evaporated to serve as the gate electrode. For further cleanliness, Al surface is briefly UV-treated prior to spin-coating the nanocomposite dielectric layer.

[0059] As aforementioned, the nanocomposite suspension is stable for weeks, however, it is recommended to ultrasonicate the suspension for 30 min on the day of fabrication. The nanocomposite dielectric film was formed by spin-coating P(VDF-HFP)-based nanocomposite suspension at 3000 rpm for 2 min and annealing at 90° C for 90 min. An ultrathin capping layer of PVP (20 mg ml⁻¹) in PGMEA with added PMF (10 mg ml⁻¹) cross-linking agent is spin-coated atop the nanocomposite layer at 5000 rpm for 2 min, followed by cross-linking at 130° C for 90 min under nitrogen (N₂). Thickness measurement of the capping layer is carried out by measuring the height of a step/trench created into the dielectric layer (i.e. the distance between the glass surface at the bottom and surface of the dielectric film on the top) using contact profilometry and atomic force microscopy (AFM). Different methods were applied to create the trench across the sample, such as manually creating a scribe line by using a diamond scribe, tip of a pair of tweezers or wooden toothpick. The thickness is measured at different points along the trench and the average value is then calculated. The resulting dielectric bilayer ~ 178 nm as measured by AFM. 50 nm-thick gold (Au) source and drain electrodes are deposited through a shadow mask by thermal evaporation. The effective area of each electrode is 1.2 mm². Au contacts are then modified by submersing samples in a PFBT solution followed by washing with IPA for several times.

[0060] As the final stage of fabrication, the semiconductor active layer is deposited. For devices using the semiconductor blend, a 7:3 by weight (10 mg ml⁻¹) of TIPS-Pentacene:PaMS solution is spin-coated at 500 rpm for 2 min, followed by heating the sample at 60° C for 20 min under N₂. OTFTs with polycrystalline polymer semiconductor layer are finalised by spin-coating PDPPTT (10 mg ml⁻¹) solution at 1000 rpm for 1 min and subsequently heating the sample at 110° C for 30 min under N₂. For devices with organic small molecule semiconductor, a thin crystalline layer (~50 nm) of DNTT is vacuum-deposited. DNTT crystals are very fragile, hence extra care has to be taken during sublimation in the vacuum evaporator.

Example 3 – Transmission Electron Microscopy

[0061] Fig. 2 shows a Transmission Electron Microscopy (TEM) image of stack structure of PVP-capped BST-P(VDF-HFP) nanocomposite layer spin-coated on an Al-coated substrate.

[0062] The TEM image confirms the presence PVP partial coverage. By only partially capping the high- k nanocomposite with a thin low- k polymer layer, a remarkable use of surface roughness is made to obtain high-capacitance dielectric, while improving dielectric-semiconductor interface to realise an exceptionally low operating voltage OTFT with reasonably high carrier mobility.

Example 4 – Contact angle

[0063] Fig. 3 shows the contact angle of a water drop on (a) an uncapped: $89^\circ \pm 0.7$ BST-P(VDF-HFP), and (b) on PVP-capped: $77^\circ \pm 0.5$, BST-P(VDF-HFP) nanocomposite layer; γ_{lv} , γ_{sv} , and γ_{sl} represent the liquid-vapour, solid-vapour, and solid-liquid interfacial tensions, respectively, and θ is the contact angle..

[0064] The presence of cross-linked PVP capping layer plays a crucial role in fabrication and performance of OTFTs by improving underlying nanocomposite surface properties (roughness, surface polarity, surface energy, and wettability) and controlling dielectric-semiconductor interface. The 14% reduction in the water contact angle on PVP-capped BST-P(VDF-HFP) nanocomposite layer compared to that of the uncapped layer confirms the presence of a thin PVP layer and its contribution to reduced surface polarity and increased wettability.

Example 5 – Atomic Force Microscopy

[0065] In order to systematically pinpoint the effect of PVP capping layer on surface properties of nanocomposite layers, adhesion profiles are mapped using tapping mode atomic force microscopy (AFM) and presented in Fig. 4. Adhesion profiles of uncapped BST and BZ nanocomposites are illustrated in Figs. 4(a) and 4(c) respectively in which darker areas correspond to nanoparticles or areas of lower adhesion and lower surface energy. According to these AFM images, nanoparticles are reasonably well dispersed in the nanocomposite film, although more aggregates are observed in the case of BZ nanocomposites.

[0066] Fig. 4(c) verifies higher degree of agglomeration between BZ nanoparticles compared to that between BST nanoparticles. This effect is originated due to smaller dimensions and larger surface-to-volume ratio of BZ nanoparticles which results in higher packing, greater tendency to aggregate and hence formation of thicker and rougher films.

[0067] It can be clearly ascertained that PVP has filled in the valleys between nanoparticles and covered areas of smaller root mean square (RMS) roughness producing greater flat areas with higher adhesion, while it has only formed a fine skin (noticeable by colour difference) over areas of higher RMS roughness. Comparing Figs. 4(b) and 4(d), despite observing larger area of PVP full coverage (over possibly only P(VDF-HFP) or smaller, better dispersed BZ nanoparticles), BZ nanocomposite layer comprises considerably more rough features (aggregates) clearly visible due to their colour contrast and super fine coating of PVP.

Example 6 – Electrical properties of dielectric films

[0068] Leakage current density measured on parallel-plate capacitors using BST and BZ nanocomposite dielectric layer are shown in Figs. 5(a) and (b) respectively.

[0069] As expected, lower leakage current densities (10^{-9} A mm⁻² at ± 1 V), at least by one order of magnitude, are measured through PVP-capped nanocomposite dielectric layers than those of the pristine nanocomposite. This is attributed to less rough, denser and thicker bilayer dielectrics.

[0070] In spite of almost matching values of leakage current density through PVP-capped BST and BZ nanocomposite dielectric layers, significant deviations in their other key surface and dielectric characteristics are pinpointed and collected in Tables 1 and 2 respectively.

Table 1 - Surface and dielectric properties of BST-P(VDF-HFP) nanocomposite layers

BST-P(VDF-HFP) nanocomposite	RMS Roughness [nm]	Thickness [nm]	C _i * [nF/cm ²]	Dielectric Constant (k)
Uncapped	28.4	148±0.3	93.7±0.2	15.7
PVP-Capped	20.32	178±0.2	64.4±0.2	13.2

*Capacitance is measured at 1 kHz

Table 2 - Surface and dielectric properties of BZ-P(VDF-HFP) nanocomposite layers

BZ-P(VDF-HFP) nanocomposite	RMS Roughness [nm]	Thickness [nm]	C_i^* [nF/cm ²]	Dielectric Constant (k)
Uncapped	33.8	269±0.6	72.3±0.8	21.9
PVP-Capped	29.3	293±0.1	27.5±0.3	8.9

*Capacitance is measured at 1 kHz

[0071] Based on data in both tables, thickness of the PVP layer is 20-30 nm. BZ nanocomposites exhibit higher dielectric constant than BST nanocomposites. However, since surface roughness and film thickness of BZ nanocomposite film are greater, their capacitance per unit area (C_i) is smaller than that of BST nanocomposite dielectrics. In accordance with observations made on corresponding AFM images (Fig 4), PVP-capped BST and BZ nanocomposite layers are found less rough, thicker and thus resulting in smaller C_i and k value

[0072] According to Table 2, capping BST-P(VDF-HFP) nanocomposite with a PVP layer results in reasonably lower C_i and k compared to that of uncapped nanocomposite. However, PVP-capped BZ-P(VDF-HFP) nanocomposite dielectrics exhibit an almost 60% drop in both C_i and k compared to those of uncapped nanocomposite layers. Therefore, PVP-capped BST-P(VDF-HFP) nanocomposite bilayers are considered a more desirable choice of gate dielectric in high performance, low-voltage OTFTs compared to PVP-capped BZ-P(VDF-HFP).

[0073] Fig. 6 shows that 2 wt% PVP provides low leakage current and good capacitance density (better than that for uncoated BST-P(VDF-HFP) nanocomposite), whilst simultaneously allowing for thinner dielectric films. Nonetheless, too large capacitance and too low leakage current are good properties for other applications, e.g. in supercapacitors.

Example 7 – Electrical properties of OTFTs

PDPPTT and DNTT OTFTs

[0074] For better understanding of how differently the two types of PVP-capped nanocomposite dielectrics impact device performance, contact-modified, bottom-gate, bottom-contact OTFTs (Fig. 1) were fabricated.

[0075] Transfer and output characteristics of low-voltage BST-P(VDF-HFP)-based OTFTs using solution-processed PDPPTT polycrystalline polymer and vacuum-deposited DNTT single molecules as the semiconductor active are shown in Fig. 7. Solution-processed PDPPTT OTFTs using high-k nanocomposite dielectric exhibit excellent device performance (Figs. 7(a) and (b)): operating voltage well below -1 V ($V_T = -0.5$ V), clean, hysteresis-free transfer characteristics, sufficiently low leakage current (at least one order of magnitude below “on” current), clear “off” and “on” operating states and satisfactorily high mobility of $0.14 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

[0076] Vacuum-deposited DNTT OTFTs operate at slightly higher voltage (< -1 V), with carrier mobility of $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

[0077] The mobility (μ) is extracted from Fig. 7(a) which is a fit of the square root of the drain current versus the gate voltage as given by Equation 2 shown below:

$$i_{D,sat} = \frac{1}{2} (\mu C_i) \left(\frac{W}{L} \right) ((V_{GS} - V_T)^2) \quad (2)$$

[0078] where $i_{D,sat}$ is the saturated drain current, V_{GS} is the gate voltage, V_T is the threshold voltage, C_i is the capacitance density of the gate dielectric and L and W are the channel length and width respectively.

[0079] Comparing Figs. 7(a) and 7(c), transistor with solution-processed PDPPTT exhibit a steeper subthreshold slope than those with vacuum-deposited DNTT, indicating that the transition between “off” and “on” states is hampered in the latter due to higher interface trap density.

[0080] The rough nanocomposite dielectric surface may lead to formation of smaller grains and more disordered domains in vacuum-deposited DNTT thin film which act as charge traps at the dielectric-semiconductor interface. Similarly, the output characteristics in Figs. 7(b) and 7(d) illustrates higher pinch-off point (where $|V_D| = |V_G| - |V_T|$) for DNTT OTFTs compared to those with PDPPTT active layer which leads to higher operating voltage in the former.

[0081] The positive shift in threshold voltage of vacuum deposited DNTT (Fig. 7(c)) is also ascribed to interfacial trap density and the possible increase in trapped charges into localised states; an effect which is time dependent and referred to as bias stress effect. Nonetheless, BST-P(VDF-HFP)-based OTFTs using both classes of semiconducting materials have shown good device performance at low operating voltage.

TIPS-Pentacene OTFTs

[0082] A blend of TIPS-Pentacene small molecules and PaMS insulating polymer is utilised in this work as the active layer. As illustrated in Fig. 8(a) and (b), PVP-capped, BST-P(VDF-HFP)-based OTFTs using solution-processed TIPS-Pentacene/ PaMS blend display excellent transfer and output characteristics below operating voltage of -1 V; almost comparable to those of solution-processed polycrystalline PDPPTT (Figs. 7(a) and (b)).

[0083] An unrivalled high mobility of $0.06 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is obtained for TIPS-Pentacene/ PaMS OTFTs; the highest value reported for such solution-deposited semiconductor blend at -1 V operating voltage ($V_{\text{T}} = -0.55 \text{ V}$). Furthermore, lower subthreshold slope and leakage current density (one order of magnitude lower than that of PDPPTT) is achieved using the semiconductor blend which is attributed to better dielectric-semiconductor interface. As a result of vertical phase separation occurring upon the semiconductor blend deposition, a TIPS-Pentacene layer is sandwiched in between two layers of PaMS, hence the bottom PaMS layer contributes to an enriched, more robust and trap-free interface at the dielectric.

[0084] To allow a more systematic understanding of how PVP-capped, P(VDF-HFP)-based nanocomposite dielectric layers using different filler particles influences the overall device performance, TIPS-Pentacene/PaMS OTFTs using BZ-P(VDF-HFP) nanocomposite dielectric layers are fabricated and characterised. Figs 8(b) and (c) show transfer and output characteristics of these OTFTs. As speculated, PVP-capped, BZ-P(VDF-HFP)-based devices could not be operated below -1 V, but satisfactorily under -1.5 V, due to higher threshold voltage ($V_{\text{T}} = -0.85$). This is believed to be ascribed to larger thickness and surface roughness and thus smaller C_i of BZ-P(VDF-HFP) nanocomposite dielectric layer (Fig. 4(d)). Nevertheless, leakage current density is still low (due to smoother interface formed by using a semiconductor blend) and a relatively high mobility of $0.08 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is measured below -1.5 V.

[0085] The full set of transistor characteristics determined using different combinations of nanocomposite dielectrics and semiconductor active layers are gathered in Table 3

Table 3 - Device characteristics of OTFTs based on different nanocomposite dielectrics and different solution-processed semiconductor active layers

PVP-Capped Nanocomposite	Semiconductor	μ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$	V_T V	SS^* mV dec^{-1}	On/Off ratio
BST-P(VDF-HFP)	PDPPTT	0.14	-0.5	221	10^3
BST-P(VDF-HFP)	DNTT	0.02	0.1	640	10^2
BST-P(VDF-HFP)	TIPS-Pentacene/PdMS	0.06	-0.55	169	10^3
BZ-P(VDF-HFP)	TIPS-Pentacene/PdMS	0.08	-0.85	153	10^3

* Subthreshold Swing

IDT-BT OTFTs

[0086] In addition to those devices discussed above in Table 3, OFETs comprising indacenodithiophene-benzothiadiazole (IDT-BT) were also fabricated and tested. Fig. 9 shows transfer and output characteristics of IDT-BT, OFET using PVP-capped, BST-P(VDF-HFP) nanocomposite dielectric layer. $V_{SD} = -3 \text{ V}$, channel length (L) = 2000 μm and channel width (W) = 60 μm .

Example 8 - OTFTs incorporating CT nanocomposites

[0087] Dielectric suspensions comprising of 5 wt % calcium titanate in 5 wt% P(VDF-HFP) were prepared and used in bottom-gated (top and bottom contact) OFETs on both glass and PEN substrates. The suspension was centrifuged at 6000 rpm for 5-8 min. The dielectric layer was then spin-coated at 3000 rpm and annealed at 90 °C for 90 min. The average thickness of the dielectric layer was 240-280nm. A PVP capping layer was then applied (spin-coated at 5000 rpm for 2 min and cross-linked at 130 °C for 90 min) with an average thickness of 30 nm. PDPPTT devices using CT-P(VDF-HFP) nanocomposite dielectric ($C = 53 \text{ nF/cm}^2$) were operative below -1.5 V with a mobility (μ) of 0.2 cm^2/Vs and threshold voltage of -0.1 V.

[0088] Fig. 10 shows (a) leakage current densities of uncapped and PVP-capped, CT-P(VDF-HFP) nanocomposite dielectric films; (b) transfer and (c) output characteristics of PDPPTT OFET using PVP-capped, CT-P(VDF-HFP) nanocomposite dielectric layer. $V_{SD} = -1.5 \text{ V}$, channel length (L) = 2000 μm and channel width (W) = 60 μm .

Example 9 - OTFTs incorporating cyanoethylated cellulose nanocomposite

[0089] Gate dielectric suspension comprising of 5 wt % barium strontium titanate (BST, $d = 100$ nm) or barium zirconate (BZ, $d = 50$ nm) in 5 wt % cyanoethylated cellulose have been processed and used in bottom-gated (top and bottom contact) OFETs.

[0090] Fig. 11 shows (a) areal capacitance of pristine and nanocomposites of cellulose; and (b) leakage current densities of uncapped and PVP-capped, BST-Cellulose nanocomposite dielectric films. Fig. 12 shows tapping mode AFM images of peak force profile of (a) uncapped and (b) PVP-capped BST-Cellulose nanocomposite layers.

[0091] PDPPTT OFETs using uncoated pristine cellulose dielectric layer were operational below -3 V. Fig. 13 shows (a) transfer and (b) output characteristics of PDPPTT OFET using uncoated BST-cellulose nanocomposite dielectric layer. $V_{SD} = -3$ V, channel length (L) = $2000\text{ }\mu\text{m}$ and channel width (W) = $80\text{ }\mu\text{m}$. Thereafter, a PVP capping layer is applied with an average thickness of 40 nm. PDPPTT OFETs using PVP-capped, BST-cellulose nanocomposite dielectric were operative below -1.5 V. Fig. 14 shows (a) transfer and (b) output characteristics of PDPPTT OFET using PVP- BST-cellulose nanocomposite dielectric layer. $V_{SD} = -1.5$ V, channel length (L) = $2000\text{ }\mu\text{m}$ and channel width (W) = $70\text{ }\mu\text{m}$.

[0092] Fig. 15 shows (a) transfer and (b) output characteristics of PDPPTT OFET using PVP-capped BZ-cellulose nanocomposite dielectric layer. $V_{SD} = -1.5$ V, channel length (L) = $2000\text{ }\mu\text{m}$ and channel width (W) = $70\text{ }\mu\text{m}$.

[0093] Based on the above-discussed data, it is clear that the addition of the PVP capping layer resulted in reduced surface roughness, leakage current and threshold voltage. Table 4 below summarizes the properties of PDPPTT OFET devices comprising a nanocomposite gate dielectric containing cyanoethylated cellulose:

	C_G nF/cm ²	RMS nm	d nm	k	μ cm ² /Vs	V_T V	ON/OFF	S mV/dec
BST-Cellulose	48.6	28	330	18.1	1.1	-1.4	10^4	165
BST-Cellulose with PVP	44.5	13	370	19.2	0.6	-0.7	10^3	253
BZ-Cellulose with PVP	39.0	19	390	17.0	0.4	-0.8	3×10^2	316

[0094] While specific embodiments of the invention have been described herein for the purpose of reference and illustration, various modifications will be apparent to a person

skilled in the art without departing from the scope of the invention as defined by the appended claims.

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CLAIMS

1. An organic thin film transistor comprising a semiconductor layer and a gate dielectric layer, and a continuous intermediate layer disposed therebetween, wherein
 - a) the gate dielectric layer has a thickness of 50 nm – 1 μ m and comprises 2 – 11 wt.% of nanoparticles dispersed in a polymer matrix, the nanoparticles having an average particle size of 20 – 200 nm and a high dielectric constant, and the polymer matrix having a high dielectric constant; and
 - b) the intermediate layer has a thickness of 10 – 55 nm and comprises a polymeric material having a low dielectric constant.
2. The organic thin film transistor of claim 1, wherein the gate dielectric layer has a thickness of 50 – 300 nm.
3. The organic thin film transistor of claim 1 or 2, wherein the gate dielectric layer has a thickness of 100 – 200 nm.
4. The organic thin film transistor of claim 1, 2 or 3, wherein the gate dielectric layer comprises 3 – 8 wt.% of nanoparticles dispersed in a polymer matrix.
5. The organic thin film transistor of any preceding claim, wherein the gate dielectric layer comprises 4 – 7 wt.% of nanoparticles dispersed in a polymer matrix.
6. The organic thin film transistor of any preceding claim, wherein the nanoparticles are identical or different.
7. The organic thin film transistor of any preceding claim, wherein the nanoparticles have a dielectric constant of greater than 10.
8. The organic thin film transistor of any preceding claim, wherein the nanoparticles have a dielectric constant of greater than 15.
9. The organic thin film transistor of any preceding claim, wherein the nanoparticles are formed from inorganic material.
10. The organic thin film transistor of any preceding claim, wherein the nanoparticles are formed from one or more ABO_3 -type perovskites.

11. The organic thin film transistor of any preceding claim, wherein the nanoparticles are formed from one or more ABO_3 -type perovskites selected from the group consisting of barium strontium titanate, barium zirconate, calcium titanate, calcium zirconate, and barium titanate.
12. The organic thin film transistor of any preceding claim, wherein the nanoparticles are formed from barium strontium titanate, barium zirconate or a mixture thereof.
13. The organic thin film transistor of any preceding claim, wherein the nanoparticles have an average particle size of 20 – 100 nm.
14. The organic thin film transistor of any preceding claim, wherein the nanoparticles have an average particle size of 20 – 50 nm.
15. The organic thin film transistor of any preceding claim, wherein the polymer matrix has a dielectric constant of greater than 5.
16. The organic thin film transistor of any preceding claim, wherein the polymer matrix has a dielectric constant of greater than 9.
17. The organic thin film transistor of any preceding claim, wherein the polymer matrix is formed from one or more homopolymers or copolymers.
18. The organic thin film transistor of any preceding claim, wherein the polymer matrix is formed from poly(vinylidene fluoride-co-hexafluoropropylene) [P(VDF-HFP)].
19. The organic thin film transistor of any preceding claim, wherein the intermediate layer has a thickness of 15 – 35 nm.
20. The organic thin film transistor of any preceding claim, wherein the intermediate layer has a dielectric constant of less than 4.
21. The organic thin film transistor of any preceding claim, wherein the intermediate layer is formed from one or more homopolymers or copolymers.
22. The organic thin film transistor of claim 21, wherein the one or more homopolymers or copolymers is cross-linked.
23. The organic thin film transistor of any preceding claim, wherein the intermediate layer is formed from cross-linked poly(4-vinylphenol), polystyrene, poly(methyl methacrylate), or a copolymer thereof.

24. The organic thin film transistor of any preceding claim, wherein the intermediate layer is formed from poly(4-vinylphenol) cross-linked with poly(melamine-co-formaldehyde).

25. The organic thin film transistor of any preceding claim, wherein the semiconductor layer comprises one or more suitable materials selected from small molecules, polycrystalline polymers, amorphous polymers and small molecule/polymer blends.

26. The organic thin film transistor of any preceding claim, wherein the semiconductor layer comprises PDPPTT, DNTT, 6,13-bis(triisopropylsilylethynyl)pentacene, or a blend of 6,13-Bis(triisopropylsilylethynyl)pentacene and poly(α -methylstyrene).

27. The organic thin film transistor of any preceding claim, wherein the semiconductor layer comprises a blend of 6,13-Bis(triisopropylsilylethynyl)pentacene and poly(α -methylstyrene).

28. The organic thin film transistor of any preceding claim, wherein the configuration of the transistor is selected from the group consisting of bottom-gate bottom-contact, bottom-gate top-contact, top-gate bottom-contact and top-gate top-contact.

29. A process for the preparation of an organic thin film transistor as claimed in any preceding claim, the process comprising the steps of:

- a) providing a gate electrode,
- b) applying the dielectric layer to an exposed surface of the gate electrode,
- c) applying the intermediate layer to the exposed surface of the dielectric layer, and
- d) applying the semiconductor layer to the exposed surface of the intermediate layer.

30. The process of claim 29, wherein the dielectric layer is applied to the gate electrode as a dispersion.

31. The process of claim 30, wherein the dielectric layer dispersion contains at least one organic solvent.

32. The process of any of claims 29, 30 or 31, wherein step b) comprises spin coating an exposed surface of the gate electrode with the dielectric layer.

33. The process of claim 32, wherein step b) further comprises the step of heating the spin coated dielectric layer at a temperature of 70 – 110°C.

34. The process of any of claims 20 to 33, wherein the intermediate layer is applied to the dielectric layer as a solution.
35. The process of claim 34, wherein the intermediate layer solution comprises at least one organic solvent.
36. The process of any of claims 29 to 35, wherein step c) comprises spin coating the exposed surface of the dielectric layer with the intermediate layer.
37. The process of claim 36, wherein step c) further comprises the step of heating the spin coated intermediate layer at a temperature of 110 – 150 °C.
38. The process of any of claims 29 to 37, wherein the semiconductor layer is applied to the intermediate layer as a solution.
39. The process of any of claims 29 to 38, wherein step d) comprises spin coating the exposed surface of the intermediate layer with the semiconductor layer.
40. The process of any of claims 29 to 39, wherein step d) further comprises heating the spin coated semiconductor layer at a temperature of 40 – 120 °C.
41. The process of any of claims 29 to 40, further comprising the step of providing source and drain electrodes.
42. An electronic device comprising an organic thin film transistor as claimed in any of claims 1 to 28.
43. The electronic device of claim 42, wherein the device is portable or wearable.
44. Use of an organic thin film transistor as claimed in any of claims 1 to 28 for water sensing applications.

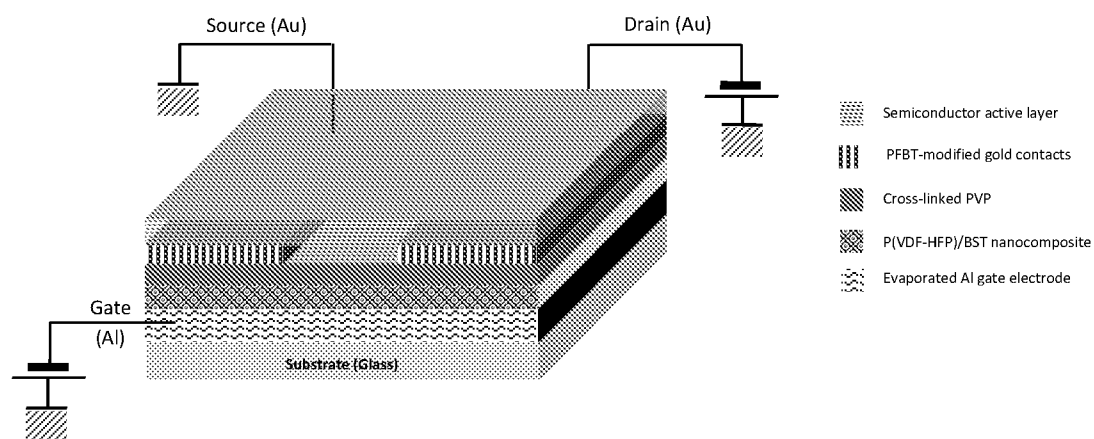


FIG. 1

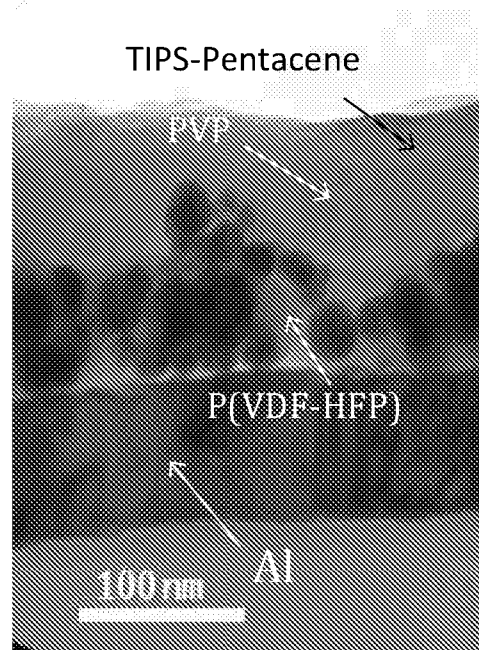


FIG. 2

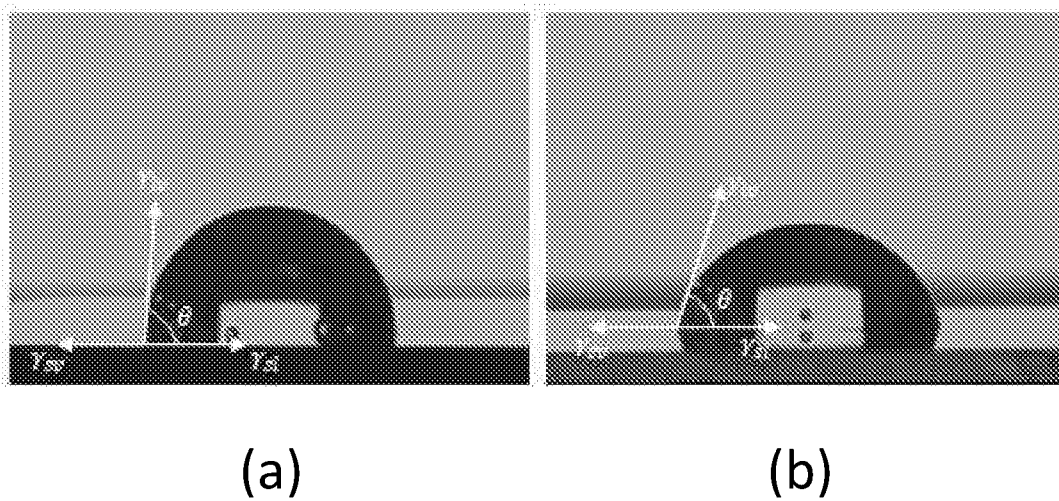


FIG. 3

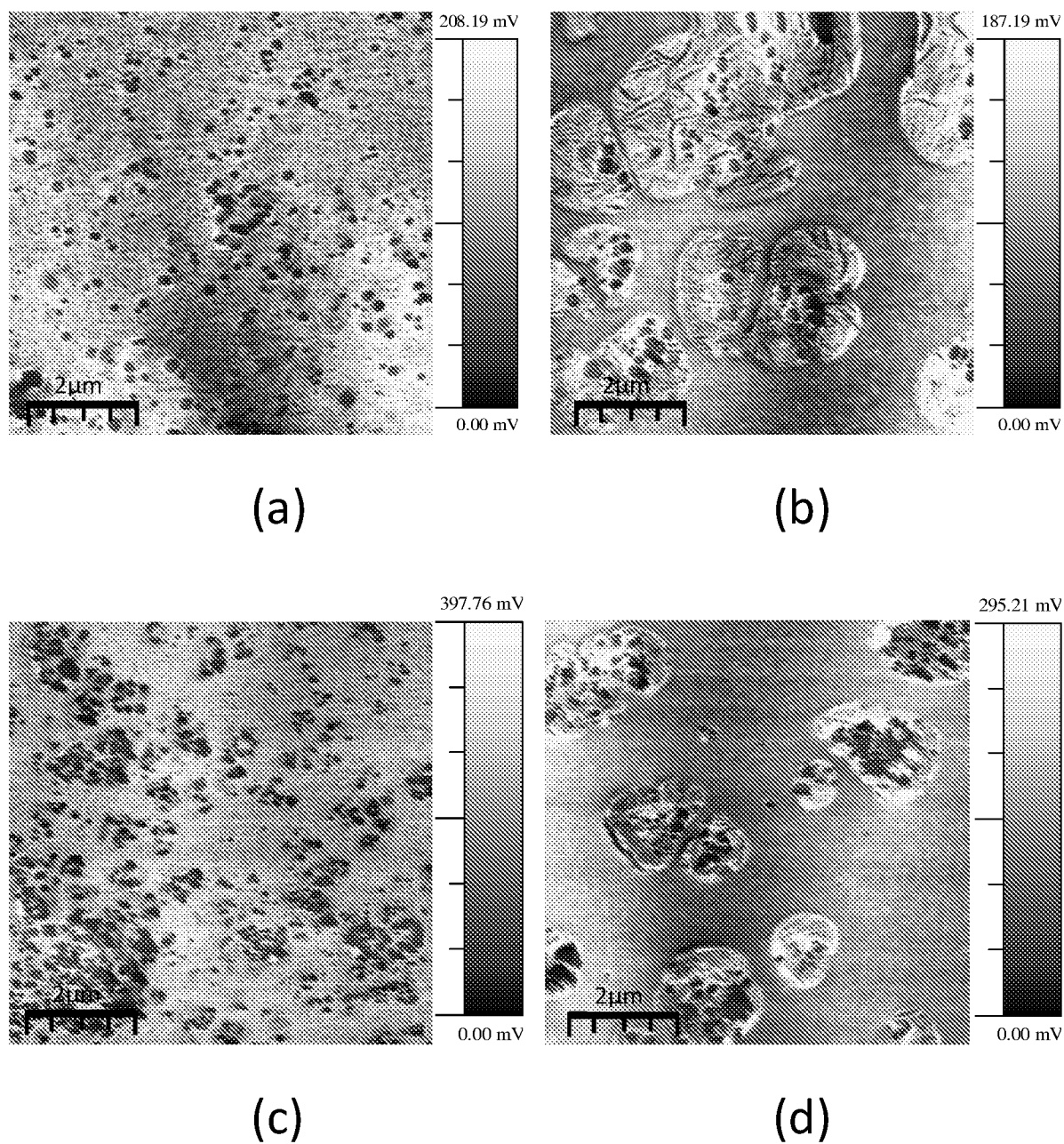
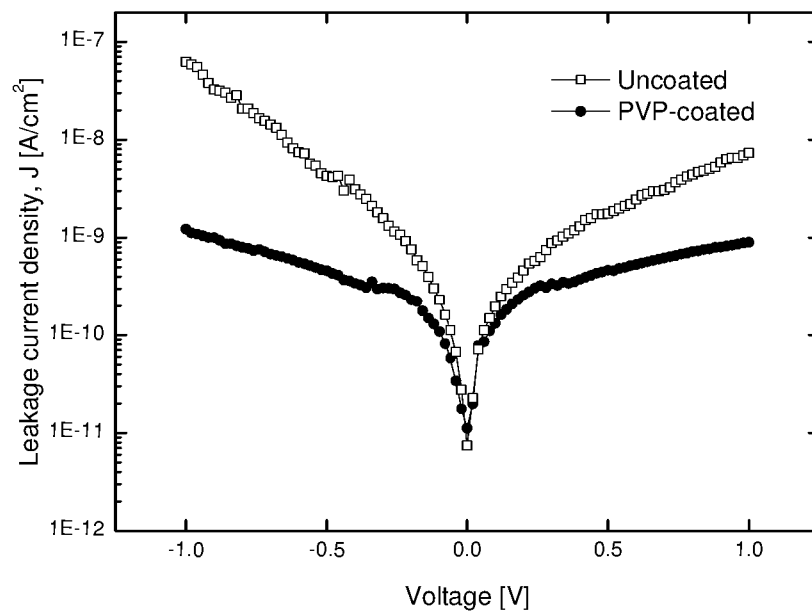
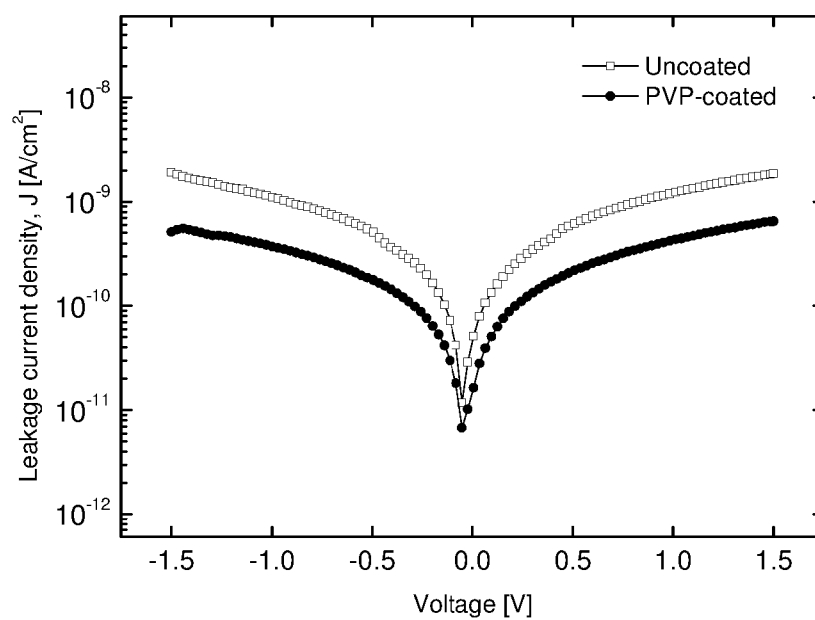


FIG. 4

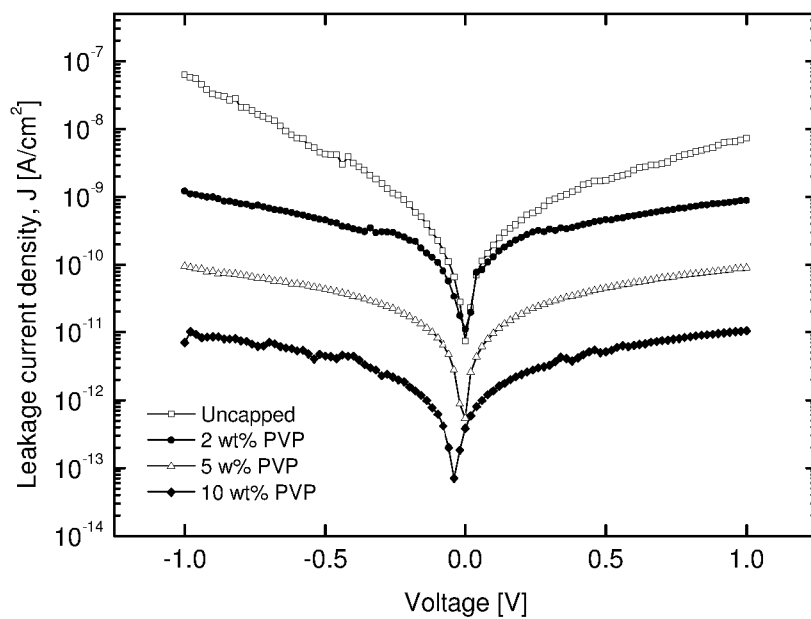


(a)

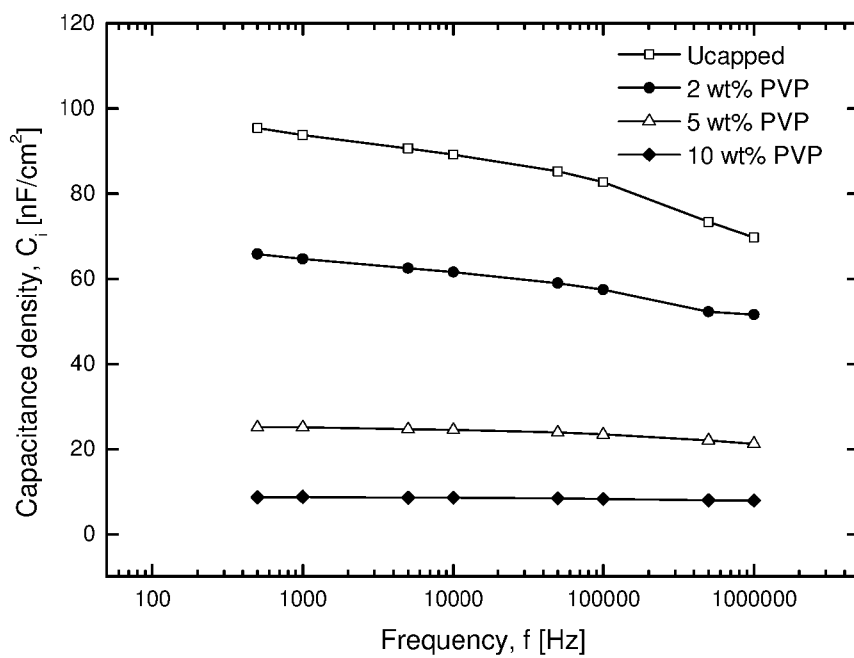


(b)

FIG. 5

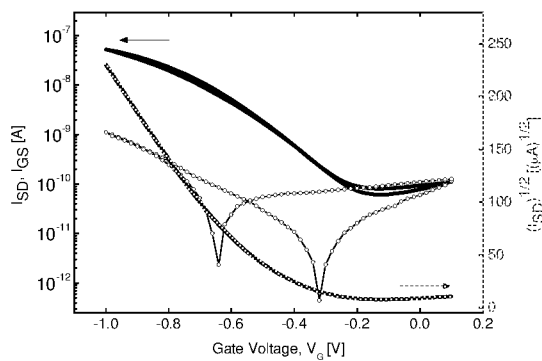


(a)

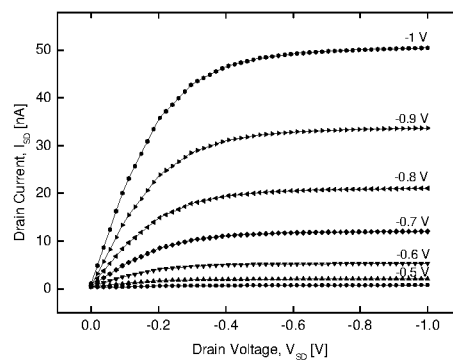


(b)

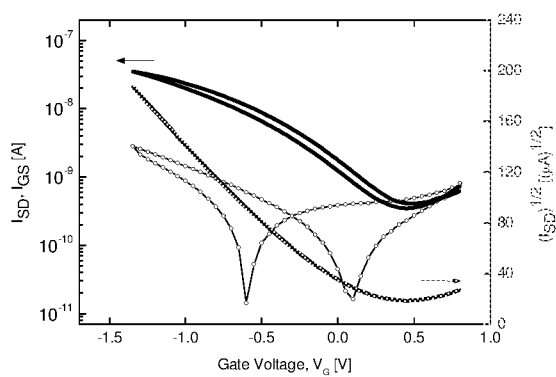
FIG. 6



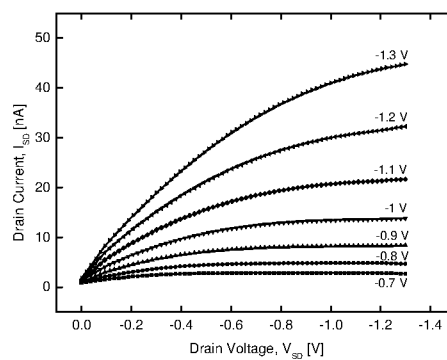
(a)



(b)

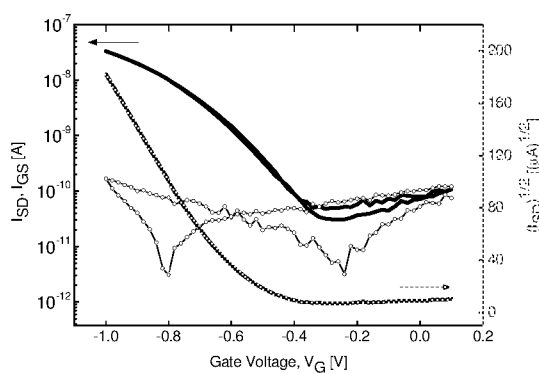


(c)

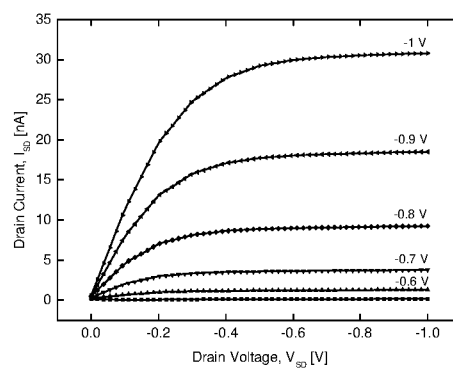


(d)

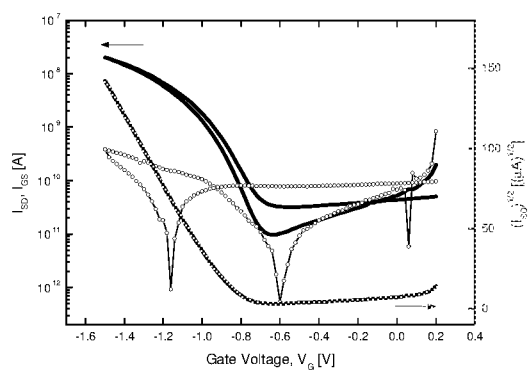
FIG. 7



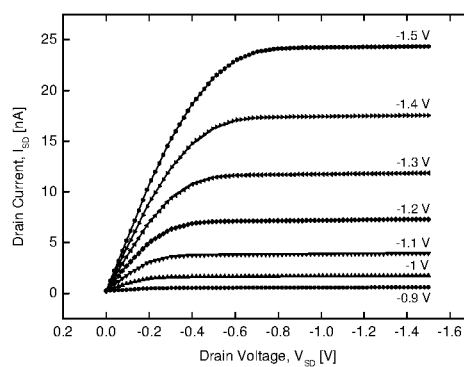
(a)



(b)



(c)



(d)

FIG. 8

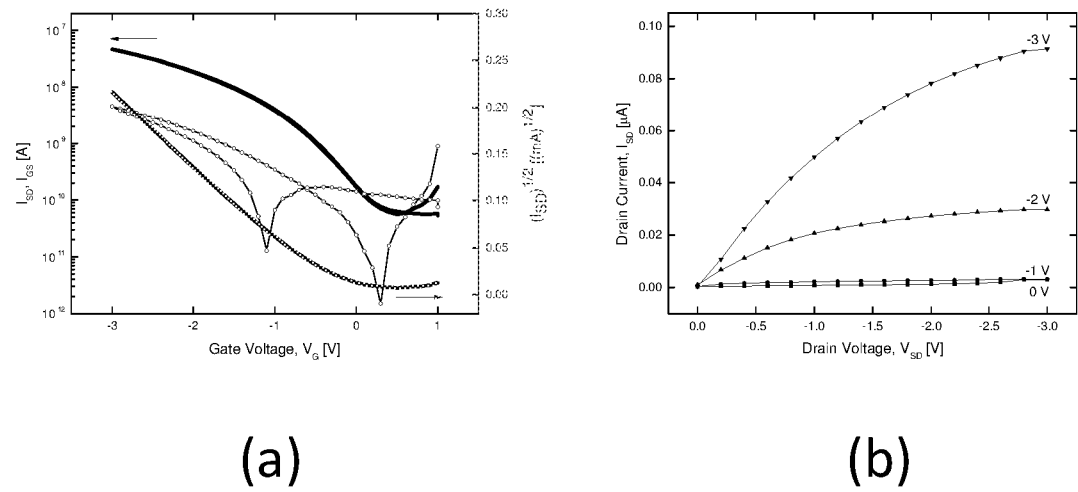
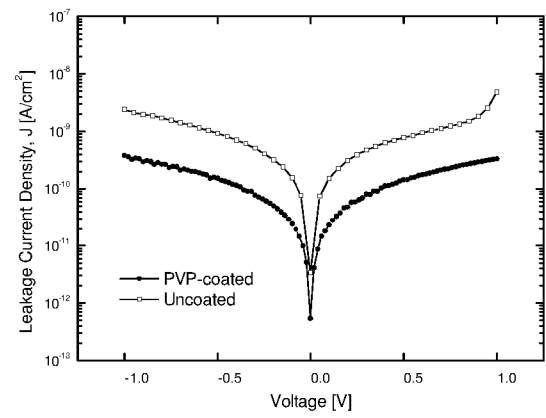
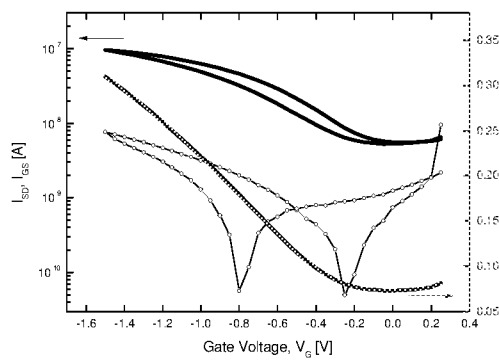


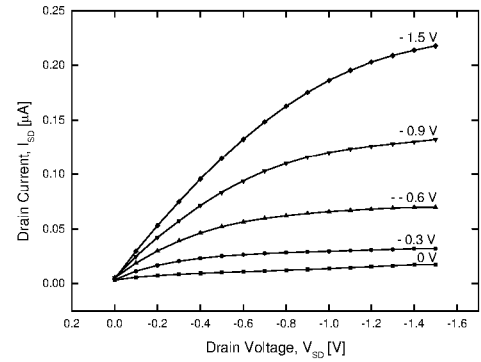
FIG. 9



(a)

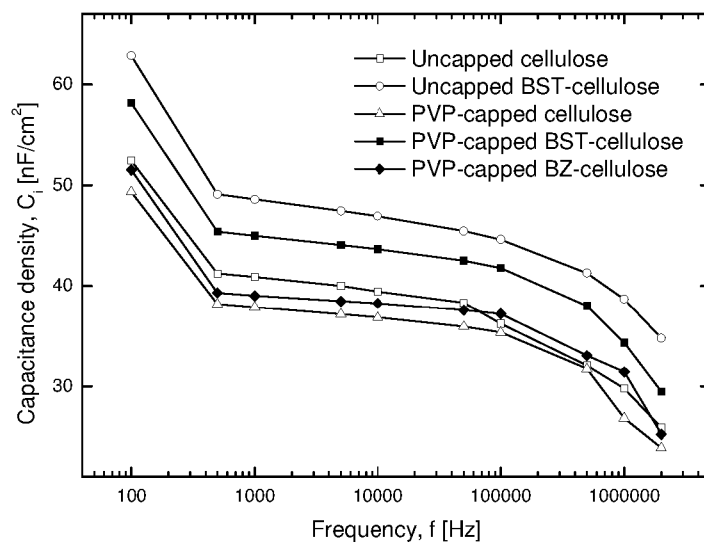


(b)

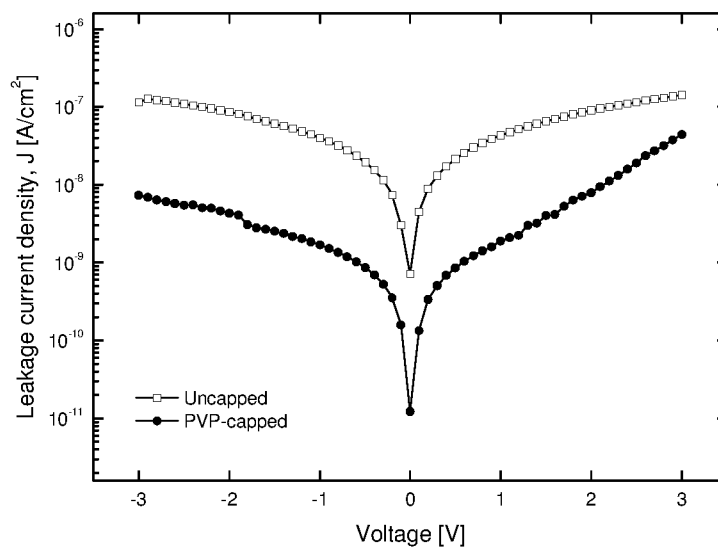


(c)

FIG. 10

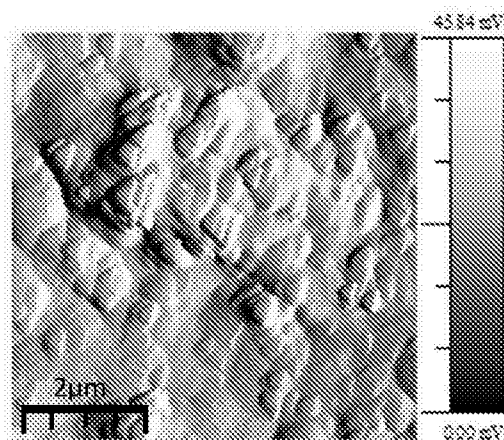


(a)

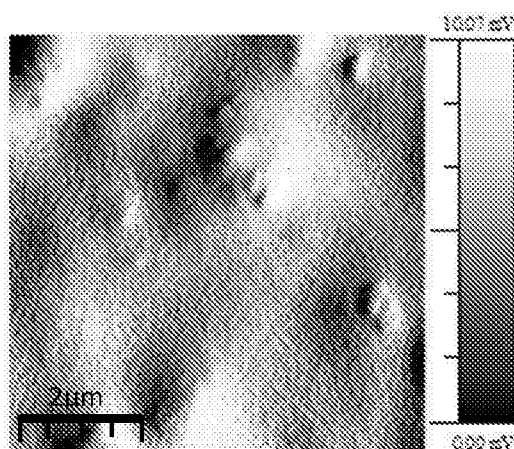


(b)

FIG. 11

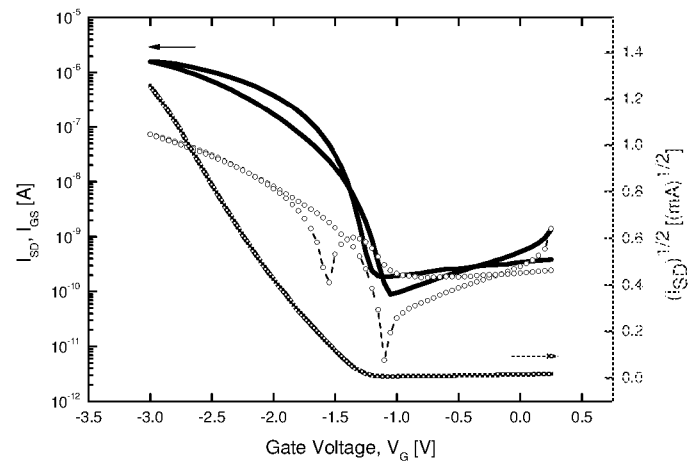


(a)

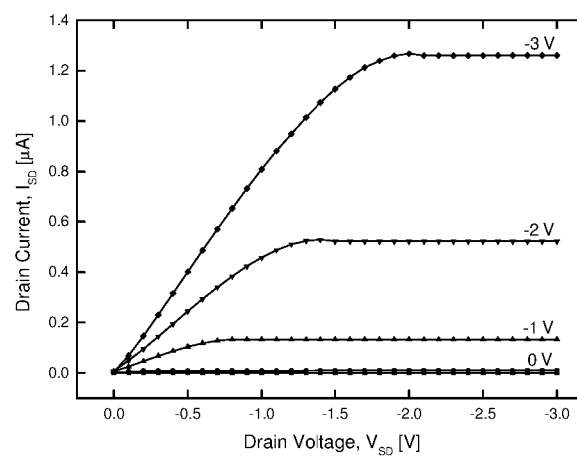


(b)

FIG. 12

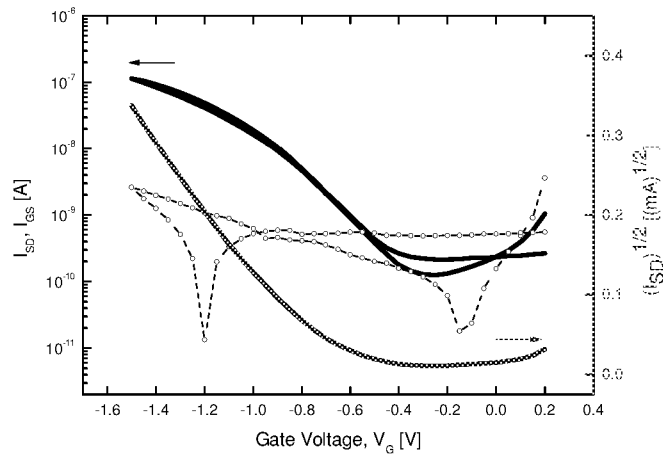


(a)

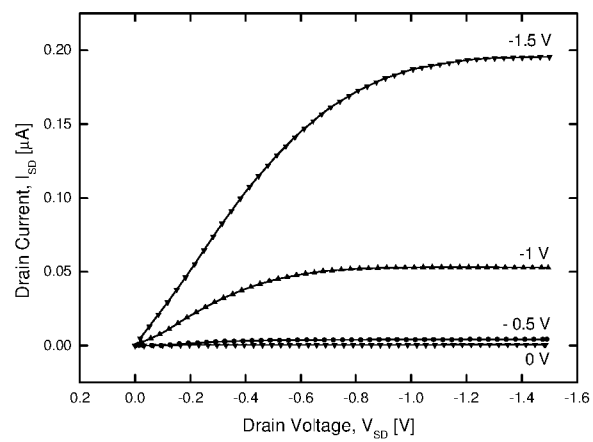


(b)

FIG. 13

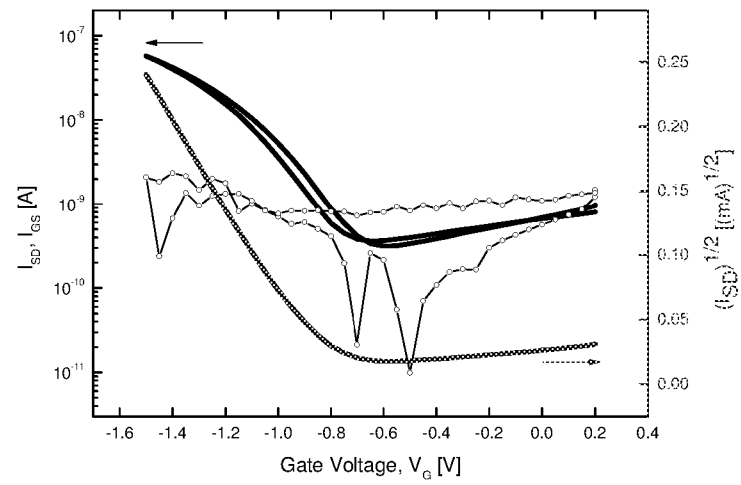


(a)

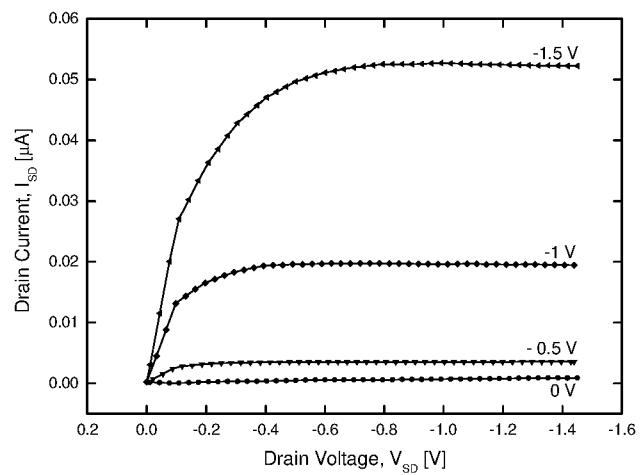


(b)

FIG. 14



(a)



(b)

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2015/051478

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L51/05 H01L51/30
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L G01N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, COMPENDEX, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JANG YUNSEOK ET AL: "High field-effect mobility pentacene thin-film transistors with nanoparticle polymer composite/polymer bilayer insulators", APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS, US, vol. 94, no. 18, 5 May 2009 (2009-05-05), pages 183301-183301, XP012121184, ISSN: 0003-6951, DOI: 10.1063/1.3124660 cited in the application	1-4, 6-14,17, 19-25, 28-32, 34-37,41
Y	pages 183301-1, column 2 - pages 183301-2, column 1; table 1 pages 183301-3, column 1 ----- -/-	5,15,16, 18,26, 27,33, 38-40, 42-44



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

15 July 2015

Date of mailing of the international search report

23/07/2015

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Beierlein, Udo

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2015/051478

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	YUNSANG KIM ET AL: "Enhancement of breakdown strength and energy density in BaTiO₃ ferroelectric polymer nanocomposites via processing-induced matrix crystallinity and uniformity", RSC ADV., vol. 4, no. 38, 16 April 2014 (2014-04-16), pages 19668-19673, XP055202397, DOI: 10.1039/C4RA00987H abstract -----	18
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2015/051478

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