

(51) International Patent Classification:
H03M 1/12 (2006.01)(21) International Application Number:
PCT/US2016/018625(22) International Filing Date:
19 February 2016 (19.02.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/180,837 17 June 2015 (17.06.2015) US
14/977,598 21 December 2015 (21.12.2015) US

(71) Applicant: CYPRESS SEMICONDUCTOR CORPORATION [US/US]; 198 Champion Court, San Jose, California 95134 (US).

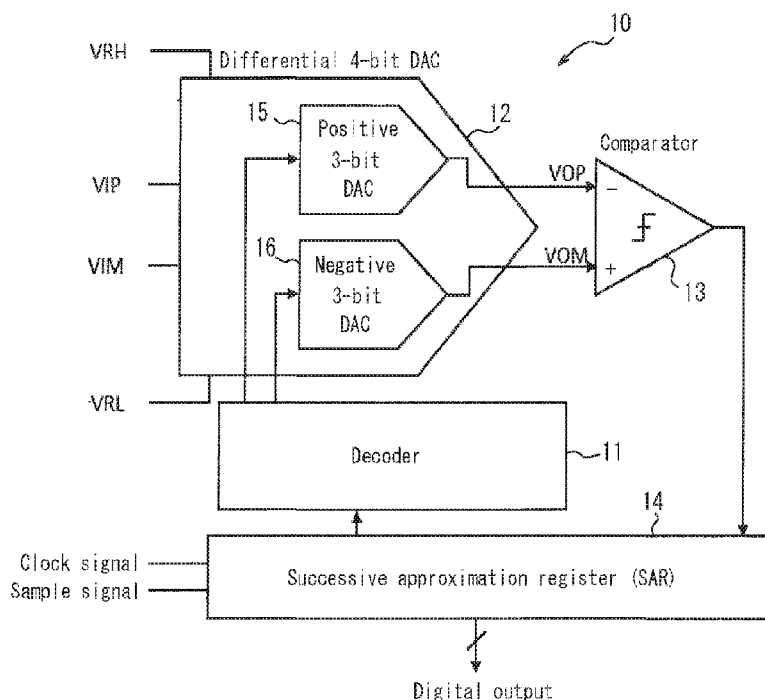
(72) Inventors: **KIJIMA, Masashi**; 2-1844-2 Kozoji-Cho, Kasugai-shi, Aichi 487-0013 (JP). **MIZUTA, Satoru**; 2-1844-2 Kozoji-Cho, Kasugai-shi, Aichi 487-0013 (JP). **TANII, Tsutomu**; 2-1844-2 Kozoji - Cho, Kasugai-shi,Aichi 487-0013 (JP). **MATSUNAMI, Hiroyuki**; Kasugai (JP).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

(54) Title: ANALOG-DIGITAL CONVERTER AND CONTROL METHOD

FIG. 1(57) Abstract: An analog-digital converter includes digital-analog converter, a comparator, and a register. The digital-analog converter is configured to output a differential voltage between a reference voltage and a voltage of an analog signal. The comparator is configured to output a comparison signal corresponding to the differential voltage output by the digital-analog converter. The register is configured to cause the digital-analog converter to generate N pairs of differential voltages ($N \geq 1$), an $(N+1)^{\text{th}}$ pair of differential voltages, and to output a digital signal corresponding to a comparison signal having a smallest voltage among $(N+1)$ comparison signals.



SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG). **Published:**

— *with international search report (Art. 21(3))*

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

ANALOG-DIGITAL CONVERTER AND CONTROL METHOD

PRIORITY

[0001] This application is an International Application of U.S. Patent Application No. 14/977,598, filed on December 21, 2015, claims the priority and benefit of U.S. Provisional Application No. 62/180,837, filed on June 17, 2015, all of which are incorporated by reference herein in their entirety.

TECHNICAL FIELD

[0002] This disclosure relates to an analog-digital converter and a control method.

BACKGROUND

[0003] A successive approximation analog-digital converter (ADC) generates different reference voltages with an internal digital-analog converter (DAC) and compares the voltage of an analog signal to be converted with the reference voltages in order to generate a digital signal corresponding to the voltage of the analog signal to be converted. An example of a successive approximation ADC has a resolution corresponding to the number of passive components in the internal DAC, i.e. a resolution of N bits for 2^N passive components (where N is a natural number).

[0004] In order to increase the resolution of such successive approximation ADC, a greater number of passive components needs to be provided in the internal DAC. Increasing the number of passive components in the DAC, however, raises manufacturing costs. Furthermore, conversion speed decreases and power consumption increases due to the increased time constant during analog-digital conversion.

SUMMARY

[0005] It would therefore be helpful to provide a more efficient analog-digital converter and control method therefor.

[0006] An analog-digital converter according to one aspect of this disclosure includes a digital-analog converter configured to output a differential voltage between a reference voltage and a voltage of an analog signal; a comparator configured to output a comparison signal corresponding to the differential voltage output by the digital-analog converter; and a register configured to cause the digital-analog converter to generate N pairs of differential voltages, where N is an

integer greater than or equal to one, to cause the digital-analog converter to generate an $(N+1)^{\text{th}}$ pair of differential voltages by causing one of a positive side and a negative side of the digital-analog converter to output an $(N+1)^{\text{th}}$ differential voltage and causing the other of the positive side and the negative side to output a differential voltage equal to an N^{th} differential voltage as an $(N+1)^{\text{th}}$ differential voltage, and to output a digital signal corresponding to a smallest comparison signal having a smallest voltage among $(N+1)$ of the comparison signals. It is noted that as used in this disclosure, “register” refers to a circuit with storage elements used to control a converter.

[0007] In the above aspect, the digital-analog converter may be a differential digital-analog converter comprising a pair of converters that each include $(N+1)$ passive components, input the reference voltage and the voltage of the analog signal into the passive components, and generate N differential voltages between the reference voltage and the voltage of the analog signal.

[0008] In the above aspect, the register may cause one passive component in one converter of the pair of converters to connect to the reference voltage and output the $(N+1)^{\text{th}}$ differential voltage.

[0009] The above aspect may further include a decoder configured to input a digital signal into the digital-analog converter based on a signal acquired from the register.

[0010] In the above aspect, the passive components in the pair of converters may be capacitors, resistors, or a combination of capacitors and resistors.

[0011] In the above aspect, the passive components in the pair of converters may be configured with a binary system or a segmented system.

[0012] In the above aspect, the analog signal may be a differential signal or a single end signal.

[0013] In the above aspect, the analog-digital converter may include a plurality of the comparators.

[0014] In the above aspect, two reference voltages with different voltage levels may be connected via a switch to an input terminal on one of a positive side and a negative side in the comparators.

[0015] In the above aspect, the register may switch the reference voltage connected to the input terminal by controlling the switch when causing the digital-analog converter to output the $(N+1)^{\text{th}}$ differential voltage.

[0016] A control method according to one aspect of this disclosure is a control method used in an analog-digital converter including a digital-analog converter, a

comparator, and a register, the control method including the digital-analog converter outputting a differential voltage between a reference voltage and a voltage of an analog signal; the comparator outputting a comparison signal corresponding to the differential voltage output by the digital-analog converter; the register causing the digital-analog converter to generate N pairs of differential voltages, where N is an integer greater than or equal to one; the register causing the digital-analog converter to generate an $(N+1)^{\text{th}}$ pair of differential voltages by causing one of a positive side and a negative side of the digital-analog converter to output an $(N+1)^{\text{th}}$ differential voltage and causing the other of the positive side and the negative side to output a differential voltage equal to an N^{th} differential voltage as an $(N+1)^{\text{th}}$ differential voltage; and the register outputting a digital signal corresponding to a smallest comparison signal having a smallest voltage among $(N+1)$ of the comparison signals.

[0017] In the above aspect, the digital-analog converter may include a pair of converters that each include $(N+1)$ passive components, and the above aspect may further include the converters each inputting the reference voltage and the voltage of the analog signal into the passive components and generating N differential voltages between the reference voltage and the voltage of the analog signal.

[0018] The above aspect may further include the register causing one passive component in one converter of the pair of converters to connect to the reference voltage and output the $(N+1)^{\text{th}}$ differential voltage.

[0019] In the above aspect, the analog-digital converter may include a decoder, and the control method may further include the decoder inputting a digital signal into the digital-analog converter based on a signal acquired from the register.

[0020] In the above aspect, the passive components in the pair of converters may be capacitors, resistors, or a combination of capacitors and resistors.

[0021] In the above aspect, the passive components in the pair of converters may be configured with a binary system or a segmented system.

[0022] In the above aspect, the analog signal may be a differential signal or a single end signal.

[0023] In the above aspect, the analog-digital converter may include a plurality of the comparators.

[0024] In the above aspect, two reference voltages with different voltage levels may be connected via a switch to an input terminal on one of a positive side and a negative side in the comparators.

[0025] The above aspect may further include the register switching the reference

voltage connected to the input terminal by controlling the switch when causing the digital-analog converter to output the $(N+1)^{\text{th}}$ differential voltage.

[0026] The analog-digital converter and control method according to the embodiments below are more efficient by using fewer passive components to improve accuracy, while reducing manufacturing costs, increasing conversion speed, and reducing power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] In the accompanying drawings:

FIG. 1 is a functional block diagram illustrating an example of a 4-bit successive approximation ADC according to Embodiment 1;

FIG. 2 is a functional block diagram illustrating an example of a differential 4-bit DAC provided with 4-bit DACs;

FIG. 3 illustrates analog voltage output by the differential 4-bit DAC of FIG. 2;

FIG. 4 illustrates the positive analog output voltage and negative analog output voltage output by the differential 4-bit DAC of FIG. 1;

FIG. 5 is a flowchart illustrating an example control method executed by the differential 4-bit DAC of FIG. 1;

FIG. 6 illustrates an example of the circuit structure of the differential 4-bit DAC of FIG. 2;

FIG. 7 illustrates an example of the circuit structure of the differential 4-bit DAC of FIG. 1;

FIGS. 8A and 8B illustrate the results of an experiment performed using a 13-bit successive approximation ADC provided with a differential 13-bit DAC configured using 12-bit DACs;

FIG. 9 is a functional block diagram illustrating an example of a successive approximation ADC;

FIG. 10 illustrates an example of the circuit structure of the differential 2-bit DAC of FIG. 9;

FIG. 11 illustrates signals input into the differential 2-bit DAC of FIG. 9;

FIG. 12 illustrates an example of digital output by the successive approximation ADC of FIG. 9;

FIG. 13 is a functional block diagram illustrating an example of a 3-bit successive approximation ADC according to Embodiment 2;

FIG. 14 is a functional block diagram illustrating an example of the

differential 3-bit DAC in FIG. 13;

FIG. 15 illustrates signals input into the differential 3-bit DAC of FIG. 13;

FIG. 16 illustrates an example of digital output by the successive approximation ADC of FIG. 13;

FIG. 17 is a functional block diagram illustrating an example of a successive approximation ADC;

FIG. 18 illustrates an example of the circuit structure of the differential 3-bit DAC of FIG. 17;

FIG. 19 is a functional block diagram illustrating an example of a 4-bit successive approximation ADC according to Embodiment 3;

FIG. 20 illustrates an example of the circuit structure of the differential 4-bit DAC of FIG. 19;

FIG. 21 illustrates signals input into the 1-bit capacitive DAC of FIG. 19;

FIG. 22 illustrates signals input to and output from the 3-bit resistive DAC of FIG. 19;

FIG. 23 illustrates an example of digital output by the successive approximation ADC of FIG. 19 in the case of inputting a single end signal;

FIG. 24 illustrates an example of digital output by the successive approximation ADC of FIG. 19 in the case of inputting a differential signal;

FIG. 25 illustrates an example of the circuit structure of a differential comparator circuit provided in a flash ADC according to this disclosure;

FIG. 26 illustrates an example of the control state of each switch in the differential comparator circuit illustrated in FIG. 25; and

FIG. 27 illustrates an example of digital output of a 3-bit flash ADC.

DETAILED DESCRIPTION

[0028] The following describes the disclosed embodiments with reference to the drawings.

Embodiment 1

[0029] FIG. 1 is a functional block diagram illustrating an example of a successive approximation ADC according to one of the disclosed embodiments. The successive approximation ADC of this embodiment is a 4-bit successive approximation ADC having a resolution of four bits. A 4-bit successive approximation ADC 10 includes a decoder 11, a differential 4-bit DAC 12, a comparator 13, and a successive approximation register (SAR) 14. Under the control of the SAR 14, the 4-bit successive approximation ADC 10 generates the

differential voltage between the input analog voltage to be converted and a 4-bit resolution reference voltage with the differential 4-bit DAC 12 and the comparator 13 and tests whether the differential voltage is minimized, thereby generating and outputting a digital signal corresponding to the analog voltage. At this time, the differential 4-bit DAC 12 and the comparator 13 pass through a sampling phase and a trial phase with at least two trials. In this embodiment, the input analog signal to be converted is a differential signal having a voltage corresponding to the difference in potential between a positive analog signal VIP and a negative analog signal VIM. The reference voltage is the differential voltage between a high-voltage reference voltage VRH and a low-voltage reference voltage VRL supplied by a non-illustrated power source. Furthermore, the differential voltage to be tested (trial voltage), i.e. the difference between the analog voltage to be converted and the reference voltage, is the differential voltage between a positive analog output voltage VOP and a negative analog output voltage VOM, which are input into the comparator 13 from the differential 4-bit DAC 12.

[0030] The SAR 14 controls the overall analog-digital conversion processing by the 4-bit successive approximation ADC 10. A clock signal and a sample signal are input into the SAR 14. The sample signal is a signal that controls sampling. When the sample signal is on, the SAR 14 executes processing for the sampling phase in the differential 4-bit DAC 12, and when the sample signal is off, the SAR 14 executes processing for the trial phase in the differential 4-bit DAC 12. The SAR 14 generates a signal for controlling processing for successive approximation in the differential 4-bit DAC 12 and the comparator 13 and outputs the signal to the decoder 11. The signal output by the SAR 14 is referred to below as a control signal for successive approximation processing.

[0031] Based on the control signal for successive approximation processing obtained from the SAR 14, the decoder 11 inputs, into the differential 4-bit DAC 12, signals for controlling the on/off operation of each switch provided in the differential 4-bit DAC 12.

[0032] In response to the switch control signals input from the decoder 11 as digital signals, the differential 4-bit DAC 12 generates the positive analog output voltage VOP and the negative analog output voltage VOM based on a positive analog input voltage VIP and a negative analog input voltage VIM input into the differential 4-bit DAC 12 and on the high-voltage reference voltage VRH and the low-voltage reference voltage VRL input into the differential 4-bit DAC 12. The positive analog output voltage VOP and the negative analog output voltage VOM

respectively represent the differential voltage between the high-voltage reference voltage VRH and the positive analog input voltage VIP and the differential voltage between the low-voltage reference voltage VRL and the negative analog input voltage VIM in each trial of the trial phase.

[0033] In this embodiment, the positive analog output voltage VOP and the negative analog output voltage VOM output by the differential 4-bit DAC 12 are respectively generated by a positive 3-bit DAC 15 and a negative 3-bit DAC 16 included in the differential 4-bit DAC 12. In response to the switch control signal input from the decoder 11, the positive 3-bit DAC 15 generates the positive analog output voltage VOP from the high-voltage reference voltage VRH and the positive analog input voltage VIP. In response to the switch control signal input from the decoder 11, the negative 3-bit DAC 16 generates the negative analog output voltage VOM from the low-voltage reference voltage VRL and the negative analog input voltage VIM. In this embodiment, the positive 3-bit DAC 15 and the negative 3-bit DAC 16 execute 4-bit processing to convert the switch control signal into the analog output voltage.

[0034] As an example related to this embodiment, an example using a 4-bit DAC to output analog voltage with 4-bit resolution is described using FIGS. 2 and 3. FIGS. 2 and 3 illustrate output of analog voltage with 4-bit resolution by a differential 4-bit DAC that includes 4-bit DACs. The differential 4-bit DAC 22 illustrated in FIG. 2 includes a positive 4-bit DAC 25 and a negative 4-bit DAC 26.

[0035] FIG. 3 illustrates trial voltage output by the differential 4-bit DAC 22 illustrated in FIG. 2. In FIG. 3, the vertical axis represents the voltage level of the analog output voltages VOP and VOM output by the differential 4-bit DAC 22, and the horizontal axis represents the passage of time by processing phases executed by the differential 4-bit DAC 22. As illustrated in FIG. 3, the differential 4-bit DAC 22 first samples the analog input signal that is input into the differential 4-bit DAC 22 (sampling phase) and then performs trials from the first bit trial to the fourth (last) bit trial (trial phase). By performing these four trials, the differential 4-bit DAC 22 outputs the positive analog output voltage VOP and negative analog output voltage VOM with 4-bit resolution. In this example, the trial voltage that is the differential voltage between the positive analog output voltage VOP and the negative analog output voltage VOM is shown changing from nearly 0 V to 4 V, 2 V, and 1 V from the first bit trial to the last (fourth) bit trial. In this way, analog-digital conversion is achieved by performing trials at the resolution corresponding to the number of bits and using the digital value corresponding to

the reference voltage when the trial voltage is minimized, i.e. when the difference between the analog input voltage and the reference voltage is minimized.

[0036] FIG. 4 illustrates the positive analog output voltage VOP and negative analog output voltage VOM output by the differential 4-bit DAC 12 (of FIG. 1) in this embodiment. In FIG. 4, the vertical axis represents the voltage level of the analog output voltages output by the differential 4-bit DAC 12, and the horizontal axis represents the passage of time by processing phases executed by the differential 4-bit DAC 12. As illustrated in FIG. 4, the differential 4-bit DAC 12 first samples the analog input signal. The differential 4-bit DAC 12 then performs the first through third bit trials by symmetrically controlling the positive 3-bit DAC 15 and the negative 3-bit DAC 16.

[0037] Finally, the differential 4-bit DAC 12 performs the last bit trial. In the last bit trial, asymmetrical control is performed on the positive 3-bit DAC 15 and the negative 3-bit DAC 16. In greater detail, in the last bit trial, similar control to the control in the third bit trial is performed on the negative 3-bit DAC 16, whereas control differing from the control in the third bit trial is performed on the positive 3-bit DAC 15. In other words, control is only performed on the positive side in the last bit trial, unlike the first through the third bit trials in which control is performed on both the positive and negative sides. By performing such asymmetrical control, the differential 4-bit DAC 12 generates a positive analog output voltage VOP and negative analog output voltage VOM that are asymmetrical in the last bit trial, unlike the symmetrical positive analog output voltage VOP and negative analog output voltage VOM output in the first to third trials. In this way, with the positive 3-bit DAC 15 and negative 3-bit DAC 16 that have 3-bit resolution, the differential 4-bit DAC 12 achieves conversion to a 4-bit resolution digital signal in the ADC. In other words, the trial voltage that is the differential voltage between the positive analog output voltage VOP and the negative analog output voltage VOM is shown changing from the first bit trial to the last (fourth) bit trial. Analog-digital conversion is performed by using the digital value corresponding to the reference voltage when the trial voltage is minimized, i.e. when the difference between the analog input voltage and the reference voltage is minimized.

[0038] The circuit structure of the positive 3-bit DAC 15 and the negative 3-bit DAC 16 that achieve the above-described asymmetrical control during the last bit trial is described below.

[0039] Referring again to FIG. 1, the comparator 13 compares the positive analog

output voltage VOP and the negative analog output voltage VOM obtained from the differential 4-bit DAC 12 and outputs a signal corresponding to the result of comparison (also referred to below simply as a "comparison signal"). In greater detail, the comparator 13 outputs a comparison signal corresponding to the trial voltage that is the difference between the positive analog output voltage VOP and the negative analog output voltage VOM.

[0040] The SAR 14 stores the comparison signal output from the comparator 13. Upon obtaining the comparison signal with 4-bit resolution from the comparator 13 and storing the comparison signal, based on the comparison signal the SAR 14 outputs a digital signal of the value corresponding to the reference voltage when the trial voltage is minimized, i.e. when the difference between the analog input voltage and the reference voltage is minimized.

[0041] FIG. 5 is a flowchart illustrating an example of control method executed by the differential 4-bit DAC 12 of FIG. 1.

[0042] First, the differential 4-bit DAC 12 symmetrically controls the positive 3-bit DAC 15 and the negative 3-bit DAC 16 (step S11).

[0043] Next, the differential 4-bit DAC 12 determines whether three bit trials have been performed (step S12). The differential 4-bit DAC 12 determines whether three bit trials have been performed for example based on whether the below-described signal CTL has been input into the differential 4-bit DAC 12 from the decoder 11.

[0044] When determining that three bit trials have not been performed (step S12: No), then the differential 4-bit DAC 12 repeats step S11 and step S12 until determining in step S12 that three bit trials have been performed.

[0045] When determining that three bit trials have been performed (step S12: Yes), the differential 4-bit DAC 12 asymmetrically controls the positive 3-bit DAC 15 and the negative 3-bit DAC 16 as the last bit trial (step S13). The processing then terminates.

[0046] Since the above description of FIG. 5 is based on the differential 4-bit DAC 12 illustrated in FIG. 1, the differential 4-bit DAC 12 has been described as determining in step S12 whether three bit trials have been performed. For example, a differential (N+1)-bit DAC, however, would determine in step S12 whether N bit trials have been performed, where N is an integer greater than or equal to one.

[0047] Next, the circuit structure of the differential 4-bit DAC is described. First, with reference to FIG. 6, the circuit structure of the differential 4-bit DAC 22 illustrated in FIG. 2 is described.

[0048] In the example illustrated in FIG. 6, in the differential 4-bit DAC 22, the positive 4-bit DAC 25 and the negative 4-bit DAC 26 each include five capacitors as passive components. In FIG. 6, the 10 capacitors are indicated as capacitors with capacitances of C , C , $2C$, $4C$, and $8C$. Below, the capacitors C_{P1} , C_{P2} , C_{P3} , C_{P4} , and C_{P5} in the positive 4-bit DAC 25 respectively have capacitances of C , C , $2C$, $4C$, and $8C$. The capacitors C_{M1} , C_{M2} , C_{M3} , C_{M4} , and C_{M5} in the negative 4-bit DAC 26 respectively have capacitances of C , C , $2C$, $4C$, and $8C$.

[0049] In the positive 4-bit DAC 25, the capacitor C_{P1} is connected to the positive analog input voltage V_{IP} and the low-voltage reference voltage V_{RL} respectively via the switches S_A and $S_{A'}$. The capacitors C_{P2} , C_{P3} , C_{P4} , and C_{P5} are connected in parallel to the positive analog input voltage V_{IP} , the high-voltage reference voltage V_{RH} , and the low-voltage reference voltage V_{RL} . The capacitors C_{P2} , C_{P3} , C_{P4} , and C_{P5} are connected to the positive analog input voltage V_{IP} via respective switches S_A . The capacitors C_{P2} , C_{P3} , C_{P4} , and C_{P5} are connected to the high-voltage reference voltage V_{RH} respectively via the switches S_{H0} , S_{H1} , S_{H2} , and S_{H3} . The capacitors C_{P2} , C_{P3} , C_{P4} , and C_{P5} are connected to the low-voltage reference voltage V_{RL} respectively via the switches S_{L0} , S_{L1} , S_{L2} , and S_{L3} . The capacitors C_{P1} , C_{P2} , C_{P3} , C_{P4} , and C_{P5} are connected to an input common voltage V_{CM} of the comparator via the switch S_A .

[0050] In the negative 4-bit DAC 26 as well, so as to be symmetrical with the positive 4-bit DAC 25, the capacitor C_{M1} is connected to the negative analog input voltage V_{IM} and the high-voltage reference voltage V_{RH} respectively via the switches S_A and $S_{A'}$. The capacitors C_{M2} , C_{M3} , C_{M4} , and C_{M5} are connected in parallel to the negative analog input voltage V_{IM} , the high-voltage reference voltage V_{RH} , and the low-voltage reference voltage V_{RL} . The capacitors C_{M2} , C_{M3} , C_{M4} , and C_{M5} are connected to the negative analog input voltage V_{IM} via respective switches S_A . The capacitors C_{M2} , C_{M3} , C_{M4} , and C_{M5} are connected to the high-voltage reference voltage V_{RH} respectively via the switches S_{L0} , S_{L1} , S_{L2} , and S_{L3} . The capacitors C_{M2} , C_{M3} , C_{M4} , and C_{M5} are connected to the low-voltage reference voltage V_{RL} respectively via the switches S_{H0} , S_{H1} , S_{H2} , and S_{H3} . The capacitors C_{M1} , C_{M2} , C_{M3} , C_{M4} , and C_{M5} are connected to the input common voltage V_{CM} of the comparator via the switch S_A .

[0051] In the differential 4-bit DAC 22, switches labeled with the same reference sign perform the same on/off operation.

[0052] In the differential 4-bit DAC 22 illustrated in FIG. 6, when sampling, the switches S_A in the positive 4-bit DAC 25 and the negative 4-bit DAC 26 are

controlled to be in a closed state, i.e. on state (referred to below simply as "on"), whereas the other switches are controlled to be in a closed state, i.e. off state (referred to below simply as "off"). When the switches S_A are on, a charge corresponding to the positive analog input voltage V_{IP} accumulates in all of the capacitors C_{P1} , C_{P2} , C_{P3} , C_{P4} , and C_{P5} in the positive 4-bit DAC 25, and a charge corresponding to the negative analog input voltage V_{IM} accumulates in all of the capacitors C_{M1} , C_{M2} , C_{M3} , C_{M4} , and C_{M5} in the negative 4-bit DAC 26.

[0053] Next, when the differential 4-bit DAC 22 performs the first bit trial, the switches $S_{A'}$, S_{L0} , S_{L1} , S_{L2} , and S_{H3} are turned on, and the other switches are turned off. By the switches $S_{A'}$ turning on, the capacitor C_{P1} is connected to the low-voltage reference voltage V_{RL} , and the capacitor C_{M1} is connected to the high-voltage reference voltage V_{RH} . By the switches S_{L0} , S_{L1} , and S_{L2} turning on, the capacitors C_{P2} , C_{P3} , and C_{P4} are connected to the low-voltage reference voltage V_{RL} , and the capacitors C_{M2} , C_{M3} , and C_{M4} are connected to the high-voltage reference voltage V_{RH} . By the switches S_{H3} turning on, the capacitor C_{P5} is connected to the high-voltage reference voltage V_{RH} , and the capacitor C_{M5} is connected to the low-voltage reference voltage V_{RL} . By the switches S_A turning off, the capacitors C_{P1} , C_{P2} , C_{P3} , C_{P4} , and C_{P5} in the positive 4-bit DAC 25 are disconnected from the positive analog input voltage V_{IP} , and the capacitors C_{M1} , C_{M2} , C_{M3} , C_{M4} , and C_{M5} in the negative 4-bit DAC 26 are disconnected from the negative analog input voltage V_{IM} .

[0054] In the first bit trial, as a result of the above-described on/off control of the switches, the positive analog output voltage V_{OP} that is output is the difference in potential between the positive analog input voltage V_{IP} and the reference voltage that is determined by the capacitors C_{P1} , C_{P2} , C_{P3} , C_{P4} , and C_{P5} and the connection with the high-voltage reference voltage V_{RH} or the low-voltage reference voltage V_{RL} .

[0055] Similarly on the negative side, the negative analog output voltage V_{OM} that is output is the difference in potential between the negative analog input voltage V_{IM} and the reference voltage that is determined by the capacitors C_{M1} , C_{M2} , C_{M3} , C_{M4} , and C_{M5} and the connection with the high-voltage reference voltage V_{RH} or the low-voltage reference voltage V_{RL} .

[0056] Next, when the differential 4-bit DAC 22 performs the second bit trial, based on the result of the first bit trial, either the switches S_{H3} are turned on and the switches S_{L3} are turned off, or vice-versa. Furthermore, the switches S_{L2} are turned off, and the switches S_{H2} are turned on. In other words, in the second bit

trial, the capacitor C_{P4} is disconnected from the low-voltage reference voltage VRL and is electrically connected to the high-voltage reference voltage VRH. In the second bit trial, the capacitor C_{M4} is electrically disconnected from the high-voltage reference voltage VRH and connected to the low-voltage reference voltage VRL. In the second bit trial as well, as in the first bit trial, the difference in potential between the reference voltage and the positive analog input voltage VIP is output as the positive analog output voltage VOP, and the difference in potential between the reference voltage and the negative analog input voltage VIM is output as the negative analog output voltage VOM.

[0057] Next, when the differential 4-bit DAC 22 performs the third bit trial, based on the result of the second bit trial, either the switches S_{H2} are turned on and the switches S_{L2} are turned off, or vice-versa. Furthermore, the switches S_{L1} are turned off, and the switches S_{H1} are turned on. In other words, in the third bit trial, the capacitor C_{P3} is disconnected from the low-voltage reference voltage VRL and is connected to the high-voltage reference voltage VRH. In the third bit trial, the capacitor C_{M3} is disconnected from the high-voltage reference voltage VRH and connected to the low-voltage reference voltage VRL. In the third bit trial as well, as in the first bit trial, the difference in potential between the reference voltage and the positive analog input voltage VIP is output as the positive analog output voltage VOP, and the difference in potential between the reference voltage and the negative analog input voltage VIM is output as the negative analog output voltage VOM.

[0058] Finally, when the differential 4-bit DAC 22 performs the fourth bit trial, based on the result of the third bit trial, either the switches S_{H1} are turned on and the switches S_{L1} are turned off, or vice-versa. Furthermore, the switches S_{L0} are turned off, and the switches S_{H0} are turned on. In other words, in the fourth bit trial, the capacitor C_{P2} is disconnected from the low-voltage reference voltage VRL and is connected to the high-voltage reference voltage VRH. In the fourth bit trial, the capacitor C_{M2} is disconnected from the high-voltage reference voltage VRH and electrically connected to the low-voltage reference voltage VRL. In the fourth bit trial as well, as in the first bit trial, the difference in potential between the reference voltage and the positive analog input voltage VIP is output as the positive analog output voltage VOP, and the difference in potential between the reference voltage and the negative analog input voltage VIM is output as the negative analog output voltage VOM.

[0059] By performing the first through fourth bit trials with the above-described

on/off operations of the switches, the differential 4-bit DAC 22 outputs the positive analog output voltage VOP and negative analog output voltage VOM with 4-bit resolution.

[0060] The positive analog output voltage VOP and negative analog output voltage VOM output from the differential 4-bit DAC 22 are then compared in the comparator 13. In greater detail, the comparator 13 amplifies and outputs the differential voltage between the positive analog output voltage VOP and the negative analog output voltage VOM. The trial voltage corresponding to the difference between the positive analog output voltage VOP and the negative analog output voltage VOM corresponds to the difference between the differential voltage between the high-voltage reference voltage VRH and the low-voltage reference voltage VRL ($VRH - VRL$) and the differential voltage between the positive analog input voltage VIP and the negative analog input voltage VIM ($VIP - VIM$). The digital signal corresponding to the reference voltage for which this difference is closest to zero is output from the ADC.

[0061] By contrast, the circuit in the differential 4-bit DAC 12 of this embodiment is structured as illustrated in FIG. 7. In the example illustrated in FIG. 7, as in the example illustrated in FIG. 6, the passive components are capacitors and are structured according to a binary system. In greater detail, the positive 3-bit DAC 15 and negative 3-bit DAC 16 each include four capacitors as passive components. The capacitors C_{P11} , C_{P12} , C_{P13} , and C_{P14} in the positive 3-bit DAC 15 respectively have capacitances of C , C , $2C$, and $4C$. The capacitors C_{M11} , C_{M12} , C_{M13} , and C_{M14} in the negative 3-bit DAC 16 respectively have capacitances of C , C , $2C$, and $4C$. The passive components may be structured according to a system other than the binary system. For example, individual passive components may be connected in parallel in a segmented system or may be structured according to any other system. The DAC may also be structured using resistors as the passive components.

[0062] In the positive 3-bit DAC 15, the capacitor C_{P11} is connected to the positive analog input voltage VIP and the low-voltage reference voltage VRL respectively via the switches S_A and S_A' . The capacitor C_{P11} is further connected to the high-voltage reference voltage VRH via a switch S_{HX} . The capacitors C_{P12} , C_{P13} , and C_{P14} are connected in parallel to the positive analog input voltage VIP, the high-voltage reference voltage VRH, and the low-voltage reference voltage VRL. The capacitors C_{P12} , C_{P13} , and C_{P14} are connected to the positive analog input voltage VIP via respective switches S_A . The capacitors C_{P12} , C_{P13} , and C_{P14} are connected to the high-voltage reference voltage VRH respectively via the

switches S_{H0} , S_{H1} , and S_{H2} . The capacitors C_{P12} , C_{P13} , and C_{P14} are connected to the low-voltage reference voltage VRL respectively via the switches S_{L0} , S_{L1} , and S_{L2} . The capacitors C_{P11} , C_{P12} , C_{P13} , and C_{P14} are connected to the input common voltage VCM of the comparator via the switch S_A .

[0063] On the other hand, in the negative 3-bit DAC 16, the capacitor C_{M11} is connected to the negative analog input voltage VIM and the high-voltage reference voltage VRH respectively via the switches S_A and S_A' . The capacitors C_{M12} , C_{M13} , and C_{M14} are connected in parallel to the negative analog input voltage VIM, the high-voltage reference voltage VRH, and the low-voltage reference voltage VRL. The capacitors C_{M12} , C_{M13} , and C_{M14} are connected to the negative analog input voltage VIM via respective switches S_A . The capacitors C_{M12} , C_{M13} , and C_{M14} are connected to the high-voltage reference voltage VRH respectively via the switches S_{L0} , S_{L1} , and S_{L2} . The capacitors C_{M12} , C_{M13} , and C_{M14} are connected to the low-voltage reference voltage VRL respectively via the switches S_{H0} , S_{H1} , and S_{H2} . The capacitors C_{M11} , C_{M12} , C_{M13} , and C_{M14} are connected to the input common voltage VCM of the comparator via the switch S_A .

[0064] In the differential 4-bit DAC 12, switches labeled with the same reference sign perform the same on/off operation, as in the differential 4-bit DAC 22.

[0065] In the differential 4-bit DAC 12 illustrated in FIG. 7, when sampling, the switches S_A in the positive 3-bit DAC 15 and the negative 3-bit DAC 16 are controlled to be on, whereas the other switches are controlled to be off. In other words, by connection of the switches S_A , a charge corresponding to the positive analog input voltage VIP accumulates in all of the capacitors C_{P11} , C_{P12} , C_{P13} , and C_{P14} in the positive 3-bit DAC 15. Furthermore, a charge corresponding to the negative analog input voltage VIM accumulates in all of the capacitors C_{M11} , C_{M12} , C_{M13} , and C_{M14} in the negative 3-bit DAC 16.

[0066] Next, when the differential 4-bit DAC 12 performs the first bit trial, the switches S_A' , S_{L0} , S_{L1} , and S_{H2} are turned on, and the other switches are turned off. By the switches S_A' turning on, the capacitor C_{P11} is connected to the low-voltage reference voltage VRL, and the capacitor C_{M11} is connected to the high-voltage reference voltage VRH. By the switches S_{L0} and S_{L1} turning on, the capacitors C_{P12} and C_{P13} are connected to the low-voltage reference voltage VRL, and the capacitors C_{M12} and C_{M13} are connected to the high-voltage reference voltage VRH. By the switches S_{H2} turning on, the capacitor C_{P14} is connected to the high-voltage reference voltage VRH, and the capacitor C_{M14} is connected to the low-voltage reference voltage VRL. By the switches S_A turning off, the capacitors C_{P11} , C_{P12} ,

C_{P13} , and C_{P14} in the positive 3-bit DAC 15 are disconnected from the positive analog input voltage VIP, and the capacitors C_{M11} , C_{M12} , C_{M13} , and C_{M14} in the negative 3-bit DAC 16 are disconnected from the negative analog input voltage VIM.

[0067] In the first bit trial, the on/off operation of each switch is controlled as described above. As a result, the positive analog output voltage VOP that is output is the difference in potential between the positive analog input voltage VIP and the reference voltage that is determined by the capacitors C_{P11} , C_{P12} , C_{P13} , and C_{P14} and the connection with the high-voltage reference voltage VRH or the low-voltage reference voltage VRL. In this way, the positive 3-bit DAC 15 converts the digital signal input from the decoder 11 (switch control signal) into an analog signal (positive analog output voltage VOP).

[0068] Similarly on the negative side, the negative analog output voltage VOM that is output is the difference in potential between the negative analog input voltage VIM and the reference voltage that is determined by the capacitors C_{M11} , C_{M12} , C_{M13} , and C_{M14} and the connection with the high-voltage reference voltage VRH or the low-voltage reference voltage VRL. In this way, the negative 3-bit DAC 16 converts the digital signal input from the decoder 11 (switch control signal) into an analog signal (negative analog output voltage VOM).

[0069] Next, when the differential 4-bit DAC 12 performs the second bit trial, based on the result of the first bit trial, either the switches S_{H2} are turned on and the switches S_{L2} are turned off, or vice-versa. Furthermore, the switches S_{L1} are turned off, and the switches S_{H1} are turned on. In other words, in the second bit trial, the capacitor C_{P13} is disconnected from the low-voltage reference voltage VRL and is connected to the high-voltage reference voltage VRH. In the second bit trial, the capacitor C_{M13} is disconnected from the high-voltage reference voltage VRH and connected to the low-voltage reference voltage VRL. In the second bit trial as well, as in the first bit trial, the difference in potential between the reference voltage and the positive analog input voltage VIP is output as the positive analog output voltage VOP, and the difference in potential between the reference voltage and the negative analog input voltage VIM is output as the negative analog output voltage VOM.

[0070] Next, when the differential 4-bit DAC 12 performs the third bit trial, based on the result of the second bit trial, either the switches S_{H1} are turned on and the switches S_{L1} are turned off, or vice-versa. Furthermore, the switches S_{L0} are turned off, and the switches S_{H0} are turned on. In other words, in the third bit trial, the

capacitor C_{P12} is disconnected from the low-voltage reference voltage V_{RL} and is connected to the high-voltage reference voltage V_{RH} . In the third bit trial, the capacitor C_{M12} is disconnected from the high-voltage reference voltage V_{RH} and connected to the low-voltage reference voltage V_{RL} . In the third bit trial as well, as in the first bit trial, the difference in potential between the reference voltage and the positive analog input voltage V_{IP} is output as the positive analog output voltage V_{OP} , and the difference in potential between the reference voltage and the negative analog input voltage V_{IM} is output as the negative analog output voltage V_{OM} .

[0071] Finally, the differential 4-bit DAC 12 performs an additional last bit trial. During the last bit trial, based on the result of the third bit trial, either the switches S_{H0} are turned on and the switches S_{L0} are turned off, or vice-versa. Furthermore, in the circuit of the positive 3-bit DAC 15 illustrated in FIG. 7, the switch S_{HX} is turned on. In other words, in the last bit trial, the capacitor C_{P11} is connected to the high-voltage reference voltage V_{RH} . On the other hand, the negative 3-bit DAC 16 does not change from the third bit trial. In this way, since the on/off state of the switches in the negative 3-bit DAC 16 does not change in the last bit trial as compared to the third bit trial, the negative analog output voltage V_{OM} does not change. On the other hand, by the switch S_{HX} in the positive 3-bit DAC 15 turning on, the positive analog output voltage V_{OP} is changed. In this way, by the positive 3-bit DAC 15 and the negative 3-bit DAC 16 operating asymmetrically, in the last bit trial the trial voltage that is the difference between the negative analog output voltage V_{OM} and the positive analog output voltage V_{OP} can be reduced from the trial voltage during the third bit trial, even though 3-bit DACs are used.

[0072] The positive analog output voltage V_{OP} and negative analog output voltage V_{OM} output from the differential 4-bit DAC 12 are then compared in the comparator 13. In greater detail, the comparator 13 amplifies and outputs the trial voltage that is the difference between the positive analog output voltage V_{OP} and the negative analog output voltage V_{OM} . The differential voltage between the positive analog output voltage V_{OP} and the negative analog output voltage V_{OM} corresponds to the difference between the differential voltage between the high-voltage reference voltage V_{RH} and the low-voltage reference voltage V_{RL} ($V_{RH} - V_{RL}$) and the differential voltage between the positive analog input voltage V_{IP} and the negative analog input voltage V_{IM} ($V_{IP} - V_{IM}$). The digital signal corresponding to the reference voltage when this difference is closest to zero is output from the 4-bit successive approximation ADC 10.

[0073] By the differential 4-bit DAC 12 controlling the positive 3-bit DAC 15 and the negative 3-bit DAC 16 asymmetrically during the last bit trial, the 4-bit successive approximation ADC 10 of this embodiment can convert an analog signal into a digital signal with 4-bit resolution. Therefore, as compared to the differential 4-bit DAC 22 that includes the positive 4-bit DAC 25 and the negative 4-bit DAC 26, the differential 4-bit DAC 12 can achieve output as a digital signal with 4-bit resolution using fewer passive components. By reducing the number of components in this way, the 4-bit successive approximation ADC 10 according to this embodiment can reduce manufacturing costs. Furthermore, by reducing the number of components, the time constant during analog-digital conversion is decreased, thereby increasing conversion speed. By reducing the number of components, the power consumption in the 4-bit successive approximation ADC 10 also decreases.

[0074] In this embodiment, a 4-bit successive approximation ADC that outputs a digital signal with 4-bit resolution using 3-bit DACs has been described, but this disclosure is not limited to this embodiment. According to this disclosure, based on the above-described principle, a successive approximation ADC that outputs a digital signal with N-bit resolution (N being an integer greater than or equal to two), i.e. an N-bit successive approximation ADC, can be achieved using (N-1)-bit DACs. In this case, the N-bit successive approximation ADC can output a digital signal with N-bit resolution by controlling a positive (N-1)-bit DAC and a negative (N-1)-bit DAC symmetrically until the (N-1)th bit trial and asymmetrically during the Nth (last) bit trial. In other words, according to this embodiment, in a successive approximation ADC configured using the same number of passive components as a typical successive approximation ADC, one bit can be added to the resolution of the successive approximation ADC by adding one switch.

[0075] FIGS. 8A and 8B illustrate the results of an experiment performed using a 13-bit successive approximation ADC provided with a differential 13-bit DAC configured using 12-bit DACs, illustrating the positive analog output voltage VOP and the negative analog output voltage VOM from the differential 13-bit DAC. As illustrated in FIG. 8A, in the bit trials after sampling, the differential 13-bit DAC outputs the positive analog output voltage VOP and the negative analog output voltage VOM. FIG. 8B is an expanded view of area D in FIG. 8A. As illustrated in FIGS. 8A and 8B, from the first bit trial through the twelfth bit trial, positive analog output voltage VOP and negative analog output voltage VOM that are

symmetrical are output. For the voltage that is output during the thirteenth (last) trial, the negative analog output voltage VOM is the same as the voltage output in the twelfth trial, whereas the positive analog output voltage VOP is higher than the voltage output in the twelfth trial and approaches the negative analog output voltage VOM.

Embodiment 2

[0076] In Embodiment 1, the positive analog input voltage VIP and the negative analog input voltage VIM are described as being differential signals, but the positive analog input voltage VIP and the negative analog input voltage VIM need not be differential signals. The positive analog input voltage VIP and the negative analog input voltage VIM may, for example, be single end signals. An example of the positive analog input voltage VIP and the negative analog input voltage VIM being single end signals is described as Embodiment 2 with comparison to a typical successive approximation ADC.

[0077] FIG. 9 illustrates an example of a typical successive approximation ADC, namely a 2-bit successive approximation ADC that converts an analog signal to a digital signal with 2-bit resolution. The 2-bit successive approximation ADC 30 illustrated in FIG. 9 includes a decoder 31, a differential 2-bit DAC 32, a comparator 33, and a SAR 34. The functions of the decoder 31, differential 2-bit DAC 32, comparator 33, and SAR 34 are similar to those of the decoder 11, differential 4-bit DAC 12, comparator 13, and SAR 14 of Embodiment 1, and therefore a description thereof is omitted. The differential 2-bit DAC 32, however, differs from the differential 4-bit DAC 12 by outputting analog output voltage with 2-bit resolution.

[0078] The SAR 34 generates IN0 and IN1 as control signals for successive approximation processing and outputs the generated control signals for successive approximation processing to the decoder 31. The SAR 34 generates a signal S_A and outputs the generated signal S_A to the differential 2-bit DAC 32. The signal S_A is a signal for performing on/off control of the switches S_A illustrated in FIG. 10.

[0079] Based on the signals IN0 and IN1 input from the SAR 34, the decoder 31 generates signals S_{H0} , S_{H1} , S_{L1} , and S_{L0} and outputs the generated signals to the differential 2-bit DAC 32. The signals S_{H0} , S_{H1} , S_{L1} , and S_{L0} are signals for performing on/off control of the switches S_{H0} , S_{H1} , S_{L1} , and S_{L0} illustrated in FIG. 10.

[0080] The comparison signal output by the comparator 33 is referred to as CMP.

[0081] The signals S_A , S_A' , S_{H0} , S_{H1} , S_{L1} , and S_{L0} are each output as either "1"

indicating "on" or "0" indicating "off". The signals S_A and S_A' perform mutually inverse on/off operations. In other words, when the signal S_A is on, the signal S_A' is off, and when the signal S_A is off, the signal S_A' is on.

[0082] The digital signal output from the 2-bit successive approximation ADC 30 is referred to as D_{out} .

[0083] FIG. 10 illustrates an example of the circuit structure of the differential 2-bit DAC 32 of FIG. 9. As illustrated in FIG. 10, the differential 2-bit DAC 32 includes a positive 2-bit DAC 35 and a negative 2-bit DAC 36. The positive 2-bit DAC 35 and the negative 2-bit DAC 36 each include five capacitors as passive components. The capacitors C_{P21} , C_{P22} , C_{P23} , C_{P24} , and C_{P25} in the positive 2-bit DAC 35 respectively have capacitances of C , C , $2C$, $2C$, and $2C$. The capacitors C_{M21} , C_{M22} , C_{M23} , C_{M24} , and C_{M25} in the negative 2-bit DAC 36 respectively have capacitances of C , C , $2C$, $2C$, and $2C$.

[0084] In the positive 2-bit DAC 35, the capacitor C_{P21} is connected to the positive analog input voltage VIP and the low-voltage reference voltage VRL respectively via the switches S_A and S_A' . The capacitor C_{P22} is connected in parallel to the positive analog input voltage VIP , the high-voltage reference voltage VRH , and the low-voltage reference voltage VRL respectively via the switches S_A , S_{H0} , and S_{L0} . The capacitor C_{P23} is connected in parallel to the positive analog input voltage VIP , the high-voltage reference voltage VRH , and the low-voltage reference voltage VRL respectively via the switches S_A , S_{H1} , and S_{L1} .

[0085] The capacitors C_{P24} and C_{P25} are connected to the positive analog input voltage VIP via respective switches S_A . The capacitor C_{P24} is connected to the high-voltage reference voltage VRH via the switch S_A' , and the capacitor C_{P25} is connected to the low-voltage reference voltage VRL via the switch S_A' . The capacitors C_{P21} , C_{P22} , C_{P23} , C_{P24} , and C_{P25} are connected to a fixed voltage via the switch S_A . The common voltage of the comparator input is fixed at $VRH/2$.

[0086] In the negative 2-bit DAC 36, the capacitor C_{M21} is connected to the negative analog input voltage VIM and the high-voltage reference voltage VRH respectively via the switches S_A and S_A' . The capacitor C_{M22} is connected in parallel to the negative analog input voltage VIM , the low-voltage reference voltage VRL , and the high-voltage reference voltage VRH respectively via the switches S_A , S_{H0} , and S_{L0} . The capacitor C_{M23} is connected in parallel to the negative analog input voltage VIM , the low-voltage reference voltage VRL , and the high-voltage reference voltage VRH respectively via the switches S_A , S_{H1} , and

S_{L1} .

[0087] The capacitors C_{M24} and C_{M25} are connected to the negative analog input voltage VIM via respective switches S_A . The capacitor C_{M24} is connected to the low-voltage reference voltage VRL via the switch $S_{A'}$, and the capacitor C_{M25} is connected to the high-voltage reference voltage VRH via the switch $S_{A'}$. The capacitors C_{M21} , C_{M22} , C_{M23} , C_{M24} , and C_{M25} are connected to the fixed voltage $VRH/2$ via the switch S_A .

[0088] In the differential 2-bit DAC 32, the capacitors C_{P24} , C_{P25} , C_{M24} , and C_{M25} are provided in order to match the differential voltage between the positive analog input voltage VIP and the negative analog input voltage VIM, which are single end signals, to the differential voltage between the high-voltage reference voltage VRH and the low-voltage reference voltage VRL. In other words, with the capacitors C_{P24} , C_{P25} , C_{M24} , and C_{M25} , even when the input voltage is a single end signal, the differential voltage between the positive analog input voltage VIP and the negative analog input voltage VIM becomes the same differential voltage as when the input voltage is a differential signal. Therefore, the resolution in the differential 2-bit DAC 32 can be maintained without any reduction.

[0089] Next, with reference to FIGS. 11 and 12, an example of each signal and of digital output in the 2-bit successive approximation ADC 30 is described. In FIGS. 11 and 12, the logic level of the signals IN0, IN1, and CMP is indicated as "0" or "1".

[0090] FIG. 11 illustrates signals input into the differential 2-bit DAC 32 of FIG. 9. In FIG. 11, the on/off states of the signals S_A , IN1, IN0, S_{H1} , S_{H0} , S_{L1} , and S_{L0} in the sampling phase and the trial phase are indicated in table form. As illustrated in FIG. 11, in the sampling phase, only the signal S_A is on, i.e. the switches S_A in FIG. 10 are on. As a result, a charge corresponding to the positive analog input voltage VIP accumulates in the capacitors C_{P21} , C_{P22} , C_{P23} , C_{P24} , and C_{P25} of the positive 2-bit DAC 35, and a charge corresponding to the negative analog input voltage VIM accumulates in the capacitors C_{M21} , C_{M22} , C_{M23} , C_{M24} , and C_{M25} of the negative 2-bit DAC 36. In the trial phase, the signals S_{L1} and S_{L0} are controlled to be on/off inversely from the signals S_{H1} and S_{H0} respectively. Therefore, the switches S_{L1} and S_{L0} are controlled to be on/off inversely from the switches S_{H1} and S_{H0} respectively.

[0091] As can be seen from FIGS. 10 and 11, the positive 2-bit DAC 35 and negative 2-bit DAC 36 are controlled symmetrically by respectively inputting the same signals S_{H1} , S_{H0} , S_{L1} , and S_{L0} .

[0092] FIG. 12 illustrates an example of digital output by the successive approximation ADC 30 of FIG. 9. In this case, as an example of single end signals, FIG. 12 illustrates the digital output D_{out} that is output in accordance with the value of the positive analog input voltage VIP when the high-voltage reference voltage VRH is 8 V, the low-voltage reference voltage VRL is 0 V, and the negative analog input voltage VIM is fixed at $VRH/2$. FIG. 12 illustrates the results for when the value of the positive analog input voltage VIP is 1 V, 3 V, 5 V, and 7 V.

[0093] In FIG. 12, the positive analog output voltage VOP and the negative analog output voltage VOM are calculated by Equations (1) and (2) below, which are derived from the law of conservation of charge.

$$VOP = VRH/2 - VIP + (1/8)*VRH*(2*S_{H1} + S_{H0} + 2) \quad (1)$$

$$VOM = VRH/2 - VIM + (1/8)*VRH*(2*S_{L1} + S_{L0} + 2) \quad (2)$$

[0094] In FIG. 12, the signals $D1$ and $D0$ are the comparison signal CMP in the first bit trial and the second bit trial respectively.

[0095] As illustrated in FIG. 12, when the positive analog input voltage VIP is 1 V, 3 V, 5 V, and 7 V, then based on the signals $D1$ and $D0$ output by the first bit trial and the second bit trial, D_{out} takes the values of 0, 1, 2, and 3 respectively. In this way, the 2-bit successive approximation ADC 30 converts an analog signal to 2-bit digital output.

[0096] FIG. 13 is a functional block diagram illustrating an example of a 3-bit successive approximation ADC according to Embodiment 2. A 3-bit successive approximation ADC 40 includes a decoder 41, a differential 3-bit DAC 42, a comparator 43, and a SAR 44 and operates with single end signals. The functions of the decoder 41, differential 3-bit DAC 42, comparator 43, and SAR 44 are similar to those of the decoder 11, differential 4-bit DAC 12, comparator 13, and SAR 14 of Embodiment 1, and therefore a description thereof is omitted. The differential 3-bit DAC 42, however, differs from the differential 4-bit DAC 12 by outputting analog output voltage with 3-bit resolution.

[0097] In addition to the control signals for successive approximation processing $IN0$ and $IN1$ and the signal S_A described in the SAR 34, the SAR 44 outputs a signal CTL . The signal CTL is an input signal for controlling the positive 3-bit DAC and the negative 3-bit DAC asymmetrically during the last bit trial. Accordingly, when performing the last bit trial, the signal CTL is output from the SAR 44 to the decoder 41.

[0098] Based on the signals $IN0$, $IN1$, and CTL input from the SAR 44, the

decoder 41 generates signals S_{HP1} , S_{HP0} , S_{HPC} , S_{LP1} , S_{LP0} , S_{LPC} , S_{HM1} , S_{HM0} , S_{LM1} , and S_{LM0} and outputs the generated signals to the differential 3-bit DAC 42. The signals S_{HP1} , S_{HP0} , S_{HPC} , S_{LP1} , S_{LP0} , S_{LPC} , S_{HM1} , S_{HM0} , S_{LM1} , and S_{LM0} are signals for performing on/off control of the respective switches S_{HP1} , S_{HP0} , S_{HPC} , S_{LP1} , S_{LP0} , S_{LPC} , S_{HM1} , S_{HM0} , S_{LM1} , and S_{LM0} illustrated in FIG. 14.

[0099] The signals S_A , $S_{A'}$, S_{HP1} , S_{HP0} , S_{HPC} , S_{LP1} , S_{LP0} , S_{LPC} , S_{HM1} , S_{HM0} , S_{LM1} , and S_{LM0} are each output as either "1" indicating "on" or "0" indicating "off". The signals S_A and $S_{A'}$ perform mutually inverse on/off control. The digital signal output from the 3-bit successive approximation ADC 40 is referred to as D_{out} .

[0100] FIG. 14 illustrates an example of the circuit structure of the differential 3-bit DAC 42 of FIG. 13. As illustrated in FIG. 14, the differential 3-bit DAC 42 includes a positive 3-bit DAC 45 and a negative 3-bit DAC 46. The positive 3-bit DAC 45 and the negative 3-bit DAC 46 each include five capacitors as passive components. In other words, the positive 3-bit DAC 45 and the negative 3-bit DAC 46 in this embodiment are structured with the same number of passive components as the positive 2-bit DAC 35 and negative 2-bit DAC 36 illustrated in FIG. 10.

[0101] In FIG. 14, the capacitors C_{P31} , C_{P32} , C_{P33} , C_{P34} , and C_{P35} in the positive 3-bit DAC 45 respectively have capacitances of C , C , $2C$, $2C$, and $2C$. The capacitors C_{M31} , C_{M32} , C_{M33} , C_{M34} , and C_{M35} in the negative 3-bit DAC 46 respectively have capacitances of C , C , $2C$, $2C$, and $2C$.

[0102] In the positive 3-bit DAC 45, the capacitor C_{P31} is connected to the positive analog input voltage V_{IP} and the low-voltage reference voltage V_{RL} respectively via the switches S_A and S_{LPC} . The capacitor C_{P31} is further connected to the high-voltage reference voltage V_{RH} via the switch S_{HPC} . The capacitor C_{P32} is connected in parallel to the positive analog input voltage V_{IP} , the high-voltage reference voltage V_{RH} , and the low-voltage reference voltage V_{RL} respectively via the switches S_A , S_{HP0} , and S_{LP0} . The capacitor C_{P33} is connected in parallel to the positive analog input voltage V_{IP} , the high-voltage reference voltage V_{RH} , and the low-voltage reference voltage V_{RL} respectively via the switches S_A , S_{HP1} , and S_{LP1} .

[0103] The capacitors C_{P34} and C_{P35} are connected to the positive analog input voltage V_{IP} via respective switches S_A . The capacitor C_{P34} is connected to the high-voltage reference voltage V_{RH} via the switch $S_{A'}$, and the capacitor C_{P35} is connected to the low-voltage reference voltage V_{RL} via the switch $S_{A'}$. The capacitors C_{P31} , C_{P32} , C_{P33} , C_{P34} , and C_{P35} are connected to a common voltage of the comparator input via the switch S_A . The common voltage is fixed at $V_{RH}/2$.

[0104] In the negative 3-bit DAC 46, the capacitor C_{M31} is connected to the negative analog input voltage V_{IM} and the high-voltage reference voltage VRH respectively via the switches S_A and $S_{A'}$. The capacitor C_{M32} is connected in parallel to the negative analog input voltage V_{IM} , the low-voltage reference voltage VRL , and the high-voltage reference voltage VRH respectively via the switches S_A , S_{HM0} , and S_{LM0} . The capacitor C_{M33} is connected in parallel to the negative analog input voltage V_{IM} , the low-voltage reference voltage VRL , and the high-voltage reference voltage VRH respectively via the switches S_A , S_{HM1} , and S_{LM1} .

[0105] The capacitors C_{M34} and C_{M35} are connected to the negative analog input voltage V_{IM} via respective switches S_A . The capacitor C_{M34} is connected to the low-voltage reference voltage VRL via the switch $S_{A'}$, and the capacitor C_{M35} is connected to the high-voltage reference voltage VRH via the switch $S_{A'}$. The capacitors C_{M31} , C_{M32} , C_{M33} , C_{M34} , and C_{M35} are connected to the fixed voltage $VRH/2$ via the switch S_A .

[0106] In the differential 3-bit DAC 42, the capacitors C_{P34} , C_{P35} , C_{M34} , and C_{M35} are provided in order to match the differential voltage between the positive analog input voltage V_{IP} and the negative analog input voltage V_{IM} , which are single end signals, to the differential voltage between the high-voltage reference voltage VRH and the low-voltage reference voltage VRL . In other words, with the capacitors C_{P34} , C_{P35} , C_{M34} , and C_{M35} , even when the input voltage is a single end signal, the differential voltage between the positive analog input voltage V_{IP} and the negative analog input voltage V_{IM} becomes the same differential voltage as when the input voltage is a differential signal. Therefore, the resolution in the differential 3-bit DAC 42 can be maintained without any reduction.

[0107] Next, with reference to FIGS. 15 and 16, an example of each signal and of digital output in the 3-bit successive approximation ADC 40 is described. In FIGS. 15 and 16, the logic level of the signals $IN0$, $IN1$, and CMP is indicated as "0" or "1".

[0108] FIG. 15 illustrates signals input into the differential 3-bit DAC 42 of FIG. 13. In FIG. 15, the on/off states of the signals S_A , $IN1$, $IN0$, CTL , S_{HP1} , S_{HP0} , S_{HPC} , S_{LP1} , S_{LP0} , S_{LPC} , S_{HM1} , S_{HM0} , S_{LM1} , and S_{LM0} in the sampling phase and the trial phase are indicated in table form. As illustrated in FIG. 15, in the sampling phase, only the signal S_A is on, i.e. the switches S_A in FIG. 14 are on. As a result, a charge corresponding to the positive analog input voltage V_{IP} accumulates in the capacitors C_{P31} , C_{P32} , C_{P33} , C_{P34} , and C_{P35} of the positive 3-bit DAC 45, and a

charge corresponding to the negative analog input voltage VIM accumulates in the capacitors C_{M31} , C_{M32} , C_{M33} , C_{M34} , and C_{M35} of the negative 3-bit DAC 46. In the trial phase, the signals S_{LP1} , S_{LP0} , S_{LPC} , S_{LM1} , and S_{LM0} are controlled to be on/off inversely from the signals S_{HP1} , S_{HP0} , S_{HPC} , S_{HM1} , and S_{HM0} respectively. Therefore, the switches S_{LP1} , S_{LP0} , S_{LPC} , S_{LM1} , and S_{LM0} are controlled to be on/off inversely from the switches S_{HP1} , S_{HP0} , S_{HPC} , S_{HM1} , and S_{HM0} respectively.

[0109] As can be seen from FIGS. 14 and 15, in the differential 3-bit DAC 42, unlike the differential 2-bit DAC 32 described in FIGS. 10 and 11, different signals S_{HP1} , S_{HP0} , S_{HPC} , S_{LP1} , S_{LP0} , S_{LPC} , S_{HM1} , S_{HM0} , S_{LM1} , and S_{LM0} are input into the positive 3-bit DAC 45 and negative 3-bit DAC 46. As a result, the positive 3-bit DAC 45 and negative 3-bit DAC 46 are controlled individually.

[0110] As can be seen from FIG. 15, in the case that the signals IN1 and IN0 are both "0", if the signal CTL is "0", then the signals S_{HP1} and S_{HP0} are both "0", whereas if the signal CTL is "1", then the signal S_{HP1} is "0" and the signal S_{HP0} is "1". In the case that the signal IN1 is "0" and the signal IN0 is "1", if the signal CTL is "0", then the signal S_{HP1} is "0" and the signal S_{HP0} is "1", whereas if the signal CTL is "1", then the signal S_{HP1} is "1" and the signal S_{HP0} is "0". In the case that the signal IN1 is "1" and the signal IN0 is "0", if the signal CTL is "0", then the signal S_{HP1} is "1" and the signal S_{HP0} is "0", whereas if the signal CTL is "1", then the signal S_{HP1} and the signal S_{HP0} are both "1". In the case that the signals IN1 and IN0 are both "1", the signals S_{HP1} and S_{HP0} are both "1". However, if the signal CTL is "0", then the signal S_{HPC} is "0", whereas if the signal CTL is "1", then the signal S_{HPC} is "1".

[0111] FIG. 16 illustrates an example of digital output by the successive approximation ADC 40 of FIG. 13. Here, it is assumed that the high-voltage reference voltage VRH is 8 V and the low-voltage reference voltage VRL is 0 V. FIG. 16 illustrates the digital output D_{out} that is output in accordance with the value of the positive analog input voltage VIP in the case that the negative analog input voltage VIM is a fixed value. In this case, FIG. 16 illustrates the results for when the negative analog input voltage VIM is VRH/2. FIG. 16 also illustrates the results for when voltages in 1 V increments from 0.5 V to 7.5 V are input as the value of the positive analog input voltage VIP.

[0112] In FIG. 16, the positive analog output voltage VOP and the negative analog output voltage VOM are calculated by Equations (3) and (4) below, which are derived from the law of conservation of charge.

$$VOP = VRH/2 - VIP + (1/8)*VRH*(2*S_{HP1} + S_{HP0} + S_{HPC} + 2) \quad (3)$$

$$VOM = VRH/2 - VIM + (1/8)*VRH*(2*S_{LM1} + S_{LM0} + 2) \quad (4)$$

[0113] In FIG. 16, the signals D2, D1, and D0 are the comparison signal CMP in the first bit trial, second bit trial, and last bit trial respectively. In the last bit trial, the signal CTL is "1".

[0114] As illustrated in FIG. 16, D_{out} is output at eight levels from 0 to 7 based on the signals D2, D1, and D0 output by the first bit trial, second bit trial, and last bit trial in accordance with the value of the positive analog input voltage VIP. In this way, as compared to the 2-bit successive approximation ADC 30, the 3-bit successive approximation ADC 40 can increase resolution by one bit with a simple structure that only adds one switch S_{HPC}, without increasing the number of passive components.

Embodiment 3

[0115] While the differential DACs in Embodiment 1 and Embodiment 2 (differential 4-bit DAC 12 and differential 3-bit DAC 32) have been described as including capacitors as passive components, the passive components in the differential DAC are not limited to capacitors. The passive components in the differential DAC may be configured using resistors. The passive components in the differential DAC may also be configured using a combination of resistors and capacitors. An example of configuring a differential DAC using a combination of resistors and capacitors is described as Embodiment 3.

[0116] FIG. 17 illustrates an example of a successive approximation ADC related to this embodiment, namely a 3-bit successive approximation ADC that includes differential 3-bit DACs configured using a combination of resistors and capacitors as passive components. The 3-bit successive approximation ADC 50 illustrated in FIG. 17 includes a decoder 51, a differential 3-bit DAC 52, a comparator 53, and a SAR 54. The functions of the decoder 51, comparator 53, and SAR 54 are similar to those of the decoder 11, comparator 13, and SAR 14 of Embodiment 1, and therefore a description thereof is omitted.

[0117] As illustrated in FIG. 17, the differential 3-bit DAC 52 includes a 1-bit capacitive DAC 55 and a 2-bit resistive DAC 56. The differential 3-bit DAC 52 outputs analog output voltage with a total of 3-bit resolution using the 1-bit capacitive DAC 55 and the 2-bit resistive DAC 56.

[0118] The SAR 54 generates IN0, IN1, and IN2 as control signals for successive approximation processing and outputs the generated control signals for successive approximation processing to the decoder 51. The SAR 54 generates a signal S_A and outputs the generated signal S_A to the differential 3-bit DAC 52.

[0119] Based on the signals IN0, IN1, and IN2 input from the SAR 54, the decoder 51 generates signals S_H and S_L , outputting the generated signals S_H and S_L to the 1-bit capacitive DAC 55, and also generates signals S_{R0} , S_{R1} , S_{R2} , and S_{R3} , outputting the generated signals S_{R0} , S_{R1} , S_{R2} , and S_{R3} to the 2-bit resistive DAC 56. The signals S_H , S_L , S_{R0} , S_{R1} , S_{R2} , and S_{R3} are signals for performing on/off control of the respective switches S_H , S_L , S_{R0} , S_{R1} , S_{R2} , and S_{R3} illustrated in FIG. 18. The signals S_H , S_L , S_{R0} , S_{R1} , S_{R2} , and S_{R3} are each output as either "1" indicating "on" or "0" indicating "off".

[0120] FIG. 18 illustrates an example of the circuit structure of the differential 3-bit DAC 52 of FIG. 17. As illustrated in FIG. 18, the 2-bit resistive DAC 56 includes a resistor string 57 with four resistors R connected in series as passive components. The high-voltage reference voltage VRH is supplied from one end 57a of the resistor string 57, and the low-voltage reference voltage VRL is supplied from the other end 57b. The voltage between resistors R is set to V3, V2, and V1 in order from the end 57a at which the high-voltage reference voltage VRH is supplied.

[0121] In the resistor string 57, a switch S_{R0} is connected to the end 57a, and in order from the end 57a, switches S_{R1} , S_{R2} , and S_{R3} are connected between the resistors R. In other words, in the resistor string 57, the switch S_{R1} is connected to the node of the voltage V3, the switch S_{R2} is connected to the node of the voltage V2, and the switch S_{R3} is connected to the node of the voltage V1. These switches S_{R0} , S_{R1} , S_{R2} , and S_{R3} are connected in parallel, and a negative reference voltage VRM is output from the other side of these switches that is not connected to the resistor string 57.

[0122] In the resistor string 57, a switch S_{R0} is connected to the other end 57b, and in order from the other end 57b, switches S_{R1} , S_{R2} , and S_{R3} are connected between the resistors R. In other words, in the resistor string 57, the switch S_{R1} is connected to the node of the voltage V1, the switch S_{R2} is connected to the node of the voltage V2, and the switch S_{R3} is connected to the node of the voltage V3. These switches S_{R0} , S_{R1} , S_{R2} , and S_{R3} are connected in parallel, and a positive reference voltage VRP is output from the other side of these switches that is not connected to the resistor string 57.

[0123] The 1-bit capacitive DAC 55 includes a positive 1-bit DAC 58 and a negative 1-bit DAC 59. The positive 1-bit DAC 58 and the negative 1-bit DAC 59 each include four capacitors as passive components. For example, the capacitors C_{P41} , C_{P42} , C_{P43} , and C_{P44} are disposed in the positive 1-bit DAC 58, and the

capacitors C_{M41} , C_{M42} , C_{M43} , and C_{M44} are disposed in the negative 1-bit DAC 59.

[0124] In the positive 1-bit DAC 58, the capacitor C_{P41} is connected to the positive analog input voltage VIP via the switch S_A . The capacitor C_{P41} is also connected to the positive reference voltage VRP output by the 2-bit resistive DAC 56 via the switch $S_{A'}$. The capacitor C_{P42} is connected to the positive analog input voltage VIP, the high-voltage reference voltage VRH, and the low-voltage reference voltage VRL respectively via the switches S_A , S_H , and S_L .

[0125] The capacitors C_{P43} and C_{P44} are connected to the positive analog input voltage VIP via respective switches S_A . The capacitor C_{P43} is connected to the high-voltage reference voltage VRH via the switch $S_{A'}$, and the capacitor C_{P44} is connected to the low-voltage reference voltage VRL via the switch $S_{A'}$. The capacitors C_{P41} , C_{P42} , C_{P43} , and C_{P44} are connected to the output voltage V2 of the 2-bit resistive DAC 56 via the switch S_A .

[0126] In the negative 1-bit DAC 59, the capacitor C_{M41} is connected to the negative analog input voltage VIM via the switch S_A . The capacitor C_{M41} is also connected to the negative reference voltage VRM output by the 2-bit resistive DAC 56 via the switch $S_{A'}$. The capacitor C_{M42} is connected to the negative analog input voltage VIM, the low-voltage reference voltage VRL, and the high-voltage reference voltage VRH respectively via the switches S_A , S_H , and S_L .

[0127] The capacitors C_{M43} and C_{M44} are connected to the negative analog input voltage VIM via respective switches S_A . The capacitor C_{M43} is connected to the high-voltage reference voltage VRH via the switch $S_{A'}$, and the capacitor C_{M44} is connected to the low-voltage reference voltage VRL via the switch $S_{A'}$. The capacitors C_{M41} , C_{M42} , C_{M43} , and C_{M44} are connected to the node of the output voltage V2 of the 2-bit resistive DAC 56 via the switch S_A .

[0128] In the differential 3-bit DAC 52, the capacitors C_{P43} , C_{P44} , C_{M43} , and C_{M44} are provided in order to match the differential voltage between the positive analog input voltage VIP and the negative analog input voltage VIM, which are single end signals, to the differential voltage between the high-voltage reference voltage VRH and the low-voltage reference voltage VRL. In other words, with the capacitors C_{P43} , C_{P44} , C_{M43} , and C_{M44} , even when the input voltage is a single end signal, the differential voltage between the positive analog input voltage VIP and the negative analog input voltage VIM becomes the same differential voltage as when the input voltage is a differential signal. Therefore, the resolution in the differential 3-bit DAC 52 can be maintained without any reduction.

[0129] In the differential 3-bit DAC 52, the switches are controlled based on the

signals input from the decoder 51, and the positive analog output voltage VOP and negative analog output voltage VOM with a total of 3-bit resolution are output.

[0130] The differential 3-bit DAC 52 uses the same signals S_{R0} , S_{R1} , S_{R2} , and S_{R3} to control the circuit that outputs the positive reference voltage VRP and the negative reference voltage VRM. Therefore, synchronous control is executed in these circuits.

[0131] FIG. 19 is a functional block diagram illustrating an example of a 4-bit successive approximation ADC according to Embodiment 3. The 4-bit successive approximation ADC 60 illustrated in FIG. 19 includes a decoder 61, a differential 4-bit DAC 62, a comparator 63, and a SAR 64. The functions of the decoder 61, comparator 63, and SAR 64 are similar to those of the decoder 11, comparator 13, and SAR 14 of Embodiment 1, and therefore a description thereof is omitted.

[0132] As illustrated in FIG. 19, the differential 4-bit DAC 62 includes a 1-bit capacitive DAC 65 and a 3-bit resistive DAC 66. The differential 4-bit DAC 62 outputs analog output voltage with a total of 4-bit resolution using the 1-bit capacitive DAC 65 and the 3-bit resistive DAC 66.

[0133] The SAR 64 generates IN0, IN1, and IN2 as control signals for successive approximation processing and outputs the generated control signals for successive approximation processing to the decoder 61. The SAR 64 generates a signal S_A and outputs the generated signal S_A to the differential 4-bit DAC 62. The SAR 64 also generates an input signal CTL for executing asynchronous control in the last bit trial and outputs the signal CTL to the decoder 61.

[0134] Based on the signals IN0, IN1, and IN2 input from the SAR 64, the decoder 61 generates signals S_H and S_L , outputting the generated signals S_H and S_L to the 1-bit capacitive DAC 55, and also generates signals S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , S_{RP4} , S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} , outputting the generated signals S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , S_{RP4} , S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} to the 3-bit resistive DAC 66. The signals S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , S_{RP4} , S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} are signals for performing on/off control of the respective switches S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , S_{RP4} , S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} illustrated in FIG. 20. The signals S_H , S_L , S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , S_{RP4} , S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} are each output as either "1" indicating "on" or "0" indicating "off".

[0135] FIG. 20 illustrates an example of the circuit structure of the differential 4-bit DAC 62 of FIG. 19. As illustrated in FIG. 20, the 3-bit resistive DAC 66 includes a resistor string 67 with four resistors R connected in series as passive components. The high-voltage reference voltage VRH is supplied from one end

67a of the resistor string 67, and the low-voltage reference voltage VRL is supplied from the other end 67b. The voltage between resistors R is set to V3, V2, and V1 in order from the end 67a at which the high-voltage reference voltage VRH is supplied.

[0136] In the resistor string 67, a switch S_{RM0} is connected to the end 67a, and in order from the end 67a, switches S_{RM1} , S_{RM2} , and S_{RM3} are connected between the resistors R. In other words, in the resistor string 67, the switch S_{RM1} is connected to the node of the voltage V3, the switch S_{RM2} is connected to the node of the voltage V2, and the switch S_{RM3} is connected to the node of the voltage V1. These switches S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} are connected in parallel, and a negative reference voltage VRM is output from the other side of these switches that is not connected to the resistor string 67.

[0137] In the resistor string 67, a switch S_{RP0} is connected to the other end 67b, and in order from the other end 67b, switches S_{RP1} , S_{RP2} , S_{RP3} , and S_{RP4} are connected between the resistors R. In other words, in the resistor string 67, the switch S_{RP1} is connected to the node of the voltage V1, the switch S_{RP2} is connected to the node of the voltage V2, the switch S_{RP3} is connected to the node of the voltage V3, and the switch S_{RP4} is connected to the node of the high-voltage reference voltage VRH. These switches S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , and S_{RP4} are connected in parallel, and a positive reference voltage VRP is output from the other side of these switches that is not connected to the resistor string 67.

[0138] The 1-bit capacitive DAC 65 includes a positive 1-bit DAC 68 and a negative 1-bit DAC 69. The structure of the 1-bit capacitive DAC 65 is similar to that of the above-described 1-bit capacitive DAC 55, and therefore a description thereof is omitted.

[0139] Next, with reference to FIGS. 21 to 24, an example of each signal and of digital output in the 4-bit successive approximation ADC 60 is described.

[0140] FIG. 21 illustrates signals input into the 1-bit capacitive DAC 65 of FIG. 19. In FIG. 21, the on/off states of the signals S_A , S_H , and S_L and the logic level of the signal IN2 in the sampling phase and the trial phase are indicated in table form. As illustrated in FIG. 21, in the sampling phase, the signal S_A is on, i.e. the switches S_A in FIG. 20 are on. As a result, a charge corresponding to the positive analog input voltage VIP accumulates in the capacitors C_{P51} , C_{P52} , C_{P53} , and C_{P54} of the positive 1-bit DAC 68, and a charge corresponding to the negative analog input voltage VIM accumulates in the capacitors C_{M51} , C_{M52} , C_{M53} , and C_{M54} of the negative 1-bit DAC 69.

[0141] FIG. 22 illustrates signals input to and output from the 3-bit resistive DAC of FIG. 19. Here, it is assumed that the high-voltage reference voltage VRH is 16 V, the low-voltage reference voltage VRL is 0 V, the voltage $V3$ is 12 V, the voltage $V2$ is 8 V, and the voltage $V1$ is 4 V. In FIG. 22, the signals $IN1$, $IN0$, and CTL input into the decoder 61, the signals S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , S_{RP4} , S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} output by the decoder 61 to the 3-bit resistive DAC 66 based on the signals $IN1$, $IN0$, and CTL , and the positive reference voltage VRP and negative reference voltage VRM output by the 3-bit resistive DAC 66 are indicated in table form.

[0142] As illustrated in FIG. 22, the signals S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} do not change regardless of whether the signal CTL is "0" or "1". Therefore, the switches S_{RM0} , S_{RM1} , S_{RM2} , and S_{RM3} perform the same on/off operations, regardless of whether the last bit trial is being performed. Conversely, when the signal CTL is "1", the on/off state of the signals S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , and S_{RP4} changes as compared to when the signal CTL is "0". Therefore, the on/off operations of the switches S_{RP0} , S_{RP1} , S_{RP2} , S_{RP3} , and S_{RP4} change between when the signal CTL is "1" and when the signal CTL is "0". In this way, the 3-bit resistive DAC 66 achieves asymmetrical control during the last bit test.

[0143] By performing asymmetrical control, the 3-bit resistive DAC 66 can output the positive reference voltage VRP and the negative reference voltage VRM with 3-bit resolution. In this way, the differential 4-bit DAC 62 outputs analog voltage with 4-bit resolution.

[0144] FIG. 23 illustrates an example of digital output by the successive approximation ADC 60 of FIG. 19. FIG. 23 illustrates the digital output D_{out} in the case of a single end signal being input into the differential 4-bit DAC 62. In other words, the negative analog input voltage VIM is $V2$ (8 V). FIG. 23 illustrates the results for when voltages in 1 V increments from 0.5 V to 15.5 V are input as the value of the positive analog input voltage VIP .

[0145] In FIG. 23, the positive analog output voltage VOP and the negative analog output voltage VOM are calculated by Equations (5) and (6) below, which are derived from the law of conservation of charge.

$$VOP = VRH/2 - VIP + (1/4)*(VRP + VRH*(S_H+1)) \quad (5)$$

$$VOM = VRH/2 - VIM + (1/4)*(VRM + VRH*(S_L+1)) \quad (6)$$

[0146] In FIG. 23, the signals $D3$, $D2$, $D1$, and $D0$ are the comparison signal CMP in the first bit trial, second bit trial, third bit trial, and last bit trial respectively. In the last bit trial, the signal CTL is "1".

[0147] FIG. 24 illustrates another example of digital output by the successive approximation ADC 60 of FIG. 19. FIG. 24 illustrates the digital output D_{out} in the case of a differential signal being input into the differential 4-bit DAC 62. Letting the difference between the positive analog input voltage V_{IP} and the negative analog input voltage V_{IM} be ΔV_I , FIG. 23 illustrates the results for when voltages in 1 V increments from -7.5 V to 7.5 V are input as ΔV_I .

[0148] As illustrated in FIGS. 23 and 24, D_{out} is output at 16 levels from 0 to 15 based on the signals D_3 , D_2 , D_1 , and D_0 output by the first bit trial, second bit trial, third bit trial, and last bit trial. In this way, as compared to the 3-bit successive approximation ADC 50, the 4-bit successive approximation ADC 60 can increase resolution by one bit with a simple structure that only adds one switch S_{RP4} , without increasing the number of passive components.

[0149] Although embodiments have been described based on examples and on the accompanying drawings, it is to be noted that various changes and modifications will be apparent to those skilled in the art based on this disclosure. Therefore, such changes and modifications are to be understood as included within the scope of this disclosure. For example, the functions and the like included in the components may be reordered in any logically coherent way. Furthermore, units, steps, and the like may be combined into one or divided, and/or additional units, steps and the like may be used within the scope of this disclosure.

[0150] For example, whereas only the positive side is controlled in the last bit trial in the above embodiments, control of the last bit trial is not limited in this way. For example, the effects of this disclosure can be obtained by controlling only the negative side in the last bit trial. In another example, the effects of this disclosure may be obtained by alternating control between the positive side and the negative side of the last bit trial in different/subsequent conversion operations, where such alternating control may be based on a bit (e.g., stored in a register) that is set by an outside control signal provided to the SAR.

[0151] For example, in Embodiments 1 to 3, a successive approximation ADC that includes a differential DAC (differential 4-bit DAC 12, differential 3-bit DAC 42, and differential 4-bit DAC 62) and a comparator (comparator 13, 43, and 63) has been described, but this disclosure is not limited to these examples. For example, instead of the differential DAC and comparator, this disclosure may be applied to a configuration with a parallel (flash) ADC that includes a differential comparator circuit.

[0152] FIG. 25 illustrates an example of the circuit structure of a differential comparator circuit provided in a flash ADC according to this disclosure. The differential comparator circuit includes a capacitor C_P connected to the positive input terminal and a capacitor C_M connected to the negative input terminal of a comparator 73. An input common voltage V_{CM} is connected to the positive and negative input terminals of the comparator 73 via respective switches S_A .

[0153] The capacitor C_P is connected to a positive analog input voltage V_{IP} and a positive reference voltage V_{RP} respectively via the switches S_A and S_R . The capacitor C_M is connected to a negative analog input voltage V_{IM} , a first negative reference voltage V_{RM1} , and a second negative reference voltage V_{RM2} respectively via the switches S_A , S_{R1} , and S_{R2} . These switches S_A , S_R , S_{R1} , and S_{R2} are controlled to be on/off based on signals provided from the decoder. By including a plurality (for example, 2^N (N being an integer greater than or equal to one)) of the differential comparator circuits illustrated in FIG. 25 the flash ADC according to this disclosure converts an analog signal into a digital signal with $(N+1)$ -bit resolution.

[0154] FIG. 26 illustrates an example of the control state of each switch in the differential comparator circuit illustrated in FIG. 25. In FIG. 26, the "on" and "off" states of each switch are illustrated respectively as "1" and "0". The differential comparator circuit performs analog-digital conversion in three steps: sampling, coarse control, and fine control.

[0155] As illustrated in FIG. 26, during sampling, the switches S_A are on, and a charge accumulates in the capacitors C_P and C_M . Next, during coarse ADC processing, the switch S_R on the positive side and the switch S_{R1} on the negative side turn on. During fine ADC processing, the switch S_R on the positive side remains on, while on the negative side, the switch S_{R1} turns off, and the switch S_{R2} turns on. In other words, in the coarse ADC processing and fine ADC processing, only the reference voltage supplied to the capacitor C_M on the negative side changes. In a typical differential comparator circuit, as compared to the differential comparator circuit illustrated in FIG. 25, since there is only one input of reference voltage on the negative side, symmetrical control is performed on the positive side and the negative side during ADC processing. By contrast, asymmetrical control is performed as described above in the differential comparator circuit provided with the flash ADC according to this disclosure.

[0156] FIG. 27 illustrates an example of digital output by a 3-bit parallel ADC that includes four of the differential comparator circuits illustrated in FIG. 25. FIG. 27

illustrates an example of the case in which the difference in potential between the positive reference voltage VRP and the first negative reference voltage VRM1 is 8 V. In the 3-bit parallel ADC, coarse 2-bit ADC processing executed when the switch S_{R1} is on and fine 1-bit ADC processing executed when the switch S_{R2} is on are executed.

[0157] In FIG. 27, the CMP# indicates the ID number of the four comparators included in the 3-bit parallel ADC. The four comparators are indicated below as CMP#1, CMP#2, CMP#3, and CMP#4. The positive analog input voltage VIP and negative analog input voltage VIM are input into the four comparators CMP#1, CMP#2, CMP#3, and CMP#4.

[0158] In FIG. 27, ΔVIN is the differential voltage (analog input differential voltage) between the positive analog input voltage VIP and the negative analog input voltage VIM and is calculated as $VIP - VIM$. Furthermore, $\Delta VREF$ is the differential voltage (reference differential voltage) between the positive reference voltage VRP and either of the negative reference voltages VRM1 or VRM2 and is calculated as $VRP - VRM1$ or $VRP - VRM2$.

[0159] In the comparators CMP#1, CMP#2, CMP#3, and CMP#4, $\Delta VREF$ in the fine 1-bit ADC processing is increased by 2 V over the $\Delta VREF$ in the coarse 2-bit ADC processing. This difference is the difference between the first negative reference voltage VRM1 and the second negative reference voltage VRM2.

[0160] In FIG. 27, CMPO is the output logic of the comparator as a result of judging the magnitude relationship between ΔVIN and $\Delta VREF$. In this example, when ΔVIN is greater than $\Delta VREF$ ($\Delta VIN > \Delta VREF$), a "1" is output, whereas when ΔVIN is less than $\Delta VREF$ ($\Delta VIN < \Delta VREF$), a "0" is output.

[0161] During the coarse 2-bit ADC processing, a 2-bit analog-digital output result D_{out1} is calculated by converting a thermometer code, which is derived based on the output from the comparators CMP#1, CMP#2, CMP#3, and CMP#4, to a digital value.

[0162] During the fine 1-bit ADC processing, a 1-bit analog-digital output result D_{out2} is calculated by converting a thermometer code, which is derived based on the output from the comparators CMP#1, CMP#2, CMP#3, and CMP#4, to a digital value.

[0163] Based on the analog-digital output result D_{out1} and the analog-digital output result D_{out2} , the 3-bit parallel ADC calculates a 3-bit digital output D_{out} .

[0164] In this way, whereas an analog signal is converted to a digital signal with N-bit resolution by 2^N ($N = 2$ in the above example) comparators in a typical flash

ADC, an analog signal is converted to an (N+1)-bit digital signal by 2^N comparators in the flash ADC according to this disclosure.

What is claimed is:

1. An analog-digital converter comprising:
 - a digital-analog converter configured to output a differential voltage between a reference voltage and a voltage of an analog signal;
 - a comparator configured to output a comparison signal corresponding to the differential voltage output by the digital-analog converter; and
 - a register configured to cause the digital-analog converter to generate N pairs of differential voltages, where N is an integer greater than or equal to one, to cause the digital-analog converter to generate an $(N+1)^{\text{th}}$ pair of differential voltages by causing one of a positive side and a negative side of the digital-analog converter to output an $(N+1)^{\text{th}}$ differential voltage and causing the other of the positive side and the negative side to output a differential voltage equal to an N^{th} differential voltage as an $(N+1)^{\text{th}}$ differential voltage, and to output a digital signal corresponding to a smallest comparison signal having a smallest voltage among $(N+1)$ of the comparison signals.
2. The analog-digital converter of claim 1, wherein the digital-analog converter is a differential digital-analog converter comprising a pair of converters that each include $(N+1)$ passive components, the reference voltage and the voltage of the analog signal are input into the passive components, and N differential voltages are generated between the reference voltage and the voltage of the analog signal.
3. The analog-digital converter of claim 2, wherein the register causes one passive component in one converter of the pair of converters to connect to the reference voltage and output the $(N+1)^{\text{th}}$ differential voltage.
4. The analog-digital converter of claim 1, further comprising a decoder configured to input a digital signal into the digital-analog converter based on a signal acquired from the register.
5. The analog-digital converter of claim 2, wherein the passive components in the pair of converters are capacitors, resistors, or a combination of capacitors and resistors.

6. The analog-digital converter of claim 2, wherein the passive components in the pair of converters are configured with a binary system or a segmented system.

7. The analog-digital converter of claim 1, wherein the analog signal is a differential signal or a single end signal.

8. The analog-digital converter of claim 1, comprising a plurality of comparators that includes the comparator.

9. The analog-digital converter of claim 8, wherein two reference voltages with different voltage levels are connected via a switch to an input terminal on one of a positive side and a negative side in the plurality of comparators.

10. The analog-digital converter of claim 9, wherein the register switches the reference voltage connected to the input terminal by controlling the switch when causing the digital-analog converter to output the $(N+1)^{\text{th}}$ differential voltage.

11. A method used in an analog-digital converter including a digital-analog converter, a comparator, and a register, the method comprising:

the digital-analog converter outputting a differential voltage between a reference voltage and a voltage of an analog signal;

the comparator outputting a comparison signal corresponding to the differential voltage output by the digital-analog converter;

the register causing the digital-analog converter to generate N pairs of differential voltages, where N is an integer greater than or equal to one;

the register causing the digital-analog converter to generate an $(N+1)^{\text{th}}$ pair of differential voltages by causing one of a positive side and a negative side of the digital-analog converter to output an $(N+1)^{\text{th}}$ differential voltage and causing the other of the positive side and the negative side to output a differential voltage equal to an N^{th} differential voltage as an $(N+1)^{\text{th}}$ differential voltage; and

the register outputting a digital signal corresponding to a smallest comparison signal having a smallest voltage among $(N+1)$ of the comparison signals.

12. The method of claim 11, wherein:
the digital-analog converter comprises a pair of converters that each include (N+1) passive components; and
the method further comprises the converters each inputting the reference voltage and the voltage of the analog signal into the passive components and generating N differential voltages between the reference voltage and the voltage of the analog signal.
13. The method of claim 12, further comprising the register causing one passive component in one converter of the pair of converters to connect to the reference voltage and output the (N+1)th differential voltage.
14. The method of claim 11, wherein:
the analog-digital converter comprises a decoder; and
the method further comprises the decoder inputting a digital signal into the digital-analog converter based on a signal acquired from the register.
15. The method of claim 12, wherein the passive components in the pair of converters are capacitors, resistors, or a combination of capacitors and resistors.
16. The method of claim 12, wherein the passive components in the pair of converters are configured with a binary system or a segmented system.
17. The method of claim 11, wherein the analog signal is a differential signal or a single end signal.
18. The method of claim 11, wherein the analog-digital converter comprises a plurality of comparators that includes the comparator.
19. The method of claim 18, wherein two reference voltages with different voltage levels are connected via a switch to an input terminal on one of a positive side and a negative side in the plurality of comparators.
20. The method of claim 19, further comprising the register switching

the reference voltage connected to the input terminal by controlling the switch when causing the digital-analog converter to output the $(N+1)^{\text{th}}$ differential voltage.

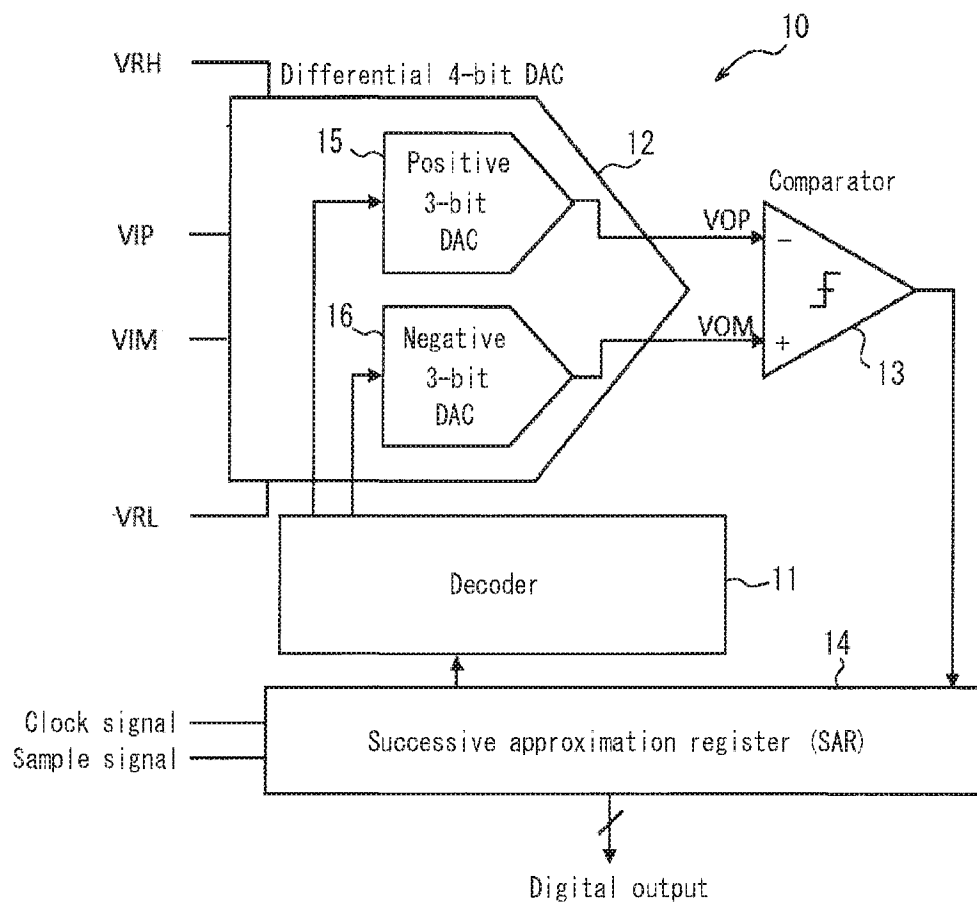
FIG. 1

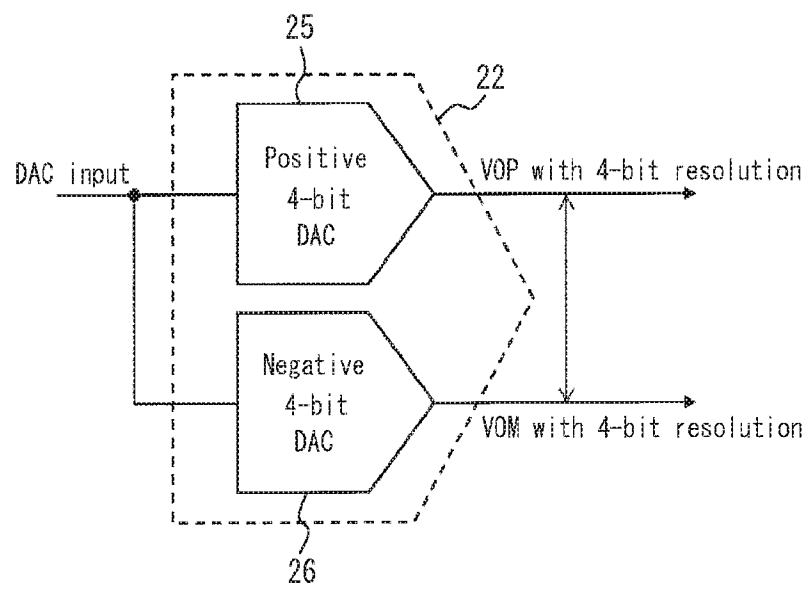
FIG. 2

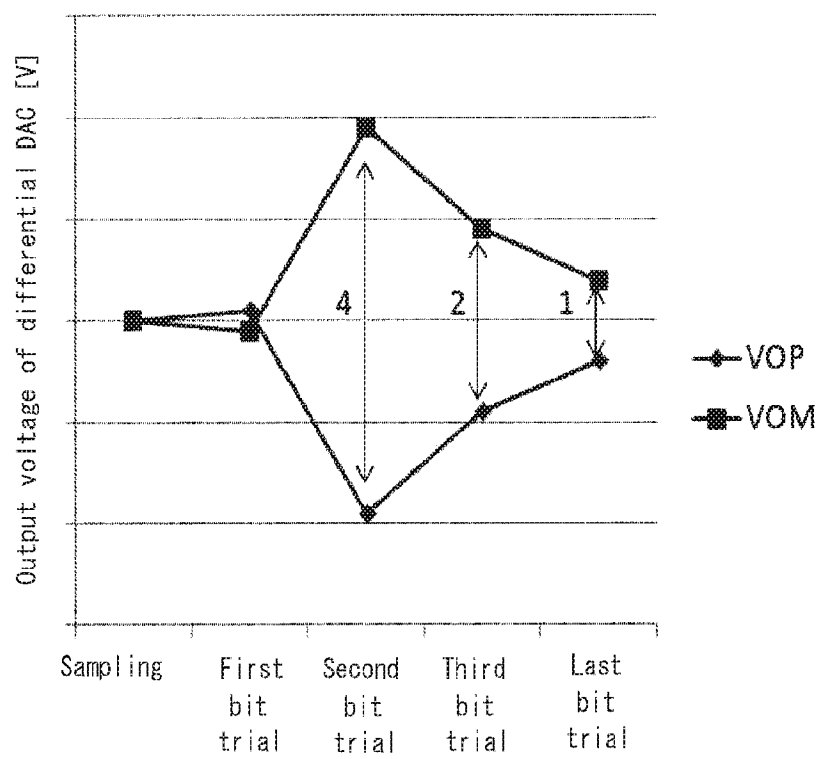
FIG. 3

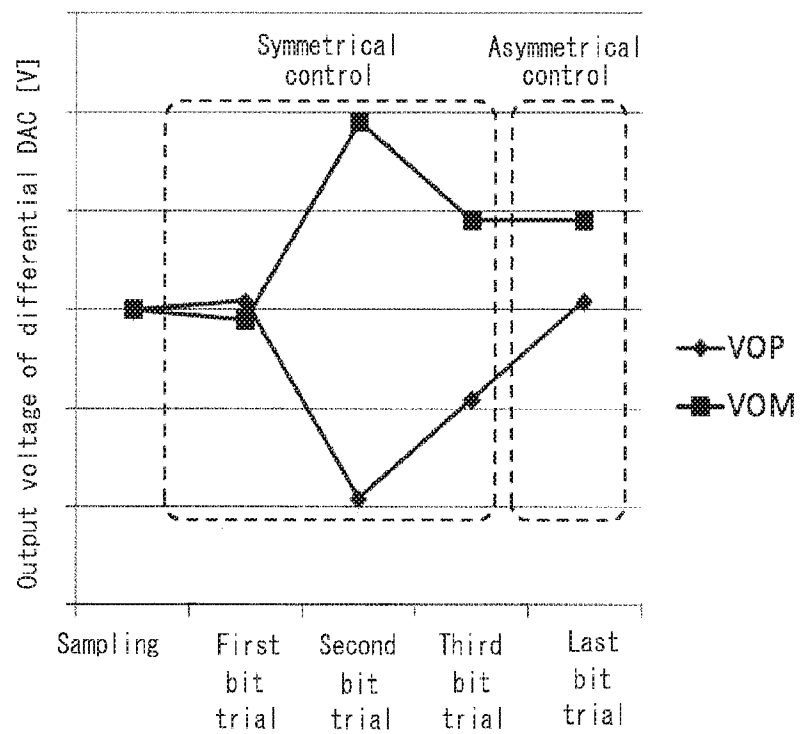
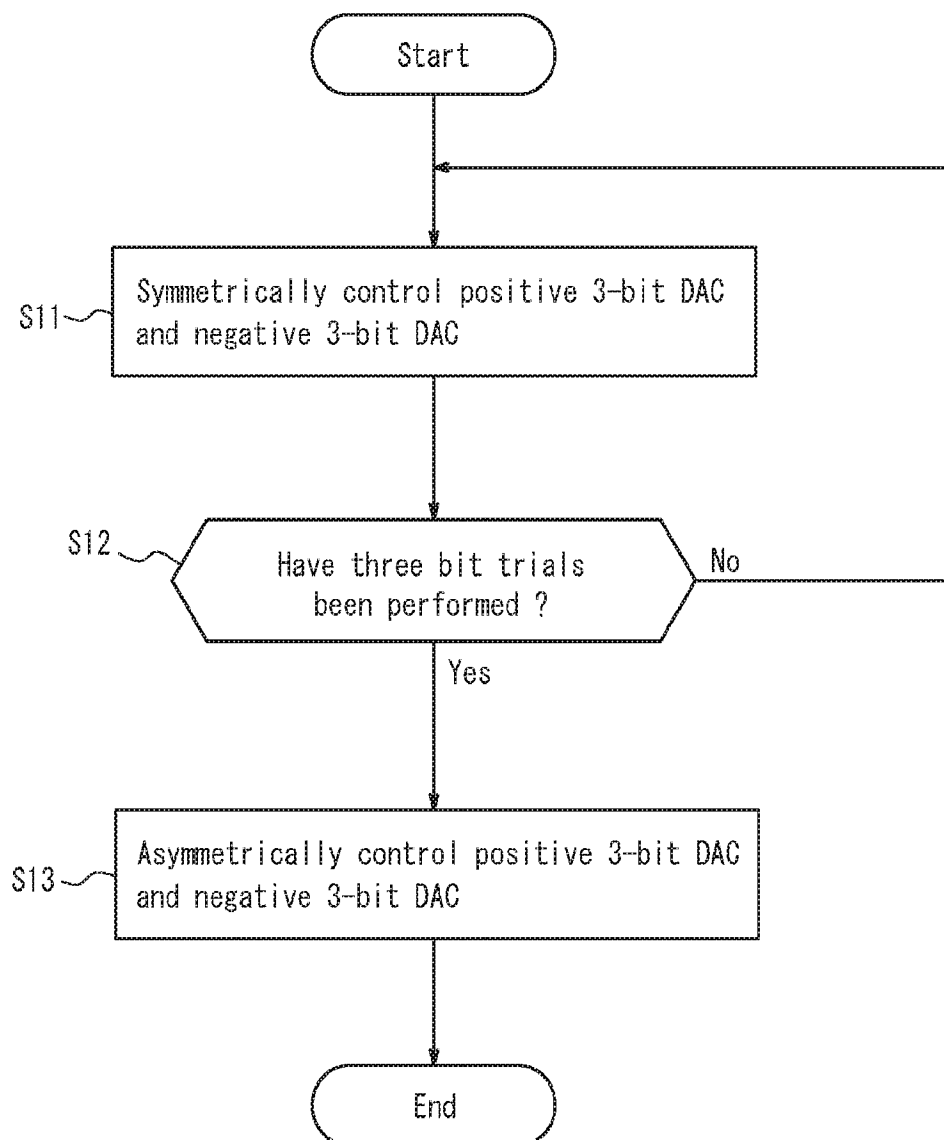
FIG. 4

FIG. 5

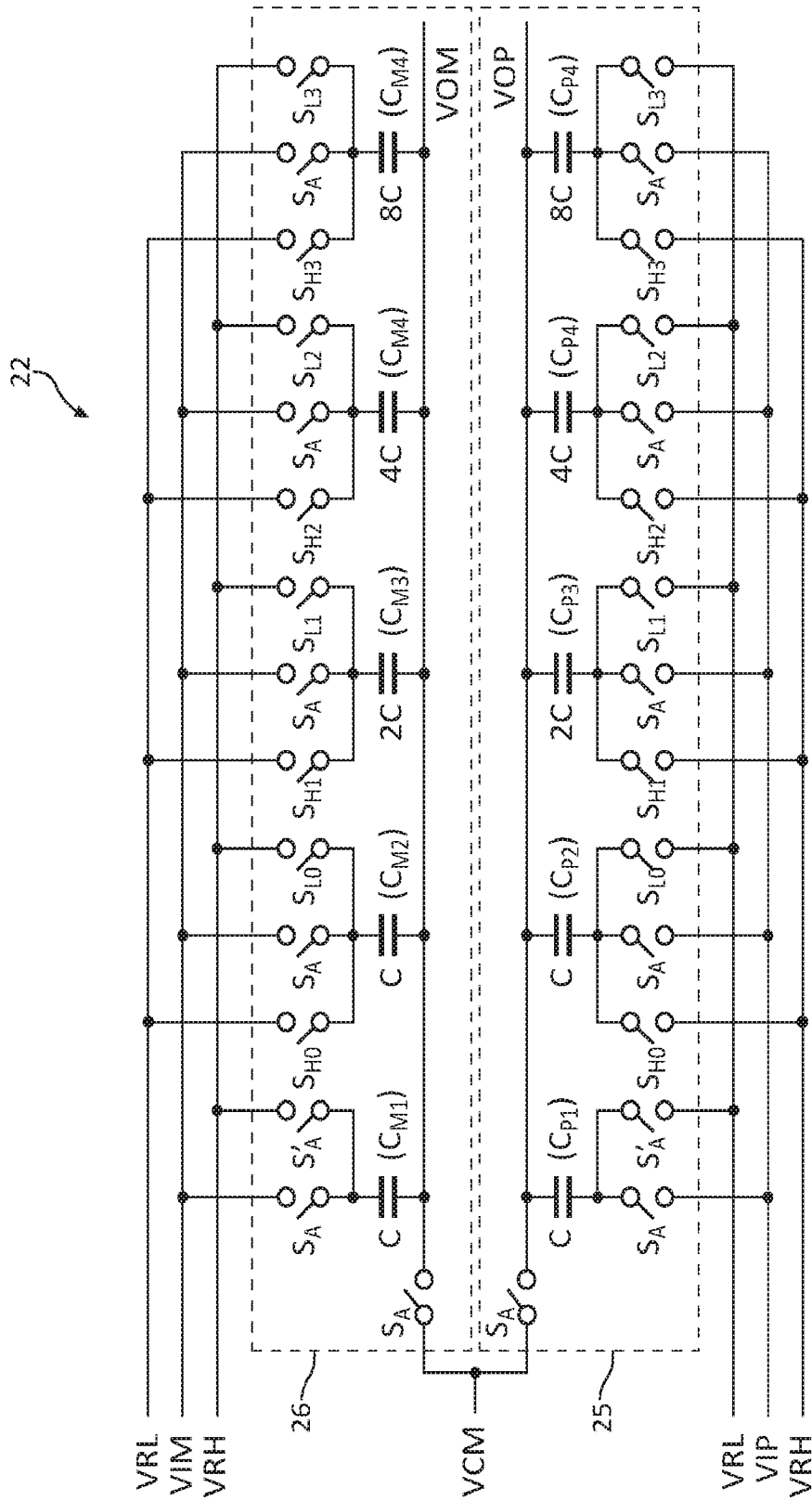


FIG. 6

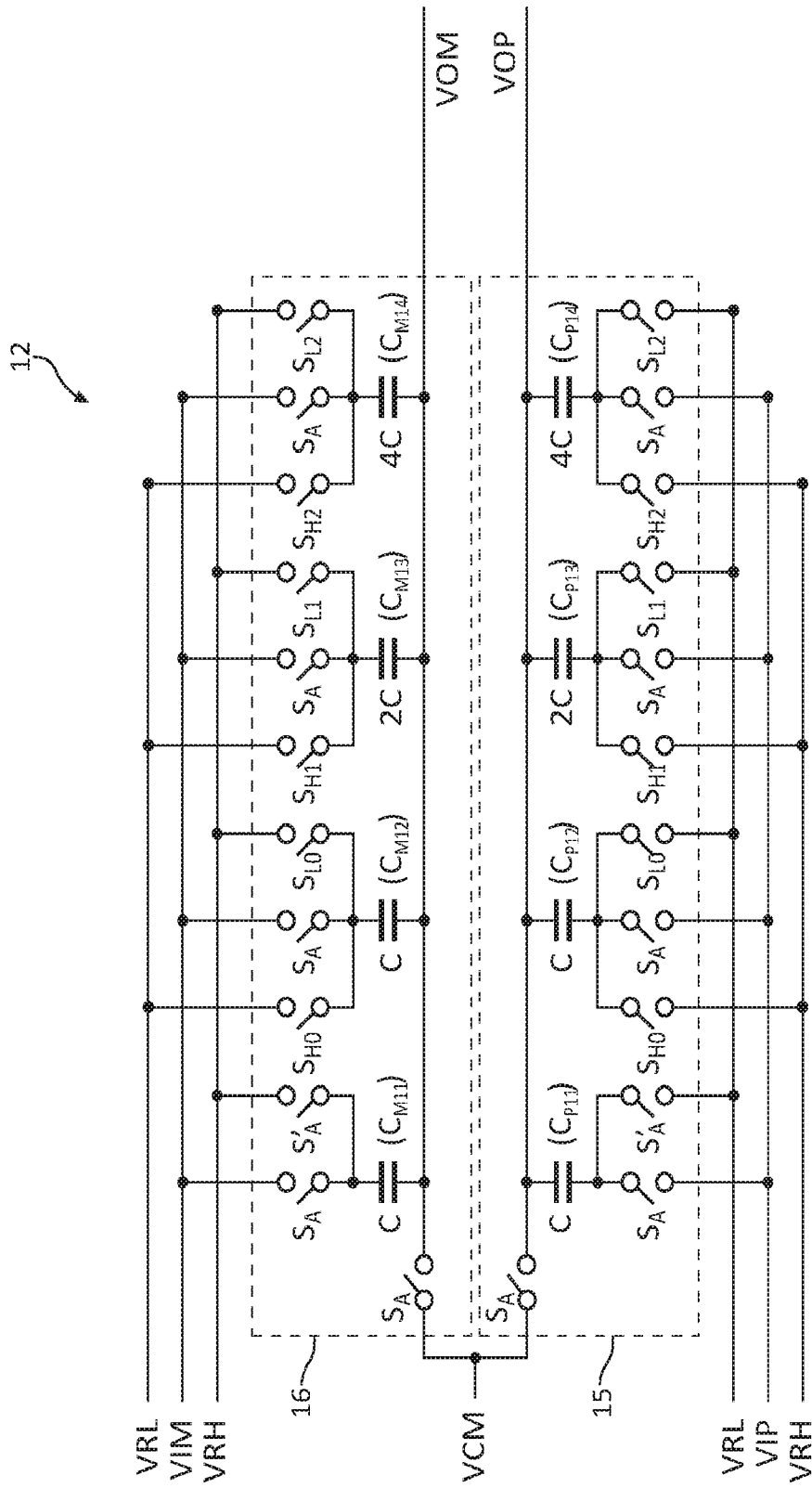
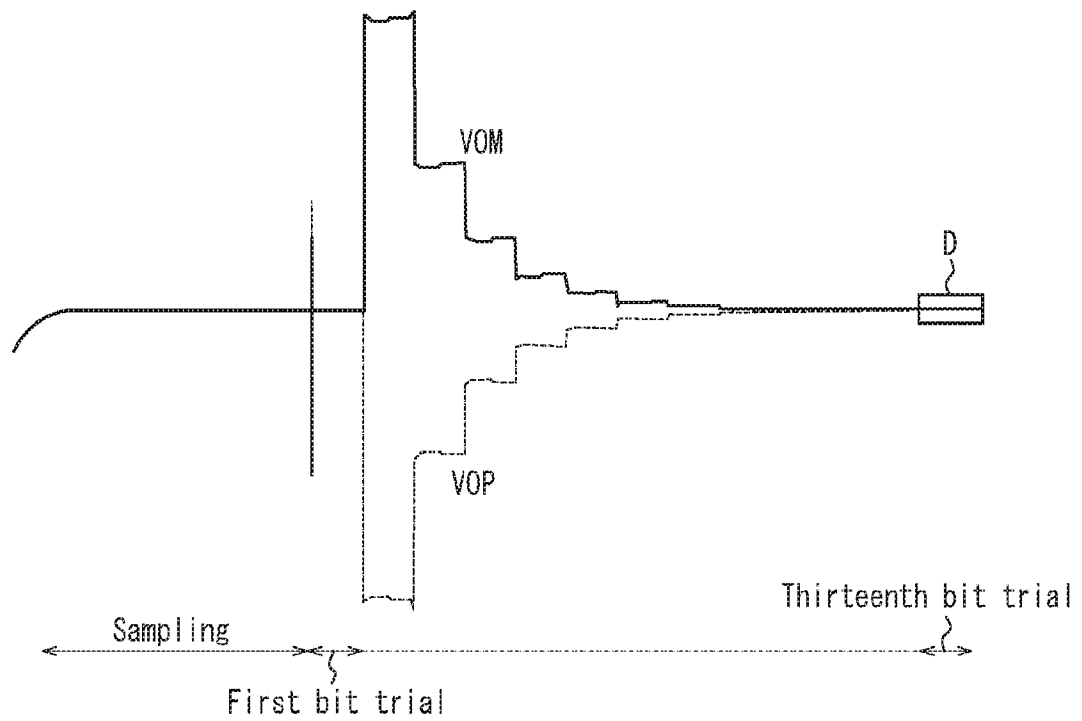
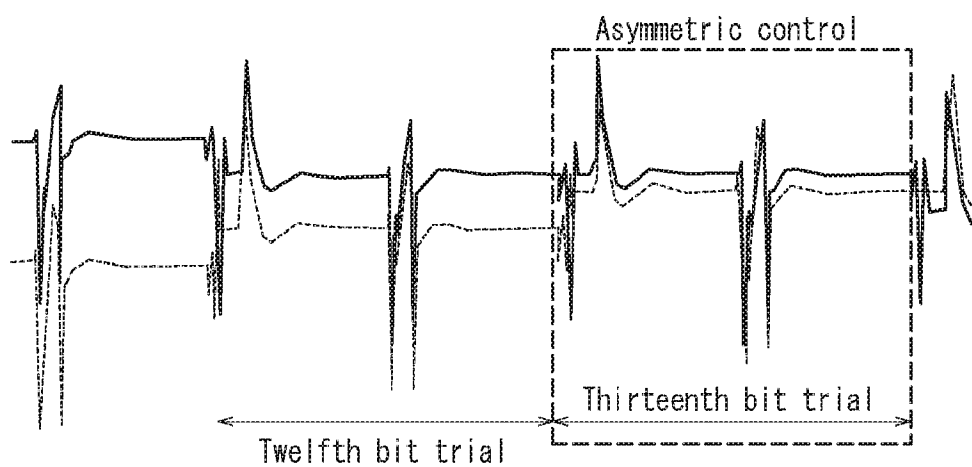


FIG. 7

FIG. 8A*FIG. 8B*

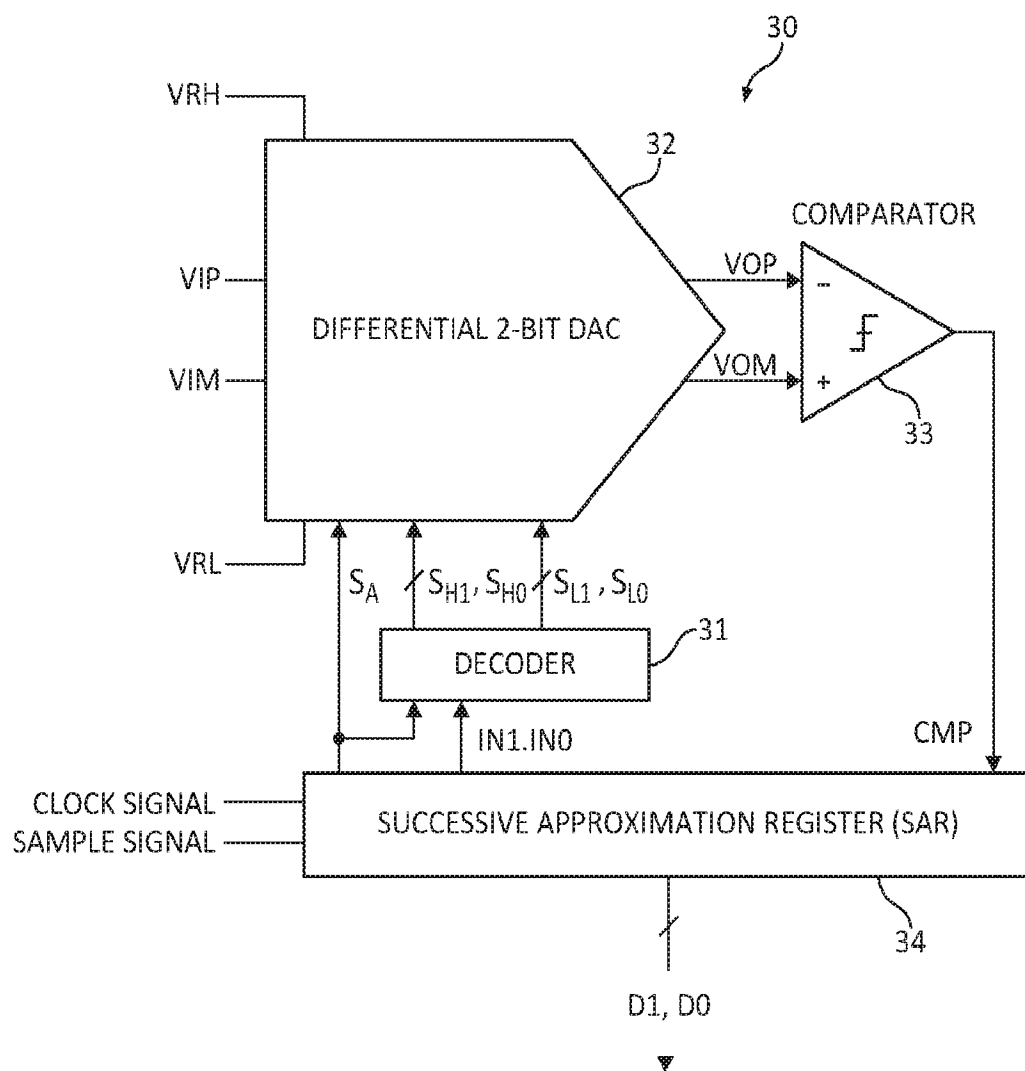
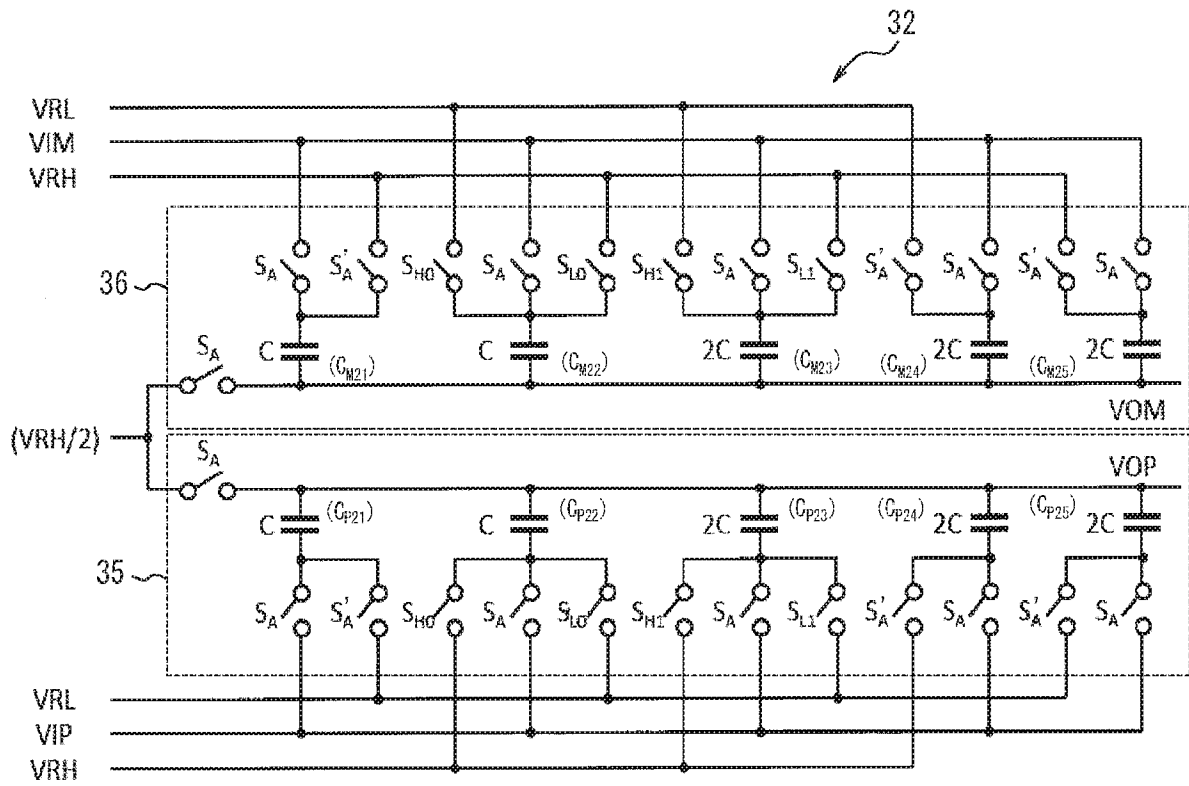
**FIG. 9**

FIG. 10



	S_A	IN1	IN0	S_{H1}	S_{H0}	S_{L1}	S_{L0}
SAMPLING STAGE	1	*	*	0	0	0	0
TRIAL STAGE	0	0	0	0	0	$\overline{S_{H1}}$	$\overline{S_{H0}}$
	0	0	1	0	1		
	0	1	0	1	0		
	0	1	1	1	1		

FIG. 11

VIP	FIRST BIT TRIAL					SECOND BIT TRIAL					DIGITAL OUTPUT		
	IN1	IN0	VOP	VOM	CMP	IN1	IN0	VOP	VOM	CMP	D1	D0	DOUT
1	1	0	7	4	0	0	1	6	5	0	0	0	0
3	1	0	5	4	0	0	1	4	5	1	0	1	1
5	1	0	3	4	1	1	1	4	3	0	1	0	2
7	1	0	1	4	1	1	1	2	3	1	1	1	3

FIG. 12

FIG. 13

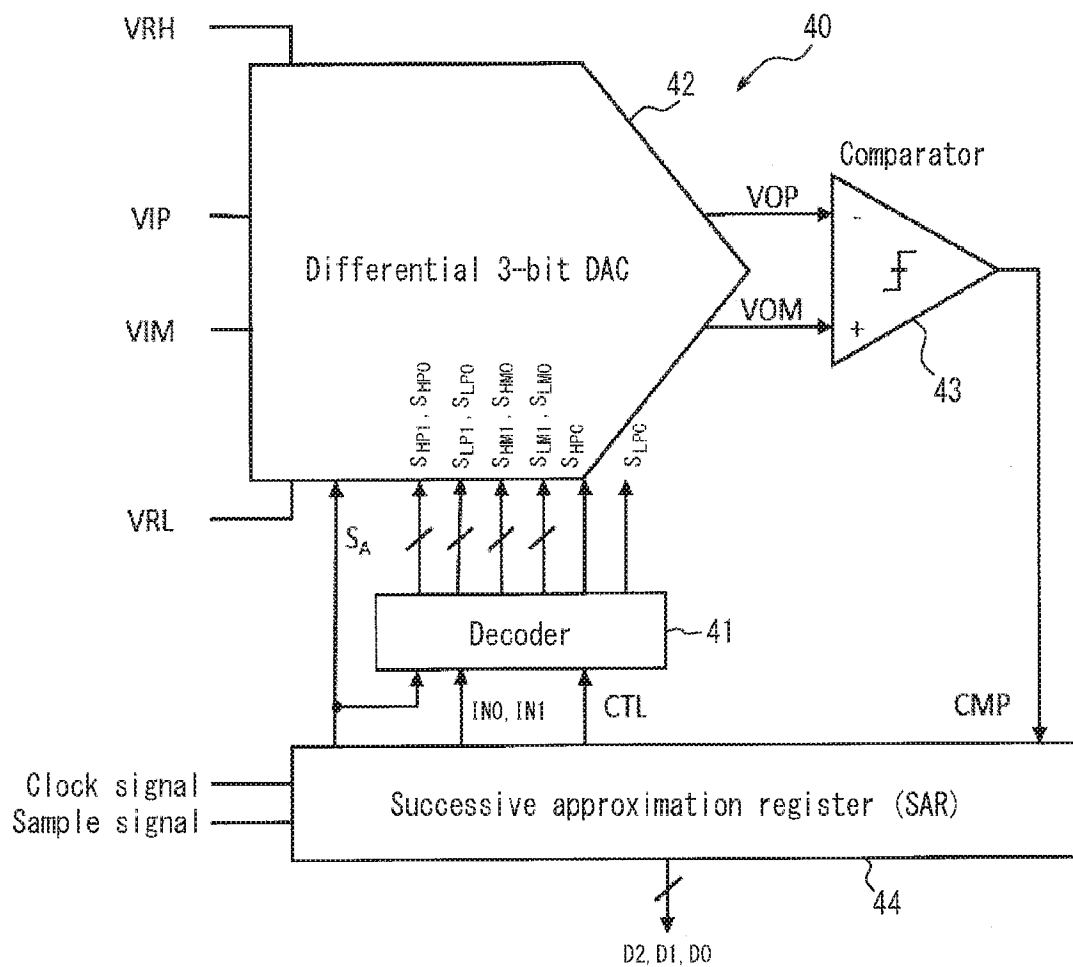
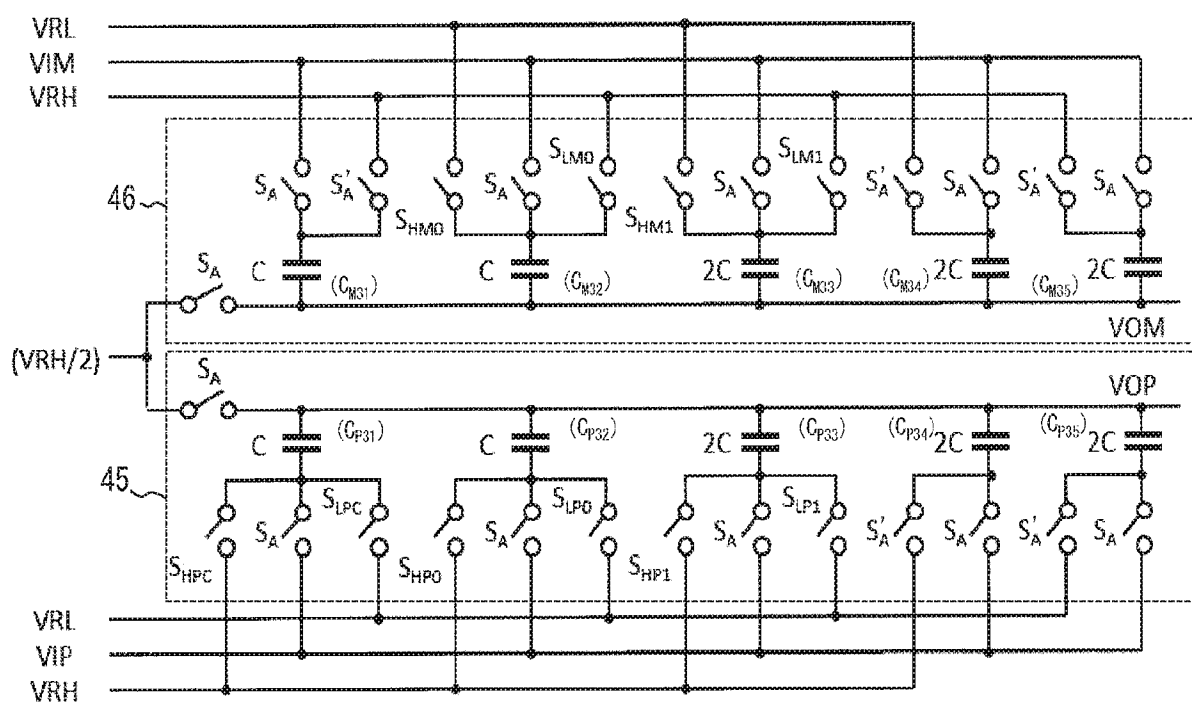


FIG. 14



	S _A	IN1	INO	CTL	S _{HP1}	S _{HP0}	S _{HPC}	S _{LP1}	S _{LP0}	S _{LPC}	S _{HM1}	S _{HM0}	S _{LM1}	S _{LM0}
SAMPLING STAGE	1	*	*	*	0	0	0	0	0	0	0	0	0	0
TRIAL STAGE	0	0	0	0	0	0	0	S _{HP1}	S _{HP0}	S _{HPC}	0	0	S _{HM1}	S _{HM0}
	0	0	0	1	0	1	0				0	0		
	0	0	1	0	0	1	0				0	1		
	0	0	1	1	1	0	0				0	1		
	0	1	0	0	1	0	0				1	0		
	0	1	0	1	1	1	0				1	0		
	0	1	1	0	1	1	0				1	1		
	0	1	1	1	1	1	1				1	1		

FIG. 15

FIG. 16

VIP	First bit trial						Second bit trial						Last bit trial						Digital output			
	IN1	IN0	CTL	VOP	VOM	CMP	IN1	IN0	CTL	VOP	VOM	CMP	IN1	IN0	CTL	VOP	VOM	CMP	D2	D1	D0	Dout
0.5	1	0	0	7.5	4	0	0	1	0	6.5	5	0	0	0	1	6.5	6	0	0	0	0	0
1.5	1	0	0	6.5	4	0	0	1	0	5.5	5	0	0	0	1	5.5	6	1	0	0	1	1
2.5	1	0	0	5.5	4	0	0	1	0	4.5	5	1	0	1	1	5.5	5	0	0	1	0	2
3.5	1	0	0	4.5	4	0	0	1	0	3.5	5	1	0	1	1	4.5	5	1	0	1	1	3
4.5	1	0	0	3.5	4	1	1	1	0	4.5	3	0	1	0	1	4.5	4	0	1	0	0	4
5.5	1	0	0	2.5	4	1	1	1	0	3.5	3	0	1	0	1	3.5	4	1	1	0	1	5
6.5	1	0	0	1.5	4	1	1	1	0	2.5	3	1	1	1	1	3.5	3	0	1	1	0	6
7.5	1	0	0	0.5	4	1	1	1	0	1.5	3	1	1	1	1	2.5	3	1	1	1	1	7

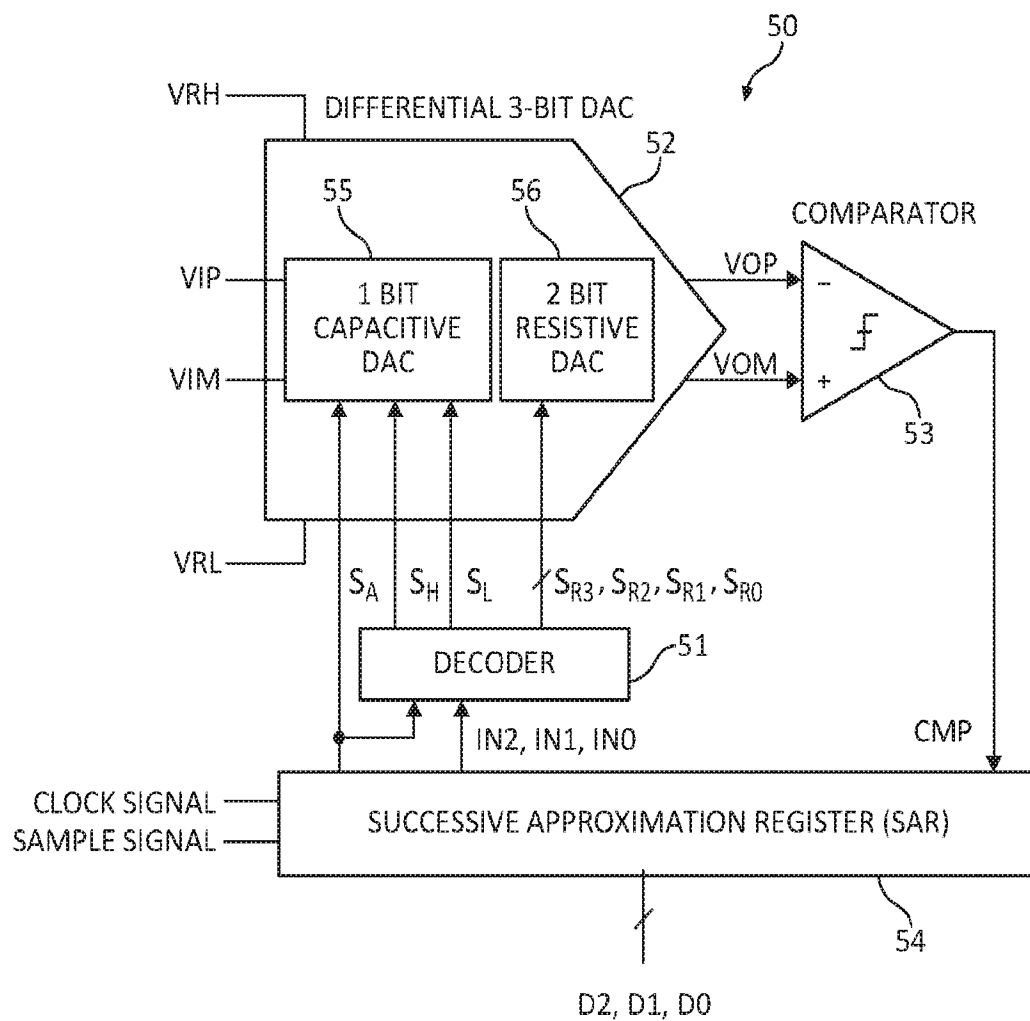
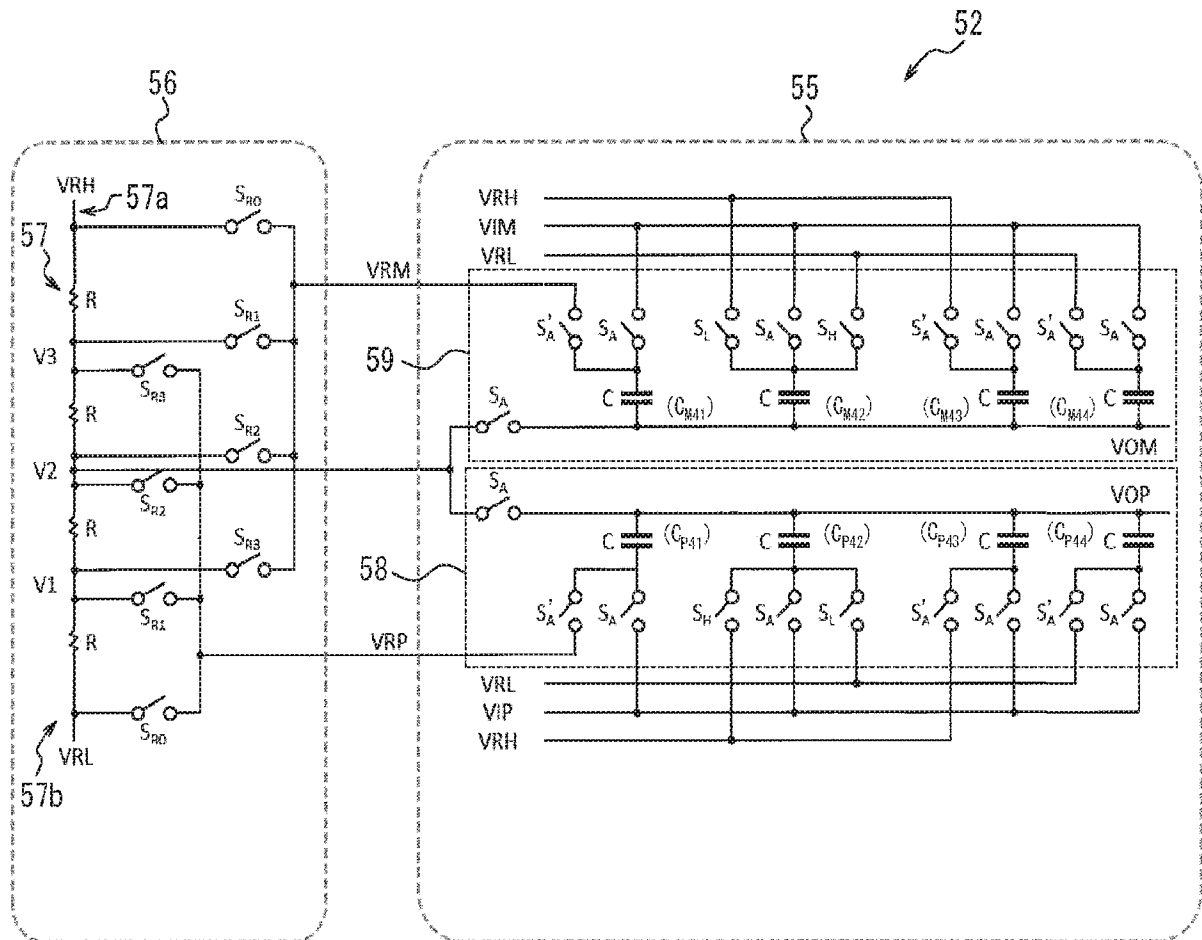
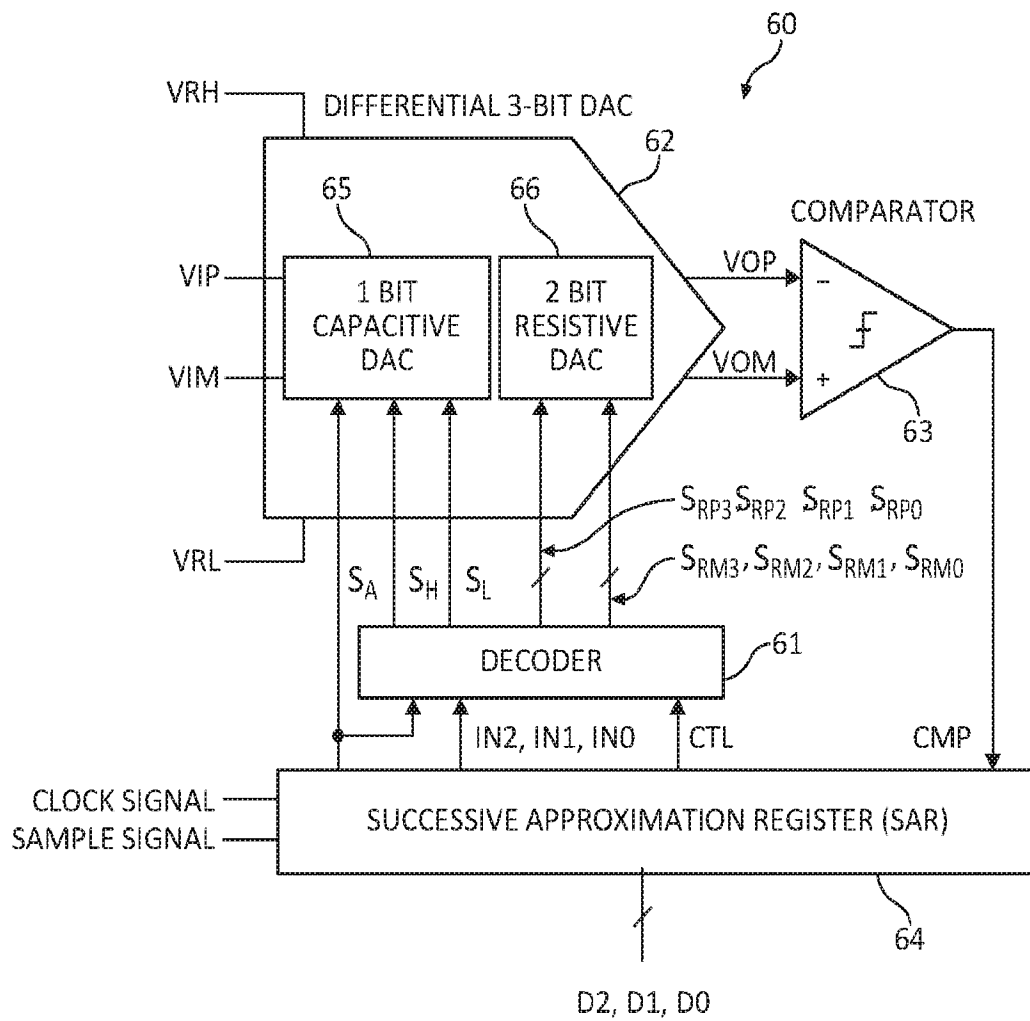


FIG. 17

FIG. 18



**FIG. 19**

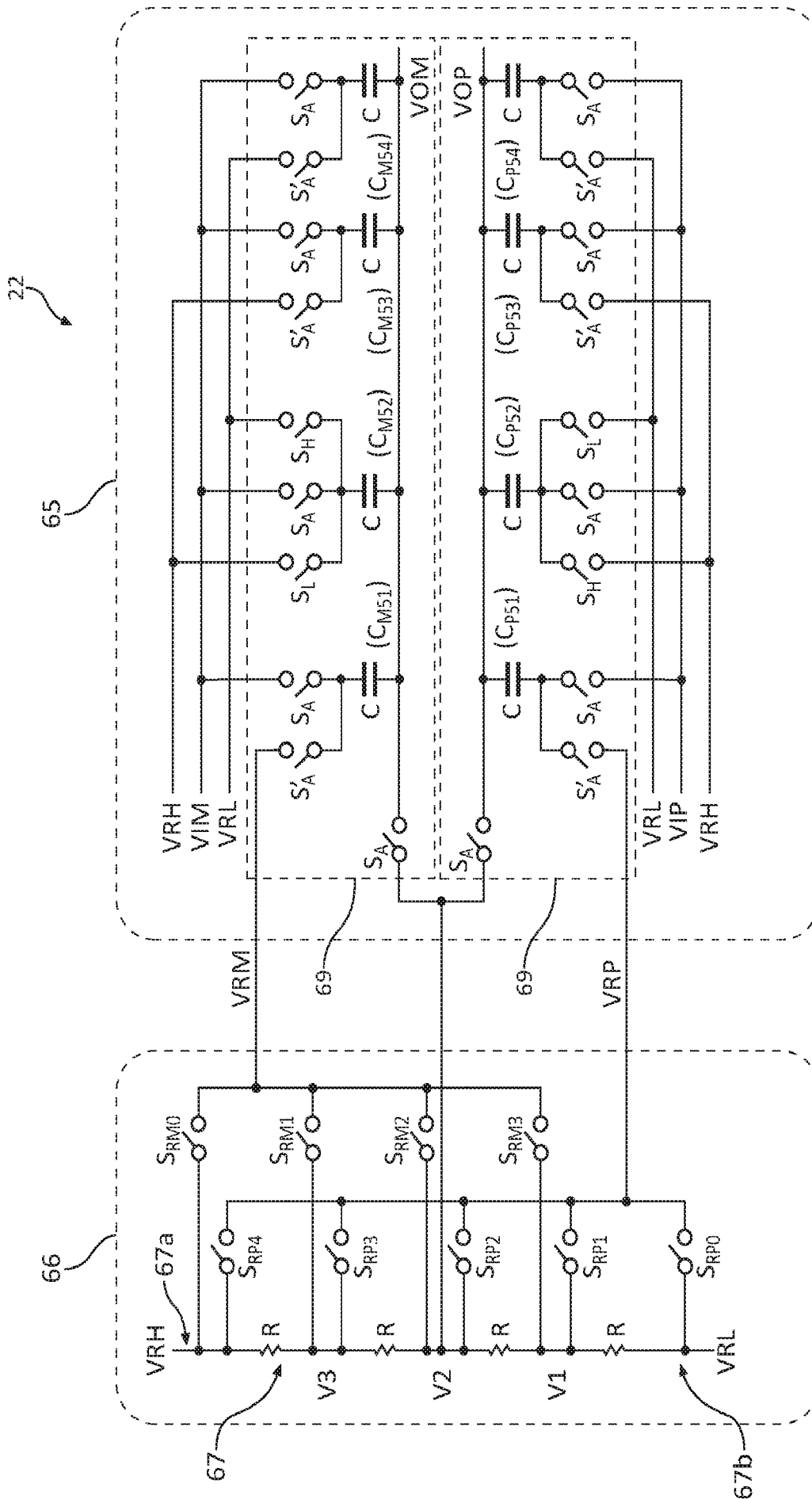


FIG. 20

FIG. 21

	S _A	IN2	S _H	S _L
Sampling stage	1	0	0	0
	1	1	0	0
Trial stage	0	0	0	1
	0	1	1	0

FIG. 22

Decoder input			Decoder output									Output		
IN1	IN0	CTL	S _{RP4}	S _{RP3}	S _{RP2}	S _{RP1}	S _{RP0}	S _{RM3}	S _{RM2}	S _{RM1}	S _{RM0}	VRP	VRM	Δ
0	0	0	0	0	0	0	1	0	0	0	1	0	16	-16
0	0	1	0	0	0	1	0	0	0	0	1	4	16	-12
0	1	0	0	0	0	1	0	0	0	1	0	4	12	-8
0	1	1	0	0	1	0	0	0	0	1	0	8	12	-4
1	0	0	0	0	1	0	0	0	1	0	0	8	8	0
1	0	1	0	1	0	0	0	0	1	0	0	12	8	4
1	1	0	0	1	0	0	0	1	0	0	0	12	4	8
1	1	1	1	0	0	0	0	1	0	0	0	16	4	12

VIP	FIRST BIT TRIAL										SECOND BIT TRIAL										THIRD BIT TRIAL										LAST BIT TRIAL										DIGITAL OUTPUT				
	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	D3	D2	D1	D0	DOUT				
-7.5	1	0	0	0	0	16	11.5	4.0	0	0	1	0	0	8	8	9.5	6.0	0	0	0	1	0	4	12	8.5	7.0	0	0	0	0	1	4	16	8.5	8.0	0	0	0	0	0	0	0			
-6.5	1	0	0	0	0	16	11.0	4.5	0	0	1	0	0	8	8	9.0	6.5	0	0	0	1	0	4	12	8.0	7.5	0	0	0	0	1	4	16	8.0	8.5	1	0	0	0	1	1	1			
-5.5	1	0	0	0	0	16	10.5	5.0	0	0	1	0	0	8	8	8.5	7.0	0	0	0	1	0	4	12	7.5	8.0	1	0	0	1	1	8	12	8.5	8.0	0	0	0	1	0	2	2			
-4.5	1	0	0	0	0	16	10.0	5.5	0	0	1	0	0	8	8	8.0	7.5	0	0	0	1	0	4	12	7.0	8.5	1	0	0	1	1	8	12	8.0	8.5	1	0	0	1	1	3	3			
-3.5	1	0	0	0	0	16	9.5	6.0	0	0	1	0	0	8	8	7.5	8.0	1	0	1	1	0	12	4	8.5	7.0	0	0	1	0	1	12	8	8.5	8.0	0	0	1	0	0	4	4			
-2.5	1	0	0	0	0	16	9.0	6.5	0	0	1	0	0	8	8	7.0	8.5	1	0	1	1	0	12	4	8.0	7.5	0	0	1	0	1	12	8	8.0	8.5	1	0	1	0	1	5	5			
-1.5	1	0	0	0	0	16	8.5	7.0	0	0	1	0	0	8	8	6.5	9.0	1	0	1	1	0	12	4	7.5	8.0	1	0	1	1	1	16	4	8.5	8.0	0	0	1	1	0	6	6			
-0.5	1	0	0	0	0	16	8.0	7.5	0	0	1	0	0	8	8	6.0	9.5	1	0	1	1	0	12	4	7.0	8.5	1	0	1	1	1	16	4	8.0	8.5	1	0	1	1	1	7	7			
0.5	1	0	0	0	0	16	7.5	8.0	1	1	1	0	0	8	8	9.5	6.0	0	1	0	1	0	4	12	8.5	7.0	0	1	0	0	1	4	16	8.5	8.0	0	1	0	0	0	8	8			
1.5	1	0	0	0	0	16	7.0	8.5	1	1	1	0	0	8	8	9.0	6.5	0	1	0	1	0	4	12	8.0	7.5	0	1	0	0	1	4	16	8.0	8.5	1	1	0	0	1	9	9			
2.5	1	0	0	0	0	16	6.5	9.0	1	1	1	0	0	8	8	8.5	7.0	0	1	0	1	0	4	12	7.5	8.0	1	1	0	1	1	8	12	8.5	8.0	0	1	0	1	0	10	10			
3.5	1	0	0	0	0	16	6.0	9.5	1	1	1	0	0	8	8	8.0	7.5	0	1	0	1	0	4	12	7.0	8.5	1	1	0	1	1	8	12	8.0	8.5	1	1	0	1	1	11	11			
4.5	1	0	0	0	0	16	5.5	10.0	1	1	1	0	0	8	8	7.5	8.0	1	1	1	1	0	12	4	8.5	7.0	0	1	1	0	1	12	8	8.5	8.0	0	1	1	0	0	12	12			
5.5	1	0	0	0	0	16	5.0	10.5	1	1	1	0	0	8	8	7.0	8.5	1	1	1	1	0	12	4	8.0	7.5	0	1	1	0	1	12	8	8.0	8.5	1	1	1	0	1	13	13			
6.5	1	0	0	0	0	16	4.5	11.0	1	1	1	0	0	8	8	6.5	9.0	1	1	1	1	0	12	4	7.5	8.0	1	1	1	1	1	16	4	8.5	8.0	0	1	1	1	0	14	14			
7.5	1	0	0	0	0	16	4.0	11.5	1	1	1	0	0	8	8	6.0	9.5	1	1	1	1	0	12	4	7.0	8.5	1	1	1	1	1	16	4	8.0	8.5	1	1	1	1	1	15	15			

FIG. 23

FIG. 24

ΔV_i	First bit trial										Second bit trial										Third bit trial										Last bit trial										Digital output				
	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	IN2	IN1	IN0	CTL	VRP	VRM	VOP	VOM	CMP	D3	D2	D1	D0	Double				
-7.5	1	0	0	0	0	16	11.5	4.0	0	0	1	0	0	8	8	9.5	6.0	0	0	0	1	0	4	12	8.5	7.0	0	0	0	0	1	4	16	8.5	8.0	0	0	0	0	0	0	0			
-6.5	1	0	0	0	0	16	11.0	4.5	0	0	1	0	0	8	8	9.0	6.5	0	0	0	1	0	4	12	8.0	7.5	0	0	0	0	0	1	4	16	8.0	8.5	1	0	0	0	1	1			
-5.5	1	0	0	0	0	16	10.5	5.0	0	0	1	0	0	8	8	8.5	7.0	0	0	0	1	0	4	12	7.5	8.0	1	0	0	0	0	1	8	12	8.5	8.0	0	0	0	1	0	2			
-4.5	1	0	0	0	0	16	10.0	5.5	0	0	1	0	0	8	8	8.0	7.5	0	0	0	1	0	4	12	7.0	8.5	1	0	0	0	0	1	8	12	8.0	8.5	1	0	0	1	1	3			
-3.5	1	0	0	0	0	16	9.5	6.0	0	0	1	0	0	8	8	7.5	8.0	1	0	1	1	0	12	4	8.5	7.0	0	0	1	0	0	1	12	8	8.5	8.0	0	0	1	0	4				
-2.5	1	0	0	0	0	16	9.0	6.5	0	0	1	0	0	8	8	7.0	8.5	1	0	1	1	0	12	4	8.0	7.5	0	0	1	0	0	1	12	8	8.0	8.5	1	0	1	0	5				
-1.5	1	0	0	0	0	16	8.5	7.0	0	0	1	0	0	8	8	6.5	9.0	1	0	1	1	0	12	4	7.5	8.0	1	0	1	0	0	1	16	4	8.5	8.0	0	0	1	1	6				
-0.5	1	0	0	0	0	16	8.0	7.5	0	0	1	0	0	8	8	6.0	9.5	1	0	1	1	0	12	4	7.0	8.5	1	0	1	0	0	1	16	4	8.0	8.5	1	0	1	1	7				
0.5	1	0	0	0	0	16	7.5	8.0	1	1	1	0	0	8	8	9.5	6.0	0	1	0	1	0	4	12	8.5	7.0	0	1	0	0	0	1	4	16	8.5	8.0	0	1	0	0	8				
1.5	1	0	0	0	0	16	7.0	8.5	1	1	1	0	0	8	8	9.0	6.5	0	1	0	1	0	4	12	8.0	7.5	0	1	0	0	0	1	4	16	8.0	8.5	1	1	0	0	9				
2.5	1	0	0	0	0	16	6.5	9.0	1	1	1	0	0	8	8	8.5	7.0	0	1	0	1	0	4	12	7.5	8.0	1	1	0	0	0	1	8	12	8.5	8.0	0	1	0	1	10				
3.5	1	0	0	0	0	16	6.0	9.5	1	1	1	0	0	8	8	8.0	7.5	0	1	0	1	0	4	12	7.0	8.5	1	1	0	0	0	1	8	12	8.0	8.5	1	1	0	1	11				
4.5	1	0	0	0	0	16	5.5	10.0	1	1	1	0	0	8	8	7.5	8.0	1	1	1	1	0	12	4	8.5	7.0	0	1	1	0	0	1	12	8	8.5	8.0	0	1	1	0	12				
5.5	1	0	0	0	0	16	5.0	10.5	1	1	1	0	0	8	8	7.0	8.5	2	1	1	1	0	12	4	8.0	7.5	0	1	1	0	0	1	12	8	8.0	8.5	1	1	1	0	13				
6.5	1	0	0	0	0	16	4.5	11.0	1	1	1	0	0	8	8	6.5	9.0	1	1	1	1	0	12	4	7.5	8.0	1	1	1	0	0	1	16	4	8.5	8.0	0	1	1	0	14				
7.5	1	0	0	0	0	16	4.0	11.5	1	1	1	0	0	8	8	6.0	9.5	1	1	1	1	0	12	4	7.0	8.5	1	1	1	0	0	1	16	4	8.0	8.5	1	1	1	1	15				

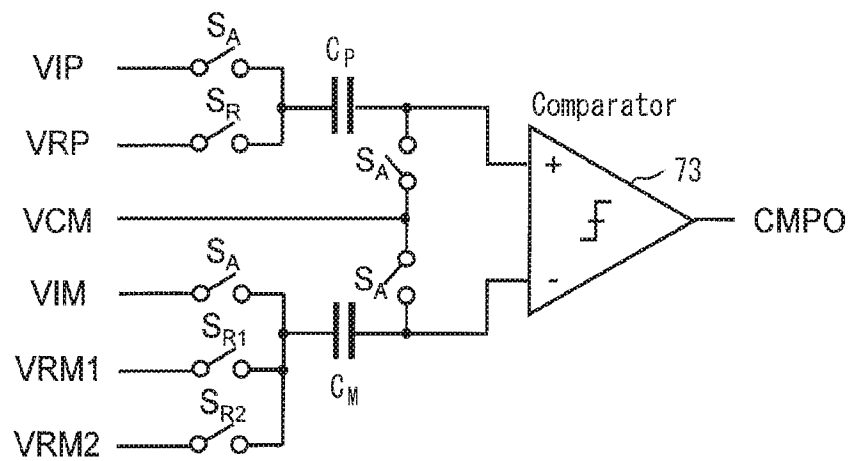
FIG. 25

FIG. 26

Sampling				Coarse ADC processing				Fine ADC processing			
S _A	S _R	S _{R1}	S _{R2}	S _A	S _R	S _{R1}	S _{R2}	S _A	S _R	S _{R1}	S _{R2}
1	0	0	0	0	1	1	0	0	1	0	1

FIG. 27

Analog input		CMP#	Coarse 2-bit ADC processing						Fine 1-bit ADC processing					Output	
VIP	VIM		VRP	VRM1	ΔV_{IN}	ΔV_{REF}	CMPO	Dout_1	VRP	VRM2	ΔV_{REF}	CMPO	Dout_2	Dout	
7.5	0.5	4	6	2	7	4	1	3	6	0	6	1	3	3.5	
		3	4	4		0	1		4	2	2	1			
		2	2	6		-4	1		2	4	-2	1			
		1	0	8		-8	1		0	6	-6	1			
6.5	1.5	4	6	2	5	4	1	3	6	0	6	0	2	3	
		3	4	4		0	1		4	2	2	1			
		2	2	6		-4	1		2	4	-2	1			
		1	0	8		-8	1		0	6	-6	1			
5.5	2.5	4	6	2	3	4	0	2	6	0	6	0	2	2.5	
		3	4	4		0	1		4	2	2	1			
		2	2	6		-4	1		2	4	-2	1			
		1	0	8		-8	1		0	6	-6	1			
4.5	3.5	4	6	2	1	4	0	2	6	0	6	0	1	2	
		3	4	4		0	1		4	2	2	0			
		2	2	6		-4	1		2	4	-2	1			
		1	0	8		-8	1		0	6	-6	1			
3.5	4.5	4	6	2	-1	4	0	1	6	0	6	0	1	1.5	
		3	4	4		0	0		4	2	2	0			
		2	2	6		-4	1		2	4	-2	1			
		1	0	8		-8	1		0	6	-6	1			
2.5	5.5	4	6	2	-3	4	0	1	6	0	6	0	0	1	
		3	4	4		0	0		4	2	2	0			
		2	2	6		-4	1		2	4	-2	0			
		1	0	8		-8	1		0	6	-6	1			
1.5	6.5	4	6	2	-5	4	0	0	6	0	6	0	0	0.5	
		3	4	4		0	0		4	2	2	0			
		2	2	6		-4	0		2	4	-2	0			
		1	0	8		-8	1		0	6	-6	1			
0.5	7.5	4	6	2	-7	4	0	0	6	0	6	0	-1	0	
		3	4	4		0	0		4	2	2	0			
		2	2	6		-4	0		2	4	-2	0			
		1	0	8		-8	1		0	6	-6	0			

INTERNATIONAL SEARCH REPORT	International application No. PCT/US16/18625
A. CLASSIFICATION OF SUBJECT MATTER IPC: H03M 1/12(2006.01) USPC: 341/155 According to International Patent Classification (IPC) or to both national classification and IPC	
B. FIELDS SEARCHED	
Minimum documentation searched (classification system followed by classification symbols) U.S. : 341/155	
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched	
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)	
C. DOCUMENTS CONSIDERED TO BE RELEVANT	
Category *	Citation of document, with indication, where appropriate, of the relevant passages
Relevant to claim No.	
X	US 8,638,248 B2 (Wu et al.) 28 January 2014 see entire document.
A	US 8,497,795 B2 (Le Tual et al.) 30 July 2013, see entire document.
A	US 7,151,475 B2 (Blemler) 19 December 2006, see entire document.
A	US 7,432,844 B2 (Mueck et al.) 07 October 2008, see entire document.

☐ Further documents are listed in the continuation of Box C.	☐ See patent family annex.
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
Date of the actual completion of the international search 30 March 2016 (30.03.2016)	Date of mailing of the international search report 07 APR 2016
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Ham Seungsook Telephone No. 571-272-2405