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(19)

(54) IMPROVEMENTS IN SEMICONDUCTOR MEMORY DEVICES

(71)We, HITACHI, LTD., of 1-5-1, Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it it to be performed, to be particularly described in and by the following statement:-

The present invention relates to a semiconductor memory device which is highly integrated.

An integrated semiconductor memory device is disclosed in U.S. Patent No.3,387,286. The memory cell is composed of diffused layers formed in a substrate, an isolation oxide which isolates different elements from each other, as well as a gate oxide film formed in contact therewith, an electrode for forming a storage capacitance which is made of polycrystalline silicon, a gate similarly made of polycrystalline silicon, an insulating film covering the electrode and the gate, and a metal electrode serving as a word line. Among these components, the gate electrode, the gate oxide film and the diffused layers constitute a switching transistor and the storage capacitance are two-dimensionally arranged on one plan so they do not overlap each other. The prior art accordingly has the disadvantage that the area of the memory cell becomes large.

One known type of one-transistor type MOS random access memory is shown in Figures 1 and 2 of the accompanying drawings, Figure 2 being a sectional view of the device in Figure 1 as taken along line II - II (a memory cell which consists of a switching MOS transistor 1 and a storage capacitance 2 is selected by a word line (Al lead) 3 and a data line (diffused layer) 4. In Figures 1 and 2, numeral 5 designates a substrate, numeral 6 an isolation oxide, numeral 7 a gate oxide film, numerals 8 and 12 a first layer of polycrystalline silicon (numeral 8 one electrode constituting the storage capacitance and numeral 12 a gate electrode), numeral 9 an inter-layer insulating film, numerals 4 and 10 diffused layers (a source region and a drain region, respectively), numeral 11 a diffused layer constituting the storage capacitance, and numeral 22 a contact hole.

As understood from the figures, the storage capacitance 2 is two-dimensionally arranged with the switching transistor 1 so as not to overlap each other. In the prior-art device, therefore, the area of the memory cell becomes large.

It is therefore an object of this invention to provide a semiconductor memory device which has a large storage capacitance and whose memory cell area per bit is small.

According to the present invention, there is provided a semiconductor memory device comprising: a semiconductor substrate; a plurality of memory cells arranged in matrix form on one surface of said semiconductor substrate, each of said memory cells comprising a source region, a channel region and a drain region, which are provided in a surface portion of said semiconductor substrate; a first conductive substance which is provided in opposition to said channel region above a gate insulating film disposed on said first conductive substance; and at least one storage capacitance unit comprising a second conductive substance which is in contact with either of said source region and said drain region and a part of which is superimposed on said first conductive substance above said first insulating film, a second insulating film which is provided on said second conductive substance, and a third conductive substance which is provided on said second insulating film; a third insulating film disposed on said memory cells; a data line disposed on said third insulating film and connecting whichever of said source region and said drain region is not in contact with said second conductive substance, through a contact hole formed

through said third insulating film, with the corresponding region of memory cells belonging to the same column of the matrix.

Since the storage capacitance is three-dimensionally stacked on a switching transistor, the memory cell area per bit can be substantially reduced.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein:

Figure 3 is a plan view of two memory cells in a matrix of cells in a first embodiment of a semiconductor memory device;

Figure 4 is a sectional view of the device shown in Figure 3, taken along the line IV-IV:

Figures 5 and *7* are plan views of second and third embodiments of semiconductor memory devices; and

Figures 6 and *8* are sectional views of the devices shown in Figures 5 and 7 taken along the lines VI-VI and VIII-VIII respectively.

Referring first to Figures 3 and 4, there are provided on a part of a P-type silicon substrate 5 having a resistivity of 15 ohm.cm and a crystal orientation of <100>, an isolating oxide layer 6 having a thickness of 1.5μm (which forms an insulating film to isolate adjacent cells in the matrix), a gate SiO_2 film 7 having a thickness of 800Å, first polycrystalline silicon gate electrodes 12 having a film thickness of 3500Å and a sheet resistance of 15 ohms/sq.cm, source and drain regions 10 and 13 having a junction depth of 1.5 μm and a sheet resistance of 10 ohms/sq.cm, and an SiO_2 film 19 having a thickness of 4000 Å. Subsequently, second polycrystalline silicon electrodes 14 having a film thickness of 5000 Å and a sheet resistance of 30 ohms/sq.cm is formed so as to contact with the impurity-doped regions (diffused regions) 10 through contact holes 18. Further, an insulating film 16 and third polycrystalline silicon electrodes 15 having a film thickness of 5000 Å and a sheet resistance of 15 ohms/sq.cm are formed, and a phosphosilicate glass layer (P_2O_5, 2 mole-% in concentration) 9 having a thickness of 8000 Å is deposited. Thereafter, a contact hole 17 is provided, and aluminium electrodes 41 are formed. The electrode 41 of one cell is connected in succession to the electrode 41 of the adjacent cells in the lateral direction, while a word line 31 which is the extension 31 of the date electrode of said one cell is connected in succession to the extension 31 of the gate electrode of the adjacent cells in the longitudinal direction. The second polycrystalline silicon electrodes 14, the insulating film 16 and the third polycrystalline silicon electrodes 15 constitute a storage capacitance. In this case, a SiO_2 film, a film of high permittivity such as a Si_3N_4 film and Ta_2O_5 film or a multiple insulating layer including these films in combination can be used, whereby a large storage capacitance can be obtained. Accordingly, in the case where the same value as that of the storage capacitance employed in the prior-art memory cell is to be attained, the area may be smaller. By way of example, consider cases where a SiO_2 film, Si_3N_4 film and Ta_2O_5 film each being 800 Å thick are employed as the insulating film. Let us assume that the diameter of the contact hole is 2 μm, that the mask alignment tolerance is 2μm, that the width of the polycrystalline silicon gate is 6 μm, that the width of the impurity-doped layer (diffused layer) is 6μm, and that the storage capacitance is 0.22 pF. Then, the memory cell areas per bit are 725 μm^2, 297μm^2 and 192μm^2, respectively. These areas are 78%, 32% and 21% of the memory cell area 925 μm^2 of the prior-art type memory fabricated under the same design values, respectively. Although, in the above, one layer of storage capacitance has been referred to for the sake of brevity, a plurality of layers of storage capacitance can of course be provided as may be needed.

The above described memory cell has information written thereinto and read therefrom as stated below. After fixing the third polycrystalline silicon electrode 15 to the earth potential, a positive voltage is applied to the word line 31. Thus, the switching transistor 1 is rendered conductive. Subsequently, a voltage corresponding to "0" or "1" is applied to the electrode 41 forming a data line. Thus, charges representative of the information are stored into the storage capacitance 2. The read-out of the information is carried out by rendering the switching transistor 1 conductive and thereafter detecting the potential change of the data line 41. In the above described memory cell, no large diffused layer is employed for forming the storage capacitance, and hence, any leakage current based thereon does not flow. This has the advantage that the storage time becomes long.

Referring next to the second embodiment shown in Figures 5 and 6, contact holes 18 and 17 for bringing impurity-doped regions (diffused regions) 10 and 13 into contact with the second polycrystalline silicon electrodes 14 and the aluminium electrodes 41 respectively are formed by self alignment.

By adopting the self-aligned contact system, a number of advantages accrue. By way of example, when the memories of the present embodiment are fabricated by using as an insulating film 16 a SiO_2 film, Si_3N_4 film and Ta_2O_5 film each being 800 Å thick and on the basis of the design values mentioned previously, the memory cell areas are 675μm^2, 270μm^2 and 176 μm^2,

These areas are 73%, 29% and 19% of the memory cell area of 925 μm^2 of the prior-art type memory fabricated under the same design values, respectively.

Referring now to the third embodiment shown in Figures 7 and 8, the isolation of elements in the lateral direction (the direction of the data lines) is effected in such a way that a negative voltage is applied to first polycrystalline silicon electrode 20 formed on a $Si0_2$ film 21 being 800 Å thick. This measure will hereinafter be referred to as the "field shield method". The field shield method has been already described in, for example. "Shielded Silicon Gate Complementary MOS Integrated Circuit" by Hang Chang Lin, Jack L. Halsor and Paul J. Hayes, IEEE Transactions on Electron Devices Vol. 19, No. 11, pp.1199 - 1207. By adopting self-aligned contacts and the field shield method, further advantages can be achieved. For example, changes in the diameter of a contact hole attributed to the lateral oxidation (bird beaks) which occur in the case of forming an isolation oxide layer by the local oxidation, and leakage current due to, for example, a crystal defect at an end of the isolation oxide layer diminish. Furthermore, the self-aligned contact system is facilitated. The point of the memory cell area is substantially the same as in the case of Figures 5 and 6. In the first three embodiments the second polycrystalline silicon electrode 14, the insulating film 16 and the third polycrystalline silicon electrode 15 which constitute the storage capacitance 2 can be worked without requiring any mask alignment tolerance by the self-aligned etching.

WHAT WE CLAIM IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of memory cells arranged in matrix form on one surface of said semiconductor substrate, each of said memory cells comprising a source region, a channel region and a drain region, which are provided in a surface portion of said semiconductor substrate; a first conductive substance which is provided in opposition to said channel region above a gate insulating film and which serves as a gate electrode; a first insulating film disposed on said first conductive substance; and at least one storage capacitance unit comprising a second conductive substance which is in contact with either of said source region and said drain region and a part of which is superimposed on said first conductive substance above said first insulating film, a second insulating film which is provided on said second conductive substance, and a third conductive substance which is provided on said second insulating film.

a third insulating film disposed on said memory cells;

a data line disposed on said third insulating film and connecting whichever of said course region and said drain region which is not in contact with said second conductive substance, through a contact hole formed through said third insulating film, with the corresponding region of memory cells belonging to the same column of the matrix.

2. A semiconductor memory device according to claim 1, including a word line connecting said first conductive substance of one cell with the corresponding region of memory cells belonging to the same row of the matrix.

3. A semiconductor memory device according to claim 1 or claim 2, wherein whichever of said source and drain regions is in contact with said data line is common to a pair of adjacent memory cells belonging to said date line.

4. A semiconductor memory device according to any one of the preceding claims wherein adjacent memory cells are insulated from one another by a polycrystalline silicon layer which is provided over the substrate on an insulating film and to which a voltage is applied.

5. A semiconductor memory device according to any one of the preceding claims wherein adjacent memory cells are isolated from one another by a thick insulating film which is provided on the substrate surface.

6. A semiconductor memory device constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 3 and 4; or Figures 5 and 6; or Figures 7 and 8; of the accompanying drawings.

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FIG. 1

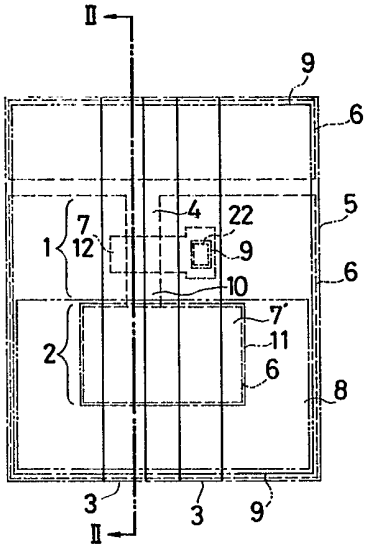

FIG. 2

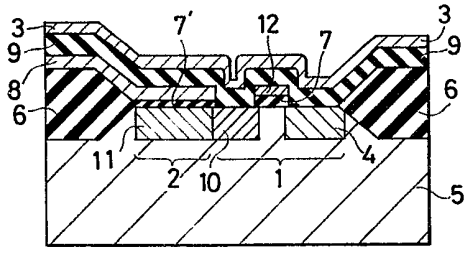

FIG. 3

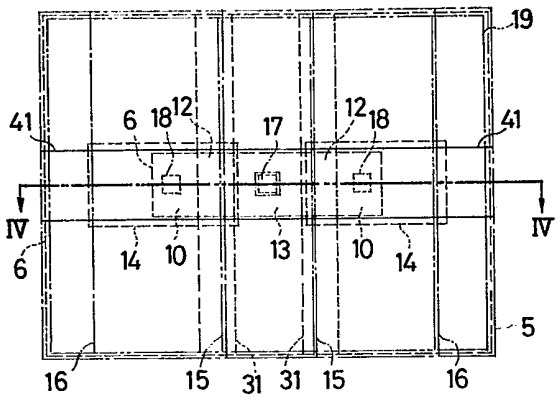
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FIG. 4

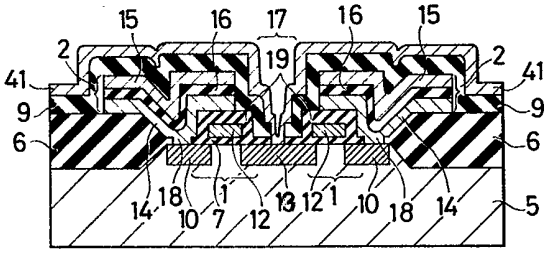
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FIG. 5

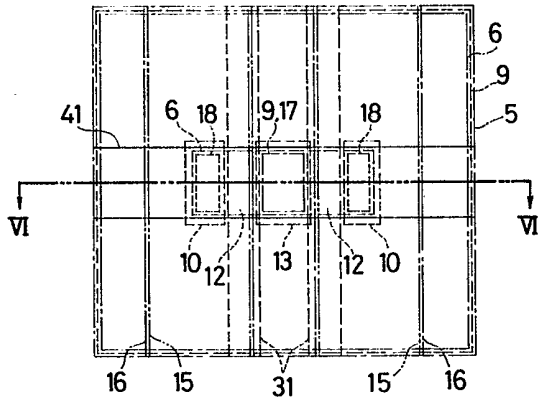
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FIG. 6

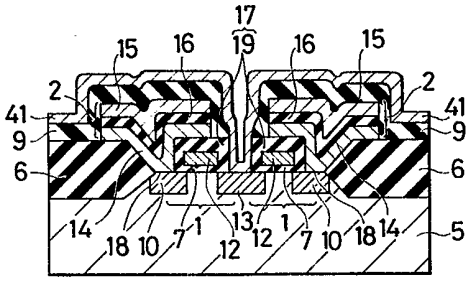
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FIG. 7

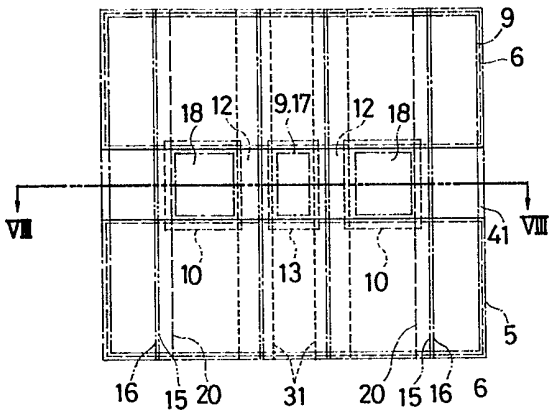
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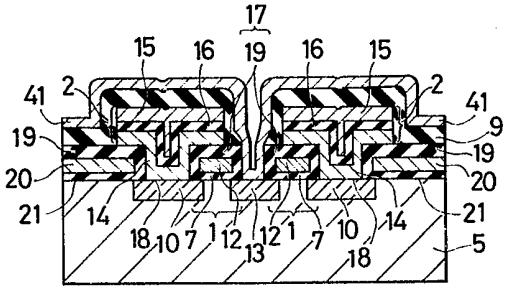
FIG. 8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