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(71) Applicant: **PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED**
Arundel Great Court 8 Arundel Street
London WC2R 3DT(GB)

(84) Designated Contracting States:
GB

(71) Applicant: **N.V. Philips' Gloeilampenfabrieken**
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

(84) Designated Contracting States:
CH DE FR LI SE

(72) Inventor: **Philips, Ian**
TMC LIMITED Swindon Road
Malmesbury Wiltshire(GB)

(72) Inventor: **Mulkerrin, Robert Anthony**
TMC LIMITED Swindon Road
Malmesbury Wiltshire(GB)

(74) Representative: **Andrews, Arthur Stanley et al,**
Philips Electronic and Associated Industries Limited
Patent Department Mullard House Torrington Place
London WC1E 7HD(GB)

(54) Alpha-numeric display device and visual display arrangement employing such devices.

(57) An alpha-numeric display device comprises seven rows of five elements (1-35) in which each element (6-10) of the second row is connected to the corresponding element (11-15) in the third row so that a single signal controls both element. Similarly each element (21-25) in the fifth row is connected to the corresponding element (26-30) in the sixth row. In addition the second element (2) in the first tow may be conected (36) to the fourth element (4) in the first row. A full alpha-numeric character set may be generated by appropriately energising selected elements. Since the display device effectively comprises either twenty four or twenty five elements rather than thirty five elements the number of electrical connections required is reduced. In addition the quantity of information required to be stored to drive the display is also reduced.

The elements (1-35) may be formed as liquid crystal cells and a plurality of devices may be formed into a multi-character display arrangement. When addressing the display devices in matrix form either a five row by five column matrix or two four row by three column matrices may be used depending on whether the link (36) between the second (2) and fourth (4) elements of the first row is provided.

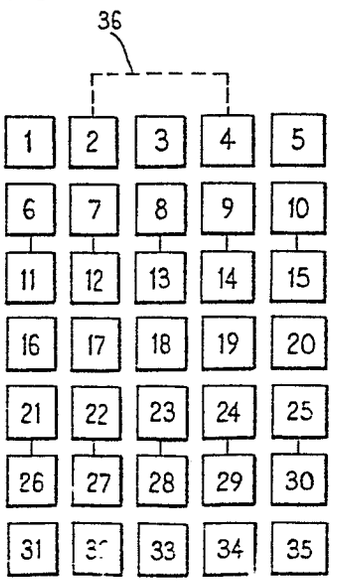

FIG.1

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ALPHA-NUMERIC DISPLAY DEVICE AND VISUAL DISPLAY ARRANGEMENT EMPLOYING SUCH DEVICES.

The invention relates to an alpha-numeric display device comprising seven rows of five display elements. The invention also relates to a visual display arrangement including a plurality of such alpha-numeric display devices.

When a plurality of display devices are used to provide a multi-character display it is usual to multiplex the drive to the display to reduce the number of external connections required. A commonly used method of interconnection with displays made from light emitting diodes is to connect together all those elements that have the same location in each display device and then to address each display device individually. However, this method of time division multiplexing is not widely used with liquid crystal displays because of limitations in the electro-optic response of liquid crystals which, at present, prevent the effective sequential addressing of more than three or four display devices. To produce liquid crystal visual display arrangements having a greater number of characters (display devices) each display device can be configured as a matrix. A description of a matrix addressed liquid crystal display array is given in an article entitled "Multiplexing Liquid Crystal Displays" by Paul Smith which appeared in Electronics dated 25th May 1978 at pages 113 to 121, the contents of which are hereby incorporated by reference.

The seven by five dot matrix array display device is normally used when a full alpha-numeric display is required and in order to drive such a device a seven by five matrix is needed. Thus five terminals are required for each character in a multi-character display plus seven terminals for the common connection to all the characters. This implies a 1 to 7 multiplex ratio. With present LCD elements such a high multiplex ratio tends to lead to a low contrast display. It is preferable to keep to the multiplex ratio to around 4 to 1. This could be achieved by splitting the 7 by 5 array into a 4 by 5 and a 3 by 5 array. However this would increase the number of connections needed to each display device to

an unacceptable number.

It is an object of the invention to provide a display device which is capable of displaying a full set of alpha-numeric characters and which may be driven in a way which requires a smaller number of connections than the standard seven row by five column matrix device.

The invention provides a alpha-numeric display device as set forth in the opening paragraph characterised in that each element in the second row is connected to or formed integrally with the corresponding element in the third row and that each element in the fifth row is connected to or formed integrally with the corresponding element in the sixth row.

Since twenty of the display elements are connected together in pairs this means that only twenty five elements need to be directly addressable. Such a display device may be driven as a five row by five column matrix array. Matrix addressing is particularly applicable to liquid crystal displays since other forms of element such as light emitting diodes or incandescent lamps are not normally driven in this manner. However, a device according to the invention still provides the advantage that the display driving information required to be stored is reduced in proportion to the reduced number of drivable elements.

The second element in the first row may be connected to the fourth element in the first row. This reduces the number of elements which can be separately addressed and selected and enables the display device to be configured as two four row by three column matrices.

The invention further provides a visual display arrangement for displaying a plurality of alpha-numeric characters comprising a plurality of such display devices, in which the display devices are driven in time division multiplex form.

The visual display arrangement may be such that each display device is electrically arranged as two four row by three column matrices, that the driving signals are applied to the four rows of each device simultaneously from a common source and that the

electrical driving signals applied to the three columns of each display device are generated from separate information sources.

An embodiment of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows schematically an alpha-numeric display device according to the invention,

Figure 2 shows an alpha-numeric character set which can be generated with a display device according to the invention,

Figure 3 shows one set of electrodes and their interconnections for a display device as shown in Figure 1 in which the display elements are formed as liquid crystal cells.

Figure 4 shows the other set of electrodes and their interconnections for a display device as shown in Figure 1 in which the display elements are formed as liquid crystal cells.

Figures 5a and 5b show in schematic form the electrical connection of one part of the display device shown in Figures 3 and 4 as two four row by three column matrices.

Figure 6 shows some waveforms of electrical driving signals for the display device of Figures 3 and 4,

Figure 7 shows in block schematic form a visual display arrangement according to the invention,

Figure 8 shows a logic diagram of a first embodiment of a multiplex waveform generator suitable for use in the arrangement of Figure 7,

Figure 9 shows a logic diagram of a second embodiment of a multiplex waveform generator suitable for use in the arrangement of Figure 7,

Figure 10 shows waveforms of signals used in third and fourth embodiments of multiplex waveform generators for use in the arrangement of Figure 7,

Figure 11 shows a logic diagram of a third embodiment of a multiplex waveform generator suitable for use in the arrangement shown in Figure 7, and

Figure 12 shows a logic diagram of a fourth embodiment of a multiple waveform generator suitable for use in the arrangement shown in Figure 7.

Figures 1 shows in schematic form a display device comprising thirty five display elements 1 to 35 arranged in seven rows of five elements. The display elements 6 to 10 in the second row are connected to corresponding ones of the display elements 11 to 15 in the third row. Similarly the display elements 21 to 25 in the fifth row are connected to corresponding ones of the display elements 26 to 30 in the sixth row. The display elements 2 and 4 in the first row may also be connected together via a link 36. The display elements may be formed in any convenient manner and could be, for example, light emitting diodes, liquid crystal cells or blocks of material having faces of contrasting colours, the blocks being selectively positionable to show a desired coloured face. If the link 36 is omitted all the elements in the first fourth and seventh rows are individually selectable, while elements in the second row are selectable only with the corresponding element in the third row and elements in the fifth row are selectable only with the corresponding element in the sixth row. Thus there are twenty fiveaddressable elements in the array. If the link between elements 2 and 4 is provided the number of addressable elements in reduced to twenty four.

The connection between the connected elements may be either a mechanical coupling when the display elements are constructed from blocks of material having contrasting coloured faces or may be electrical connections where light emitting diodes or liquid crystal cells are used. A possible modification to this embodiment is to make the elements of the second and third rows into elongate elements so that a single element covers both the second and third row in any position along the row. A similar arrangement may be used for rows 5 and 6.

Figure 2 shows an alpha-numeric character set which can be displayed by appropriately energising the elements of the display device shown in Figure 1. It can be seen from Figure 2 that a recognisable character can be generated to represent each numeral from 0 to 9 and each letter of the alphabet. The character set

shown in Figure 2 is not the only character set which could be generated using the display device of Figure 1. Various modifications could be made to individual characters particularly if the link 36 is omitted.

It is not essential that each display element is square but rather the elements may be shaped to provide a more aesthetically pleasing or readable character. The relative sizes and spacing of the element may be changed to provide the most readable character for a given size of display device.

Figures 3 and 4 show the electrodes and their connections in a display device of the type shown in Figure 1, in which the display elements are formed by liquid crystal cells. The display elements are configured as two matrices for addressing. The first matrix mainly corresponds to the upper half of the character while the second matrix mainly corresponds to the lower half of the character. Figure 3 shows the separate connections for each character while Figure 4 shows the common connections for all the display devices in a serial array.

For each display device (character) in the serial array the upper matrix comprises elements 1 to 15, 17, 19 and 20, while the lower matrix comprises the other display elements. In the upper matrix a first connection S1 is connected to electrodes 1a, 6a, 7a, 11a, 12a and 17a; a second connection S2 is connected to electrodes 2a, 3a, 4a, 8a, 13a and 19a; and a third connection S3 is connected to electrodes 5a, 9a, 10a, 14a, 15a and 20a. These electrodes are one electrode of the correspondingly numbered display element of Figure 1. In the serial direction of the array a connection B1 is connected to electrodes 1b, 2b, 4b and 5b; a connection B2 is connected to electrodes 7b, 3b, 9b, 12b and 14b; a connection B3 is connected to electrodes 6b, 11b, 13b, 8b, 15b and 10b; and a connection B4 is connected electrodes 17b, 19b and 20b. These electrodes form the other electrode of the liquid crystal cell which makes up the display element of the corresponding number.

Similarly for the second matrix which provides the lower half of the character connection S4 is connected to electrodes 31a, 26a,

21a, 16a, 22a and 27a; connection S5 is connected to electrodes 33a, 32a, 28a, 23a and 18a; and connection S6 is connected to electrodes 34a, 35a, 29a, 24a, 25a and 30a. In the serial direction of the array connection B5 is connected to electrodes 16b, 18b, 25b and 30b; connection B6 is connected to electrodes 22b, 27b, 23b, 28b, 24b and 29b; connection B7 is connected to electrodes 26b, 21b, 32b and 35b; and connection B8 is connected to electrodes 31b, 33b and 34b.

Depending on the signals applied to the first and second electrodes of the elements the liquid crystals forming elements will become either transparent or opaque and hence by selectively applying appropriate signals to the connections S1 to S6 and B1 to B8 the display devices can be operated to display a desired character.

With a matrix addressed liquid crystal display each element together with its associated back plane is electrically equivalent to a lossy non-linear voltage dependent capacitor. Thus each display device may be represented schematically as row and column conductors interconnected at each intersection by a capacitor as shown in Figures 5a and 5b. The reference numbers of the capacitors are the same as those of the elements which they represent. A series of select pulses drives each row while a series of data pulses drives each column. Figures 6b, c,d and e show the waveforms of the select pulses applied to the back plane terminals B1 to B4 and B5 to B8 respectively. The basic waveform of period T is shown in Figure 6a. Each period T is divided in 8 sub-periods t_1 to t_8. Each row is selected for a quarter of the period T by taking the basic waveform shown in Figure 6f and modifying it to produce a positive going pulse in the first half of the period T and a negative going pulse in the second half of the period T. The positive going pulses occur for 1/8 of the period T, the periods t_1,t_2,t_3 and t_4 corresponding to the periods of the positive going pulses for the rows B1,B2,B3 and B4 respectively or B5,B6,B7 and B8 respectively. Similarly the negative going pulses also occur for 1/8 of the period T, the periods t_5,t_6,t_7 and t_8

corresponding to the periods of negative going pulses for the rows B1,B2,B3 and B4 respectively or B5,B6,B7 and B8 respectively.

Examples of data pulses which may be applied to the columns S1,S2 and S3 or S4,S5 and S6 are shown in Figures 6f to 6j. Referring to the line S1, the waveform shown in Figure 6f will cause all the elements 1,7,12,6,11 and 17 to be off; the waveform shown in Figure 6g will cause element 1 only to switch on; the waveform shown in Figure 6h will cause elements 7 and 12 to switch on; the waveform shown in Figure 6i will cause elements 6 and 11 to switch on; and the waveform shown in Figure 6j will cause element 17 to switch on. It will be readily apparent that these waveforms shown in Figure 6f to 6j may be combined to select several of the elements simultaneously. Similarly,referring to the line S4, the waveform shown in Figure 6f will cause all the elements 16,22,27,21,26 and 31 to be off; the waveform shown in Figure 6g will cause element 16 only to switch on; the waveform shown in Figure 6h will cause elements 22 and 27 to switch on; the waveform shown in Figure 6j will cause elements 21 and 26 to switch on;and waveform j will cause element 31 only to switch on. It will be readily apparent that these waveforms shown in Figure 6 f to j may be combined to select more than one of the elements simultaneously.

In a particular construction the amplitude of the waveforms in Figures 6a to j may be as shown in the Figure. The liquid crystal elements are operated by a.c. signals and the contrast ratio is dependent on the RMS voltage of the a.c. signal across the element. Using the waveform shown in Figure 6 it can be derived that the RMS voltage across an element which is switched off is 1 volt and that across an element which is switched on is 1.73 volts. Other voltages may be used dependent on the requirements of the liquid crystals cells used.

Figure 7 shows in block schematic form an arrangement for driving an n character display; where n is an integer, for example 16. Such a display may, for example, be used on a telephone instrument to display the number dialled or to display simple messages such as NUMBER ENGAGED.

The arrangement shown in Figure 7 has an input terminal 100 to which input data in the form of characters to be displayed is fed. The input data may be in the form of a serial ASCII code which is clocked into a shift register 101 under the control of a clock signal on a line 102 which is generated in a clock signal generator 103. The clock signals produced by the generator 103 must either be synchronised with the input data or some means must be provided to synchronise the clock and data. When a character has been received it is fed in parallel to a decoder 104 over lines 105-1 to 105-n. The decoder 104 which may be in the form of a read only memory (ROM) produces outputs which are fed via an appropriate one of the lines 106-1 to 106-n to an encoder 107 which converts the decoded character into an element code which indicates which elements of the display device are to be driven to display that character. The encoder 107 may also be formed by a ROM and may be combined with the ROM 104 to provide the element drive code directly from the input code. The output of the encoder 107 is fed via lines 108-1 to 108-n and clocked into a register 109 in parallel under the control of clock signals from a clock signal generator 103 over a line 110. A further clock signal causes the data to be read out of the register 109 into a selected one of a plurality of registers 111-1 to 111-n, the particular register being selected by means of address signals generated in the clock generator 103 and fed to the registers 111-1 to 111-n over lines 112-1 to 112-n. The outputs of the register 111-1 to 111-n are fed via lines 113-1 to 113-n to inputs of respective multiplex waveform generators 114-1 to 114-n. The multiplex waveform generators 114-1 to 114-n are also fed with clock signals from the clock generator 103 over lines 115-1 to 115-n. The multiplex waveform generators 114-1 to 114-n produce three separate waveforms at three separate outputs, the three waveforms being for application to respective ones of the lines S1,S2 and S3 of each individual display device. These waveforms are fed via respective driver circuits 116-1 to 116-n to the S1,S2 and S3 inputs of each device within a display unit 117.

The clock pulse generator 103 is connected via a line 118 to a further multiplex waveform generator 119 which generates the four waveforms which are applied via a driver circuit 120 to lines B1,B2,B3 and B4 of the display unit 117, the lines B1,B2,B3 and B4 of each display device in the display unit 117 being serially connected.

The arrangement so far described up to but not including the display arrangement 117 is duplicated in the box indicated 125. The arrangement in box 125 produces the driving signals for the S4,S5 and S6 inputs of each of the display devices and the B5,B6,B7 and B8 lines of the display unit 117. Thus block 125 produces the signals for the lower half of each character.

In the following description of the operation of the arrangement only the generation of the driving signals for the upper half of each character will be described in detail. The generation of the signals for the lower half of each character is achieved in the same manner.

In operation the characters to be displayed are encoded and fed to the input 100 and read into the shift register 101. If the encoded characters are present in parallel form then a parallel input register will be used instead of the shift register 101. When a data word corresponding to a single character has been read into the shift register 101 a clock signal on line 102 causes the parallel outputs of the shift register 101 to be connected to the inputs of the decoder 104 which converts the ASCII code to individual characters and causes one of the lines 106-1 to 106-n to be activated to address the encoder 107. The individual characters are encoded by the encoder 107 into a code which indicates which of the display elements are to be operated to form the top half of the character. The encoder 107 produces a 12 bit binary code for that purpose and this code is read into the register 109 under the control of clock signals from the clock signal generator 103 over the line 110. The output from the register 109 is fed under the control of further clocks signals on line 110 to a selected one of the registers 111-1 to 111-n, the particular register being

selected by an address generated in the clock signal generator 103. Normally the registers 111-1 to 111-n will be addressed sequentially whenever information to be displayed is changed and the addresses generated will allow for the display of blank characters e.g. to mark the end of complete words. For this purpose the address generator section of the display needs to have an indication of when a new character or set of characters is available and is/are to be displayed. This would be derived from the source of the characters for example when push buttons are depressed or from the output of a computer. It should be noted that the registers 111-1 to 111-n are only addressed when the information to be displayed is altered. The outputs of the register 111-1 to 111-n are connected to respective multiplex waveform generators 114-1 to 114-n which generate the waveforms required to drive the corresponding individual character display devices. These waveforms are generated with the aid of clock signals from the clock signal generator 103 which are conveyed to the multiplex waveform generators over the lines 115-1 to 115-n. The multiplex waveform generators produce waveforms such as those shown in Figure 6f to j, the precise waveform produced being dependent on the contents of the register 111 associated with it. Each multiplex waveform generator 114 produces three separate waveforms which are for application to the S1,S2 and S3 lines of its associated display device via respective driver circuits 116.

A further multiplex waveform generator 119 generates the waveforms which are applied to the B1,B2,B3 and B4 lines of all the display devices in the display unit 117. The waveforms generated by the multiplex waveform generator 119 are not dependent on the character to be displayed and are generated with the aid of clock pulses fed from the clock pulse generator over line 118. Signals produced by the multiplex waveform generator 119 are fed to the display unit 117 via the driver circuit 120.

Clearly it is not essential to duplicate all the driving circuitry for each half of each character. The input shift register 101, decoder 104, encoder 107 and register 109 could drive

both halves of the circuit separately and be common to both halves. Similarly the clock generator 103 may be common to both sections as may also be multiplex waveform genertor 119 and driver 120 with the B1 connection being directly connected to the B5 connection, the B2 connection beomg directly connected to the B6 connection, the B3 connection being directly connected to the B7 connection and the B4 connection being directly connected to the B8 connection. Also, the register 111 could be common to both halves of the display. The actual partition will depend on the practicalities of the number of connections to the integrated circuits required in each particular case.

Figure 8 shows part of one embodiment of the multiplex waveform generators 114-1 to 114-n. Each multiplex waveform generator comprising three of the circuits shown in Figure 8. As shown in Figure 8 the first terminal 201 is connected to the first input of an AND gate 211 and to the first input of an AND gate 221. The output of AND gate 211 is connected to a control input of an analogue switch 231 while the output of the gate 221 is connected to a control input of an analogue switch 241. The pole of switch 231 is connected to a first input 251 of a single pole eight way switch 260 while the pole of switch 241 is connected to a second input 252 of the switch 260. A first terminal of switch 231 is connected to 0V while a second terminal is connected to 2V A first terminal of the switch 241 is connected to 3V while a second terminal is connected to 1V. As can be seen from Figure 8 three further identical arrangements are provided to which input terminals 202,203 and 204 are connected and which are connected to inputs 253 to 258 of the switch 260.

The pole 259 of the switch 260 is the output of the multiplex waveform generator and is connected to the line S1. The timing signals t_1 to t_8 are also connected to a control input 261 of the switch 260 and are operative to cause the pole 259 of the switch to be connected to selected inputs at the appropriate time, that is to input 251 during time t_1 to input 252 during time t_5 and so on.

Thus to produce the waveform shown in Figure 6g a logical '1'

is applied to terminal 201 and and logical '0' to terminals 202,203 and 204. As a result of this the AND gate 211 produces a logical '1' at its output during the time t_1 and causes the pole of switch 231 to be connected to 0V. Hence 0V is applied to input 251 of the switch 260. During the period t_1 the pole of 259 of switch 260 is connected to input 251 and hence 0V is applied to line S1. During the periods t_2 to t_4 the pole switch 260 is connected to inputs 253,255 and 257 in turn. As the inputs 202,203 and 204 are at a logical '0' the poles of switches 232,233 and 234 are all connected to 2V and hence during the periods t_2 to t_4 line S1 carries 2V. Similarly during the period t_5 the pole of switch 241 carries 3V and hence this voltage is transferred to the line S1 during the time t_5 but during the periods t_6 to t_8 the poles of switches 242 to 244 are connected to 1V and hence line S1 is at 1Vfrom t_6 to t_8.

Similarly if a logical '1' is applied to terminal 202 a voltage of 0V will be applied to line S1 during the period t_2 and during the period t_6 a voltage of 3V will be applied to the line S1. The signal applied to terminal 203 will determine the voltages applied to line S1 during the periods t_3 and t_7 and the signal applied to terminal 204 will determine the voltages applied to the line S1 during the periods t_4 and t_8.

To complete the multiplex waveform generators 114-1 to 114-n two further identical arrangements are provided which produce the outputs for lines S2 and S3 from the other 8 bits of information received from the registers 111-1 to 111-n, the arrangement shown using the first four bits from the respective register 111.

The multiplex waveform generator 119 which provides the driving waveforms shown in Figures 6b to e, produces unchanging waveforms, that is waveforms which do not change with the characters to be displayed. Consequently the multiplex waveform generator 119 receives a clock signal input but not data inputs. The embodiment of the multiplex waveform generator 119 shown in Figure 9comprises four similar circuits the only difference between the circuits being the timing signals applied to them. The first circuit comprises two controlled single pole changeover switches

301 and 302, the switching of which is controlled by timing signals t_1 and t_5 respectively. The poles of switches of 301 and 302 are connected to first and second inputs of a further controlled single pole changeover switch 303, the pole of which is connected to B1. The control input of switch 303 is connected to the output of an RS bistable circuit 304 which is set by the timing pulse t_1 and reset by the timing pulse t_5.

In operation when the pulse t_1 occurs switch 301 is set so that the movable contact connects the pole to 3V and the bistable 304 is set so that the pole of switch 303 is connected to the pole of switch 301. Consequently during the period t_1 3V is applied to the line B1. At the end of the period t_1 the pole of switch 301 is connected to 1V but the state of switch 303 remains unchanged and hence 1V is applied to the line B1 until the start of the period t_5. At the start of the period t_5 the pole of switch 302 is connected to 0V and the bistable 304 is reset thus causing the pole of switch 303 to be connected to switch 302. Thus during the period t_5 0V is applied to the line B1. At the end of the period t_5 the pole of switch 202 is connected to 2V but the state of switch 303 remains unchanged and hence 2V is applied to the line B1 for the periods t_6 to t_8. Consequently the line B1 is at 3V during t_1, 1V from t_2 to t_4, 0V during t_5 and 2V from t_6 to t_8. Similarly switches 311,312 and 313 bistable 314 and timing pulses t_2 and t_6 produce the waveform on line B2; switches 321,322,323, bistable 341 and timing pulses t_3 and t_7 produce the waveform on B3; and switches 331,332 and 333 bistable 334 and timing pulses t_6 and t_8 produce the waveform on line B4.

The clock signal generator 103 comprises an oscillator and a number of divider and decoder stages to produce the required timing and address waveforms. It is not necessary for the input data clocks, that is the clocking of the shift register 101, register 109 and registers 111-1 to 111-n, to be synchronised with the waveforms of the multiplex waveform generators. The clock rate for the registers may be chosen to suit the speed of the technology

chosen to implement them and the rate at which a character data is applied. Clearly if the character data is received serially the shift register 101 must be clocked at the data rate. Similarly there must be external inputs to the clock signal generator to enable the appropriate characters or registers to be reset when new display information is to be received so that the information can be routed to the appropriate display device.

Alternative arrangements for the multiplex waveform generators 114 and 119 are illustrated in Figures 11 and 12 respectively and waveforms generated in the clock pulse generator 103 and applied to the multiplex waveform generators 114 and 119 are shown in Figure 10. The waveforms shown in Figure 10 comprise square waves of period T each half of the square wave is divided into four periods P_0, P_1, P_2, P_3 and signals corrsponding to these periods are generated in the clock pulse generator 103 by means of appropriate divider and decoder circuits. In this embodiment the waveform shown in Figure 10a has peak amplitudes of 1V and 2V, the waveform shown in Figure 10b has peak amplitudes of 0V and 3V, the waveform shown in Figure 10c has peak amplitudes of 1V and 2V, and the waveform shown in Figure 10d has peak amplitudes of 0V and 3V.

Figure 11 shows an alternative form for the multiplex waveform generator 119 which generates the backplane waveforms for application to the terminals B1,B2,B3 and B4 or B5,B6,B7 and B8 of the display arrangement 117. The multiplex waveform generator shown in Figure 11 comprises four changeover switching arrangements 400, 401, 402, and 403, a control input of which is conected to control signal input terminals 410, 411, 412, and 413 respectively. The waveform shown in Figure 10a is applied to a first contact of each switching arrangement via terminals 420, 421, 422, and 423, respectively, while the waveform shown in Figure 10b is applied to a second contact of each switching arrangement via terminals 430, 431, 432, and 433 respectively. The pole of each switching arrangement is connected to respective output terminals 440, 441, 442, and 443 which carry the signals for application to the terminals B1,B2,B3, and B4 or B5,B6,B7, and B8 of the display

arrangement 117. Thus, in operation, signals P_0, P_1, P_2, and P_3 are applied to the respective changeover switching arrangements 400,401,402 and 403 and cause the changeover switches to change state for the periods P_0, P_1, P_2 and P_3, respectively. Hence during the period P_0 the waveform shown in Figure 10b is applied to terminal 440 as the signal B1 (or B5) while the waveform shown in Figure 10a is applied to terminals 441,442, and 443. Similarly during the period P_1 the waveform shown in Figure 10b is applied to terminal 441 as the signal B2 (or B6) while the waveform shown in Figure 10a is applied to the terminals 440, 442, and 443. During the periods P_2 and P_3 the waveform shown in Figure 10b is applied to terminals 442 and 443, respectively (as signals B3 or B7 and B4 or B8) while the other terminals carry the waveform shown in Figure 10a.

Figure 12 shows an alternative form for the waveform generator 114-n, the arrangement in Figure 12 being triplicated to form the complete waveform generator 114-n. The arrangement shown in Figure 12 comprises four two input AND gates 500,501,502 and 503 having respective first inputs connected to terminals 510,511,512 and 513 and respective second inputs connected to terminals 520,521,522 and 523. The outputs of the AND gates 500 to 503 are conected to respective inputs of a four input OR gate 530 whose output is connected to a control input of a changeover switching arrangement 531. First and second contacts of the changeover switching arrangement 531 are connected to respective input terminals 532 and 533 while the pole of the changeover switching arrangement 531 is connected to an output terminal 534. The output terminal 534 is arranged to convey the signal S1, S2, or S3 (or S4,S5 or S6) to each display device in the display arrangement 117.

In operation data signals D1,D2,D3, and D4 are applied to the first inputs of the AND gates 500,501,502, and 503, the data signals being derived from the register 111, while the timing signal P_0, P_1, P_2, and P_3 are applied to the second inputs of the AND gates 500,501,502, and 503. The waveform shown in Figure 10c is applied to the terminal 532 while the waveform shown in Figure

10d is applied to the terminal 533. Thus for each period P_0, P_1, P_2, and P_3 the state of the appropriate data signal will determine which of the waveforms applied to the terminals 532 and 533 will be passed to the output terminal 534. Consequently any combination of elements in the display can be selected by the application of appropriate data signals D1 to D4.

The switches shown in Figures 8, 9, 11 and 12 are in the form of solid state switches which may be take different forms depending on the technology used to produce a display arrangement, for example bipolar or MOS integrated circuits using small, medium or large scale integration. Such switching arrangements are well known to those skilled in the art.

The form of the display devices shown in Figure 1 enables a full alpha-numeric character set to be displayed while reducing the multiplex factor that needs to be used in a matrix addressed display device. Further the display information required to be stored is reduced by approximately 30%. When producing a display arrangement in the form of a LSI circuit in combination with the display unit a significant overall saving in chip area can be achieved.

While the detailed embodiments have been described with reference to the display devices of liquid crystal cells any other form of display element could be used, although the driving circuitry would have to be re-designed to suit the characteristics of the particular display device. The advantage of a smaller quantity of stored information required would still exist. The arrangement described with reference to Figures 7 to 9 or 7 and 10 to 12 particularly suited to the display device in which the link 36 is provided. If the link 36 is omitted it would be more convenient to drive the display in the form of a five row by five column matrix rather than two four row by three column matrices. While particular forms of multiplex waveform generators and driving circuitry have been described persons skilled in the art would readily appreciate that many alternative arrangements would be possible.

CLAIMS:

1. An alpha-numeric display device comprising seven rows of five display elements characterised in that each element of the second row is connected to or is formed integrally with the corresponding element in the third row and each element in the fifth row is connected to or formed integrally with the corresponding element in the sixth row.

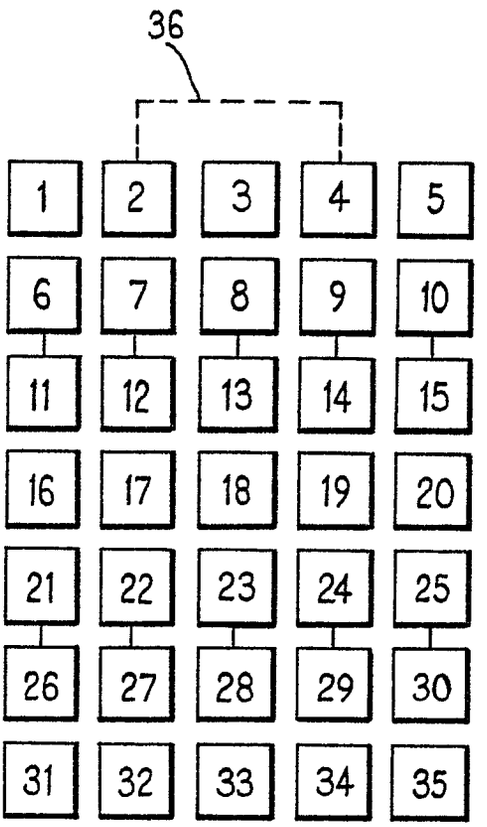
2. An alpha-numeric display device as claimed in Claim 1, in which the second in the first row is connected to the fourth element in the first row.

3. An alpha-numeric display device as claimed in Claim 1 or 2, in which each display element comprising a liquid crystal cell.

4. A visual display arrangement for displaying a plurality of alpha-numeric characters comprising a plurality of display devices as claimed in any of Claims 1 to 3.

5. An arrangement as claimed in Claim 4, in which the display devices are driven in time division multiplex form.

6. An arrangement as claimed in Claim 5 when dependent on Claim 2, characterised in that each display device is electrically arranged as two four row by three column matrices, that for each matrix electrical driving signals are applied to the four rows in each display device simultaneously from a common source and that the electrical driving signal applied to three columns of each matrix of each display device are generated from separate information sources.


36
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
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27
28
29
30
31
32
33
34
35

FIG.1

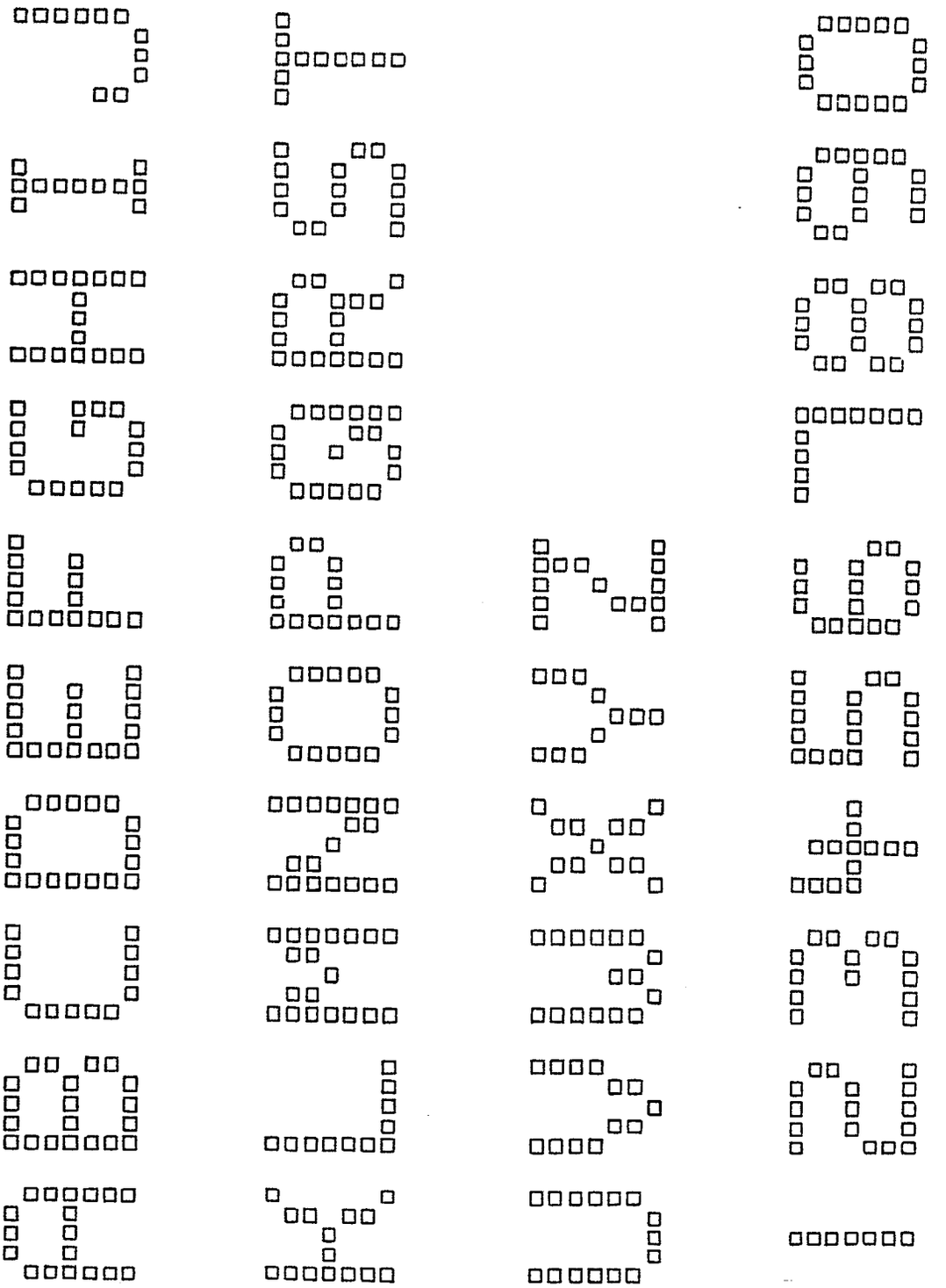

FIG.2

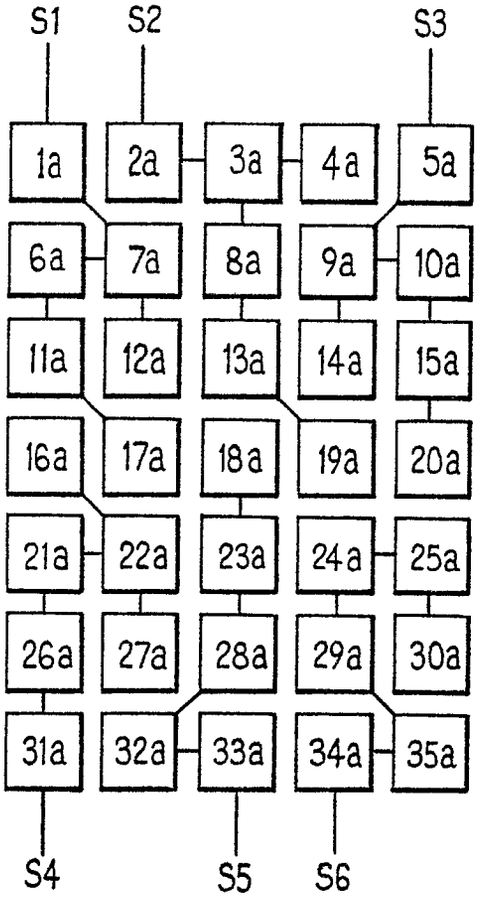
S1
S2
S3
1a
2a
3a
4a
5a
6a
7a
8a
9a
10a
11a
12a
13a
14a
15a
16a
17a
18a
19a
20a
21a
22a
23a
24a
25a
26a
27a
28a
29a
30a
31a
32a
33a
34a
35a
S4
S5
S6

FIG.3

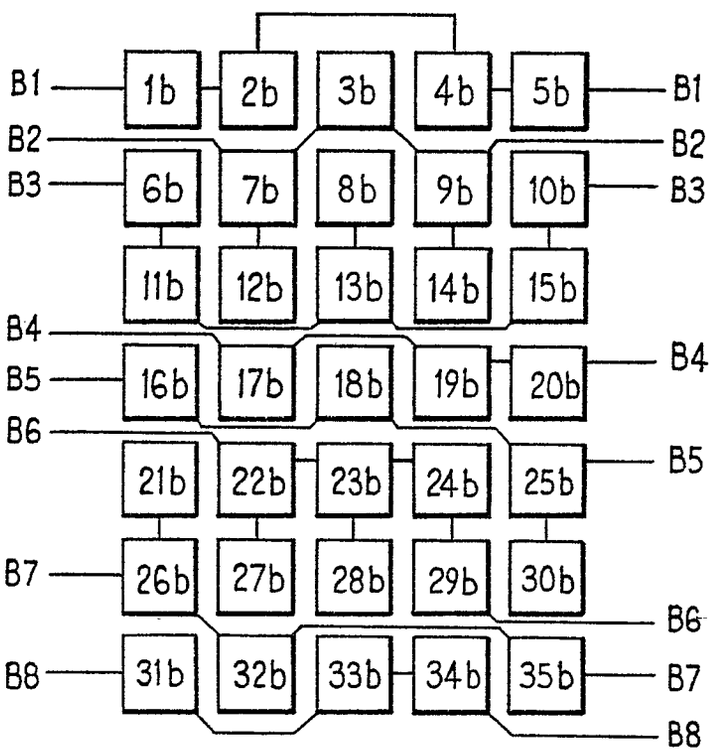
B1
B2
B3
B4
B5
B6
B7
B8
1b
2b
3b
4b
5b
6b
7b
8b
9b
10b
11b
12b
13b
14b
15b
16b
17b
18b
19b
20b
21b
22b
23b
24b
25b
26b
27b
28b
29b
30b
31b
32b
33b
34b
35b

FIG.4

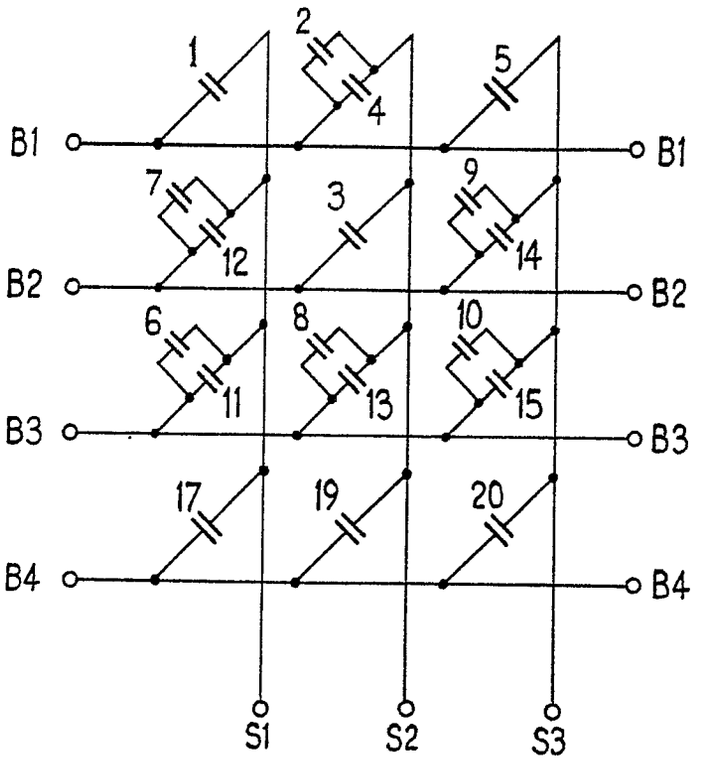
1
2
4
5
B1
B1
7
12
3
9
14
B2
B2
6
11
8
13
10
15
B3
B3
17
19
20
B4
B4
S1
S2
S3

FIG.5a

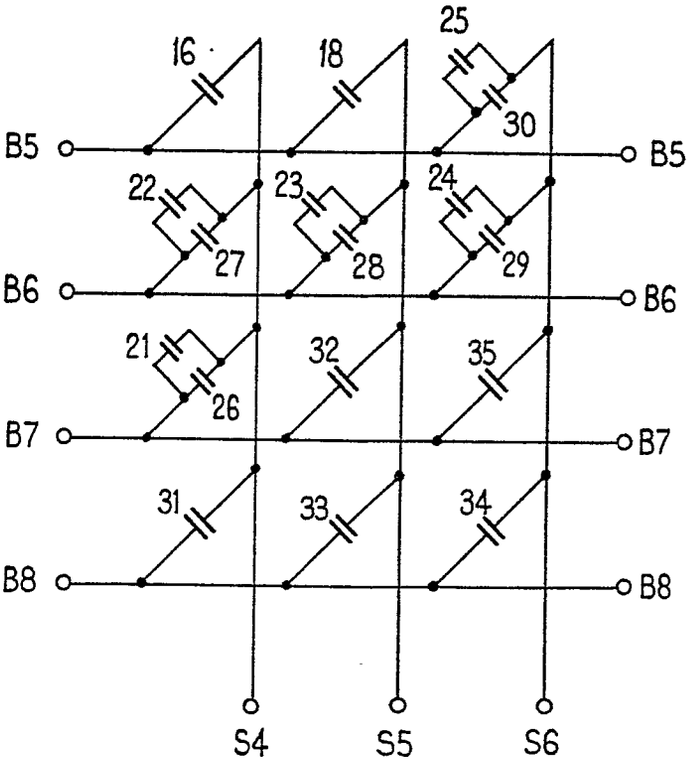
16
18
25
30
B5
B5
22
27
23
28
24
29
B6
B6
21
26
32
35
B7
B7
31
33
34
B8
B8
S4
S5
S6

FIG.5b

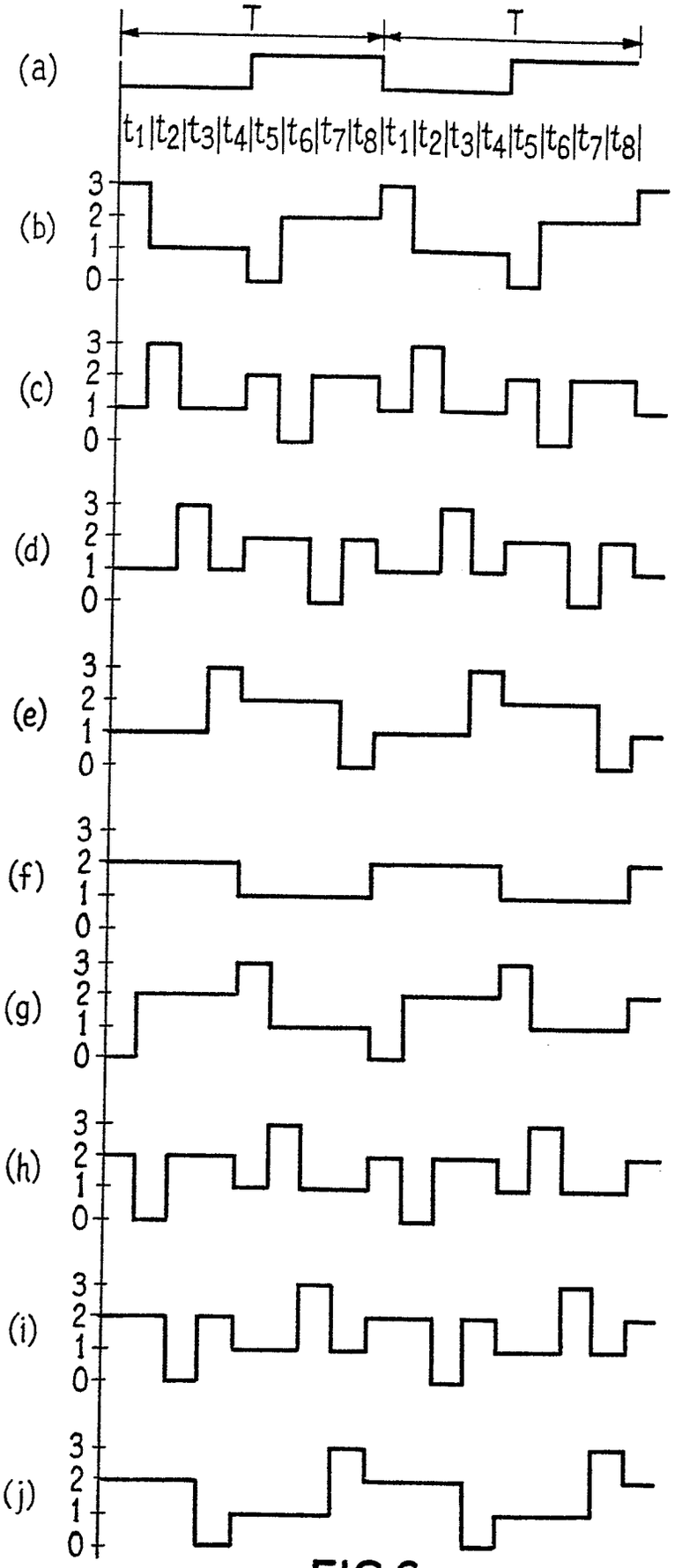

FIG.6

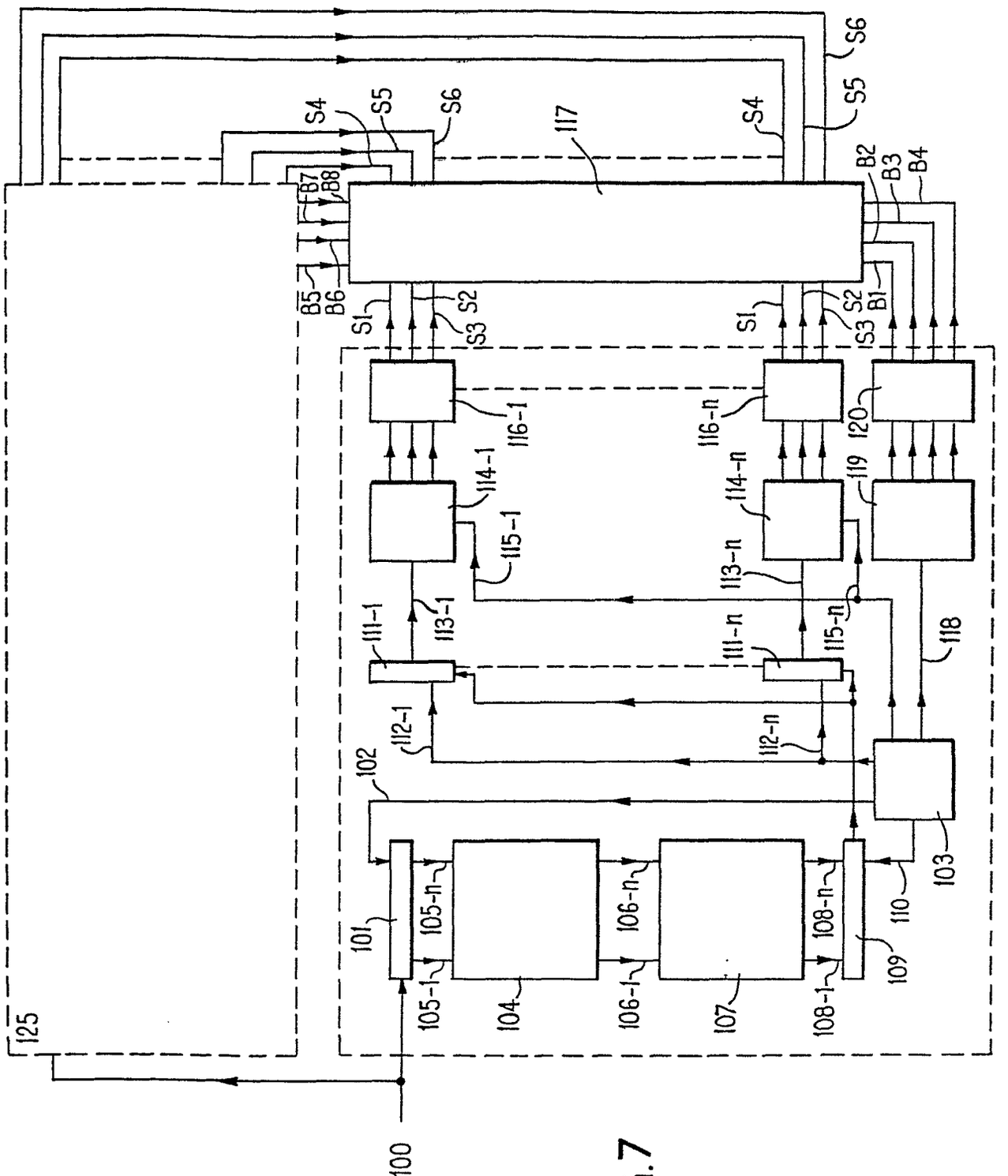
S6
S5
S4
S5
S6
117
S4
B2
B3
B4
B7
B8
B5
B6
S1
S2
S3
S1
S2
S3
B1
116-1
116-n
120
114-1
114-n
119
115-1
113-n
111-1
113-1
111-n
115-n
118
112-1
112-n
102
101
105-n
106-n
108-n
110
103
109
105-1
104
106-1
107
108-1
125
100

FIG.7

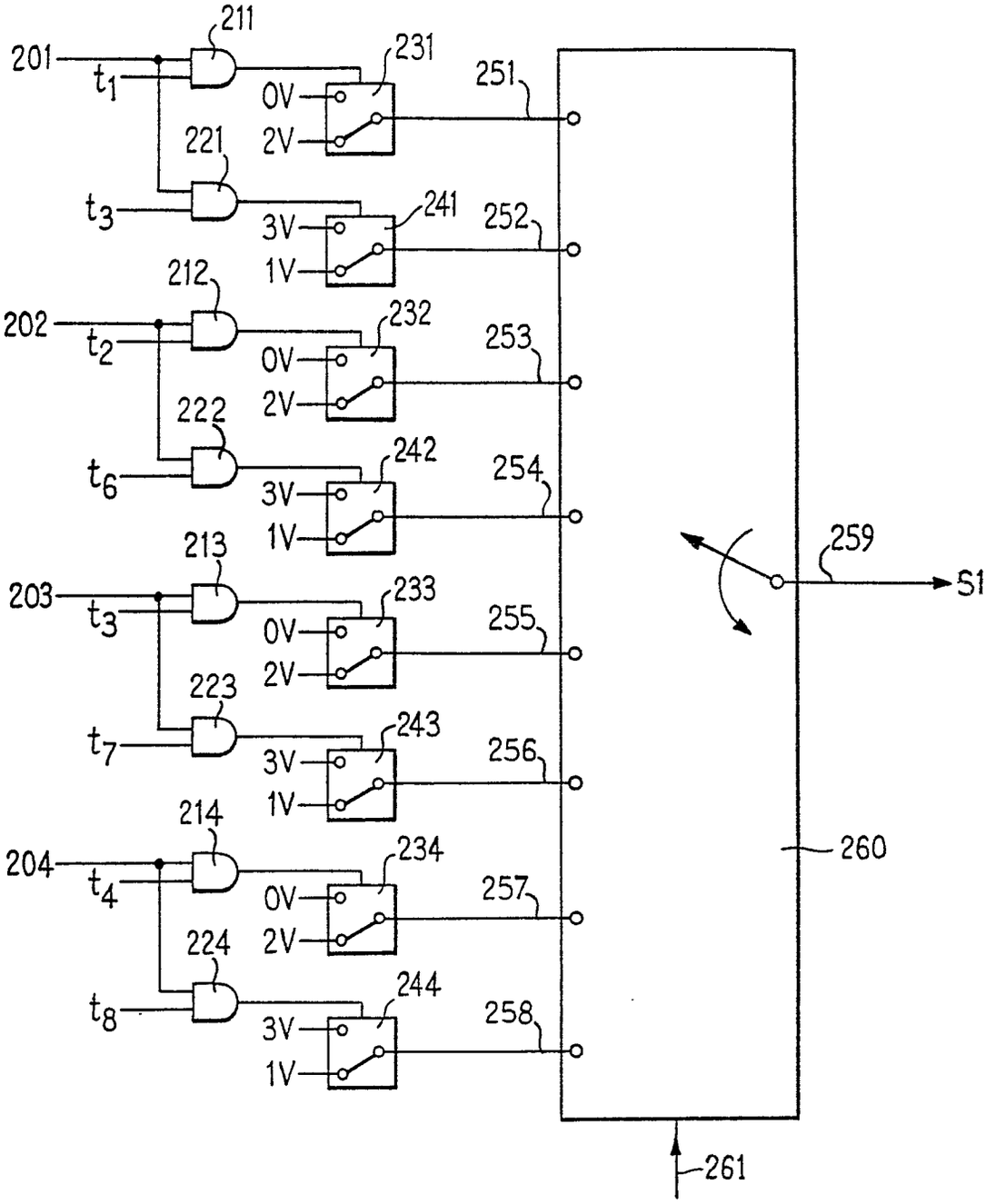
201
t_1
211
231
0V
2V
251
221
t_3
241
3V
1V
252
202
t_2
212
232
0V
2V
253
222
t_6
242
3V
1V
254
203
t_3
213
233
0V
2V
255
223
t_7
243
3V
1V
256
204
t_4
214
234
0V
2V
257
224
t_8
244
3V
1V
258
259
S1
260
261

FIG.8

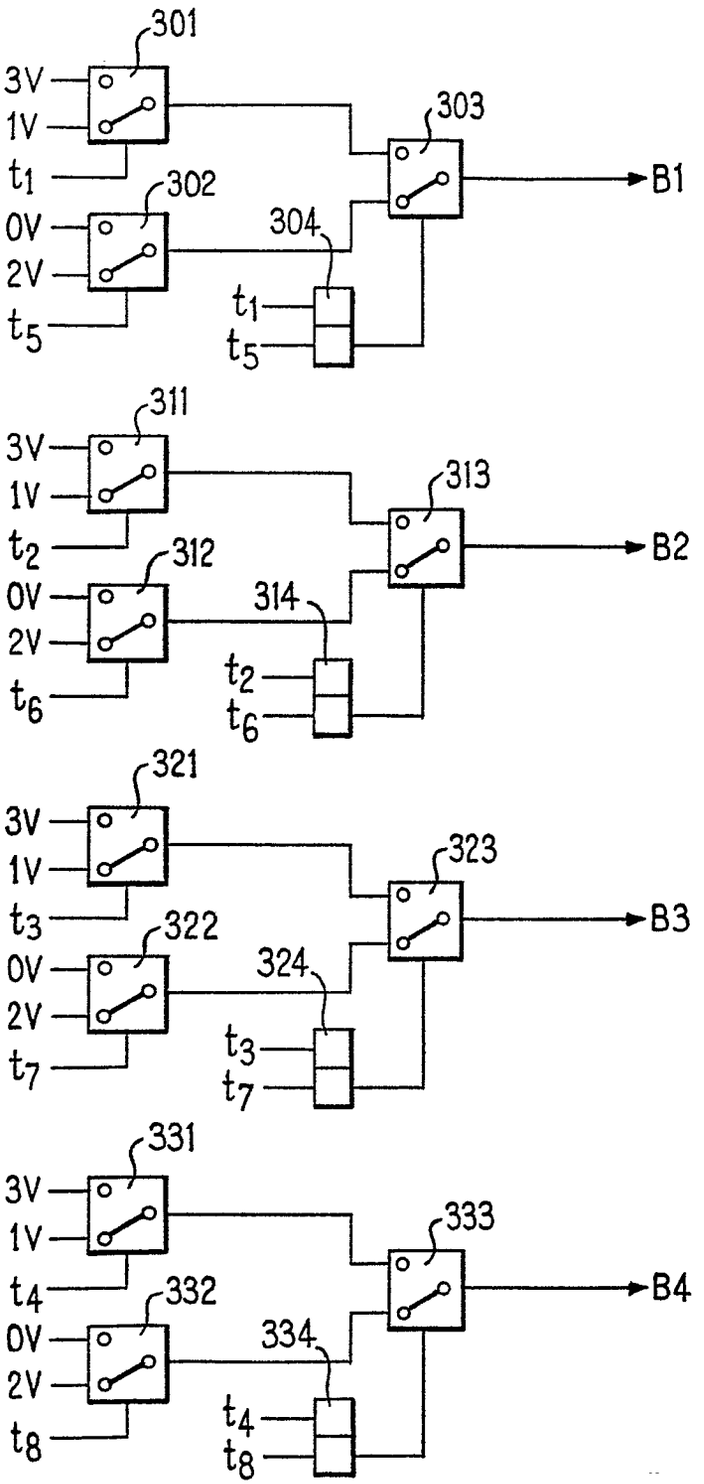
301
3V
1V
t1
302
0V
2V
t5
303
304
t1
t5
B1
311
3V
1V
t2
312
0V
2V
t6
313
314
t2
t6
B2
321
3V
1V
t3
322
0V
2V
t7
323
324
t3
t7
B3
331
3V
1V
t4
332
0V
2V
t8
333
334
t4
t8
B4

FIG. 9

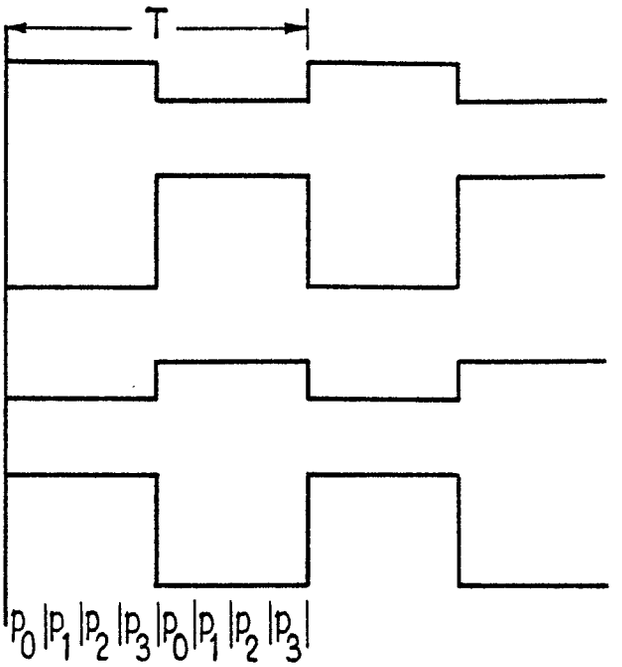

FIG.10

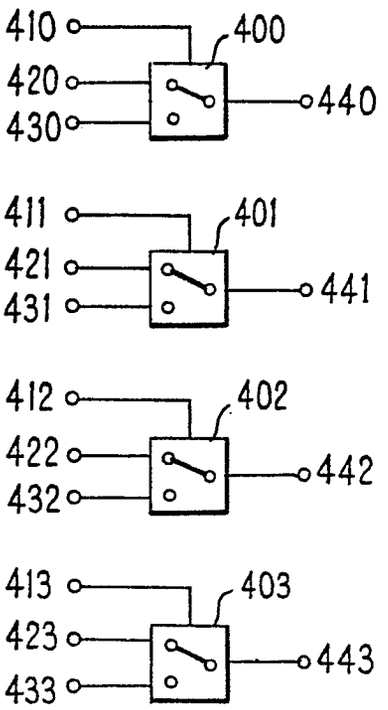

FIG.11

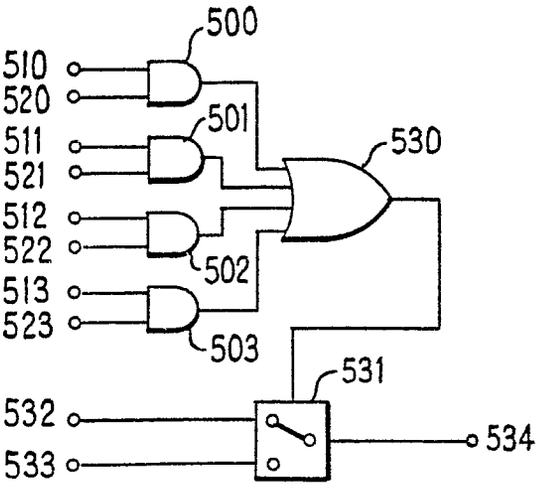

FIG.12