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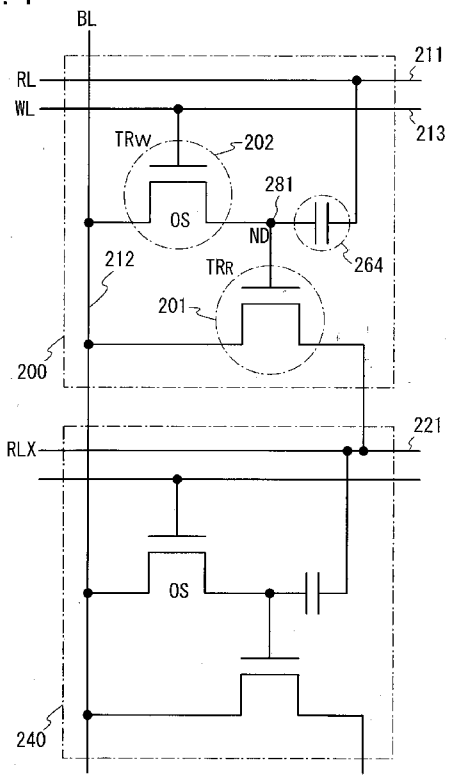
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[Continued on next page]

(54) Title: SEMICONDUCTOR DEVICE AND METHOD OF DRIVING SEMICONDUCTOR DEVICE

FIG. 1



(57) Abstract: The number of wirings per unit memory cell is reduced by sharing a bit line by a writing transistor and a reading transistor. Data is written by turning on the writing transistor so that a potential of the bit line is supplied to a node where one of a source and drain electrodes of the writing transistor and a gate electrode of the reading transistor are electrically connected, and then turning off the writing transistor so that a predetermined amount of charge is held in the node. Data is read by using a signal line connected to a capacitor as a reading signal line or a signal line connected to one of a source and drain electrodes of the reading transistor as a reading signal line so that a reading potential is supplied to the reading signal line, and then detecting a potential of the bit line.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD OF DRIVING SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The invention disclosed herein relates to a semiconductor device using a semiconductor element and a method of driving the semiconductor device.

BACKGROUND ART

[0002]

Memory devices using semiconductor elements are broadly classified into two categories: volatile memory devices that lose memory data when power supply stops, and non-volatile memory devices that store memory data even when power supply stops.

[0003]

A typical example of a volatile memory device is a DRAM (dynamic random access memory). A DRAM stores data in such a manner that a transistor included in a memory element is selected and charge is held in a capacitor.

[0004]

When data is read from a DRAM, charge in a capacitor is lost on the above-described principle; thus, another writing operation is necessary whenever data is read out. Moreover, a transistor included in a memory element has leakage current and charge flows into or out of a capacitor even when the transistor is not selected, so that a data (information) storing time is short. For that reason, another writing operation (refresh operation) is necessary at predetermined intervals, and it is difficult to reduce power consumption sufficiently. Furthermore, since memory data is lost when power supply stops, an additional memory device using a magnetic material or an optical material is needed in order to store the data for a long time.

[0005]

Another example of a volatile memory device is an SRAM (static random

access memory). An SRAM stores memory data by using a circuit such as a flip-flop and thus does not need a refresh operation. This means that an SRAM has an advantage over a DRAM. However, cost per memory capacity is increased because a circuit such as a flip-flop is used. Moreover, as in a DRAM, memory data in an SRAM is lost when power supply stops.

[0006]

A typical example of a non-volatile memory device is a flash memory. A flash memory includes a floating gate between a gate electrode and a channel formation region in a transistor and stores data by holding of charge in the floating gate. Therefore, a flash memory has advantages in that a data storing time is extremely long (almost permanent) and a refresh operation which is necessary in a volatile memory device is unnecessary (e.g., see Patent Document 1).

[0007]

However, a gate insulating layer included in a memory element deteriorates by tunneling current generated in writing, so that the memory element stops its function after a predetermined number of writing operations. In order to reduce adverse effects of this problem, a method in which the number of writing operations for memory elements is equalized is employed, for example. However, complicated supplemental circuits are additionally needed to realize this method. Moreover, employing such a method does not solve the fundamental problem of lifetime. In other words, a flash memory is not suitable for applications in which data is frequently rewritten.

[0008]

In addition, a high voltage is necessary for holding of charge in the floating gate or removal of the charge, and a circuit for generating a high voltage is also necessary. Further, it takes a relatively long time to hold or remove charge, and it is not easy to perform writing and erasing at higher speed.

[Reference]

[Patent Document]

[0009]

[Patent Document 1] Japanese Published Patent Application No. S57-105889

DISCLOSURE OF INVENTION

[0010]

In view of the foregoing problems, an object of one embodiment of the disclosed invention is to provide a semiconductor device with a novel structure, in which memory data can be stored even when power is not supplied and in which there is no limitation on the number of times of writing.

[0011]

It is another object to provide a semiconductor device with higher integration and larger memory capacity.

[0012]

It is another object to provide a highly reliable semiconductor device with stable operation.

[0013]

It is another object to provide a semiconductor device capable of high-speed operation.

[0014]

It is another object to provide a semiconductor device which consumes low power.

[0015]

Each embodiment of the invention disclosed in this specification achieves at least one of the above objects.

[0016]

One embodiment of the present invention is a semiconductor device including a nonvolatile memory cell, a reading signal line, a bit line, and a word line. The nonvolatile memory cell includes a reading transistor, a writing transistor including an oxide semiconductor, and a capacitor. One of a source electrode and a drain electrode of the writing transistor and a gate electrode of the reading transistor are electrically connected to one electrode of the capacitor. The other electrode of the capacitor is electrically connected to the reading signal line. One of a source electrode and a drain electrode of the reading transistor is electrically connected to a reading signal line of a different memory cell. The other of the source electrode and the drain electrode of the writing transistor and the other of the source electrode and the drain electrode of the reading transistor are electrically connected to the bit line. A gate electrode of the

writing transistor is electrically connected to the word line.

[0017]

Another embodiment of the present invention is a semiconductor device including a nonvolatile memory cell, a reading signal line, a bit line, and a word line. The nonvolatile memory cell includes a reading transistor, a writing transistor including an oxide semiconductor, and a capacitor. One of a source electrode and a drain electrode of the writing transistor and a gate electrode of the reading transistor are electrically connected to one electrode of the capacitor. One of a source electrode and a drain electrode of the reading transistor is electrically connected to the reading signal line. The other of the source electrode and the drain electrode of the writing transistor and the other of the source electrode and the drain electrode of the reading transistor are electrically connected to the bit line. A gate electrode of the writing transistor is electrically connected to the word line. The other electrode of the capacitor is electrically connected to a reading signal line of a different memory cell.

[0018]

Another embodiment of the present invention is a semiconductor device including a nonvolatile memory cell, a first wiring, a second wiring, and a third wiring. The nonvolatile memory cell includes a first transistor, a second transistor, and a capacitor. One of a source electrode and a drain electrode of the second transistor and a gate electrode of the first transistor are electrically connected to one electrode of the capacitor. The other electrode of the capacitor is electrically connected to the first wiring. One of a source electrode and a drain electrode of the first transistor is electrically connected to a first wiring of a different memory cell. The other of the source electrode and the drain electrode of the second transistor and the other of the source electrode and the drain electrode of the first transistor are electrically connected to the second wiring. A gate electrode of the second transistor is electrically connected to the third wiring.

[0019]

Another embodiment of the present invention is a semiconductor device including a nonvolatile memory cell, a first wiring, a second wiring, and a third wiring. The nonvolatile memory cell includes a first transistor, a second transistor, and a capacitor. One of a source electrode and a drain electrode of the second transistor and

a gate electrode of the first transistor are electrically connected to one electrode of the capacitor. One of a source electrode and a drain electrode of the first transistor is electrically connected to the first wiring. The other of the source electrode and the drain electrode of the second transistor and the other of the source electrode and the drain electrode of the first transistor are electrically connected to the second wiring. A gate electrode of the second transistor is electrically connected to the third wiring. The other electrode of the capacitor is electrically connected to a first wiring of a different memory cell.

[0020]

In any of the semiconductor devices, a transistor including an oxide semiconductor is used as the writing transistor or the second transistor, whereby frequency of refresh operations can be extremely low.

[0021]

In any of the semiconductor device, the off-state current of the writing transistor or the second transistor is preferably lower than the off-state current of the reading transistor or the first transistor.

[0022]

In the semiconductor device, the second transistor preferably includes a material having an energy gap larger than 3 eV.

[0023]

In the semiconductor device, the switching rate of the first transistor is preferably higher than the switching rate of the second transistor.

[0024]

Another embodiment of the present invention is a method of driving a semiconductor device in which data writing is performed in the following manner. When the first transistor is in an off state, the second transistor is turned on. Through the second transistor, a potential of the second wiring is supplied to a node where one of the source electrode and the drain electrode of the second transistor is connected to the gate electrode of the first transistor, and the second transistor is turned off, whereby a predetermined amount of charge is held in the node.

[0025]

Another embodiment of the present invention is a method of driving a

semiconductor device in which data stored in a node is read in the following manner: after supplying charge to a second wiring such that the second wiring has a second potential when a second transistor is in an off state, a first potential is supplied to a first wiring of a different memory cell to which one of a source electrode and a drain electrode of a first transistor is connected, a reading potential is supplied to a first wiring which is connected to a capacitor, and a potential of the second wiring is detected.

[0026]

Another embodiment of the present invention is a method of driving a semiconductor device in which data stored in a node is read in the following manner: after supplying charge to a second wiring such that the second wiring has a second potential when a second transistor is in an off state, a first potential is supplied to a first wiring to which one of a source electrode and a drain electrode of a first transistor is connected, and a potential of the second wiring is detected.

[0027]

Note that the first potential is different from the second potential.

[0028]

Note that in this specification and the like, a nonvolatile semiconductor device indicates a semiconductor device which can store data for a given period of time or longer (1×10^4 seconds or longer, preferably 1×10^6 seconds or longer) even when no power is supplied thereto.

[0029]

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating layer" can mean the case where there is an additional component between the gate insulating layer and the gate electrode. Moreover, the terms such as "over" and "below" are only used for convenience of description and can include the case where the relation of components is reversed, unless otherwise specified.

[0030]

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is

sometimes used as part of a "wiring", and vice versa. Furthermore, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or "wirings" are formed in an integrated manner.

[0031]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be replaced with each other in this specification.

[0032]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric function. There is no particular limitation on an object having any electric function as long as electric signals can be transmitted and received between components that are connected through the object.

[0033]

Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0034]

With one embodiment of the present invention, the area of a semiconductor device can be reduced. Thus, a semiconductor device with higher integration and larger memory capacity can be provided.

[0035]

Since data writing does not need a high voltage, problems such as deterioration of a gate insulating layer do not easily arise; thus, the number of times data can be rewritten is greatly increased, and reliability is greatly increased.

[0036]

Furthermore, data is written depending on the on state and the off state of the transistor, and operation for erasing data is not needed, whereby high-speed operation can be easily realized.

[0037]

A transistor including an oxide semiconductor is used for a memory cell,

whereby memory data can be stored for a quite long period of time. In other words, power consumption of the semiconductor device can be reduced because a refresh operation becomes unnecessary or the frequency of refresh operations can be extremely low. Moreover, memory data can be stored for a long time even when power is not supplied.

[0038]

By using a combination of a transistor including an oxide semiconductor and a transistor including a material other than an oxide semiconductor which can be operated at high speed, various circuits (such as a logic circuit and a driver circuit) which are required to be operated at high speed can be favorably realized.

BRIEF DESCRIPTION OF DRAWINGS

[0039]

FIG. 1 is a circuit diagram of a semiconductor device.

FIG. 2 is a circuit diagram of a semiconductor device.

FIG. 3 is a circuit diagram of a semiconductor device.

FIGS. 4A and 4B are timing charts showing operation of a semiconductor device.

FIG. 5 is a circuit diagram of a semiconductor device.

FIG. 6 is a circuit diagram of a semiconductor device.

FIG. 7 is a circuit diagram of a semiconductor device.

FIGS. 8A and 8B are timing charts showing operation of a semiconductor device.

FIGS. 9A and 9B are a cross-sectional view and a plan view of a semiconductor device.

FIGS. 10A to 10H are cross-sectional views showing manufacturing steps of a semiconductor device.

FIGS. 11A to 11E are cross-sectional views showing manufacturing steps of a semiconductor device.

FIGS. 12A and 12B are a cross-sectional view and a plan view of a semiconductor device.

FIGS. 13A to 13D are cross-sectional views showing manufacturing steps of

the semiconductor device.

FIGS. 14A and 14B are a cross-sectional view and a plan view of a semiconductor device.

FIGS. 15A to 15C are cross-sectional views showing manufacturing steps of the semiconductor device.

FIGS. 16A and 16B are cross-sectional views showing manufacturing steps of the semiconductor device.

FIGS. 17A to 17F are diagrams each illustrating an electronic device including a semiconductor device.

FIG. 18 is a graph showing characteristics of a transistor including an oxide semiconductor.

FIG. 19 is a circuit diagram for evaluating characteristics of a transistor including an oxide semiconductor.

FIG. 20 is a timing chart for evaluating characteristics of a transistor including an oxide semiconductor.

FIG. 21 is a graph showing characteristics of a transistor including an oxide semiconductor.

FIG. 22 is a graph showing characteristics of a transistor including an oxide semiconductor.

BEST MODE FOR CARRYING OUT THE INVENTION

[0040]

Hereinafter, embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be construed as being limited to the description in the following embodiments.

[0041]

A transistor is a kind of semiconductor elements and can achieve amplification of current or voltage, a switching operation for controlling conduction or non-conduction, or the like. A transistor in this specification includes an

insulated-gate field effect transistor (IGFET) and a thin film transistor (TFT).

[0042]

Note that the position, the size, the range, or the like of each structure illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like as disclosed in the drawings and the like. Note also that in each of circuit diagrams, in some cases, "OS" is written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

[0043]

In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not mean limitation of the number of components.

[0044]

(Embodiment 1)

In this embodiment, a circuit structure and operation of a semiconductor device which is one embodiment of the disclosed invention will be described with reference to FIG. 1, FIG. 2, FIG. 3, FIGS. 4A and 4B, and FIG. 5. In this embodiment, the case where n-channel transistors are used will be described.

[0045]

In FIG. 1, the circuit structure of the semiconductor device disclosed in this embodiment is illustrated. The semiconductor device illustrated in FIG. 1 includes a nonvolatile memory cell 200 including a first transistor 201, a second transistor 202, and a capacitor 264. In FIG. 1, a third wiring 213 (also referred to as a word line WL) and a gate electrode of the second transistor 202 (also referred to as a transistor TR_W) are electrically connected to each other. One of a source electrode and a drain electrode of the second transistor 202, a gate electrode of the first transistor 201 (also referred to as a transistor TR_R), and one electrode of the capacitor 264 are electrically connected to one another. The other electrode of the capacitor 264 and a first wiring 211 (also referred to as a reading signal line RL) are electrically connected to each other. One of a source electrode and a drain electrode of the first transistor 201 and a first wiring 221 (also referred to as a reading signal line RL_X) of a memory cell 240, which is different from the memory cell 200, are electrically connected to each other. The other

of the source electrode and the drain electrode of the first transistor 201 and the other of the source electrode and the drain electrode of the second transistor 202 are electrically connected to a second wiring 212 (also referred to as a bit line BL). The first transistor 201 functions as a reading transistor, and the second transistor 202 functions as a writing transistor.

[0046]

The semiconductor device illustrated in FIG. 1 is a three-terminal semiconductor device in which the bit line BL is shared by the writing transistor and the reading transistor, and a wiring is shared as the wiring that is connected to the one of the source electrode and the drain electrode of the reading transistor and as the wiring of the different memory cell, so that the number of connection wirings per unit memory cell is three.

[0047]

The off-state current of the second transistor 202, which is the writing transistor, is 100 zA (1×10^{-19} A) or less, preferably 10 zA (1×10^{-20} A) or less, more preferably 1 zA (1×10^{-21} A) or less at an ambient temperature (e.g., 25 °C). Although such a low off-state current is difficult to achieve with a transistor including a general silicon semiconductor, it can be achieved with a transistor including an oxide semiconductor that is processed under an appropriate condition and has a large energy gap of 3.0 eV to 3.5 eV. Therefore, the transistor including the oxide semiconductor is preferably used as the writing transistor.

[0048]

Further, by using the transistor including the oxide semiconductor as the writing transistor, rising of a writing pulse to the memory cell can be extremely sharp due to a small subthreshold swing (S value).

[0049]

In this embodiment, as the second transistor 202, which is the writing transistor, the transistor including the oxide semiconductor is used. The transistor including the oxide semiconductor has a characteristic of an extremely low leakage current (off-state current) between a source and a drain in an off state. Therefore, by turning off the second transistor 202, charge in a node 281 (also referred to as a node ND) can be held

for a very long time. In the node ND, the one of the source electrode and the drain electrode of the second transistor 202, the gate electrode of the first transistor 201, and the one electrode of the capacitor 264 are electrically connected to one another. In addition, the capacitor 264 facilitates holding of the charge given to the node ND and reading of stored data.

[0050]

As the first transistor 201, which is the reading transistor, a transistor which is operated at high speed is preferably used in order to increase the reading rate. For example, a transistor with a switching rate of 1 nanosecond or less is preferably used as the reading transistor.

[0051]

The off-state current of the first transistor 201 does not need to be as low as that of the second transistor 202. A transistor with a higher switching rate (e.g., a transistor with higher field effect mobility) than the second transistor 202 can be used as the first transistor 201 in order to increase operation speed of the memory cell. That is, as the first transistor 201, a transistor including a semiconductor material other than the oxide semiconductor can be used. Note that in some cases, the off-state current of the first transistor 201 is higher than that of the second transistor 202 depending on the semiconductor material selected. As the semiconductor material used for the first transistor 201, for example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used. Alternatively, an organic semiconductor material or the like may be used. The first transistor 201 including such a semiconductor material can be operated at sufficiently high speed, so that it can perform reading of stored data at high speed. That is, the semiconductor device can be operated at high speed.

[0052]

Note that when the second transistor 202 is in an off state, the node 281 can be regarded as being embedded in an insulator (a so-called floating state) and thus holds charge. That is, the node 281 has the same effect as a floating gate of a floating-gate transistor that is used as a nonvolatile memory element. The off-state current of the second transistor 202 including the oxide semiconductor is smaller than or equal to one hundred thousandth of the off-state current of a transistor including a silicon

semiconductor or the like; thus, loss of the charge accumulated in the node 281 due to a leakage current of the second transistor 202 is negligible. That is, with the second transistor 202 including the oxide semiconductor, a nonvolatile memory cell can be realized.

[0053]

As long as the off-state current of the second transistor 202 is substantially 0 for example, a refresh operation needed for a conventional DRAM can be unnecessary or performed much less often (e.g., about once a month or a year). Accordingly, power consumption of the semiconductor device can be reduced sufficiently.

[0054]

Further, in the semiconductor device disclosed in this embodiment, data can be directly rewritten by rewriting of new data to a memory cell. Therefore, an erasing operation needed for a flash memory or the like is unnecessary, so that a reduction in operation speed due to the erasing operation can be prevented. That is, the semiconductor device can be operated at high speed. In addition, a high voltage needed for writing and erasing operations in a conventional floating gate transistor is unnecessary; thus, power consumption of the semiconductor device can be further reduced.

[0055]

Next, a writing (rewriting) operation of data to the memory cell 200 will be described. First, a potential of the first wiring 211 (the reading signal line RL) connected to the memory cell 200 which is selected as a memory cell to which data is to be written is set to a low-level potential V_{RLL}. Then, a potential of the third wiring 213 (the word line WL) is set to a potential at which the second transistor 202, which is the writing transistor, is turned on, so that the second transistor 202 is turned on. A high-level potential V_{WLH} is given to the third wiring 213 here. Accordingly, a potential of the second wiring 212 (the bit line BL) connected to the selected memory cell 200 is supplied to the node 281 (the node ND). A low-level potential V_{BLL} or a high-level potential V_{BLH} is supplied here. After that, the potential of the third wiring 213 is set to a potential at which the second transistor 202 is turned off, so that the second transistor 202 is turned off; thus, the node 281 is in a floating state, and predetermined charge remains held in the node 281. In the above-described manner,

by accumulating and holding a predetermined amount of charge in the node 281, the memory cell 200 can store data (a writing mode).

[0056]

It is important that the first transistor 201, which is the reading transistor, is kept in an off state throughtout the writing operation. If the first transistor 201 is turned on when V_{BLH} or V_{BLL} is supplied to the node 281, the second wiring 212 (the bit line BL) and the first wiring 221 of the different memory cell 240 are brought into conduction via the first transistor 201. Accordingly, potentials of the second wiring 212 and the first wiring 221 interfere with each other, and accurate data cannot be given to the node 281.

[0057]

The low-level potential V_{RLL} or a high-level potential V_{RLH} is supplied to the first wiring 211. That is, the low-level potential V_{RLL} or the high-level potential V_{RLH} is also supplied to the first wiring 221 of the different memory cell 240. Throughout the writing operation, both the first wiring 211 and the first wiring 221 of the different memory cell 240 are kept supplied with the low-level potential V_{RLL}. When the threshold voltage of the first transistor 201 is represented as V_{th1}, in order to keep the off state of the first transistor 201 in the writing operation, V_{BLH}, V_{RLL}, and V_{th1} are set so as to satisfy Formula 1.

$$V_{BLH} - V_{RLL} < V_{th1} \qquad \text{[Formula 1]}$$

[0058]

In some cases, V_{BLH} is held in a node 281 of a non-selected memory cell. In those cases, in order to select another memory cell which shares the second wiring 212 with the non-selected memory cell and supply V_{BLL} to the selected memory cell, V_{BLL} is supplied to the second wiring 212. At this time, in order to keep the off state of the first transistor 201 of the non-selected memory cell, V_{BLH}, V_{BLL}, and V_{th1} are set so as to satisfy Formula 2. Formula 2 shows that a difference between the high-level potential and the low-level potential supplied to the bit line needs to be smaller than the threshold voltage of the first transistor 201.

$$V_{BLH} - V_{BLL} < V_{th1} \qquad \text{[Formula 2]}$$

[0059]

In the semiconductor device described in this embodiment, charge travel in a gate insulating film (a tunnel insulating film) is not caused in the writing (rewriting) operation unlike a floating-gate transistor, but the charge travel is caused by a switching operation of the second transistor 202. Therefore, there is no limitation on the number of the writing operations in principle, and the resistance to rewriting is extremely high. In addition, a high voltage needed for writing and erasing in the floating-gate transistor is unnecessary; thus, power consumption of the semiconductor device can be reduced.

[0060]

Next, a reading operation in which data stored in a memory cell is read is described. First, the potential of the third wiring 213 is set to a potential at which the second transistor 202, which is the writing transistor, is turned off, so that the second transistor 202 is turned off. A low-level potential V_{WLL} is supplied to the third wiring 213 here. In addition, V_{RLL} is supplied to the first wiring 221 of the different memory cell 240. Next, charge is given (precharging) to the second wiring 212, so that the potential of the second wiring 212 is V_{BLH}. Then, a high-level potential V_{RLH} is supplied as a reading potential to the first wiring 211 of a memory cell from which data is to be read, and the potential of the second wiring 212 at this time is detected, so that data stored in the memory cell can be read (a reading mode). Note that the potential supplied to the second wiring 212 by the precharging is not limited to the above potential as long as the difference between the potential and a potential held in the node 281 is smaller than V_{th1} and the potential is different from the reading potential.

[0061]

The high-level potential V_{RLH} of the first wiring 211 is set so as to satisfy Formula 3 and Formula 4 in the case where the capacitance value of the capacitor 264 is sufficiently larger than the gate capacitance value of the first transistor 201.

$V_{RLH} + V_{BLH} > V_{th1}$ [Formula 3]

$V_{RLH} + V_{BLL} < V_{th1}$ [Formula 4]

[0062]

That is, Formula 3 shows that when V_{RLH} is supplied to the first wiring 211 in the case where V_{BLH} is held in the node 281, a potential of the gate electrode of the first transistor 201 is larger than the threshold voltage V_{th1}, so that the first transistor 201 is

turned on. When the first transistor 201 is turned on, the low-level potential V_{RLL} of the first wiring 221 of the different memory cell 240 is supplied to the second wiring 212 via the first transistor 201.

[0063]

In addition, Formula 4 shows that even when V_{RLH} is supplied to the first wiring 211 in the case where V_{BLL} is held in the node 281, the potential of the gate electrode of the first transistor 201 is smaller than the threshold voltage V_{th1}, so that the first transistor 201 remains in an off state. That is, the potential of the second wiring 212 remains to be the precharged potential (V_{BLH} here).

[0064]

From Formula 3 and Formula 4, the high-level potential V_{RLH}, which is the reading potential, can be set in a range satisfying Formula 5.

$$V_{th1} - V_{BLH} < V_{RLH} < V_{th1} - V_{BLL} \quad \text{[Formula 5]}$$

[0065]

In addition, the reading potential V_{RLH} is preferably set so as to satisfy Formula 6.

$$V_{RLH} = V_{th1} - (V_{BLH} + V_{BLL})/2 \quad \text{[Formula 6]}$$

[0066]

The third wiring 213 (the word line WL) is supplied with the high-level potential V_{WLH} at which the second transistor 202 is turned on or the low-level potential V_{WLL} at which the second transistor 202 remains in an off state. When the threshold voltage of the second transistor 202 is represented as V_{th2}, the high-level potential V_{WLH} and the low-level potential V_{WLL} are set so as to satisfy Formula 7 and Formula 8, respectively.

$$V_{WLH} > V_{th2} + V_{BLH} \quad \text{[Formula 7]}$$

$$V_{WLL} < V_{th2} + V_{BLL} \quad \text{[Formula 8]}$$

[0067]

Note that when the high-level potential V_{RLH} is supplied to the first wiring 211 in the reading mode, among other memory cells connected to the first wiring 211, a first transistor 201 of a memory cell in which a node 281 has V_{BLH} is also turned on; however, the node 281 is in a floating state, so that charge held in the node 281 remains

held.

[0068]

The semiconductor device illustrated in FIG. 1 can be replaced with a circuit illustrated in FIG. 2 in which the components such as the transistors in the semiconductor device include a resistor and a capacitor. That is, in FIG. 2, the first transistor 201 and the capacitor 264 are each regarded as including a resistor and a capacitor. Note that a capacitor in general is formed of two electrodes and a dielectric layer (an insulating layer) that is interposed between the electrodes. In addition, the capacitance value of the capacitor is determined by the area where the two electrodes and the dielectric layer overlap with one another and the thickness and permittivity of the dielectric layer. R1 and C1 denote the resistance value and the capacitance value of the capacitor 264, respectively. The resistance value R1 corresponds to the resistance value which depends on an insulating layer included in the capacitor 264. R2 and C2 denote the resistance value and the capacitance value of the first transistor 201, respectively. The resistance value R2 corresponds to a resistance value which depends on a gate insulating layer at the time when the first transistor 201 is in an on state. The resistance value C2 corresponds to a so-called gate capacitance value. Note that since the resistance value R2 only denotes the resistance value between the gate electrode and the channel formation region of the first transistor 201, in order to clarify this point, part of connection is denoted by a dotted line.

[0069]

Assuming that the resistance value (also referred to as effective resistance) between the source electrode and the drain electrode of the second transistor 202 in an off state is ROS, when $R1 \geq ROS$ and $R2 \geq ROS$ are satisfied, a holding period of charge (also referred to as a data storing period) is determined mainly by the off-state current of the second transistor 202.

[0070]

On the other hand, when the condition is not satisfied, it is difficult to sufficiently secure the holding period even when the off-state current of the second transistor 202 is sufficiently low. This is because a leakage current other than the leakage current generated in the second transistor 202 is high. Therefore, the semiconductor device disclosed in this embodiment desirably satisfies the above

relation.

[0071]

In addition, C1 and C2 desirably satisfy C1 > C2. By making C1 large enough, when the potential of the node 281 is controlled by the first wiring 211 (e.g., when data is read), change in the potential of the first wiring 211 can be efficiently transmitted to the node 281. That is, the difference between V_{RLH} and V_{RLL} can be small, and thus the power consumption of the semiconductor device can be reduced.

[0072]

When the above relation is satisfied, a more preferable semiconductor device can be realized. Note that R1 and R2 are controlled by the gate insulating layers of the first transistor 201 and the second transistor 202. The same relation is applied to C1 and C2. Therefore, the material, the thickness, and the like of the gate insulating layers are desirably set as appropriate to satisfy the above relation.

[0073]

In the case where the dielectric constant εr1 of the insulating layer in the capacitor 264 is different from the dielectric constant εr2 of the gate insulating layer of the first transistor 201, it is easy to satisfy C1 > C2 while $2 \cdot S2 \geq S1$ (desirably, $S2 \geq S1$) is satisfied where S1 is the area of the capacitor 264 and S2 is the area of a region where the gate insulating layer and a semiconductor layer of the first transistor 201 overlap with each other. Specifically, for example, a film formed of a high-k material such as hafnium oxide or a stack of a film formed of a high-k material such as hafnium oxide and a film formed of an oxide semiconductor is used for the capacitor 264 so that εr1 can be set to 15, and silicon oxide is used for the gate insulating layer of the first transistor 201 so that εr2 can be set to 3 to 4.

[0074]

Combination of such structures enables even higher integration of the semiconductor device which is one embodiment of the disclosed invention.

[0075]

Here, operation of the above-described three-terminal semiconductor device in the writing mode and the reading mode is more specifically described with reference to timing charts in FIGS. 4A and 4B. The timing charts in FIGS. 4A and 4B show

change of potentials or states of each portion in the charts over time. In FIGS. 4A and 4B, shown are examples in each of which the threshold voltage of each of the TR_W and TR_R is 2 V, the potential V_{WLH} is 4 V, the potential V_{WLL} is 0 V, the potential V_{BLH} is 1 V, the potential V_{BLL} is 0 V, the potential V_{RLH} is 1.5 V, the potential V_{RLL} is 0 V, and a precharge voltage that is applied to the bit line in the reading mode is V_{BLH}.

[0076]

FIG. 4A is a timing chart for describing the operation in the writing mode. Here, operation for holding the high-level potential V_{BLH} in the node ND is described. First, as first operation, a potential of the word line WL is set to V_{WLH}, so that the transistor TR_W is turned on. In addition, the potentials of the reading signal line RL and the reading signal line RL_X of the different memory cell are set to V_{RLL}.

[0077]

Next, as second operation, a potential of the bit line BL is set to V_{BLH}, so that V_{BLH} is supplied to the node ND via the transistor TR_W.

[0078]

Then, as third operation, the potential of the word line WL is set to V_{WLL}, so that the transistor TR_W is turned off. The charge supplied to the node ND is held after the transistor TR_W is turned off.

[0079]

Note that an accurate potential might not be held in the node ND in the case where the potentials of the reading signal line RL and the bit line BL vary before the transistor TR_W is turned off. In the case where the potentials of the reading signal line RL and the bit line BL are made to vary, the variation needs to be performed after the transistor TR_W is turned off. Even when the potential of the reading signal line RL or the bit line BL varies after the third operation, the charge held in the node ND remains held.

[0080]

Note that the first operation and the second operation can be performed in the reverse order.

[0081]

Throughout the writing mode, the potentials of the reading signal line RL and the reading signal line RL_X of the different memory cell are kept to be V_{RLL}, so that the

transistor TR_R is kept in an off state. Since V_{RLL} is 0 V, the potential V_{BLH} is 1 V, and the potential V_{BLL} is 0 V here, Formula 1 is satisfied and the transistor TR_R remains in an off state.

[0082]

Note that the operation for holding the low-level potential V_{BLL} in the node ND can be described by replacing V_{BLH} with V_{BLL} in FIG. 4A.

[0083]

FIG. 4B is a timing chart for describing the operation in the reading mode. Here, operation of the case where the high-level potential V_{BLH} is held in the node ND is described. First, as first operation, the potential of the word line WL is set to V_{WLL}, so that the transistor TR_W is turned off. In addition, the potential of the reading signal line RL_X of the different memory cell is set to V_{RLL}.

[0084]

Next, as second operation, charge is given (precharging) to the bit line BL, so that the bit line BL is precharged to have the potential V_{BLH} (1 V).

[0085]

Then, as third operation, the potential of the reading signal line RL is set to V_{RLH}. Since the potential V_{BLH} is 1 V and the potential V_{RLH} is 1.5 V, Formula 3 is satisfied and the transistor TR_R is turned on. When the transistor TR_R is in an on state, V_{RLL} is supplied to the bit line BL via the transistor TR_R.

[0086]

In the case where the low-level potential V_{BLL} is held in the node ND, Formula 3 is not satisfied but Formula 4 is satisfied, so that the bit line BL is not supplied with V_{RLL} but with a potential set by the precharging, which is V_{BLH} in this case. In the above manner, by detecting the potential of the bit line BL at the time when the potential of the reading signal line RL is set to V_{RLH}, data stored in the node ND can be read.

[0087]

Charge held in the node ND remains held until new charge is supplied in a writing mode, without being affected during and after the operation in the reading mode. Since the off-state current of the transistor TR_W including an oxide semiconductor is extremely low, the charge in the node ND can be held for a long time.

[0088]

The semiconductor device described in this embodiment is a capacitively-coupled semiconductor device in which data stored in a memory cell is read by control of a potential (charge) held in the node ND.

[0089]

By the way, in the case of a so-called flash memory, it is necessary to keep a proper distance between cells in order to prevent a potential of a control gate from affecting a floating gate of the adjacent cell. This is one of factors inhibiting high integration of the semiconductor device. The factor is attributed to a basic principle of a flash memory, in which a tunneling current flows in applying a high electrical field.

[0090]

Further, because of the above principle of a flash memory, deterioration of a gate insulating film proceeds and thus another problem of the limit on the number of times of rewriting (approximately 10,000 times) occurs.

[0091]

The semiconductor device which is one embodiment of the disclosed invention is operated by switching of a transistor including an oxide semiconductor and does not use the above-described principle of charge injection by a tunneling current. That is, a high electrical field for charge injection is unnecessary unlike a flash memory. Accordingly, it is unnecessary to consider an influence of a high electrical field from a control gate on an adjacent cell, which facilitates high integration.

[0092]

Further, charge injection by a tunneling current is not utilized, which means that there are no factors for deterioration of a memory cell. That is, the semiconductor device which is one embodiment of the disclosed invention has higher durability and reliability than a flash memory.

[0093]

In addition, it is also advantageous that a high electrical field is unnecessary and a large peripheral circuit (such as a booster circuit) is unnecessary as compared to a flash memory.

[0094]

FIG. 3 is an example of a circuit diagram of a semiconductor device having

memory capacity of $m \times n$ bits in which the semiconductor device illustrated in FIG. 1 is used. FIG. 3 is a circuit diagram of a so-called NOR semiconductor device in which memory cells 1200 are connected in parallel.

[0095]

The semiconductor device illustrated in FIG. 3 includes a memory cell array and peripheral circuits such as a first driver circuit 1211, a second driver circuit 1212, and a third driver circuit 1213. The memory cell array includes m word lines WL, m reading signal lines RL, n bit lines BL, and a plurality of memory cells 1200 arranged in matrix of m rows (arranged in a vertical direction) $\times$ n columns (arranged in a horizontal direction) (m and n are natural numbers). Here, the structure illustrated in FIG. 1 is applied to the memory cell 1200.

[0096]

That is, each memory cell 1200 includes a first transistor 1201 functioning as a reading transistor and a second transistor 1202 functioning as a writing transistor. A gate electrode of the first transistor 1201, one of a source electrode and a drain electrode of the second transistor 1202, and one electrode of the capacitor 1264 are electrically connected to one another. The reading signal line RL and the other electrode of the capacitor 1264 are electrically connected to each other. One of a source electrode and a drain electrode of the first transistor 1201 is electrically connected to a reading signal line RL (RL_X) of a different memory cell. The bit line BL, the other of the source electrode and the drain electrode of the first transistor 1201, and the other of the source electrode and the drain electrode of the second transistor 1202 are electrically connected to one another. The word line WL and a gate electrode of the second transistor 1202 are electrically connected to each other.

[0097]

In addition, a memory cell 1200 (i,j) of an i-th row and a j-th column (i is an integer which is greater than or equal to 1 and less than or equal to m, and j is an integer which is greater than or equal to 1 and less than or equal to n) is connected to a reading signal line RL(i), a bit line BL(j), and a word line WL(i).

[0098]

The bit line BL is connected to the second driver circuit 1212. The reading

signal line RL is connected to the first driver circuit 1211. The word line WL is connected to the third driver circuit 1213. Note that the second driver circuit 1212, the first driver circuit 1211, and the third driver circuit 1213 are independently provided here; however, a decoder having one or more functions may also be used.

[0099]

The reading signal line RL (RL_X) of a different memory cell which is connected to the one of the source electrode and the drain electrode of the first transistor 1201 may be connected to a reading signal line RL of any memory cell as long as the memory cell including the reading signal line RL (RL_X) is different from the memory cell including the first transistor 1201. For example, the following structure in which the connection is different by a row may be employed. One of a source electrode and a drain electrode of a first transistor 1201 in the i-th row is connected to a reading signal line RL of a memory cell in an (i+1)-th row. One of a source electrode and a drain electrode of a first transistor 1201 in the (i+1)-th row is connected to a reading signal line RL of a memory cell in an (i+2)-th row. One of a source electrode and a drain electrode of a first transistor 1201 in the (i+2)-th row is connected to a reading signal line RL of a memory cell in an (i+3)-th row.

[0100]

Alternatively, a reading signal line RL of the memory cell in the i-th row may be connected to the one of the source electrode and the drain electrode of the first transistor 1201 of the memory cell in the (i+1)-th row, and the reading signal line RL of the memory cell in the (i+1)-th row may be connected to the one of the source electrode and the drain electrode of the first transistor 1201 of the memory cell in the i-th row. FIG. 3 shows an example in which the reading signal line RL of the memory cell in the i-th row is connected to the one of the source electrode and the drain electrode of the first transistor 1201 of the memory cell in the (i+1)-th row, and the reading signal line RL of the memory cell in the (i+1)-th row is connected to the one of the source electrode and the drain electrode of the first transistor 1201 of the memory cell in the i-th row.

[0101]

Note that n-channel transistors in which electrons are majority carriers are used

in the above description; it is needless to say that p-channel transistors in which holes are majority carriers can be used instead of the n-channel transistors. In the case of using the p-channel transistors, potentials supplied to respective wirings may be set based on the above-described operation principle.

[0102]

In addition, the oxide semiconductor is included in the second transistor 202 in this embodiment; however, a transistor including a semiconductor material such as silicon carbide may be used as the second transistor 202, for example. Alternatively, both the first transistor 201, which is the reading transistor, and the second transistor 202, which is the writing transistor, may be a transistor including the oxide semiconductor.

[0103]

In FIG. 5, a schematic view of a reading circuit for reading data stored in a memory cell is illustrated. The reading circuit includes a transistor and a sense amplifier circuit.

[0104]

In reading of the data, a terminal A is connected to a bit line BL connected to a memory cell from which data is to be read. Further, a bias potential Vbias is applied to a gate electrode of the transistor so that a potential of the terminal A is controlled.

[0105]

The sense amplifier circuit outputs high data when the potential of the terminal A is higher than a reference potential Vref (e.g., 0 V) or low data when the potential of the terminal A is lower than the reference potential Vref. First, the transistor is turned on, and the bit line BL connected to the terminal A is precharged to have the potential V_{BLH}. Next, the memory cell from which data is to be read is set to a reading mode, and the potential of the bit line BL connected to the terminal A is compared with the reference potential Vref. Thus, the high data or low data is output in accordance with the data stored in the memory cell.

[0106]

By using the reading circuit in the above manner, the data stored in the memory cell can be read. Note that the reading circuit of this embodiment is one of examples. Alternatively, another known circuit may be used.

[0107]

As described above, a semiconductor device which is one embodiment of the disclosed invention includes a nonvolatile memory cell including a writing transistor where a leakage current (off-state current) between a source and a drain is low in an off state, a reading transistor including a semiconductor material different from that of the writing transistor, and a capacitor.

[0108]

The memory cell provided in the semiconductor device which is the disclosed invention may include at least the writing transistor and the reading transistor. Accordingly, the area of each memory cell can be sufficiently small as compared to an SRAM which requires six transistors in each memory cell, for example; thus, the memory cells can be arranged in a semiconductor device at high density.

[0109]

In addition, by sharing the bit line BL with the writing transistor and the reading transistor, the number of wirings per unit memory cell can be reduced. Therefore, the area per unit memory cell can be further reduced and integration of the memory cells can be further increased. For example, given that the minimum processing dimension is F, the area occupied by a memory cell can be $15F^2$ to $25F^2$.

[0110]

In a conventional floating-gate transistor, charge travels in a gate insulating film (a tunnel insulating film) during a writing operation, so that the gate insulating film (the tunnel insulating film) inevitably deteriorates. In contrast, in the memory cell which is one embodiment of the present invention, data is written by a switching operation of the writing transistor; therefore, the deterioration of the gate insulating film, which has been traditionally recognized as a problem, can be neglected. This means that there is no limit on the number of times of writing in principle and that writing durability is very high.

[0111]

As a result of intensive research, the inventors have succeeded in finding for the first time that a transistor including an oxide semiconductor has excellent characteristics in that off-state current is lower than or equal to 100 zA which is extremely small. In one embodiment of the disclosed invention, by using such a

transistor having excellent characteristics as the writing transistor of the memory cell, a semiconductor device having a novel feature is provided.

[0112]

Note that the structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0113]

(Embodiment 2)

In this embodiment, a semiconductor device having a structure different from that in Embodiment 1 is described with reference to FIG. 6, FIG. 7, and FIGS. 8A and 8B.

[0114]

In FIG. 6, a circuit structure of the semiconductor device disclosed in this embodiment is illustrated. The semiconductor device illustrated in FIG. 6 includes a nonvolatile memory cell 250 including a first transistor 201, a second transistor 202, and a capacitor 264. In FIG. 6, a first wiring 211 (also referred to as a reading signal line RL) and one of a source electrode and a drain electrode of the first transistor 201 are electrically connected to each other. One of a source electrode and a drain electrode of the second transistor 202 (also referred to as a transistor TR_W) and a gate electrode of the first transistor 201 (also referred to as a transistor TR_R) are electrically connected to one electrode of the capacitor 264. A second wiring 212 (also referred to as a bit line BL) is electrically connected to the other of the source electrode and the drain electrode of the first transistor 201 and the other of the source electrode and the drain electrode of the second transistor 202. A third wiring 213 (also referred to as a word line WL) and a gate electrode of the second transistor 202 are electrically connected to each other. The other electrode of the capacitor 264 is electrically connected to a first wiring 221 (also referred to as a reading signal line RL_X) of a memory cell 290 which is different from the memory cell 250. The first transistor 201 functions as a reading transistor, and the second transistor 202 functions as a writing transistor.

[0115]

The semiconductor device illustrated in FIG. 6 is a three-terminal

semiconductor device in which the bit line BL is shared by the writing transistor and the reading transistor, and a wiring is shared as the other electrode of the capacitor 264 and as the reading signal line RL (the reading signal line RL_X) of the different memory cell, so that the number of connection wirings per unit memory cell is three. The three-terminal semiconductor device described in this embodiment has a structure in which a connection portion of the reading signal line RL_X of the different memory cell is different from that in the three-terminal semiconductor device described in Embodiment 1.

[0116]

In this embodiment, as the second transistor 202, which is the writing transistor, a transistor including an oxide semiconductor is used, as in Embodiment 1. The transistor including the oxide semiconductor has a characteristic of an extremely low leakage current (off-state current) between a source and a drain in an off state. Therefore, by turning off the second transistor 202, a potential in a node 281 (also referred to as a node ND) can be held for a very long time. In the node ND, the one of the source electrode and the drain electrode of the second transistor 202, the gate electrode of the first transistor 201, and the one electrode of the capacitor 264 are electrically connected to one another.

[0117]

As in Embodiment 1, the off-state current of the first transistor 201 does not need to be as low as that of the second transistor 202. A transistor with a higher switching rate (e.g., a transistor with higher field effect mobility) than the second transistor 202 can be used as the first transistor 201 in order to increase operation speed of the memory cell. That is, as the first transistor 201, a transistor including a semiconductor material other than the oxide semiconductor can be used. Note that in some cases, the off-state current of the first transistor 201 is higher than that of the second transistor 202 depending on the semiconductor material selected. As the semiconductor material used for the first transistor 201, for example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used. Alternatively, an organic semiconductor material or the like may be used. The first transistor 201 including such a semiconductor material can be operated at sufficiently high speed, so that it can perform reading of stored data at high speed.

That is, the semiconductor device can be operated at high speed.

[0118]

Note that as in the semiconductor device described in Embodiment 1, the node 281 has the same effect as a floating gate of a floating-gate transistor that is used as a nonvolatile memory element. That is, a nonvolatile memory cell can be realized also with the semiconductor device described in this embodiment.

[0119]

Next, a writing (rewriting) operation of data to the memory cell 250 in the semiconductor device described in this embodiment will be described. First, a potential of the first wiring 221 connected to the different memory cell 290 is set to a high-level potential V_{RLH}. In addition, a potential of the third wiring 213 (the word line WL) which is connected to the memory cell 250 which is selected as a memory cell to which data is to be written is set to a potential at which the second transistor 202, which is the writing transistor, is turned on, so that the second transistor 202 is turned on. A high-level potential V_{WLH} is given to the third wiring 213 here. Accordingly, a potential of the second wiring 212 (the bit line BL) connected to the selected memory cell 250 is supplied to the node 281 (the node ND). A low-level potential V_{BLL} or a high-level potential V_{BLH} is supplied here. After that, the potential of the third wiring 213 is set to a potential at which the second transistor 202 is turned off, so that the second transistor 202 is turned off; thus, the node 281 is in a floating state, and predetermined charge remains held in the node 281. In the above-described manner, by accumulating and holding a predetermined amount of charge in the node 281, the memory cell 250 can store data (a writing mode).

[0120]

It is important that the first transistor 201, which is the reading transistor, is kept in an off state throughout the writing operation. If the first transistor 201 is turned on when V_{BLH} or V_{BLL} is supplied to the node 281, the first wiring 211 (the reading signal line RL) and the second wiring 212 are brought into conduction via the first transistor 201. Accordingly, potentials of the first wiring 211 and the second wiring 212 interfere with each other, and accurate data cannot be given to the node 281.

[0121]

In addition, a low-level potential V_{RLL} and the high-level potential V_{RLH} are

supplied to the first wiring 211; however, throughout the writing operation, the first wiring 211 is kept supplied with the high-level potential V_{RLH}. When the threshold voltage of the first transistor 201 is represented as V_{th1}, in order to keep the off state of the first transistor 201 in the writing operation, V_{BLH}, V_{RLH}, and V_{th1} are set so as to satisfy Formula 9.

$$V_{BLH} - V_{RLH} < V_{th1} \quad \text{[Formula 9]}$$

[0122]

In some cases, V_{BLH} is held in a node 281 of a non-selected memory cell. In those cases, in order to select another memory cell which shares the second wiring 212 with the non-selected memory cell and supply V_{BLL} to the selected memory cell, V_{BLL} is supplied to the second wiring 212. At this time, in order to keep the off state of the first transistor 201 of the non-selected memory cell, V_{BLH}, V_{BLL}, and V_{th1} are set so as to satisfy Formula 10. Formula 10 shows that a difference between the high-level potential and the low-level potential supplied to the bit line needs to be smaller than the threshold voltage of the first transistor 201.

$$V_{BLH} - V_{BLL} < V_{th1} \quad \text{[Formula 10]}$$

[0123]

Note that the semiconductor device illustrated in FIG. 6 has a structure in which the other electrode of the capacitor 264 is electrically connected to the first wiring 221 of the different memory cell 290. The reading signal line RL of each memory cell is always supplied with the high-level potential V_{RLH} except in the reading mode, and is supplied with the low-level potential V_{RLL} in the reading mode. In this embodiment, since an n-channel transistor is used as the first transistor 201, which is the reading transistor, even when the potential of the first wiring 221 of the different memory cell varies to the low-level potential V_{RLL} after data is written in the node 281, the first transistor 201 remains in an off state.

[0124]

In the semiconductor device described in this embodiment, charge travel in a gate insulating film (a tunnel insulating film) is not caused in the writing (rewriting) operation unlike a floating-gate transistor, but the charge travel is caused by a switching operation of the second transistor 202. Therefore, there is no limitation on the number

of the writing operations in principle, and the resistance to rewriting is extremely high. In addition, a high voltage needed for writing and erasing in the floating-gate transistor is unnecessary; thus, power consumption of the semiconductor device can be reduced.

[0125]

Next, a reading operation in which data stored in a memory cell is read is described. First, the potential of the first wiring 221 of the different memory cell 290 is set to the high-level potential V_{RLH}. In addition, the potential of the third wiring 213 is set to a potential at which the second transistor 202, which is the writing transistor, is turned off, so that the second transistor 202 is turned off. A low-level potential V_{WLL} is supplied to the third wiring 213 here. Next, charge is given (precharging) to the second wiring 212, so that the potential of the second wiring 212 is V_{BLH}. Then, the low-level potential V_{RLL} is supplied as a reading potential to the first wiring 211 of a memory cell from which data is to be read, and the potential of the second wiring 212 at this time is detected, so that data stored in the memory cell can be read (a reading mode). Note that the potential supplied to the second wiring 212 by the precharging is not limited to the above potential as long as the difference between the potential and a potential held in the node 281 is smaller than V_{th1} and the potential is different from the reading potential.

[0126]

The low-level potential V_{RLL} of the first wiring 211 is set so as to satisfy Formula 11 and Formula 12.

$V_{BLH} - V_{RLL} > V_{th1}$ [Formula 11]

$V_{BLL} - V_{RLL} < V_{th1}$ [Formula 12]

[0127]

That is, Formula 11 shows that when V_{RLL} is supplied to the first wiring 211 in the case where V_{BLH} is held in the node 281, a difference between a potential of the gate electrode of the first transistor 201 and a potential of the one of the source electrode and the drain electrode of the first transistor 201 to which the first wiring 211 is connected is larger than the threshold voltage, so that the first transistor 201 is turned on. When the first transistor 201 is turned on, the low-level potential V_{RLL} of the first wiring 211 is supplied to the second wiring 212 via the first transistor 201.

[0128]

In addition, Formula 12 shows that when V_{RLL} is supplied to the first wiring 211 in the case where V_{BLL} is held in the node 281, the difference between the potential of the gate electrode of the first transistor 201 and the potential of the one of the source electrode and the drain electrode of the first transistor 201 to which the first wiring 211 is connected is smaller than the threshold voltage, so that the first transistor 201 remains in an off state. That is, the potential of the second wiring 212 remains to be the precharged potential (V_{BLH} here).

[0129]

From Formula 11 and Formula 12, the low-level potential V_{RLL}, which is the reading potential, can be set in a range satisfying Formula 13.

$$V_{BLL} - V_{th1} < V_{RLL} < V_{BLH} - V_{th1} \quad \text{[Formula 13]}$$

[0130]

In addition, the reading potential V_{RLL} is preferably set so as to satisfy Formula 14.

$$V_{RLL} = (V_{BLH} + V_{BLL})/2 - V_{th1} \quad \text{[Formula 14]}$$

[0131]

The third wiring 213 (the word line WL) is supplied with the high-level potential V_{WLH} at which the second transistor 202 is turned on or the low-level potential V_{WLL} at which the second transistor 202 remains in an off state. When the threshold voltage of the second transistor 202 is represented as V_{th2}, the high-level potential V_{WLH} and the low-level potential V_{WLL} are set so as to satisfy Formula 15 and Formula 16, respectively.

$$V_{WLH} > V_{th2} + V_{BLH} \quad \text{[Formula 15]}$$

$$V_{WLL} < V_{th2} + V_{BLL} \quad \text{[Formula 16]}$$

[0132]

Note that when the low-level potential V_{RLL} is supplied to the first wiring 211 in the reading mode, among other memory cells connected to the first wiring 211, a first transistor 201 of a memory cell in which a node 281 has V_{BLH} is also turned on; however, the node 281 is in a floating state, so that charge held in the node 281 remains held.

[0133]

Here, operation of the above-described three-terminal semiconductor device described in this embodiment in the writing mode and the reading mode is more specifically described with reference to timing charts in FIGS. 8A and 8B. The timing charts in FIGS. 8A and 8B show change of potentials or states of each portion in the charts over time. In FIGS. 8A and 8B, shown are examples in each of which the threshold voltage of each of the TR_W and TR_R is 2 V, the potential V_{WLH} is 4 V, the potential V_{WLL} is 0 V, the potential V_{BLH} is 1 V, the potential V_{BLL} is 0 V, the potential V_{RLH} is 1 V, the potential V_{RLL} is −1.5 V, and a precharge voltage that is applied to the bit line in the reading mode is V_{BLH}.

[0134]

FIG. 8A is a timing chart for describing the operation in the writing mode. Here, operation for holding the high-level potential V_{BLH} in the node ND is described. First, as first operation, a potential of the reading signal line RL_X is set to V_{RLH}. In addition, a potential of the word line WL is set to V_{WLH}, so that the transistor TR_W is turned on.

[0135]

Next, as second operation, a potential of the bit line BL is set to V_{BLH}, so that V_{BLH} is supplied to the node ND via the transistor TR_W.

[0136]

Then, as third operation, the potential of the word line WL is set to V_{WLL}, so that the transistor TR_W is turned off. The charge supplied to the node ND is held after the transistor TR_W is turned off.

[0137]

Note that an accurate potential might not be held in the node ND in the case where the potentials of the reading signal line RL_X and the bit line BL vary before the transistor TR_W is turned off. In the case where the potentials of the reading signal line RL_X and the bit line BL are made to vary, the variation needs to be performed after the transistor TR_W is turned off. Even when the potential of the reading signal line RL_X or the bit line BL varies after the third operation, the charge held in the node ND remains held.

[0138]

Note that the first operation and the second operation can be performed in the reverse order.

[0139]

Throughout the writing mode, the potentials of the reading signal line RL and the reading signal line RL_X are kept to be V_{RLH}, so that the transistor TR_R is kept in an off state. Since V_{RLH} is 1 V, the potential V_{BLH} is 1 V, and the potential V_{BLL} is 0 V here, Formula 1 is satisfied and the transistor TR_R remains in an off state.

[0140]

Note that the operation for holding the low-level potential V_{BLL} in the node ND can be described by replacing V_{BLH} with V_{BLL} in FIG. 8A.

[0141]

FIG. 8B is a timing chart for describing the operation in the reading mode. Here, operation of the case where the high-level potential V_{BLH} is held in the node ND is described. First, as first operation, the potential of the reading signal line RL_X is set to V_{RLH}. In addition, the potential of the word line WL is set to V_{WLL}, so that the transistor TR_W is turned off.

[0142]

Next, as second operation, charge is given (precharging) to the bit line BL, so that the bit line BL is precharged to have the potential V_{BLH} (1 V).

[0143]

Then, as third operation, the potential of the reading signal line RL is set to V_{RLL}. Since the potential V_{BLH} is 1 V and the potential V_{RLL} is −1.5 V, Formula 11 is satisfied and the transistor TR_R is turned on. When the transistor TR_R is in an on state, V_{RLL} is supplied to the bit line BL via the transistor TR_R.

[0144]

In the case where the low-level potential V_{BLL} is held in the node ND, Formula 11 is not satisfied but Formula 12 is satisfied, so that the bit line BL is not supplied with V_{RLL} but with a potential set by the precharging, which is V_{BLH} in this case. In the above manner, by detecting the potential of the bit line BL at the time when the potential of the reading signal line RL is set to V_{RLL}, data stored in the node ND can be read.

[0145]

Charge held in the node ND remains held until new charge is supplied in a writing mode, without being affected during and after the operation in the reading mode. Since the off-state current of the transistor TR_W including an oxide semiconductor is extremely low, the charge in the node ND can be held for a long time.

[0146]

The semiconductor device described in this embodiment is a source potential variation semiconductor device in which data stored in a memory cell is read by varying the potential of the source electrode (the drain electrode) of the reading transistor TR_R and detecting the difference between a potential (charge) held in the node ND and the potential of the source electrode.

[0147]

The capacitor 264 in the source potential variation semiconductor device is not used for addition of the potential of the reading signal line RL and the potential of the node ND in the reading mode of the capacitively-coupled semiconductor device. That is, there is no need to consider the relation between C1 and C2 described in Embodiment 1 with reference to FIG. 2; thus, the semiconductor device can be operated even when the capacitor 264 is not provided.

[0148]

However, in a structure in which the capacitor 264 is omitted, the potential of the node ND may unintentionally vary depending on a planar structure or a layered structure of the memory cell. For that reason, by provision of the capacitor 264, the variation in the potential of the node ND can be reduced and the source potential variation semiconductor device can be operated more stably. That is, reliability of a semiconductor device can be improved.

[0149]

In addition, with use of a transistor with an extremely low off-state current such as the transistor including the oxide semiconductor as the second transistor 202, the potential of the node ND can be held for a long time. With addition of the capacitor 264, the potential of the node ND can be held for a longer time.

[0150]

FIG. 7 is an example of a circuit diagram of a semiconductor device having memory capacity of $m \times n$ bits in which the semiconductor device illustrated in FIG. 6 is

used. FIG. 7 is a circuit diagram of a so-called NOR semiconductor device in which memory cells 1250 are connected in parallel.

[0151]

The semiconductor device illustrated in FIG. 7 includes a memory cell array and peripheral circuits such as a first driver circuit 1211, a second driver circuit 1212, and a third driver circuit 1213. The memory cell array includes *m* word lines WL, *m* reading signal lines RL, *n* bit lines BL, and a plurality of memory cells 1250 arranged in matrix of *m* rows (arranged in a vertical direction) × *n* columns (arranged in a horizontal direction) (*m* and *n* are natural numbers). Here, the structure illustrated in FIG. 6 is applied to the memory cell 1250.

[0152]

That is, each memory cell 1250 includes a first transistor 1201 functioning as a reading transistor and a second transistor 1202 functioning as a writing transistor. A gate electrode of the first transistor 1201, one of a source electrode and a drain electrode of the second transistor 1202, and one electrode of the capacitor 1264 are electrically connected to one another. The reading signal line RL and one of a source electrode and a drain electrode of the first transistor 1201 are electrically connected to each other. The bit line BL, the other of the source electrode and the drain electrode of the first transistor 1201, and the other of the source electrode and the drain electrode of the second transistor 1202 are electrically connected to one another. The word line WL and a gate electrode of the second transistor 1202 are electrically connected to each other. The other electrode of the capacitor 1264 is electrically connected to the reading signal line RL (RL_X) of the different memory cell.

[0153]

In addition, a memory cell 1250 (*i*,*j*) of an *i*-th row and a *j*-th column (*i* is an integer which is greater than or equal to 1 and less than or equal to *m*, and *j* is an integer which is greater than or equal to 1 and less than or equal to *n*) is connected to a reading signal line RL(*i*), a bit line BL(*j*), and a word line WL(*i*).

[0154]

The bit line BL is connected to the second driver circuit 1212. The reading signal line RL is connected to the first driver circuit 1211. The word line WL is connected to the third driver circuit 1213. Note that the second driver circuit 1212, the

first driver circuit 1211, and the third driver circuit 1213 are independently provided here; however, a decoder having one or more functions may also be used.

[0155]

The structure in FIG. 7 is the same or substantially the same as that in FIG. 3; however, FIG. 7 is different from FIG. 3 in that the one of the source electrode and the drain electrode of the first transistor 1201 is electrically connected to the reading signal line RL and the other electrode of the capacitor 1264 is electrically connected to the reading signal line RL (RL_X) of the different memory cell. The reading signal line RL (RL_X) which is connected to the other electrode of the capacitor 1264 may be connected to a reading signal line RL of any memory cell as long as the reading signal line RL (RL_X) is the reading signal line RL of the different memory cell. For example, the following structure in which the connection is different by a row may be employed. The other electrode of a capacitor 1264 of a memory cell in the i-th row is connected to a reading signal line RL of a memory cell in an (i+1)-th row. The other electrode of a capacitor 1264 of a memory cell in the (i+1)-th row is connected to a reading signal line RL of a memory cell in an (i+2)-th row. The other electrode of a capacitor 1264 of a memory cell in the (i+2)-th row is connected to a reading signal line RL of a memory cell in an (i+3)-th row.

[0156]

Alternatively, a reading signal line RL of the memory cell in the i-th row may be connected to the other electrode of the capacitor 1264 of the memory cell in the (i+1)-th row, and the reading signal line RL of the memory cell in the (i+1)-th row may be connected to the other electrode of the capacitor 1264 of the memory cell in the i-th row. FIG. 7 shows an example in which the reading signal line RL of the memory cell in the i-th row is connected to the other electrode of the capacitor 1264 of the memory cell in the (i+1)-th row, and the reading signal line RL of the memory cell in the (i+1)-th row is connected to the other electrode of the capacitor 1264 of the memory cell in the i-th row.

[0157]

In addition, the oxide semiconductor is included in the second transistor 202 in this embodiment; however, a transistor including a semiconductor material such as

silicon carbide may be used as the second transistor 202, for example. Alternatively, both the first transistor 201, which is the reading transistor, and the second transistor 202, which is the writing transistor, may be a transistor including the oxide semiconductor.

[0158]

Note that n-channel transistors in which electrons are majority carriers are used in the above description; it is needless to say that p-channel transistors in which holes are majority carriers can be used instead of the n-channel transistors. In the case of using the p-channel transistors, potentials supplied to respective wirings may be set based on the above-described operation principle.

[0159]

The semiconductor device disclosed in this embodiment does not necessarily include a capacitor that is needed for a DRAM; therefore, the area per unit memory cell can be reduced and integration of the memory cells can be increased. In addition, by sharing the bit line BL with the writing transistor and the reading transistor, the number of wirings per unit memory cell can be reduced. Therefore, the area per unit memory cell can be further reduced and integration of the memory cells can be further increased. For example, given that the minimum processing dimension is F, the area occupied by a memory cell can be $15F^2$ to $25F^2$.

[0160]

Note that the structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0161]

(Embodiment 3)

In this embodiment, a structure and a manufacturing method of a semiconductor device which is another embodiment of the disclosed invention will be described with reference to FIGS. 9A and 9B, FIGS. 10A to 10H, and FIGS. 11A to 11E.

[0162]

<Cross-sectional Structure and Planar Structure of Semiconductor Device>

In FIGS. 9A and 9B, an example of the structure of the semiconductor device is

illustrated. FIG. 9A is a cross section of the semiconductor device, and FIG. 9B is a top view of the semiconductor device. Here, FIG. 9A corresponds to a cross section taken along lines A1-A2 and B1-B2 of FIG. 9B. The semiconductor device illustrated in FIGS. 9A and 9B includes a transistor 101 including a semiconductor material other than an oxide semiconductor, and a transistor 102 including an oxide semiconductor. The transistor including the semiconductor material other than the oxide semiconductor can be easily operated at high speed. On the other hand, the transistor including the oxide semiconductor can hold charge for a long time owing to its characteristics.

[0163]

Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. Further, it is not necessary to limit a specific structure of a semiconductor device to the structure described here.

[0164]

The transistor 101 illustrated in FIGS. 9A and 9B includes a channel formation region 116 provided over a substrate 100 containing a semiconductor material (e.g., silicon), impurity regions 114 and high-concentration impurity regions 120 (these regions can be collectively referred to simply as impurity regions) with the channel formation region 116 provided therebetween, a gate insulating layer 108 provided over the channel formation region 116, a gate electrode 110 provided over the gate insulating layer 108, and a source or drain electrode 130a and a source or drain electrode 130b which are electrically connected to the impurity regions. Further, a wiring 142c and a wiring 142d are provided over the source or drain electrode 130a and the source or drain electrode 130b.

[0165]

Sidewall insulating layers 118 are provided on side surfaces of the gate electrode 110. The high-concentration impurity regions 120 are provided in regions of the substrate 100 that do not overlap with the sidewall insulating layers 118 when seen from a direction perpendicular to a surface of the substrate 100. Metal compound regions 124 are placed in contact with the high-concentration impurity regions 120. On the substrate 100, an element isolation insulating layer 106 is provided so as to surround the transistor 101, and an interlayer insulating layer 126 and an interlayer insulating layer 128 are provided so as to cover the transistor 101. Each of the source

or drain electrode 130a and the source or drain electrode 130b is electrically connected to the metal compound region 124 through an opening formed in the interlayer insulating layers 126 and 128. That is, each of the source or drain electrode 130a and the source or drain electrode 130b is electrically connected to the high-concentration impurity region 120 and the impurity region 114 through the metal compound region 124. In addition, an electrode 130c is electrically connected to the gate electrode 110 through an opening formed in the interlayer insulating layers 126 and 128. Note that the sidewall insulating layers 118 are not formed in some cases, for integration or the like of the transistor 101.

[0166]

The transistor 102 in FIG. 9A and FIG. 9B includes the following: a source or drain electrode 142a and a source or drain electrode 142b which are provided over the interlayer insulating layer 128; an oxide semiconductor layer 144 electrically connected to the source or drain electrode 142a and the source or drain electrode 142b; a gate insulating layer 146 which covers the source or drain electrode 142a, the source or drain electrode 142b, and the oxide semiconductor layer 144; and a gate electrode 148a provided over the gate insulating layer 146 so that the gate electrode 148a overlaps with the oxide semiconductor layer 144.

[0167]

Note that the oxide semiconductor layer 144 is preferably an oxide semiconductor layer which is highly purified by sufficient removal of impurities such as hydrogen therefrom or by supplying a sufficient amount of oxygen thereto. Specifically, the hydrogen concentration of the oxide semiconductor layer 144 is 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, more preferably 5×10^{17} atoms/cm^3 or less. Note that the hydrogen concentration of the oxide semiconductor layer 144 is measured by secondary ion mass spectrometry (SIMS).

[0168]

In the oxide semiconductor layer 144 which is highly purified by sufficiently reducing the hydrogen concentration and in which a defect level in an energy gap due to oxygen deficiency is reduced by supplying a sufficient amount of oxygen thereto, the carrier density is lower than 1×10^{12}/cm^3, preferably lower than 1×10^{11}/cm^3, more

preferably lower than $1.45 \times 10^{10}/cm^3$. For example, the off-state current (per unit channel width (1 μm) here) at room temperature (25 °C) is 100 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A) or less, preferably 10 zA/μm or less. The off-state current at 85 °C is 100 zA/μm (1×10^{-19} A/μm) or less, preferably 10 zA/μm (1×10^{-20} A/μm) or less. The transistor 102 with very excellent off-state current characteristics can be obtained with the use of such an oxide semiconductor that is made to be i-type (intrinsic) or substantially i-type.

[0169]

Note that since the oxide semiconductor layer 144 is not processed into an island shape in the transistor 102 in FIGS. 9A and 9B, the oxide semiconductor layer 144 is prevented from being contaminated by etching for the processing.

[0170]

The capacitor 164 includes the source or drain electrode 142a, the oxide semiconductor layer 144, the gate insulating layer 146, and an electrode 148b. That is, the source or drain electrode 142a functions as one electrode of the capacitor 164, and the electrode 148b functions as the other electrode of the capacitor 164.

[0171]

Note that in the capacitor 164 illustrated in FIGS. 9A and 9B, insulating properties between the source or drain electrode 142a and the electrode 148b can be sufficiently secured by stacking the oxide semiconductor layer 144 and the gate insulating layer 146.

[0172]

Note that in the transistor 102 and the capacitor 164, edge portions of the source or drain electrode 142a and the source or drain electrode 142b are preferably tapered. Here, the taper angle is greater than or equal to 30° and less than or equal to 60°, for example. Note that the taper angle means an inclination angle formed with a side surface and a bottom surface of a layer having a tapered shape (for example, the source or drain electrode 142a) when seen from a direction perpendicular to a cross section (a plane perpendicular to a surface of a substrate) of the layer. When the edge portions of the source or drain electrode 142a and the source or drain electrode 142b are tapered, the coverage with the oxide semiconductor layer 144 can be improved and

disconnection can be prevented.

[0173]

Further, an interlayer insulating layer 150 is provided over the transistor 102 and the capacitor 164, and an interlayer insulating layer 152 is provided over the interlayer insulating layer 150.

[0174]

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the semiconductor device will be described. First, a manufacturing method of the transistor 101 will be described below with reference to FIGS. 10A to 10H, and then a manufacturing method of the transistor 102 will be described with reference to FIGS. 11A to 11E.

[0175]

<Method for Manufacturing Transistor 101>

[0176]

First, the substrate 100 containing a semiconductor material is prepared (see FIG. 10A). As the substrate 100 containing a semiconductor material, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like; a compound semiconductor substrate made of silicon germanium or the like; an SOI substrate; or the like can be used. Here, an example of using a single crystal silicon substrate as the substrate 100 containing a semiconductor material is described. Note that in general, the term "SOI substrate" means a substrate where a silicon semiconductor layer is provided on an insulating surface. In this specification and the like, the term "SOI substrate" also includes a substrate where a semiconductor layer formed using a material other than silicon is provided over an insulating surface in its category. That is, a semiconductor layer included in the "SOI substrate" is not limited to a silicon semiconductor layer. Moreover, the SOI substrate can be a substrate having a structure in which a semiconductor layer is provided over an insulating substrate such as a glass substrate, with an insulating layer interposed therebetween.

[0177]

A protective layer 105 serving as a mask for forming an element isolation insulating layer is formed over the substrate 100 (see FIG. 10A). As the protective

layer 105, an insulating layer formed using silicon oxide, silicon nitride, silicon oxynitride, or the like can be used, for example. Note that before or after this step, an impurity element imparting n-type conductivity or an impurity element imparting p-type conductivity may be added to the substrate 100 in order to control the threshold voltage of the transistor. When the semiconductor is silicon, as the impurity imparting n-type conductivity, for example, phosphorus, arsenic, or the like can be used. As the impurity imparting p-type conductivity, for example, boron, aluminum, gallium, or the like can be used.

[0178]

Next, part of the substrate 100 in a region that is not covered with the protective layer 105 (i.e., an exposed region) is removed by etching with the use of the protective layer 105 as a mask. Thus, a semiconductor region 104 which is separated from another semiconductor region is formed (see FIG. 10B). As the etching, dry etching is preferably performed, but wet etching can be performed. An etching gas and an etchant can be selected as appropriate depending on a material of layers to be etched.

[0179]

Then, an insulating layer is formed so as to cover the semiconductor region 104, and the insulating layer in a region overlapping with the semiconductor region 104 is selectively removed, so that the element isolation insulating layer 106 is formed (see FIG. 10B). The insulating layer is formed using silicon oxide, silicon nitride, silicon oxynitride or the like. As a method for removing the insulating layer, any of etching treatment and polishing treatment such as CMP can be employed. Note that the protective layer 105 is removed either after the semiconductor region 104 is formed or after the element isolation insulating layer 106 is formed.

[0180]

Next, an insulating layer is formed over the semiconductor region 104, and a layer containing a conductive material is formed over the insulating layer.

[0181]

The insulating layer is to be a gate insulating layer later and preferably has a single-layer structure or a layered structure using a film containing silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, tantalum oxide, yttrium

oxide, hafnium silicate ($HfSi_xO_y$, ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium aluminate to which nitrogen is added ($HfAl_xO_y$, ($x > 0$, $y > 0$)), or the like which is obtained by a CVD method, a sputtering method, or the like. Alternatively, the insulating layer can be formed by oxidizing or nitriding a surface of the semiconductor region 104 by high-density plasma treatment or thermal oxidation treatment. The high-density plasma treatment can be performed using, for example, a mixed gas of a rare gas such as He, Ar, Kr, or Xe and a gas such as oxygen, nitrogen oxide, ammonia, nitrogen, or hydrogen. The thickness of the insulating layer can be, for example, greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0182]

The layer containing a conductive material can be formed using a metal material such as aluminum, copper, titanium, tantalum, or tungsten. The layer containing a conductive material may be formed using a semiconductor material such as polycrystalline silicon. There is no particular limitation on the method for forming the layer containing a conductive material, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, or a spin coating method can be employed. Note that this embodiment shows an example of the case where the layer containing a conductive material is formed using a metal material.

[0183]

After that, the insulating layer and the layer containing a conductive material are selectively etched, so that the gate insulating layer 108 and the gate electrode 110 are formed (see FIG. 10C).

[0184]

Next, an insulating layer 112 that covers the gate electrode 110 is formed (see FIG. 10C). Then, impurity regions 114 with a shallow junction depth are formed by adding phosphorus (P), arsenic (As), or the like to the semiconductor region 104 (see FIG. 10C). Note that phosphorus or arsenic is added here in order to form an n-channel transistor; an impurity element such as boron (B) or aluminum (Al) may be added in the case of forming a p-channel transistor. With the formation of the impurity regions 114, the channel formation region 116 is formed in the semiconductor region 104 below the gate insulating layer 108 (see FIG. 10C). Here, the concentration of the

impurity added can be set as appropriate; the concentration is preferably increased when the size of a semiconductor element is extremely decreased. The step in which the impurity regions 114 are formed after the formation of the insulating layer 112 is employed here; alternatively, the insulating layer 112 may be formed after the formation of the impurity regions 114.

[0185]

Next, the sidewall insulating layers 118 are formed (see FIG. 10D). An insulating layer is formed so as to cover the insulating layer 112 and then subjected to highly anisotropic etching, whereby the sidewall insulating layers 118 can be formed in a self-aligned manner. At this time, it is preferable to partly etch the insulating layer 112 so that a top surface of the gate electrode 110 and top surfaces of the impurity regions 114 are exposed. Note that the sidewall insulating layers 118 are not provided in some cases so that high integration or the like are realized.

[0186]

Then, an insulating layer is formed so as to cover the gate electrode 110, the impurity regions 114, the sidewall insulating layers 118, and the like. Next, phosphorus (P), arsenic (As), or the like is added to part of regions of the impurity regions 114, so that the high-concentration impurity regions 120 that are in contact with the impurity regions 114 are formed (see FIG. 10E). After that, the insulating layer is removed, and a metal layer 122 is formed so as to cover the gate electrode 110, the sidewall insulating layers 118, the high-concentration impurity regions 120, and the like (see FIG. 10E). A variety of film formation methods such as a vacuum evaporation method, a sputtering method, or a spin coating method can be employed for forming the metal layer 122. The metal layer 122 is preferably formed using a metal material that reacts with a semiconductor material contained in the semiconductor region 104 to be a low-resistance metal compound. Examples of such metal materials include titanium, tantalum, tungsten, nickel, cobalt, and platinum.

[0187]

Next, heat treatment is performed so that the metal layer 122 reacts with the semiconductor material. Thus, the metal compound regions 124 that are in contact with the high-concentration impurity regions 120 are formed (see FIG. 10F). Note that when the gate electrode 110 is formed using polycrystalline silicon or the like, a metal

compound region is also formed in a region of the gate electrode 110 in contact with the metal layer 122.

[0188]

As the heat treatment, irradiation with a flash lamp can be employed, for example. Although it is needless to say that another heat treatment method may be used, a method by which heat treatment for an extremely short time can be achieved is preferably used in order to improve the controllability of chemical reaction in formation of the metal compound. Note that the metal compound regions are formed by reaction of the metal material and the semiconductor material and have sufficiently high conductivity. The formation of the metal compound regions can properly reduce the electric resistance and improve element characteristics. Note that the metal layer 122 is removed after the metal compound regions 124 are formed.

[0189]

Then, the interlayer insulating layer 126 and the interlayer insulating layer 128 are formed so as to cover the components formed in the above steps (see FIG. 10G). The interlayer insulating layers 126 and 128 can be formed using a material containing an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, or tantalum oxide. Moreover, the interlayer insulating layers 126 and 128 can be formed using an organic insulating material such as a polyimide or an acrylic resin. Note that although a layered structure of the interlayer insulating layer 126 and the interlayer insulating layer 128 is employed here, one embodiment of the disclosed invention is not limited thereto. A single-layer structure or a layered structure including three or more layers can also be used. After the formation of the interlayer insulating layer 128, a surface of the interlayer insulating layer 128 is preferably planarized with CMP, etching, or the like.

[0190]

Then, openings that reach the metal compound regions 124 are formed in the interlayer insulating layers, and the source or drain electrode 130a and the source or drain electrode 130b are formed in the openings (see FIG. 10H). The source or drain electrode 130a and the source or drain electrode 130b can be formed in such a manner, for example, that a conductive layer is formed in a region including the openings by a PVD method, a CVD method, or the like and then part of the conductive layer is

removed by etching, CMP, or the like.

[0191]

Specifically, it is possible to employ a method, for example, in which a thin titanium film is formed in a region including the openings by a PVD method and a thin titanium nitride film is formed by a CVD method, and then, a tungsten film is formed so as to be embedded in the openings. Here, the titanium film formed by a PVD method has a function of deoxidizing a surface of an oxide film (e.g., a native oxide film) over which the titanium film is formed, and lowering the contact resistance with the lower electrodes (e.g., the metal compound region 124 here) or the like. The titanium nitride film formed after the formation of the titanium film has a barrier function of preventing diffusion of the conductive material. A copper film may be formed by a plating method after the formation of titanium or the barrier film of titanium nitride or the like.

[0192]

Note that in the case where the source or drain electrode 130a and the source or drain electrode 130b are formed by removal of part of the conductive layer, a process is preferably performed so that the surfaces are planarized. For example, when a thin titanium film or a thin titanium nitride film is formed in a region including the openings and then a tungsten film is formed to be embedded in the openings, excess tungsten, titanium, titanium nitride, or the like is removed and the planarity of the surface can be improved by subsequent CMP. By reducing unevenness and increasing the planarity of surfaces including the surfaces of the source or drain electrode 130a and the source or drain electrode 130b as described above, favorable coverage with electrodes, wirings, insulating layers, semiconductor layers, or the like formed in a later step can be obtained.

The unevenness of the surface including surfaces of the source or drain electrode 130a and the source or drain electrode 130b is reduced to improve the planarity, whereby an electrode, a wiring, an insulating layer, a semiconductor layer, and the like formed in later steps can cover the surface favorably.

[0193]

Note that although only the source or drain electrode 130a and the source or drain electrode 130b which are in contact with the metal compound regions 124 are described here, an electrode which is in contact with the gate electrode 110 and the like

can be formed in the same step. There is no particular limitation on a material used for the source or drain electrode 130a and the source or drain electrode 130b, and a variety of conductive materials can be used. For example, a conductive material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium can be used. In view of heat treatment performed later, the source or drain electrode 130a and the source or drain electrode 130b are preferably formed using a material having heat resistance high enough to withstand the heat treatment.

[0194]

Through the above steps, the transistor 101 using the substrate 100 containing a semiconductor material is formed (see FIG. 10H). The transistor 101 formed using a semiconductor material other than an oxide semiconductor can be operated at high speed.

[0195]

Note that an electrode, a wiring, an insulating layer, or the like may be further formed after the above step. When the wirings have a multi-layer structure of a layered structure including an interlayer insulating layer and a conductive layer, a highly integrated semiconductor device can be provided.

[0196]

<Method for Manufacturing Transistor 102>

Next, steps for manufacturing the transistor 102 over the interlayer insulating layer 128 will be described with reference to FIGS. 11A to 11E. Note that FIGS. 11A to 11E illustrate steps for manufacturing electrodes, the transistor 102, and the like over the interlayer insulating layer 128; thus, the transistor 101 and the like are omitted.

[0197]

First, a conductive layer is formed over the interlayer insulating layer 128 and is selectively etched, so that the source or drain electrode 142a and the source or drain electrode 142b are formed (see FIG. 11A).

[0198]

The conductive layer can be formed by a PVD method such as a sputtering method, or a CVD method such as a plasma CVD method. As a material for the conductive layer, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten; an alloy containing any of these elements as a

component; or the like can be used. Moreover, one or more materials selected from manganese, magnesium, zirconium, and beryllium may be used. Alternatively, aluminum combined with one or more of elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used.

[0199]

The conductive layer can have a single-layer structure or a layered structure including two or more layers. For example, a single-layer structure of a titanium film or a titanium nitride film, a single-layer structure of an aluminum film containing silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, and the like can be given. Note that in the case where the conductive layer has a single-layer structure of a titanium film or a titanium nitride film, there is an advantage that the conductive layer is easily processed into the source or drain electrode 142a and the source or drain electrode 142b having tapered shapes.

[0200]

The conductive layer may also be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an indium oxide-tin oxide alloy (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), an indium oxide-zinc oxide alloy (In_2O_3-ZnO), or any of these metal oxide materials in which silicon or silicon oxide is contained can be used.

[0201]

The conductive layer is preferably etched so that edge portions of the source or drain electrode 142a and the source or drain electrode 142b are tapered. Here, the taper angle is preferably greater than or equal to 30° and less than or equal to 60°, for example. The edge portions of the source or drain electrode 142a and the source or drain electrode 142b are etched so as to be tapered; accordingly, the coverage with the gate insulating layer 146 to be formed later is improved and disconnection can be prevented.

[0202]

The channel length (L) of the transistor is determined by a distance between a lower edge portion of the source or drain electrode 142a and a lower edge portion of the

source or drain electrode 142b. Note that in the case where the channel length (*L*) of the transistor is less than 25 nm, light exposure for forming a mask is preferably performed with extreme ultraviolet rays whose wavelength is short, which is several nanometers to several tens of nanometers. In the light exposure with extreme ultraviolet rays, the resolution is high and the focus depth is large. For these reasons, the channel length (*L*) of the transistor to be formed later can be in the range of greater than or equal to 10 nm and less than or equal to 1,000 nm (1 μm), and the circuit can be operated at higher speed. Moreover, miniaturization can lead to low power consumption of a semiconductor device.

[0203]

Note that an insulating layer functioning as a base may be provided over the interlayer insulating layer 128. The insulating layer can be formed by a PVD method, a CVD method, or the like.

[0204]

Note also that an insulating layer may be formed over the source or drain electrode 142a and the source or drain electrode 142b. By providing the insulating layer, parasitic capacitance formed between a gate electrode to be formed later and the source or drain electrode 142a and between the gate electrode and the source or drain electrode 142b can be reduced.

[0205]

Next, the oxide semiconductor layer 144 is formed so as to cover the source or drain electrode 142a and the source or drain electrode 142b (see FIG. 11B).

[0206]

The oxide semiconductor layer 144 can be formed using any of the following oxide semiconductors: an oxide of four metal elements such as an In-Sn-Ga-Zn-O-based oxide semiconductor; oxides of three metal elements such as an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, and a Sn-Al-Zn-O-based oxide semiconductor; oxides of two metal elements such as an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, an In-Mg-O-based oxide

semiconductor, and an In-Ga-O-based oxide semiconductor; and oxides of one metal element such as an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, and a Zn-O-based oxide semiconductor.

[0207]

The oxide semiconductor layer 144 preferably contains In, more preferably In and Ga. In order to obtain an i-type (intrinsic) oxide semiconductor layer 144, dehydration treatment or dehydrogenation treatment to be performed later is effective.

[0208]

In particular, an In-Ga-Zn-O-based oxide semiconductor material has sufficiently high resistance when there is no electrical field and thus off-state current can be sufficiently reduced. In addition, with high field-effect mobility, the In-Ga-Zn-O-based oxide semiconductor material is suitable for a semiconductor device.

[0209]

As a typical example of the In-Ga-Zn-O-based oxide semiconductor material, one represented by $InGaO_3(ZnO)_m$ ($m>0$) is given. There is also an oxide semiconductor material represented by $InMO_3(ZnO)_m$ ($m > 0$) in which M is used instead of Ga. Here, M denotes one or more metal elements selected from gallium (Ga), aluminum (Al), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), and the like. For example, M may be Ga, Ga and Al, Ga and Fe, Ga and Ni, Ga and Mn, Ga and Co, or the like. Note that the above-described compositions are derived from the crystal structures that the oxide semiconductor material can have and are mere examples.

[0210]

As a target for forming the oxide semiconductor layer 144 by a sputtering method, a target having a composition ratio of In:Ga:Zn = 1:x:y (x is 0 or more and y is more than or equal to 0.5 and less than or equal to 5) is preferably used. For example, a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio], a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio], a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 2:2:1 [molar ratio], a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:4 [molar ratio], or the like can be used. Alternatively, a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 2:0:1 [molar ratio] can be used.

[0211]

In this embodiment, the oxide semiconductor layer 144 having an amorphous structure is formed by a sputtering method using an In-Ga-Zn-O-based metal oxide target.

[0212]

The relative density of the metal oxide in the metal oxide target is higher than or equal to 80 %, preferably higher than or equal to 95 %, and more preferably higher than or equal to 99.9 %. With the use of the metal oxide target with high relative density, the oxide semiconductor layer 144 having a dense structure can be formed.

[0213]

A sputtering gas used in the formation of the oxide semiconductor layer 144 is preferably a rare gas (typically argon), oxygen, or a mixed gas of a rare gas (typically argon) and oxygen. In addition, it is preferable to use a high-purity gas atmosphere, for example, from which impurities such as hydrogen, water, hydroxyl group, or hydride is removed so that the concentration is 1 ppm or less (preferably 10 ppb or less).

[0214]

In forming the oxide semiconductor layer 144, the object is held in a treatment chamber that is maintained at reduced pressure and is heated so that the temperature of the object is higher than or equal to 100 °C and lower than 550 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. Alternatively, the temperature of the object in forming the oxide semiconductor layer 144 may be room temperature. Then, a sputtering gas from which hydrogen, water, and the like are removed is introduced while moisture in the treatment chamber is removed, whereby the oxide semiconductor layer 144 is formed using the above-described target. The oxide semiconductor layer 144 is formed while the object is heated, so that impurities contained in the oxide semiconductor layer 144 can be reduced. In addition, damage due to the sputtering can be reduced. In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. A turbo pump provided with a cold trap may be used. By evacuation with the cryopump or the like, hydrogen, water, and the like can be removed from the treatment chamber, whereby the

concentration of impurities contained in the oxide semiconductor layer 144 can be reduced.

[0215]

The oxide semiconductor layer 144 can be formed under the following conditions, for example: the distance between the object and the target is 170 mm; the pressure is 0.4 Pa; the direct-current (DC) power is 0.5 kW; and the atmosphere is an oxygen (the proportion of the oxygen flow is 100 %) atmosphere, an argon (the proportion of the argon flow is 100 %) atmosphere, or a mixed atmosphere of oxygen and argon. A pulse direct current (DC) power supply is preferable because powder substances (also referred to as particles or dust) generated in the film formation can be reduced and the film thickness can be made uniform. The thickness of the oxide semiconductor layer 144 is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 1 nm and less than or equal to 30 nm, more preferably greater than or equal to 1 nm and less than or equal to 10 nm. Using the oxide semiconductor layer 144 with such a thickness can suppress a short-channel effect due to miniaturization. Note that the appropriate thickness varies depending on the material for the oxide semiconductor, the usage of the semiconductor device, or the like, and thus the thickness can be selected as appropriate depending on the material, the usage, or the like.

[0216]

Note that before the oxide semiconductor layer 144 is formed by a sputtering method, a material attached to a surface over which the oxide semiconductor layer 144 is formed (e.g., a surface of the interlayer insulating layer 128) is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. Here, the reverse sputtering is a method by which ions collide with a surface to be processed so that the surface is modified, in contrast to normal sputtering by which ions collide with a sputtering target. An example of a method for making ions collide with a surface to be processed is a method in which high-frequency voltage is applied to the surface in an argon atmosphere so that plasma is generated near an object. Note that an atmosphere of nitrogen, helium, oxygen, or the like may be used instead of an argon atmosphere.

[0217]

After that, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer 144. Excess hydrogen (including water and hydroxyl group) contained in the oxide semiconductor layer 144 can be removed by the first heat treatment; thus, the structure of the oxide semiconductor layer can be improved and a defect level in an energy gap can be reduced. The first heat treatment is performed at a temperature higher than or equal to 300 °C and lower than 550 °C, or higher than or equal to 400 °C and lower than or equal to 500 °C, for example.

[0218]

The heat treatment can be performed in the following manner, for example: an object is introduced into an electric furnace in which a resistance heating element or the like is used and heated, under a nitrogen atmosphere at 450 °C for 1 hour. The oxide semiconductor layer 144 is not exposed to the air during the heat treatment so that entry of water and hydrogen can be prevented.

[0219]

The heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object by thermal conduction or thermal radiation from a medium such as a heated gas. For example, an RTA (rapid thermal anneal) apparatus such as a GRTA (gas rapid thermal anneal) apparatus or an LRTA (lamp rapid thermal anneal) apparatus can be used. An LRTA apparatus is an apparatus for heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0220]

For example, as the first heat treatment, a GRTA process may be performed as follows. The object is put in an inert gas atmosphere that has been heated, heated for several minutes, and taken out from the inert gas atmosphere. The GRTA process enables high-temperature heat treatment for a short time. Moreover, the GRTA process

can be employed even when the temperature exceeds the upper temperature limit of the object. Note that the inert gas may be switched to a gas containing oxygen during the process. This is because a defect level in an energy gap due to oxygen deficiency can be reduced by performing the first heat treatment in an atmosphere containing oxygen.

[0221]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is greater than or equal to 6N (99.9999 %), preferably greater than or equal to 7N (99.99999 %) (that is, the concentration of the impurities is less than or equal to 1 ppm, preferably less than or equal to 0.1 ppm).

[0222]

In any case, impurities are reduced by the first heat treatment so that the i-type (intrinsic) or substantially i-type oxide semiconductor layer 144 is obtained. Accordingly, a transistor having extremely excellent characteristics can be realized.

[0223]

The above heat treatment (first heat treatment) can be referred to as dehydration treatment, dehydrogenation treatment, or the like because it has an effect of removing hydrogen, water, and the like. The dehydration treatment or dehydrogenation treatment can be performed, for example, after the oxide semiconductor layer is formed, after the gate insulating layer is formed, or after the gate electrode is formed. Such dehydration treatment or dehydrogenation treatment may be conducted once or plural times.

[0224]

Next, the gate insulating layer 146 which is in contact with the oxide semiconductor layer 144 is formed (see FIG. 11C). The gate insulating layer 146 can be formed by a CVD method, a sputtering method, or the like. The gate insulating layer 146 is preferably formed so as to contain silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, tantalum oxide, hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which

nitrogen is added, hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, or the like. Note that the gate insulating layer 146 may have a single-layer structure or a layered structure. There is no particular limitation on the thickness; however, in the case where a semiconductor device is miniaturized, the thickness is preferably small for ensuring operation of the transistor. For example, in the case where silicon oxide is used, the thickness can be set to greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0225]

As described above, when the gate insulating layer is thin, there is a problem of gate leakage due to a tunneling effect or the like. In order to solve a problem of gate leakage, the gate insulating layer 146 is preferably formed using a material with a high dielectric constant (a high-k material) such as hafnium oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, or hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added. By using a high-k material for the gate insulating layer 146, electrical characteristics can be ensured and the thickness can be large to prevent gate leakage. Note that a layered structure of a film containing a high-k material and a film containing any one of silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, and the like may be employed.

[0226]

After the gate insulating layer 146 is formed, second heat treatment is desirably performed in an inert gas atmosphere or an oxygen atmosphere. The heat treatment is performed at a temperature higher than or equal to 200 °C and lower than or equal to 450 °C, preferably higher than or equal to 250 °C and lower than or equal to 350 °C. For example, the heat treatment may be performed at 250 °C for 1 hour in a nitrogen atmosphere. The second heat treatment can reduce variation in electrical characteristics of the transistor. Moreover, in the case where the gate insulating layer 146 contains oxygen, oxygen is supplied to the oxide semiconductor layer 144 to compensate for oxygen deficiency in the oxide semiconductor layer 144, whereby an i-type (intrinsic) or substantially i-type oxide semiconductor layer can be formed.

[0227]

Note that the second heat treatment is performed in this embodiment after the gate insulating layer 146 is formed; the timing of the second heat treatment is not limited thereto. For example, the second heat treatment may be performed after the gate electrode is formed. Alternatively, the second heat treatment may be performed following the first heat treatment, the first heat treatment may double as the second heat treatment, or the second heat treatment may double as the first heat treatment.

[0228]

Next, over the gate insulating layer 146, the gate electrode 148a is formed in a region overlapping with the oxide semiconductor layer 144, and the electrode 148b is formed in a region overlapping with the source or drain electrode 142a (see FIG. 11D). The gate electrode 148a and the electrode 148b can be formed in such a manner that a conductive layer is formed over the gate insulating layer 146 and then etched selectively. The conductive layer to be the gate electrode 148a and the electrode 148b can be formed by a PVD method such as a sputtering method, or a CVD method such as a plasma CVD method. The details are the same or substantially the same as those of the source or drain electrode 142a or the like; thus, the description thereof can be referred to.

[0229]

Next, the interlayer insulating layer 150 and the interlayer insulating layer 152 are formed over the gate insulating layer 146, the gate electrode 148a, and the electrode 148b (see FIG. 11E). The interlayer insulating layers 150 and 152 can be formed by a PVD method, a CVD method, or the like. The interlayer insulating layers 150 and 152 can be formed using a material containing an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, or tantalum oxide. Note that a layered structure of the interlayer insulating layers 150 and 152 is used in this embodiment, but one embodiment of the disclosed invention is not limited to this example. A single-layer structure or a layered structure including three or more layers can also be used. Alternatively, the interlayer insulating layers can be omitted.

[0230]

Note that the interlayer insulating layer 152 is desirably formed so as to have a

planar surface. This is because an electrode, a wiring, or the like can be favorably formed over the interlayer insulating layer 152 even in the case where the semiconductor device is miniaturized, for example. The interlayer insulating layer 152 can be planarized using a method such as CMP (chemical mechanical polishing).

[0231]

Through the above steps, the transistor 102 including the highly purified oxide semiconductor layer 144 is completed (see FIG. 11E). The capacitor 164 is also completed.

[0232]

The transistor 102 illustrated in FIG. 11E includes the oxide semiconductor layer 144; the source or drain electrode 142a and the source or drain electrode 142b which are electrically connected to the oxide semiconductor layer 144; the gate insulating layer 146 which covers the oxide semiconductor layer 144, the source or drain electrode 142a, and the source or drain electrode 142b; and the gate electrode 148a over the gate insulating layer 146. Further, the capacitor 164 includes the source or drain electrode 142a, the oxide semiconductor layer 144, the gate insulating layer 146 which covers the source or drain electrode 142a, and the electrode 148b over the gate insulating layer 146.

[0233]

Since the oxide semiconductor layer 144 is highly purified in the transistor 102 illustrated in this embodiment, the hydrogen concentration is 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, more preferably 5×10^{17} atoms/cm^3 or less. In addition, the value of the carrier concentration of the oxide semiconductor layer 144 is sufficiently low (e.g., lower than 1×10^{12}/cm^3, preferably lower than 1.45×10^{10}/cm^3) in comparison with that of a general silicon wafer (approximately 1×10^{14}/cm^3). As a result, a sufficiently low off-state current can be obtained. For example, the off-state current (per unit channel width (1 μm) here) of the transistor 102 at room temperature (25 °C) is 100 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A) or less, preferably 10 zA/μm or less.

[0234]

With the use of the oxide semiconductor layer 144 which is highly purified and

becomes intrinsic, the off-state current of the transistor can be sufficiently reduced. By using such a transistor, a semiconductor device in which memory data can be stored for an extremely long time can be obtained.

[0235]

Note that the structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0236]

(Embodiment 4)

In this embodiment, a structure and a manufacturing method of a semiconductor device which is another embodiment of the disclosed invention, which are different from those in Embodiment 3, will be described with reference to FIGS. 12A and 12B and FIGS. 13A to 13D.

[0237]

<Cross-sectional Structure and Planar Structure of Semiconductor Device>

In FIGS. 12A and 12B, an example of the structure of the semiconductor device is illustrated. FIG. 12A is a cross section of the semiconductor device, and FIG. 12B is a top view of the semiconductor device. Here, FIG. 12A corresponds to a cross section taken along lines A1-A2 and B1-B2 of FIG. 12B. The semiconductor device illustrated in FIGS. 12A and 12B includes a transistor 101 including a semiconductor material other than an oxide semiconductor, and a transistor 102 including an oxide semiconductor. The transistor including the semiconductor material other than the oxide semiconductor can be easily operated at high speed. On the other hand, the transistor including the oxide semiconductor can hold charge for a long time owing to its characteristics.

[0238]

Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. Since the technical nature of the disclosed invention is to use an oxide semiconductor in the transistor 102 so that data can be stored, it is not necessary to limit a specific structure of a semiconductor device to the structure described here.

[0239]

The transistor 101 illustrated in FIGS. 12A and 12B includes a channel formation region 116 provided over a substrate 100 containing a semiconductor material (e.g., silicon), impurity regions 114 and high-concentration impurity regions 120 (these regions can be collectively referred to simply as impurity regions) with the channel formation region 116 provided therebetween, a gate insulating layer 108 provided over the channel formation region 116, a gate electrode 110 provided over the gate insulating layer 108, and a source or drain electrode 130a and a source or drain electrode 130b which are electrically connected to the impurity regions. Further, a wiring 142c and a wiring 142d are provided over the source or drain electrode 130a and the source or drain electrode 130b.

[0240]

Sidewall insulating layers 118 are provided on side surfaces of the gate electrode 110. The high-concentration impurity regions 120 are provided in regions of the substrate 100 that do not overlap with the sidewall insulating layers 118 when seen from a direction perpendicular to a surface of the substrate 100. Metal compound regions 124 are placed in contact with the high-concentration impurity regions 120. On the substrate 100, an element isolation insulating layer 106 is provided so as to surround the transistor 101. An opening is provided over the gate electrode 110, and the interlayer insulating layer 126 and the interlayer insulating layer 128 are provided so as to cover the transistor 101. Each of the source or drain electrode 130a and the source or drain electrode 130b is electrically connected to the metal compound region 124 through an opening formed in the interlayer insulating layer 126. That is, each of the source or drain electrode 130a and the source or drain electrode 130b is electrically connected to the high-concentration impurity region 120 and the impurity region 114 through the metal compound region 124. Note that the sidewall insulating layers 118 are not formed in some cases, for integration or the like of the transistor 101.

[0241]

The transistor 102 in FIG. 12A and FIG. 12B includes the following: a source or drain electrode 142a and a source or drain electrode 142b which are provided over the interlayer insulating layer 128; an island-shaped oxide semiconductor layer 144 electrically connected to the source or drain electrode 142a and the source or drain electrode 142b; a gate insulating layer 146 which covers the source or drain electrode

142a, the source or drain electrode 142b, and the island-shaped oxide semiconductor layer 144; and a gate electrode 148a provided over the gate insulating layer 146 so that the gate electrode 148a overlaps with the island-shaped oxide semiconductor layer 144.

[0242]

Here, the source or drain electrode 142a is formed directly on the gate electrode 110, whereby the transistor 101 and the transistor 102 are electrically connected to each other. That is, the semiconductor device described in this embodiment has a structure in which the transistor 102 is formed above the transistor 101, and from which a portion over the top surface of the gate electrode 110 is removed, in the semiconductor device described in Embodiment 3.

[0243]

Note that the oxide semiconductor layer 144 is preferably an oxide semiconductor layer which is highly purified by sufficient removal of impurities such as hydrogen therefrom or by supplying a sufficient amount of oxygen thereto. Specifically, the hydrogen concentration of the oxide semiconductor layer 144 is 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, more preferably 5×10^{17} atoms/cm^3 or less. Note that the hydrogen concentration of the oxide semiconductor layer 144 is measured by secondary ion mass spectrometry (SIMS). In the oxide semiconductor layer 144 which is highly purified by sufficiently reducing the hydrogen concentration and in which a defect level in an energy gap due to oxygen deficiency is reduced by supplying a sufficient amount of oxygen thereto, the carrier density is lower than 1×10^{12}/cm^3, preferably lower than 1×10^{11}/cm^3, more preferably lower than 1.45×10^{10}/cm^3. For example, the off-state current (per unit channel width (1 μm) here) at room temperature (25 °C) is 100 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A) or less, preferably 10 zA/μm or less. The transistor 102 with very excellent off-state current characteristics can be obtained with the use of such an oxide semiconductor that is made to be i-type (intrinsic) or substantially i-type.

[0244]

The capacitor 164 includes the source or drain electrode 142a, the oxide semiconductor layer 144, the gate insulating layer 146, and an electrode 148b. That is, the source or drain electrode 142a functions as one electrode of the capacitor 164, and

the electrode 148b functions as the other electrode of the capacitor 164.

[0245]

Note that in the capacitor 164 illustrated in FIGS. 12A and 12B, insulating properties between the source or drain electrode 142a and the electrode 148b can be sufficiently secured by stacking the oxide semiconductor layer 144 and the gate insulating layer 146.

[0246]

Note that in the transistor 102 and the capacitor 164, edge portions of the source or drain electrode 142a and the source or drain electrode 142b are preferably tapered. Here, the taper angle is greater than or equal to 30° and less than or equal to 60°, for example. Note that the taper angle means an inclination angle formed with a side surface and a bottom surface of a layer having a tapered shape (for example, the source or drain electrode 142a) when seen from a direction perpendicular to a cross section (a plane perpendicular to a surface of a substrate) of the layer. When the edge portions of the source or drain electrode 142a and the source or drain electrode 142b are tapered, the coverage with the oxide semiconductor layer 144 can be improved and disconnection can be prevented.

[0247]

Further, an interlayer insulating layer 150 is provided over the transistor 102 and the capacitor 164, and an interlayer insulating layer 152 is provided over the interlayer insulating layer 150.

[0248]

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the semiconductor device will be described. Steps performed after formation of the transistor 101, i.e., a method for manufacturing the transistor 102, will be described below with reference to FIGS. 13A to 13D. The transistor 101 can be manufactured by a method which is the same or substantially the same as that described in Embodiment 3, and description in Embodiment 3 can be referred to.

[0249]

First, the transistor 101 is formed by the method described in Embodiment 3,

and then a portion of the transistor 101 over the top surface of the gate electrode 110 is removed (see FIG. 13A). The portion of the transistor 101 over the top surface of the gate electrode 110 is removed by performing polishing treatment (e.g., CMP treatment) on the transistor 101 until the top surface of the gate electrode 110 is exposed. Thus, portions of the interlayer insulating layers 126 and 128, the source or drain electrode 130a, and the source or drain electrode 130b over the gate electrode 110 are removed. At this time, the surface including the interlayer insulating layers 126 and 128, the source or drain electrode 130a, and the source or drain electrode 130b is planarized, so that an electrode, a wiring, an insulating layer, a semiconductor layer, and the like can be favorably formed in later steps. In addition, the electrode 130c described in Embodiment 3 would be completely removed by the CMP treatment and thus does not need to be formed.

[0250]

The top surface of the gate electrode 110 is exposed by the CMP treatment in this manner, whereby the gate electrode 110 and the source or drain electrode 142a can be directly connected to each other; accordingly, the transistor 101 and the transistor 102 can be easily electrically connected to each other.

[0251]

Next, a conductive layer is formed over the interlayer insulating layers 126 and 128 and etched selectively, so that the source or drain electrode 142a, the source or drain electrode 142b, the wiring 142c, and the wiring 142d are formed (see FIG. 13B). Here, the source or drain electrode 142a, the wiring 142c, and the wiring 142d are formed so as to be directly connected to the gate electrode 110, the source or drain electrode 130a, and the source or drain electrode 130b, respectively.

[0252]

Here, for the conductive layer used for forming the source or drain electrode 142a, the source or drain electrode 142b, the wiring 142c, and the wiring 142d, a material which is the same or substantially the same as that described in Embodiment 3 can be used and description in Embodiment 3 can be referred to. Etching of the conductive layer can also be performed in a manner which is the same or substantially the same as the method described in Embodiment 3, and description in Embodiment 3 can be referred to.

[0253]

Note also that an insulating layer may be formed over the source or drain electrode 142a and the source or drain electrode 142b as in Embodiment 3. By providing the insulating layer, parasitic capacitance formed between a gate electrode to be formed later and the source or drain electrode 142a and between the gate electrode and the source or drain electrode 142b can be reduced.

[0254]

Next, an oxide semiconductor layer is formed so as to cover the source or drain electrode 142a, the source or drain electrode 142b, the wiring 142c, and the wiring 142d, and the oxide semiconductor layer is selectively etched, so that the island-shaped oxide semiconductor layer 144 is formed in contact with the source or drain electrode 142a and the source or drain electrode 142b (see FIG. 13C).

[0255]

The oxide semiconductor layer can be formed using a material and a method which are the same or substantially the same as those described in Embodiment 3. Therefore, Embodiment 3 can be referred to for a material and a formation method of the oxide semiconductor layer.

[0256]

As a method for etching the oxide semiconductor layer, either dry etching or wet etching may be employed. It is needless to say that dry etching and wet etching can be used in combination. The etching conditions (e.g., an etching gas or an etchant, etching time, and temperature) are set as appropriate depending on the material so that the oxide semiconductor layer can be etched into a desired shape.

[0257]

Further, the oxide semiconductor layer 144 is preferably subjected to heat treatment (first heat treatment) in a manner which is the same or substantially the same as that described in Embodiment 3. The first heat treatment can be performed by the method described in Embodiment 3, and Embodiment 3 can be referred to. Impurities are reduced by the first heat treatment so that the i-type (intrinsic) or substantially i-type oxide semiconductor layer 144 is obtained. Accordingly, a transistor having extremely excellent characteristics can be realized. Note that the first heat treatment may be performed before the oxide semiconductor layer is etched or after the oxide

semiconductor layer is etched to be processed into an island shape.

[0258]

Next, the gate insulating layer 146 is formed in contact with the oxide semiconductor layer 144 (see FIG. 13C).

[0259]

The gate insulating layer 146 can be formed using a material and a method which are the same or substantially the same as those described in Embodiment 3. Therefore, Embodiment 3 can be referred to for a material and a formation method of the gate insulating layer 146.

[0260]

After the gate insulating layer 146 is formed, second heat treatment is preferably performed in an inert gas atmosphere or an oxygen atmosphere in a manner which is the same or substantially the same as that described in Embodiment 3. The second heat treatment can be performed by the method described in Embodiment 3, and Embodiment 3 can be referred to. The second heat treatment can reduce variation in electric characteristics of the transistor. Moreover, in the case where the gate insulating layer 146 contains oxygen, oxygen is supplied to the oxide semiconductor layer 144 to compensate for oxygen deficiency in the oxide semiconductor layer 144, whereby an i-type (intrinsic) or substantially i-type oxide semiconductor layer can be formed.

[0261]

Note that the second heat treatment is performed in this embodiment after the gate insulating layer 146 is formed; the timing of the second heat treatment is not limited thereto. For example, the second heat treatment may be performed after the gate electrode is formed. Alternatively, the second heat treatment may be performed following the first heat treatment, the first heat treatment may double as the second heat treatment, or the second heat treatment may double as the first heat treatment.

[0262]

Next, over the gate insulating layer 146, the gate electrode 148a is formed in a region overlapping with the oxide semiconductor layer 144, and the electrode 148b is formed in a region overlapping with the source or drain electrode 142a (see FIG. 13D). The gate electrode 148a and the electrode 148b can be formed in such a manner that a

conductive layer is formed over the gate insulating layer 146 and then etched selectively. The conductive layer to be the gate electrode 148a and the electrode 148b can be formed by a PVD method such as a sputtering method, or a CVD method such as a plasma CVD method. The details are the same or substantially the same as those of the source or drain electrode 142a or the like; thus, description thereof can be referred to.

[0263]

Next, in a manner which is the same or substantially the same as that described in Embodiment 3, the interlayer insulating layer 150 and the interlayer insulating layer 152 are formed over the gate insulating layer 146, the gate electrode 148a, and the electrode 148b. The interlayer insulating layer 150 and the interlayer insulating layer 152 can be formed using materials and methods which are the same or substantially the same as those described in Embodiment 3. Therefore, Embodiment 3 can be referred to for materials and formation methods of the interlayer insulating layer 150 and the interlayer insulating layer 152.

[0264]

Note that the interlayer insulating layer 152 is desirably formed so as to have a planar surface. This is because an electrode, a wiring, or the like can be favorably formed over the interlayer insulating layer 152 even in the case where the semiconductor device is miniaturized, for example. The interlayer insulating layer 152 can be planarized using a method such as CMP (chemical mechanical polishing).

[0265]

Through the above steps, the transistor 102 including the purified oxide semiconductor layer 144 is completed (see FIG. 13D). The capacitor 164 is also completed.

[0266]

The transistor 102 illustrated in FIG. 13D includes the oxide semiconductor layer 144; the source or drain electrode 142a and the source or drain electrode 142b which are electrically connected to the oxide semiconductor layer 144; the gate insulating layer 146 which covers the oxide semiconductor layer 144, the source or drain electrode 142a, and the source or drain electrode 142b; and the gate electrode 148a over the gate insulating layer 146. Further, the capacitor 164 includes the source

or drain electrode 142a, the oxide semiconductor layer 144, the gate insulating layer 146 which covers the source or drain electrode 142a, and the electrode 148b over the gate insulating layer 146.

[0267]

Since the oxide semiconductor layer 144 is highly purified in the transistor 102 illustrated in this embodiment, the hydrogen concentration is 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, more preferably 5×10^{17} atoms/cm^3 or less. In addition, the value of the carrier density of the oxide semiconductor layer 144 is sufficiently low (e.g., lower than 1×10^{12}/cm^3, preferably lower than 1.45×10^{10}/cm^3) in comparison with that of a general silicon wafer (approximately 1×10^{14}/cm^3). As a result, a sufficiently low off-state current can be obtained. For example, the off-state current (per unit channel width (1 μm) here) of the transistor 102 at room temperature is 100 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A) or less, preferably 10 zA/μm or less.

[0268]

With the use of the oxide semiconductor layer 144 which is highly purified and becomes intrinsic, the off-state current of the transistor can be sufficiently reduced. By using such a transistor, a semiconductor device in which memory data can be stored for an extremely long time can be obtained.

[0269]

Note that the structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0270]

(Embodiment 5)

In this embodiment, a structure and a manufacturing method of a semiconductor device which is another embodiment of the disclosed invention, which are different from those in Embodiment 3 and Embodiment 4, will be described with reference to FIGS. 14A and 14B, FIGS. 15A to 15C, and FIGS. 16A and 16B.

[0271]

<Cross-sectional Structure and Planar Structure of Semiconductor Device>

In FIGS. 14A and 14B, an example of the structure of the semiconductor

device is illustrated. FIG. 14A is a cross section of the semiconductor device, and FIG. 14B is a top view of the semiconductor device. Here, FIG. 14A corresponds to a cross section taken along lines C1-C2 and D1-D2 of FIG. 14B. The semiconductor device illustrated in FIGS. 14A and 14B includes a transistor 101 including a semiconductor material other than an oxide semiconductor, and a transistor 102 including an oxide semiconductor. The transistor including the semiconductor material other than the oxide semiconductor can be easily operated at high speed. On the other hand, the transistor including the oxide semiconductor can hold charge for a long time owing to its characteristics.

[0272]

Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. In addition, it is not necessary to limit a specific structure of a semiconductor device to the structure described here.

[0273]

The semiconductor device in FIGS. 14A and 14B is different from the semiconductor devices described in the above embodiments in a planar layout of the semiconductor device. In this embodiment, the transistor 102 and the capacitor 164 are provided so as to overlap with the transistor 101. By adopting such a planar layout, high integration can be realized. For example, given that the minimum processing dimension is F, the area occupied by a memory cell can be $15F^2$ to $25F^2$.

[0274]

The semiconductor device in FIGS. 14A and 14B is different from the semiconductor devices described in the above embodiments in that sidewall insulating layers 118 are not provided in the transistor 101. That is, the semiconductor device in FIGS. 14A and 14B does not include a sidewall insulating layer. Since a sidewall insulating layer is not formed, an impurity region 114 is not formed. Thus, in the case where a sidewall insulating layer is not provided, high integration is easy as compared to the case where the sidewall insulating layers 118 are provided. In addition, the manufacturing process can be simplified as compared to the case where the sidewall insulating layers 118 are provided.

[0275]

The semiconductor device in FIGS. 14A and 14B is different from the

semiconductor devices described in the above embodiments in that the interlayer insulating layer 125 is provided in the transistor 101. That is, the semiconductor device in FIGS. 14A and 14B includes the interlayer insulating layer 125. By using an insulating layer containing hydrogen as the interlayer insulating layer 125, hydrogen can be supplied to the transistor 101 and the characteristics of the transistor 101 can be improved. As the interlayer insulating layer 125, for example, a silicon nitride layer containing hydrogen, which is formed by a plasma CVD method, is given. Further, by using an insulating layer in which the hydrogen is sufficiently reduced as an interlayer insulating layer 126, hydrogen which can adversely affect the characteristics of the transistor 102 can be prevented from entering the transistor 102. As the interlayer insulating layer 126, for example, a silicon nitride layer formed by a sputtering method is given. When such a structure is employed, the characteristics of the transistors 101 and 102 can be improved sufficiently.

[0276]

The semiconductor device in FIGS. 14A and 14B is different from the semiconductor devices described in the above embodiments also in that an insulating layer 143a and an insulating layer 143b are provided in the transistor 102. That is, the semiconductor device in FIGS. 14A and 14B includes the insulating layer 143a and the insulating layer 143b. By thus providing the insulating layers 143a and 143b, so-called gate capacitance formed by a gate electrode 148a and the source or drain electrode 142a (or the gate electrode 148a and the source or drain electrode 142b) can be reduced to increase the operation speed of the transistor 102.

[0277]

Note that as in Embodiment 4, the source or drain electrode 142a is formed directly on the gate electrode 110, whereby the transistor 101 and the transistor 102 are electrically connected to each other. With such a structure, an integration degree can be increased as compared to the case where an electrode and a wiring are provided additionally. In addition, the manufacturing process can be simplified.

[0278]

Although the structure including all the differences is described in this embodiment, a structure including any one of the differences may be employed.

[0279]

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the semiconductor device will be described. Steps performed after formation of the transistor 101, i.e., a method for manufacturing the transistor 102, will be described below with reference to FIGS. 15A to 15C and FIGS. 16A and 16B. The transistor 101 can be manufactured by a method which is the same or substantially the same as that described in Embodiment 3, and description in Embodiment 3 can be referred to for the details. Note that the source or drain electrode 130a and the source or drain electrode 130b are not formed in the manufacturing process of the transistor 101 in this embodiment, and even the structure in which the source or drain electrode 130a and the source or drain electrode 130b are not formed is called the transistor 101 for convenience.

[0280]

First, the transistor 101 is formed by the method described in Embodiment 3, and then a portion of the transistor 101 over the top surface of the gate electrode 110 is removed. For the removing step, polishing treatment such as CMP (chemical mechanical polishing) may be used. Thus, portions of the interlayer insulating layers 125, 126, and 128 over the top surface of the gate electrode 110 are removed. Note that the surface subjected to such polishing treatment is planarized sufficiently, whereby an electrode, a wiring, an insulating layer, a semiconductor layer, or the like can be formed favorably in later steps.

[0281]

Next, a conductive layer is formed over the gate electrode 110 and the interlayer insulating layers 125, 126, and 128 and is selectively etched, so that the source or drain electrode 142a and the source or drain electrode 142b are formed (see FIG. 15A). Here, the source or drain electrode 142a is formed in direct contact with the gate electrode 110.

[0282]

The conductive layer used for forming the source or drain electrode 142a and the source or drain electrode 142b can be formed using a material which is the same or substantially the same as that described in Embodiment 3. Further, the conductive layer can be etched by a method which is the same or substantially the same as the method described in Embodiment 3. Embodiment 3 can be referred to for the details.

[0283]

Next, an insulating layer is formed so as to cover the source or drain electrode 142a and the source or drain electrode 142b and selectively etched, so that the insulating layer 143a and the insulating layer 143b are formed over the source or drain electrode 142a and the source or drain electrode 142b, respectively (see FIG. 15B).

[0284]

By providing the insulating layer 143a and the insulating layer 143b, parasitic capacitance formed between a gate electrode to be formed later and the source or drain electrode 142a and between the gate electrode and the source or drain electrode 142b can be reduced.

[0285]

After that, the oxide semiconductor layer 144 is formed so as to cover the source or drain electrode 142a and the source or drain electrode 142b, and a gate insulating layer 146 is formed over the oxide semiconductor layer 144 (see FIG. 15C).

[0286]

The oxide semiconductor layer 144 can be formed using the material and the method described in Embodiment 3. In addition, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer 144. Embodiment 3 can be referred to for the details.

[0287]

The gate insulating layer 146 can be formed using the material and the method described in Embodiment 3. Further, the formed gate insulating layer 146 is desirably subjected to heat treatment (second heat treatment) in an inert gas atmosphere or an oxygen atmosphere. Embodiment 3 can be referred to for the details.

[0288]

Then, over the gate insulating layer 146, the gate electrode 148a is formed in a region overlapping with a region of the transistor 102, which serves as a channel formation region, and the electrode 148b is formed in a region overlapping with the source or drain electrode 142a (see FIG. 16A).

[0289]

The gate electrode 148a and the electrode 148b can be formed in such a manner that a conductive layer is formed over the gate insulating layer 146 and then etched

selectively. The conductive layer to be the gate electrode 148a and the electrode 148b can be formed by a PVD method such as a sputtering method, or a CVD method such as a plasma CVD method. The details are the same or substantially the same as those of the source or drain electrode 142a or the like; thus, the description thereof can be referred to.

[0290]

Next, the interlayer insulating layer 150 and the interlayer insulating layer 152 are formed over the gate insulating layer 146, the gate electrode 148a, and the electrode 148b. The interlayer insulating layer 150 and the interlayer insulating layer 152 can be formed using the materials and the methods described in Embodiment 3. Embodiment 3 can be referred to for the details.

[0291]

Note that the interlayer insulating layer 152 is desirably formed so as to have a planar surface. This is because an electrode, a wiring, or the like can be favorably formed over the interlayer insulating layer 152 even in the case where the semiconductor device is miniaturized, for example. The interlayer insulating layer 152 can be planarized using a method such as CMP (chemical mechanical polishing).

[0292]

Thus, the semiconductor device including the transistor 101, the transistor 102, and the capacitor 164 is completed (see FIG. 16B).

[0293]

In the semiconductor device described in this embodiment, for example, the transistor 102 and the capacitor 164 overlap with the transistor 101, the transistor 101 does not include a sidewall insulating layer, and the source or drain electrode 142a is formed directly on the gate electrode 110; therefore, high integration is possible. Further, the manufacturing process is simplified.

[0294]

Further, in the semiconductor device described in this embodiment, an insulating layer containing hydrogen and an insulating layer with sufficiently reduced hydrogen are used as the interlayer insulating layers 125 and 126, respectively; thus, characteristics of the transistors 101 and 102 are improved. Owing to the insulating layer 143a and the insulating layer 143b, so-called gate capacitance is reduced and thus,

the operation speed of the transistor 102 is increased.

[0295]

The above features described in this embodiment make it possible to provide a semiconductor device having significantly excellent characteristics.

[0296]

Note that the structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0297]

(Embodiment 6)

In this embodiment, application of the semiconductor device described in any of the above embodiments to an electronic device is described with reference to FIGS. 17A to 17F. The case where the above described semiconductor device is applied to electronic devices such as a computer, a mobile phone set (also referred to as a mobile phone or a mobile phone device), a portable information terminal (including a portable game machine, an audio reproducing device, and the like), a digital camera, a digital video camera, electronic paper, a television set (also referred to as a television or a television receiver) and the like is described.

[0298]

FIG. 17A is a laptop personal computer including a housing 701, a housing 702, a display portion 703, a keyboard 704, and the like. In each of the housings 701 and 702, the semiconductor device described in any of the above embodiments is provided. Therefore, a laptop personal computer in which writing and reading of data are performed at high speed, data is stored for a long time, and power consumption is sufficiently reduced can be realized.

[0299]

FIG. 17B is a portable information terminal (personal digital assistance (PDA)). In a main body 711, a display portion 713, an external interface 715, an operation button 714, and the like are provided. Further, a stylus 712 and the like for operation of the portable information terminal are provided. In the main body 711, the semiconductor device described in any of the above embodiments is provided. Therefore, a portable information terminal in which writing and reading of data are performed at high speed,

data is stored for a long time, and power consumption is sufficiently reduced can be realized.

[0300]

FIG. 17C is an e-book reader 720 mounted with electronic paper, which includes two housings: a housing 721 and a housing 723. The housing 721 and the housing 723 are provided with a display portion 725 and a display portion 727, respectively. The housings 721 and 723 are connected by a hinge portion 737 and can be opened or closed with the hinge portion 737. The housing 721 is provided with a power supply 731, an operation key 733, a speaker 735, and the like. At least one of the housings 721 and 723 is provided with the semiconductor device described in any of the above embodiments. Therefore, an e-book reader in which writing and reading of data are performed at high speed, data is stored for a long time, and power consumption is sufficiently reduced can be realized.

[0301]

FIG. 17D is a mobile phone including two housings: a housing 740 and a housing 741. Moreover, the housings 740 and 741 which are developed in FIG. 17D can overlap with each other by sliding; thus, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried. The housing 741 includes a display panel 742, a speaker 743, a microphone 744, a touch panel 745, a pointing device 746, a camera lens 747, an external connection terminal 748, and the like. The housing 740 includes a solar cell 749 for charging the mobile phone, an external memory slot 750, and the like. In addition, an antenna is incorporated in the housing 741. At least one of the housings 740 and 741 is provided with the semiconductor device described in any of the above embodiments. Therefore, a mobile phone in which writing and reading of data are performed at high speed, data is stored for a long time, and power consumption is sufficiently reduced can be realized.

[0302]

FIG. 17E is a digital camera including a main body 761, a display portion 767, an eyepiece 763, an operation switch 764, a display portion 765, a battery 766, and the like. In the main body 761, the semiconductor device described in any of the above embodiments is provided. Therefore, a digital camera in which writing and reading of data are performed at high speed, data is stored for a long time, and power consumption

is sufficiently reduced can be realized.

[0303]

FIG. 17F illustrates a television set 770 including a housing 771, a display portion 773, a stand 775, and the like. The television set 770 can be operated with an operation switch of the housing 771 or a remote controller 780. The semiconductor device described in any of the above embodiments is mounted on the housing 771 and the remote controller 780. Therefore, a television set in which writing and reading of data are performed at high speed, data is stored for a long time, and power consumption is sufficiently reduced can be realized.

[0304]

As described above, a semiconductor device related to the above embodiments is mounted in the electronic devices shown in this embodiment. Therefore, an electronic device whose power consumption is sufficiently reduced can be realized.

[Example 1]

[0305]

In this example, measurement results of the off-state current of a transistor including a highly purified oxide semiconductor will be described with reference to FIG. 18, FIG. 19, FIG. 20, FIG. 21, and FIG. 22.

[0306]

First, a transistor with a channel width (W) of 1 m, which is sufficiently wide, was prepared in consideration of very low off-state current of a transistor including a highly purified oxide semiconductor, and the off-state current was measured. FIG. 18 shows the measurement results of the off-state current of the transistor with a channel width (W) of 1 m. In FIG. 18, the horizontal axis shows a gate voltage V_G and the vertical axis shows a drain current I_D. In the case where the drain voltage V_D is +1 V or +10 V and the gate voltage V_G is within the range of −5 V to −20 V, the off-state current of the transistor was found to be lower than or equal to 1×10^{-13} A which is the detection limit. Moreover, the off-state current (per unit channel width (1 μm) here) of the transistor was found to be lower than or equal to 1 aA/μm (1×10^{-18} A/μm).

[0307]

Next, more accurate measurement results of the off-state current of the

transistor including a highly purified oxide semiconductor will be described. As described above, the off-state current of the transistor including a highly purified oxide semiconductor was found to be lower than or equal to 1×10^{-13} A which is the detection limit of measurement equipment. Here, the results of measurement of more accurate off-state current (the value smaller than or equal to the detection limit of measurement equipment in the above measurement) with the use of an element for characteristic evaluation will be described.

[0308]

First, the element for characteristic evaluation used in a method for measuring current will be described with reference to FIG. 19.

[0309]

In the element for characteristic evaluation in FIG. 19, three measurement systems 800 are connected in parallel. Each of the measurement systems 800 includes a capacitor 802, a transistor 804, a transistor 805, a transistor 806, and a transistor 808. A transistor including a highly purified oxide semiconductor was used as each of the transistors 804, 805, and 806.

[0310]

In the measurement system 800, one of a source terminal and a drain terminal of the transistor 804, one terminal of the capacitor 802, and one of a source terminal and a drain terminal of the transistor 805 are connected to a power source (for supplying V_2). The other of the source terminal and the drain terminal of the transistor 804, one of a source terminal and a drain terminal of the transistor 808, the other terminal of the capacitor 802, and a gate terminal of the transistor 805 are connected to one another. The other of the source terminal and the drain terminal of the transistor 808, one of a source terminal and a drain terminal of the transistor 806, and a gate terminal of the transistor 806 are connected to a power source (for supplying V_1). The other of the source terminal and the drain terminal of the transistor 805, the other of the source terminal and the drain terminal of the transistor 806 are connected to each other, and the node serves as an output terminal of V_{out}.

[0311]

A potential V_{ext_b2} for controlling an on state and an off state of the transistor

804 is supplied to the gate terminal of the transistor 804. A potential V_{ext_b1} for controlling an on state and an off state of the transistor 808 is supplied to the gate terminal of the transistor 808. A potential V_{out} is output from the output terminal.

[0312]

Next, a method for measuring current with the use of the element for characteristic evaluation will be described.

[0313]

First, an initialization period in which a potential difference is applied to measure the off-state current will be described briefly. In the initialization period, the potential V_{ext_b1} for turning on the transistor 808 is input to the gate terminal of the transistor 808, and a potential V_1 is supplied to a node A that is a node connected to the other of the source terminal and the drain terminal of the transistor 804 (that is, the node connected to one of the source terminal and the drain terminal of the transistor 808, the other terminal of the capacitor 802, and the gate terminal of the transistor 805). Here, the potential V_1 is, for example, a high potential. The transistor 804 is in an off-state.

[0314]

After that, the potential V_{ext_b1} for turning off the transistor 808 is input to the gate terminal of the transistor 808, so that the transistor 808 is turned off. After the transistor 808 is turned off, the potential V_1 is set to low. Still, the transistor 804 is in an off-state. The potential V_2 is the same potential as V_1. Thus, the initialization period is completed. When the initialization period is completed, a potential difference is generated between the node A and the one of the source terminal and the drain terminal of the transistor 804. In addition, a potential difference is generated between the node A and the other of the source terminal and the drain terminal of the transistor 808. Accordingly, a small amount of charge flows through the transistor 804 and the transistor 808. That is, the off-state current flows.

[0315]

Next, a measurement period of the off-state current will be briefly described. In the measurement period, the potential (that is, V_2) of the one of the source terminal and the drain terminal of the transistor 804 and the potential (that is, V_1) of the other of the source terminal and the drain terminal of the transistor 808 are set to low and fixed.

On the other hand, the potential of the node A is not fixed (the node A is in a floating state) in the measurement period. Accordingly, charge flows through the transistor 804, and the amount of charge stored in the node A varies as time passes. The potential of the node A varies depending on the variation in the amount of charge held in the node A. That is, the output potential V_{out} of the output terminal also varies.

[0316]

FIG. 20 shows details of the relation between potentials in the initialization period in which the potential difference is applied and in the following measurement period (timing chart).

[0317]

In the initialization period, first, the potential V_{ext_b2} is set to a potential (high potential) at which the transistor 804 is turned on. Thus, the potential of the node A becomes V_2, that is, a low potential (V_{SS}). After that, the potential V_{ext_b2} is set to a potential (a low potential) at which the transistor 804 is turned off, whereby the transistor 804 is turned off. Next, the potential V_{ext_b1} is set to a potential (a high potential) at which the transistor 808 is turned on. Thus, the potential of the node A becomes V_1, that is, a high potential (V_{DD}). After that, the potential V_{ext_b1} is set to a potential at which the transistor 808 is turned off. Thus, the node A is brought into a floating state and the initialization period is completed.

[0318]

In the following measurement period, the potential V_1 and the potential V_2 are individually set to potentials at which charge flow to or from the node A. Here, the potential V_1 and the potential V_2 are low potentials (V_{SS}). Note that at the timing of measuring the output potential V_{out}, an output circuit needs to be operated; thus, V_1 is set to a high potential (V_{DD}) temporarily in some cases. The period in which V_1 is a high potential (V_{DD}) is set to be short so that the measurement is not influenced.

[0319]

When the potential difference is generated and the measurement period is started as described above, the amount of charge stored in the node A varies as time passes, whereby the potential of the node A varies. This means that the potential of a gate terminal of the transistor 805 varies and thus, the output potential V_{out} of the output

terminal also varies as time passes.

[0320]

A method for calculating the off-state current on the basis of the obtained output potential V_{out} is described below.

[0321]

The relation between a potential V_A of the node A and the output potential V_{out} is obtained in advance of calculation of the off-state current. Thus, the potential V_A of the node A can be obtained using the output potential V_{out}. In accordance with the above relation, the potential V_A of the node A can be expressed as a function of the output potential V_{out} by the following formula.

[0322]

$$V_A = F(Vout)$$

[0323]

Charge Q_A of the node A can be expressed by the following formula with the use of the potential V_A of the node A, capacitance C_A connected to the node A, and a constant (*const*). Here, the capacitance C_A connected to the node A is the sum of the capacitance of the capacitor 802 and other capacitance.

[0324]

$$Q_A = C_A V_A + const$$

[0325]

Since a current I_A of the node A is obtained by differentiating charge flowing to the node A (or charge flowing from the node A) with respect to time, the current I_A of the node A is expressed by the following formula.

[0326]

$$I_A \equiv \frac{\Delta Q_A}{\Delta t} = \frac{C_A \cdot \Delta F(Vout)}{\Delta t}$$

[0327]

In this manner, the current I_A of the node A can be obtained from the capacitance C_A connected to the node A and the output potential V_{out} of the output terminal.

[0328]

In accordance with the above method, it is possible to measure a leakage current (off-state current) which flows between a source and a drain of a transistor in an off state.

[0329]

In Example 1, the transistor 804, the transistor 805, the transistor 806, and the transistor 808 were fabricated using a highly purified oxide semiconductor with a channel length (L) of 10 μm and a channel width (W) of 50 μm. In each of the measurement systems 800 arranged in parallel, capacitance values of capacitors 802a, 802b, and 802c were 100 fF, 1 pF, and 3 pF, respectively.

[0330]

Note that the measurement in Example 1 was performed assuming that V_{DD} = 5 V and V_{SS} = 0 V are satisfied. In the measurement period, the potential V_1 was basically set to V_{SS} and set to V_{DD} only in a period of 100 msec every 10 to 300 seconds, and V_{out} was measured. Further, Δt used in calculation of current I flowing through the element was about 30,000 sec.

[0331]

FIG. 21 shows the relation between elapsed time (Time) in measuring the current and the output potential V_{out}. The potential change can be observed after about 90 hours.

[0332]

FIG. 22 shows the off-state current which was calculated in the above measurement of the current. In FIG. 22, the relation between source-drain voltage V and off-state current I is shown. According to FIG. 22, the off-state current was about 40 zA/μm under the condition where the source-drain voltage was 4 V. When the source-drain voltage was 3 V, the off-state current was smaller than or equal to 4 zA/μm. Note that 1 zA represents 10^{-21} A.

[0333]

According to Example 1, it was confirmed that the off-state current can be sufficiently small in a transistor including a highly purified oxide semiconductor.

This application is based on Japanese Patent Application serial no.

2010-024889 filed with Japan Patent Office on February 5, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising memory cells,

the memory cells each comprising:

a first transistor;

a second transistor;

a capacitor;

a first wiring;

a second wiring; and

a third wiring,

wherein one of a source electrode and a drain electrode of the second transistor and a gate electrode of the first transistor are electrically connected to one electrode of the capacitor,

wherein the other electrode of the capacitor is electrically connected to the first wiring,

wherein one of a source electrode and a drain electrode of the first transistor is electrically connected to the first wiring of a different memory cell,

wherein the other of the source electrode and the drain electrode of the second transistor and the other of the source electrode and the drain electrode of the first transistor are electrically connected to the second wiring, and

wherein a gate electrode of the second transistor is electrically connected to the third wiring.

2. The semiconductor device according to claim 1, wherein the second transistor comprises an oxide semiconductor.

3. The semiconductor device according to claim 1, wherein an off-state current of the second transistor is lower than an off-state current of the first transistor.

4. The semiconductor device according to claim 1, wherein a switching rate of the first transistor is higher than a switching rate of the second transistor.

5. A method of driving a semiconductor device comprising a memory cell,

the memory cell comprising:

a first transistor;

a second transistor;

a capacitor;

a first wiring; and

a second wiring,

wherein the second transistor is connected between the second wiring and a gate electrode of the first transistor, and

wherein one electrode of the capacitor of is connected to the gate electrode of the first transistor and the other electrode of the capacitor is connected to the first wiring,

the method comprising the steps of:

turning on the second transistor when the first wiring is supplied with a low-level potential and the first transistor is in an off-state,

supplying a high-level potential or a low-level potential supplied to the second wiring to the gate electrode of the first transistor when the first wiring is supplied with a low-level potential and the first transistor is in an off-state, and

turning off the second transistor after the step of turning on the second transistor and the step of supplying the high-level potential or the low-level potential to the gate electrode of the first transistor so that a potential of the gate electrode of the first transistor is held.

6. The method of driving the semiconductor device according to claim 5, wherein a difference between the high-level potential and the low-level potential supplied to the second wiring is lower than a threshold voltage of the first transistor.

7. A method of driving a semiconductor device comprising memory cells,

the memory cells each comprising:

a first transistor;

a second transistor;

a capacitor;

a first wiring; and

a second wiring,

wherein the first transistor is connected between the first wiring of a different memory cell and the second wiring,

wherein the second transistor is connected between the second wiring and a gate electrode of the first transistor, and

wherein one electrode of the capacitor is connected to the gate electrode of the first transistor and the other electrode of the capacitor is connected to the first wiring,

the method comprising the steps of:

supplying a first potential to the first wiring of the different memory cell and supplying a second potential to the second wiring when the second transistor is in an off-state, and

supplying a third potential of the first wiring which is connected to the other electrode of the capacitor to the gate electrode of the first transistor via the capacitor after the step of supplying the second potential to the second wiring, so that on or off of the first transistor is detected.

8. The method of driving the semiconductor device according to claim 7, wherein the first potential is different from the second potential.

9. A semiconductor device comprising memory cells,

the memory cells each comprising:

a first transistor;

a second transistor;

a capacitor;

a first wiring;

a second wiring; and

a third wiring,

wherein one of a source electrode and a drain electrode of the second transistor and a gate electrode of the first transistor are electrically connected to one electrode of the capacitor,

wherein one of a source electrode and a drain electrode of the first transistor is

electrically connected to the first wiring,

wherein the other of the source electrode and the drain electrode of the second transistor and the other of the source electrode and the drain electrode of the first transistor are electrically connected to the second wiring,

wherein a gate electrode of the second transistor is electrically connected to the third wiring, and

wherein the other electrode of the capacitor is electrically connected to the first wiring of a different memory cell.

10. The semiconductor device according to claim 9, wherein the second transistor comprises an oxide semiconductor.

11. The semiconductor device according to claim 9, wherein an off-state current of the second transistor is lower than an off-state current of the first transistor.

12. The semiconductor device according to claim 9, wherein a switching rate of the first transistor is higher than a switching rate of the second transistor.

13. A method of driving a semiconductor device comprising a memory cell,

the memory cell comprising:

a first transistor;

a second transistor;

a capacitor;

a first wiring; and

a second wiring,

wherein the first transistor is connected between the first wiring and the second wiring,

wherein the second transistor is connected between the second wiring and a gate electrode of the first transistor, and

wherein one electrode of the capacitor is connected to the gate electrode of the first transistor,

the method comprising the steps of:

turning on the second transistor when the first transistor is in an off-state,

supplying a high-level potential or a low-level potential supplied to the second wiring to the gate electrode of the first transistor when the first transistor is in an off-state, and

turning off the second transistor after the step of turning on the second transistor and the step of supplying the high-level potential or the low-level potential to the gate electrode of the first transistor, so that a potential of the gate electrode of the first transistor is held.

14. The method of driving the semiconductor device according to claim 13, wherein a difference between the high-level potential and the low-level potential supplied to the second wiring is lower than a threshold voltage of the first transistor.

15. A method of driving a semiconductor device comprising a memory cell,

the memory cell comprising:

a first transistor;

a second transistor;

a capacitor;

a first wiring; and

a second wiring,

wherein the first transistor is connected between the first wiring and the second wiring,

wherein the second transistor is connected between the second wiring and a gate electrode of the first transistor, and

wherein one electrode of the capacitor is connected to the gate electrode of the first transistor,

the method comprising the steps of:

supplying a second potential to the second wiring when the second transistor is in an off-state, and

supplying a first potential to the first wiring after the step of supplying the second potential to the second wiring, so that on or off of the first transistor is

detected.

16. The method of driving the semiconductor device according to claim 15, wherein the first potential is different from the second potential.

FIG. 1

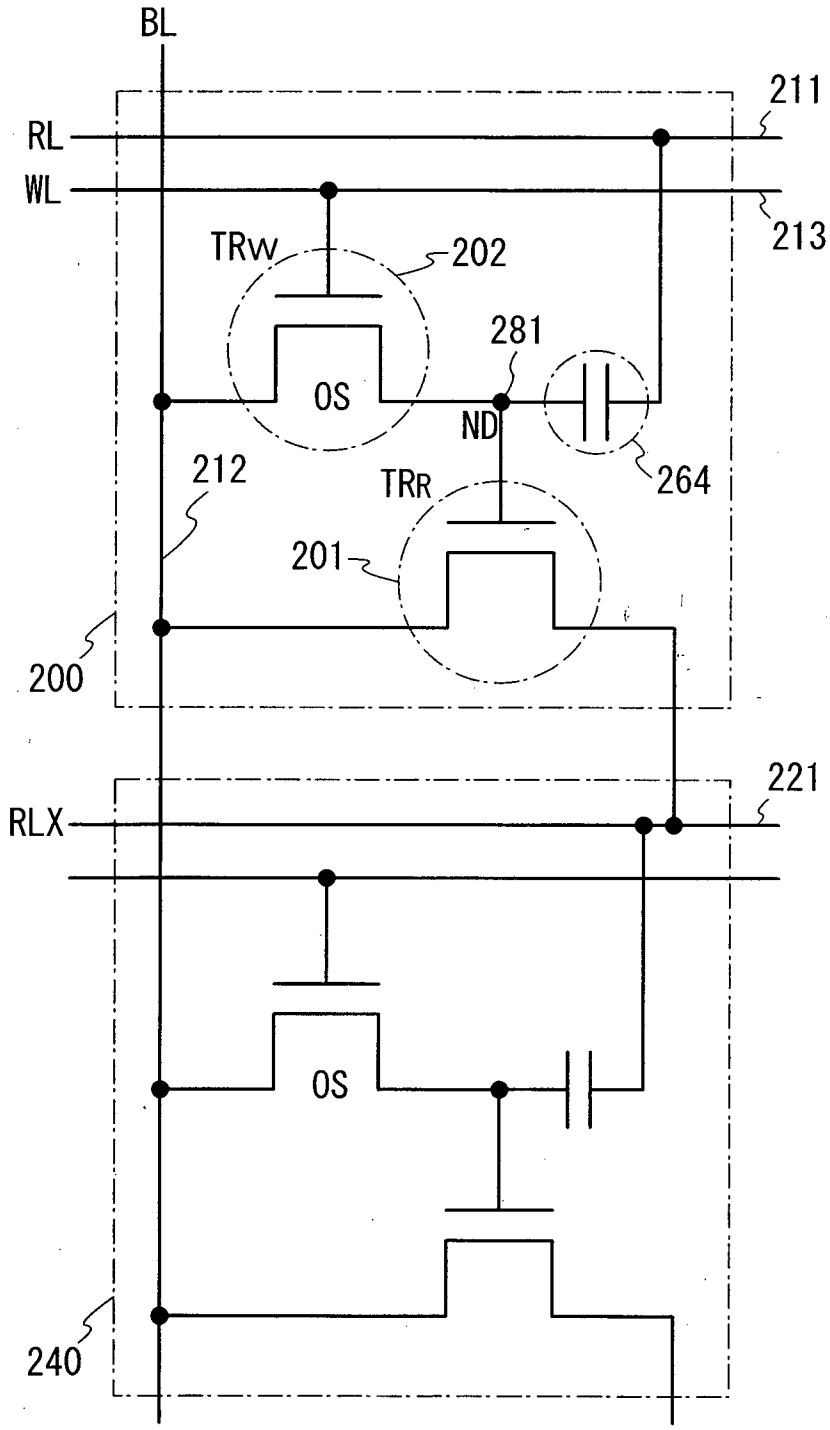

BL
211
RL
WL
213
TRW
202
281
OS
ND
264
212
TRR
201
200
221
RLX
OS
240

FIG. 2

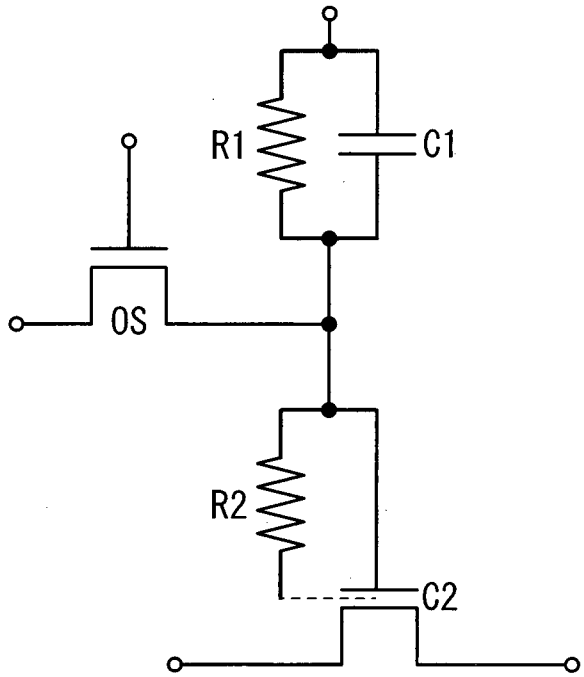


FIG. 3

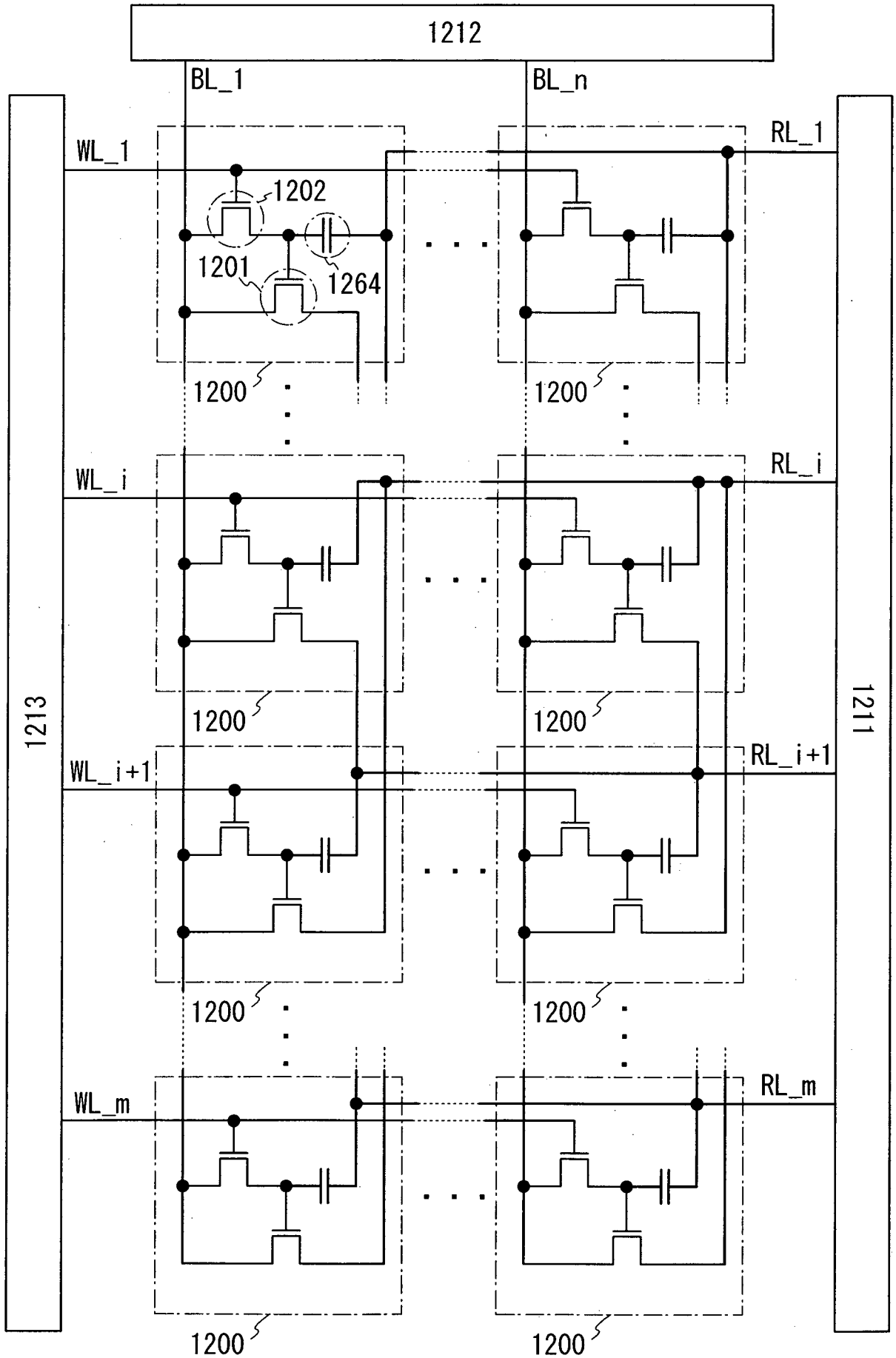

1212
BL_1
BL_n
WL_1
RL_1
1202
1201
1264
1200
WL_i
RL_i
WL_i+1
RL_i+1
WL_m
RL_m
1213
1211

FIG. 4A

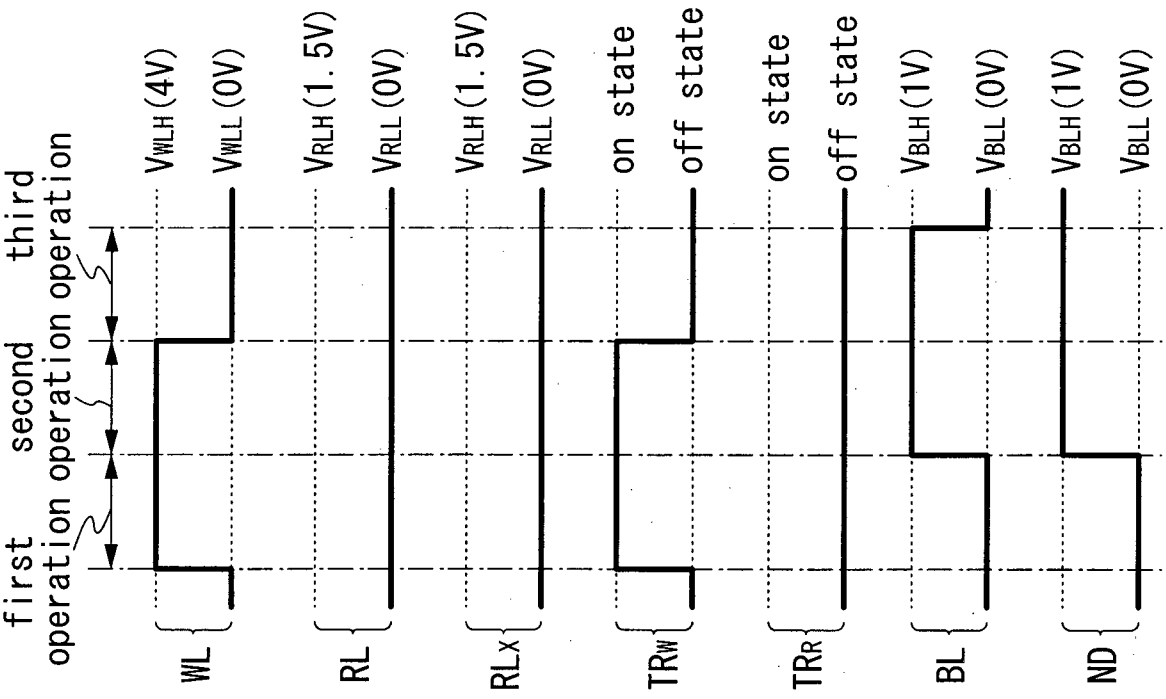

first operation
second operation
third operation
WL
RL
RLX
TRW
TRR
BL
ND
VWLH (4V)
VWLL (0V)
VRLH (1.5V)
VRLL (0V)
VRLH (1.5V)
VRLL (0V)
on state
off state
on state
off state
VBLH (1V)
VBLL (0V)
VBLH (1V)
VBLL (0V)

FIG. 4B

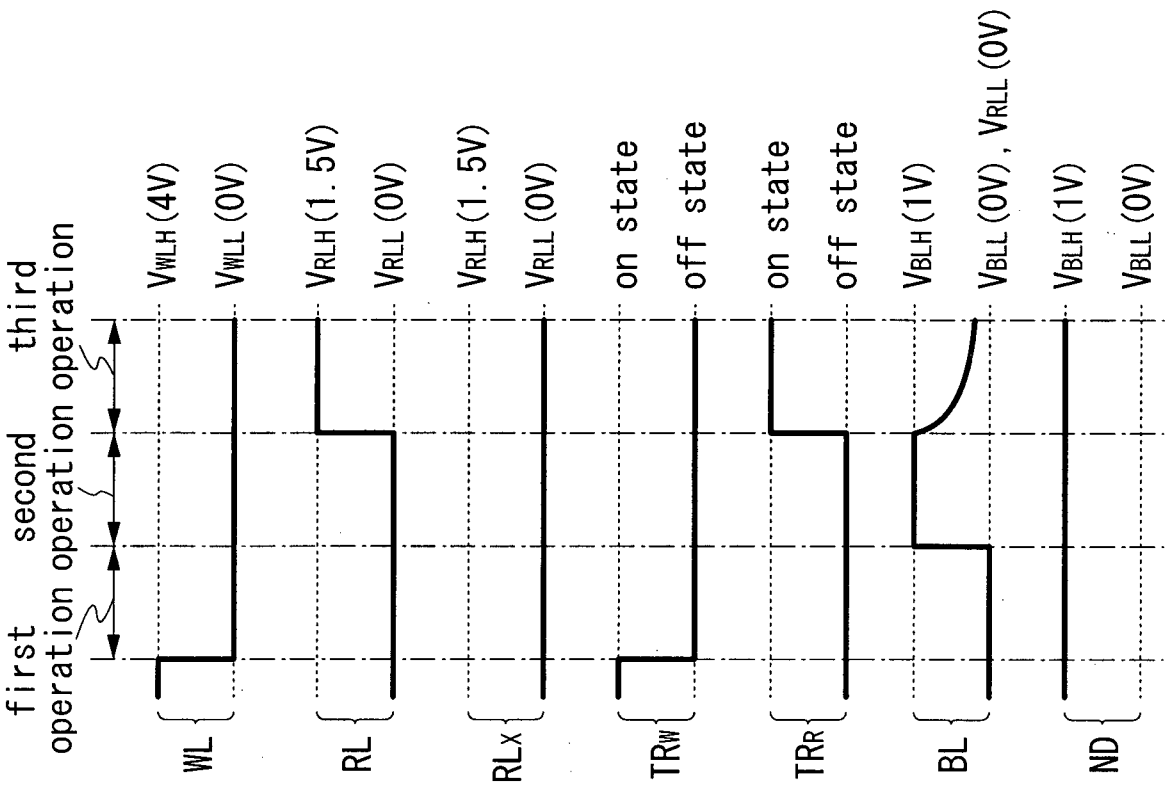

first operation
second operation
third operation
WL
RL
RLX
TRW
TRR
BL
ND
VWLH (4V)
VWLL (0V)
VRLH (1.5V)
VRLL (0V)
VRLH (1.5V)
VRLL (0V)
on state
off state
on state
off state
VBLH (1V)
VBLL (0V), VRLL (0V)
VBLH (1V)
VBLL (0V)

FIG. 5

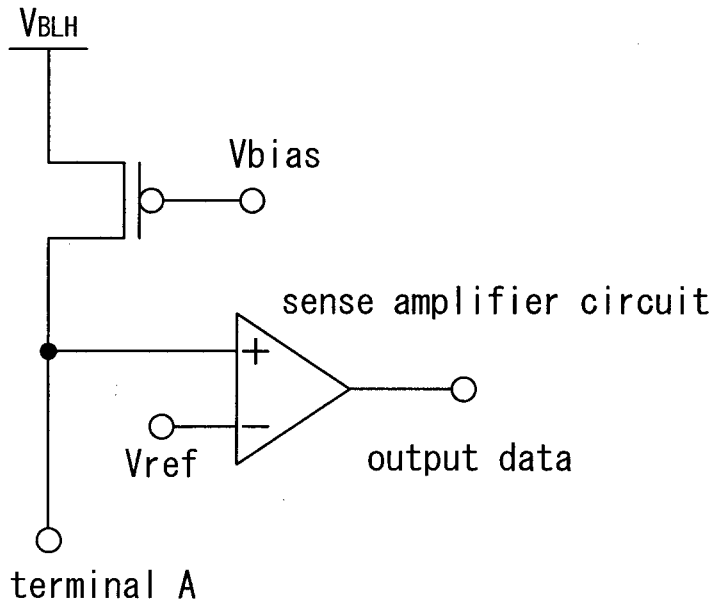

VBLH
Vbias
sense amplifier circuit
+
−
Vref
output data
terminal A

FIG. 6

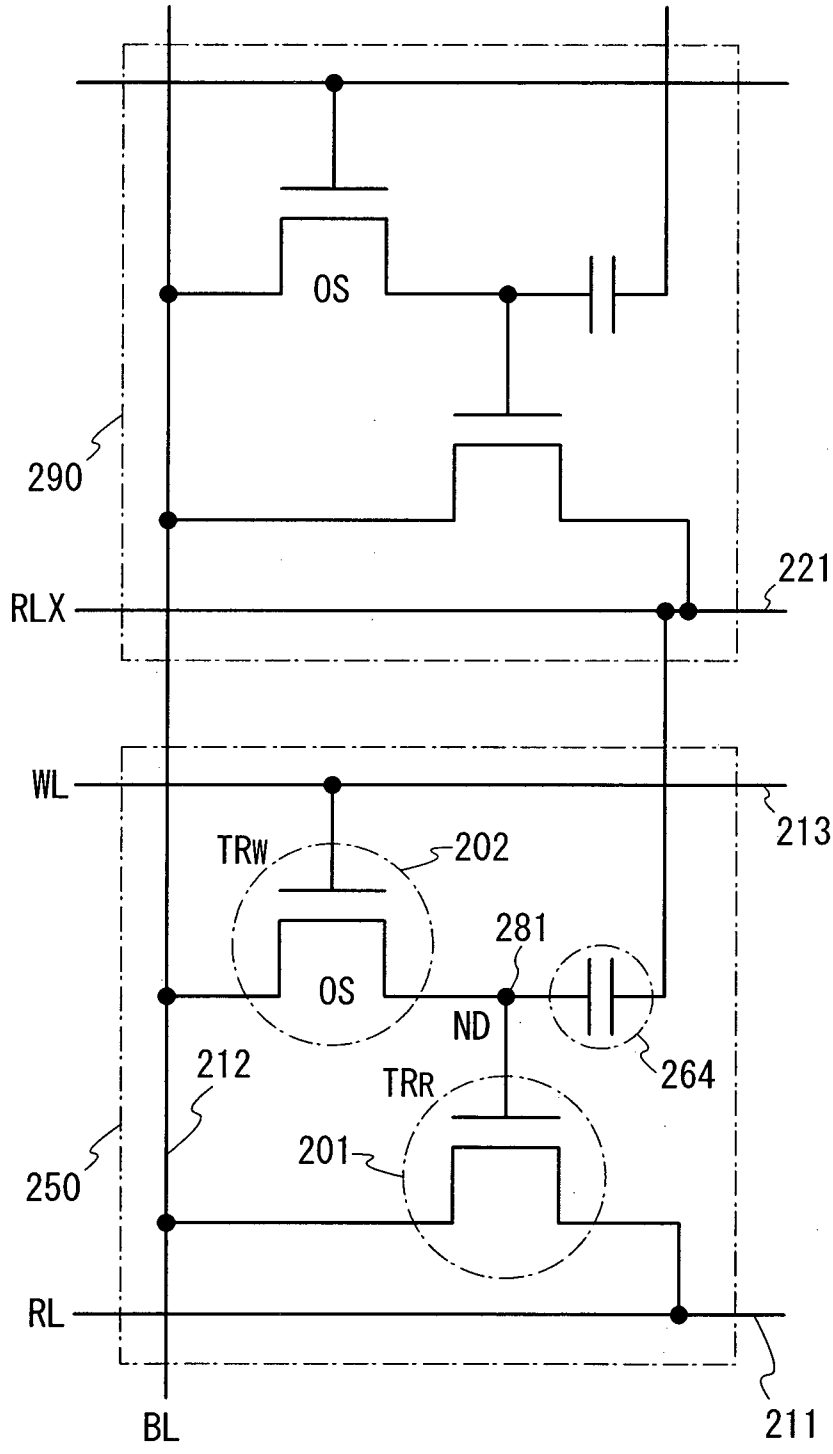

OS
290
RLX
221
WL
213
TRW
202
281
OS
ND
264
212
TRR
201
250
RL
BL
211

FIG. 7

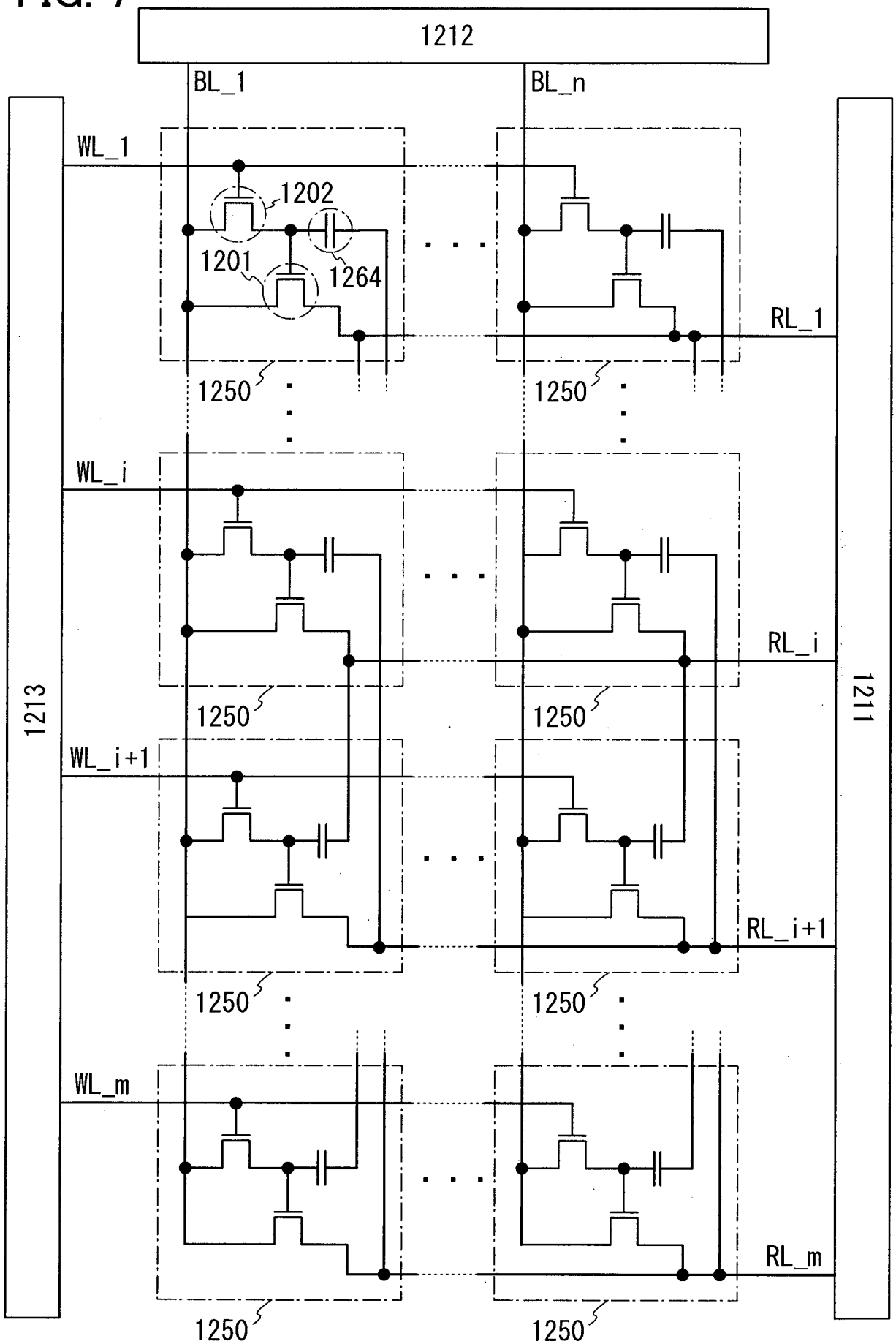

1212
BL_1
BL_n
WL_1
1202
1201
1264
RL_1
1250
WL_i
RL_i
WL_i+1
RL_i+1
WL_m
RL_m
1213
1211

FIG. 8A

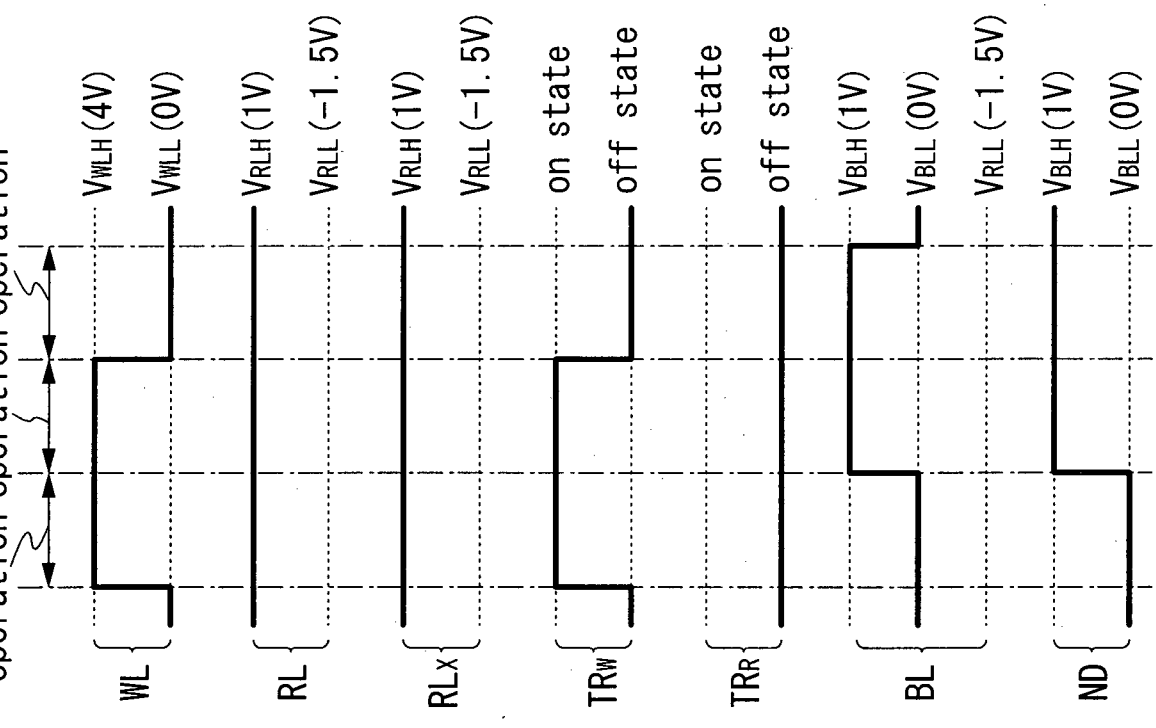

first operation
second operation
third operation
WL
RL
RLX
TRW
TRR
BL
ND
VWLH (4V)
VWLL (0V)
VRLH (1V)
VRLL (−1.5V)
VRLH (1V)
VRLL (−1.5V)
on state
off state
on state
off state
VBLH (1V)
VBLL (0V)
VRLL (−1.5V)
VBLH (1V)
VBLL (0V)

FIG. 8B

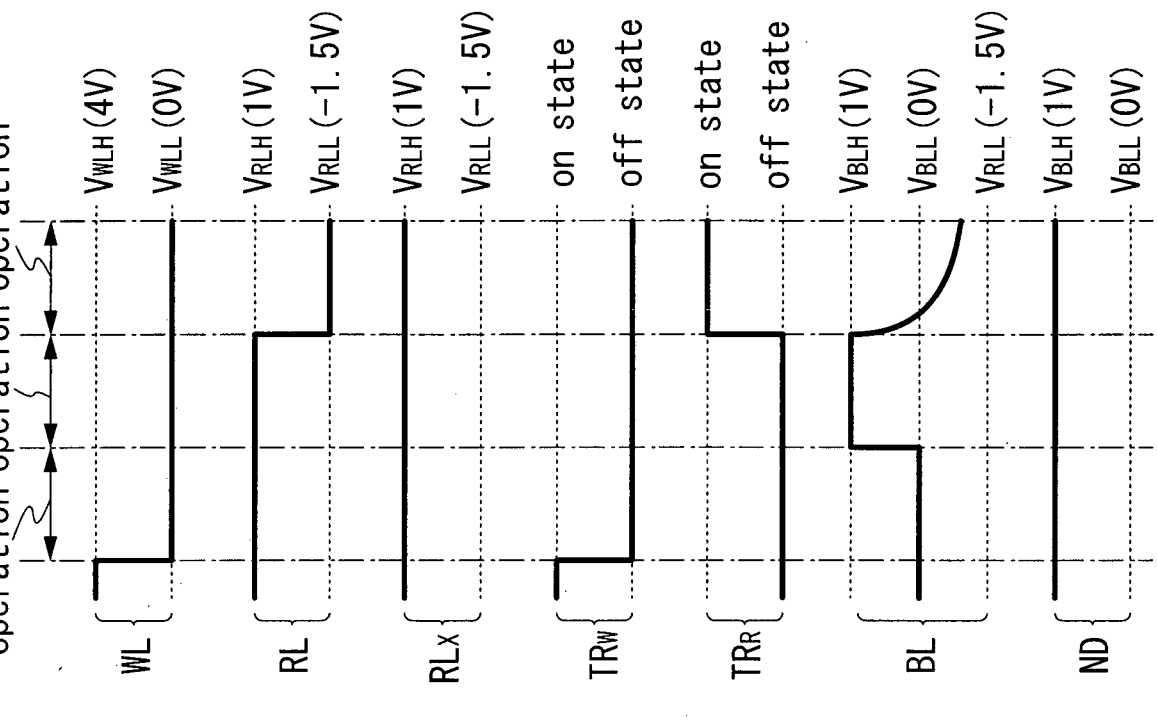

first operation
second operation
third operation
WL
RL
RLX
TRW
TRR
BL
ND
VWLH (4V)
VWLL (0V)
VRLH (1V)
VRLL (−1.5V)
VRLH (1V)
VRLL (−1.5V)
on state
off state
on state
off state
VBLH (1V)
VBLL (0V)
VRLL (−1.5V)
VBLH (1V)
VBLL (0V)

FIG. 9A

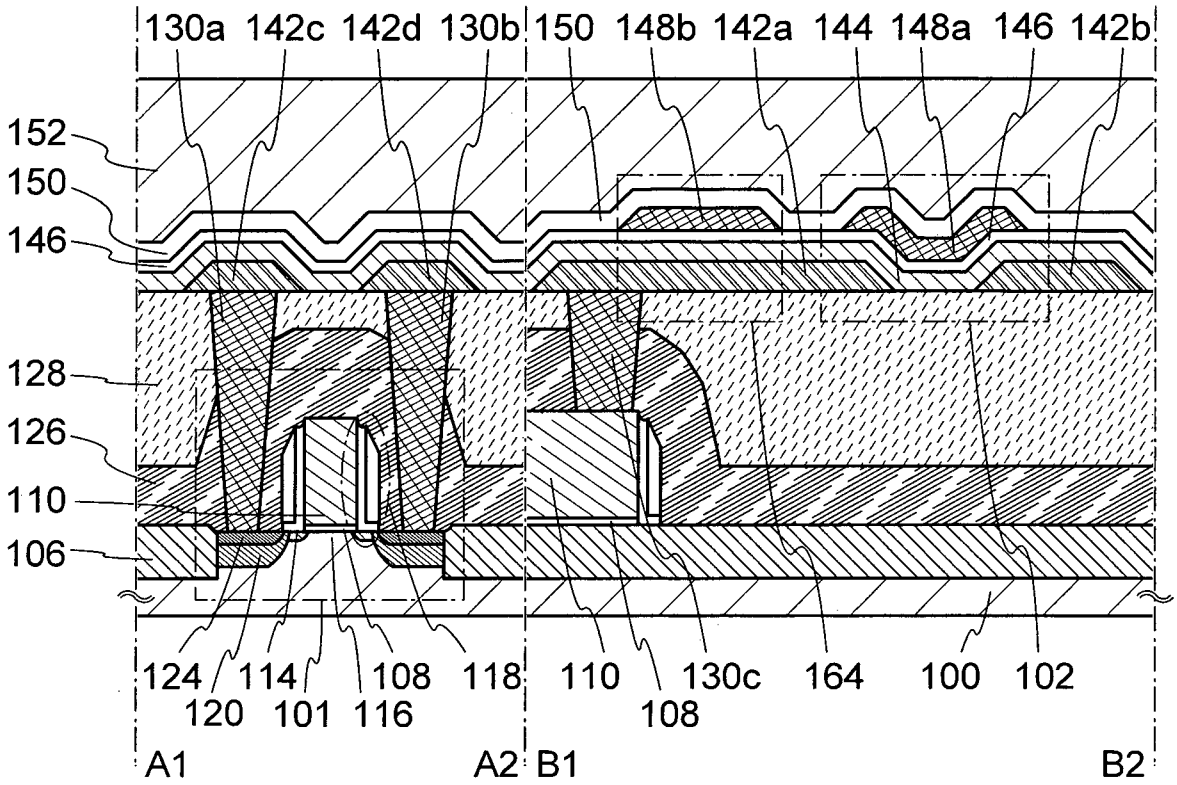

130a
142c
142d
130b
150
148b
142a
144
148a
146
142b
152
150
146
128
126
110
106
124
120
114
101
108
116
118
110
108
130c
164
100
102
A1
A2
B1
B2

FIG. 9B

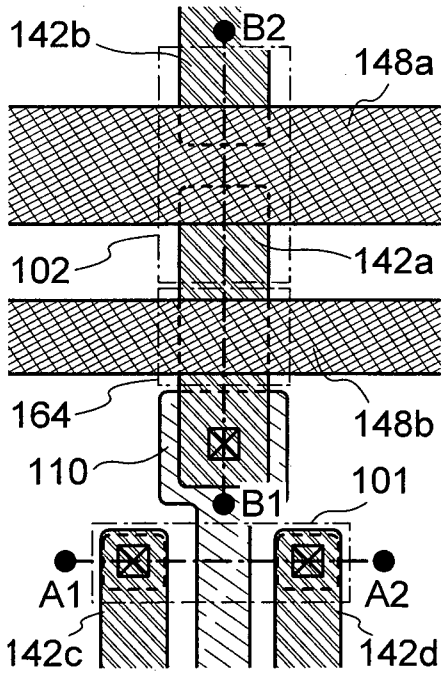

142b
B2
148a
102
142a
164
148b
110
101
B1
A1
A2
142c
142d

FIG. 10A

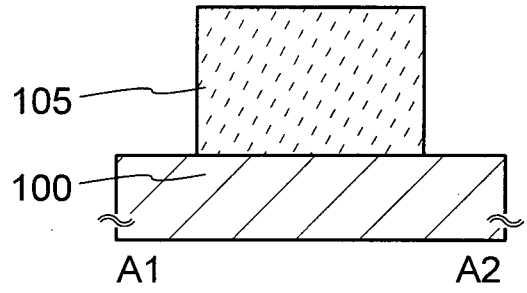


FIG. 10B

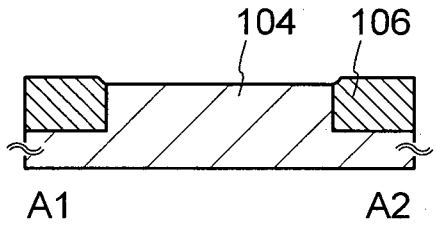


FIG. 10C

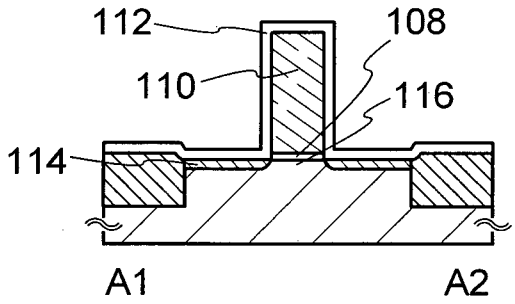


FIG. 10D

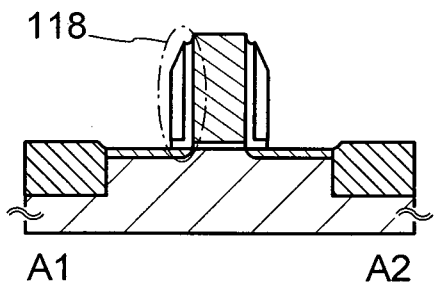


FIG. 10E

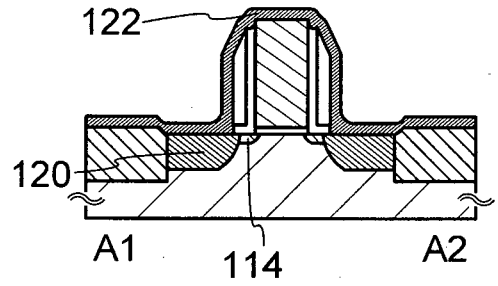


FIG. 10F

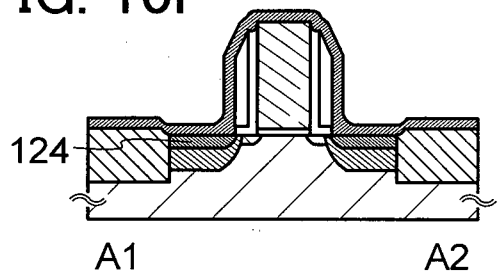


FIG. 10G

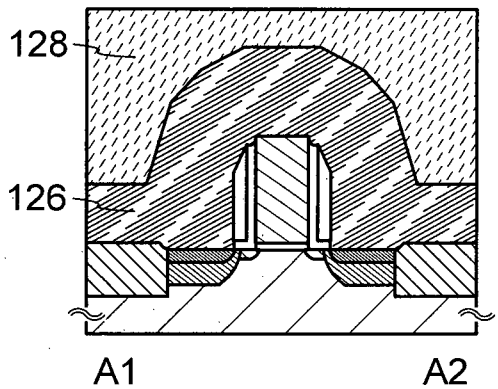


FIG. 10H

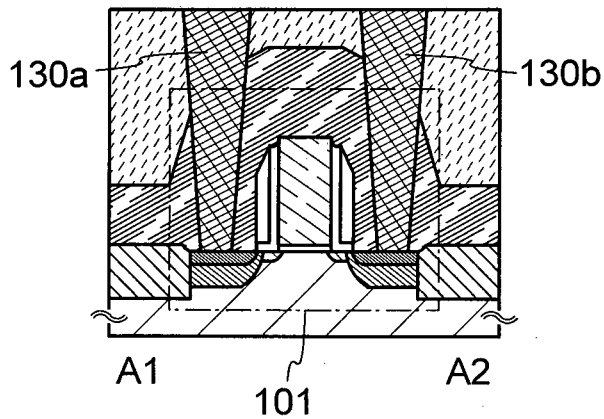


FIG. 11A

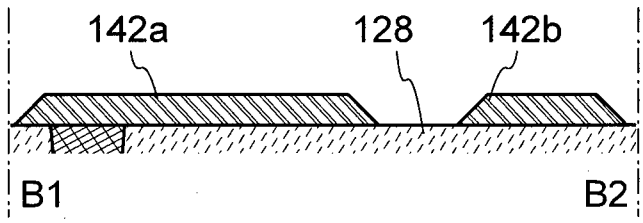


FIG. 11B

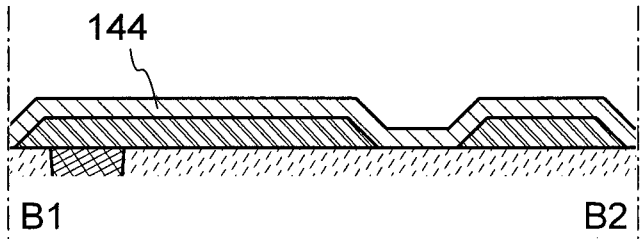


FIG. 11C

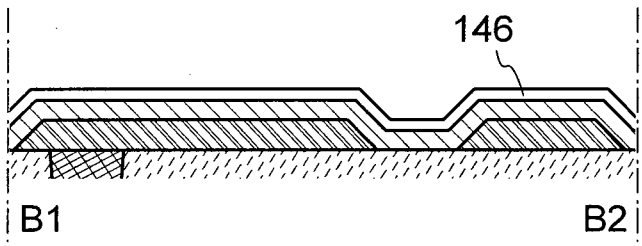


FIG. 11D

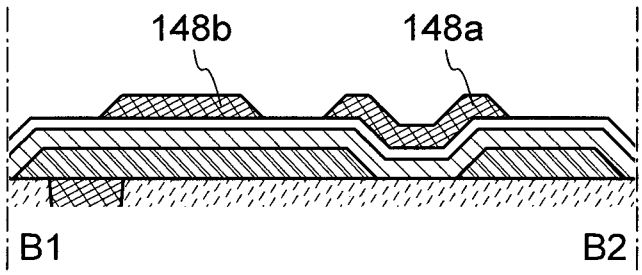


FIG. 11E

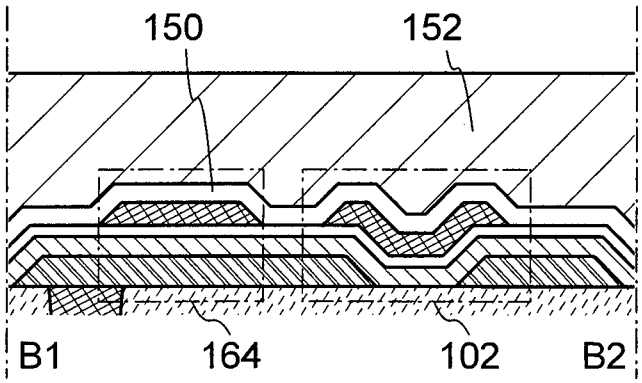


FIG. 12A

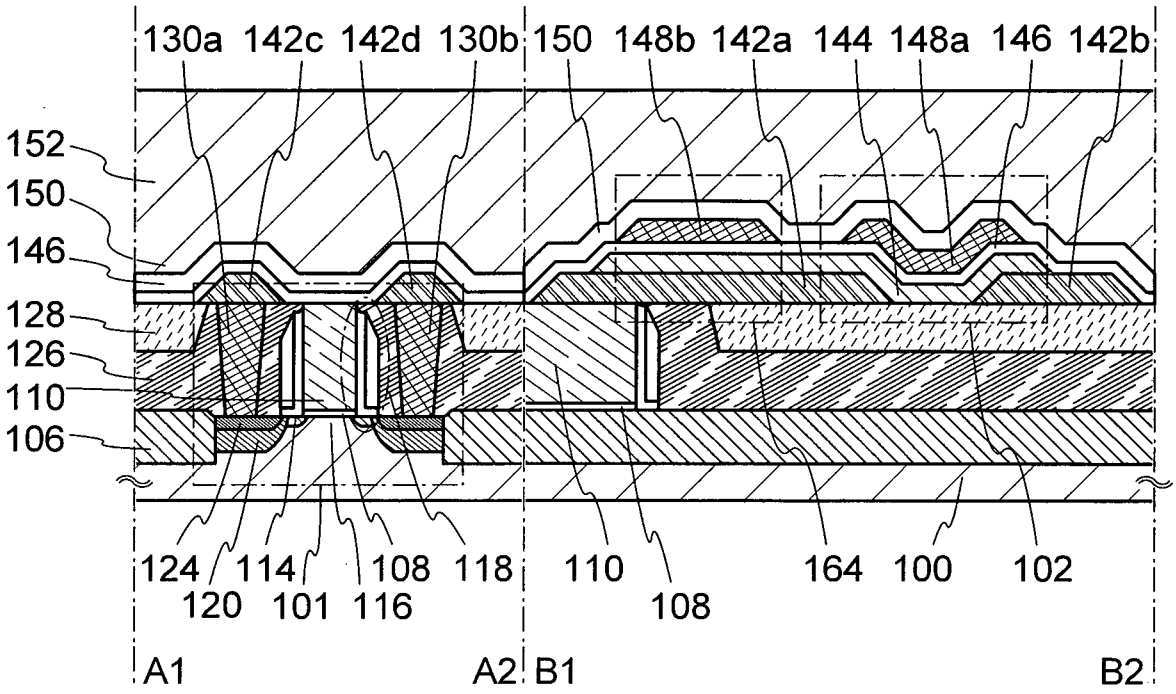


FIG. 12B

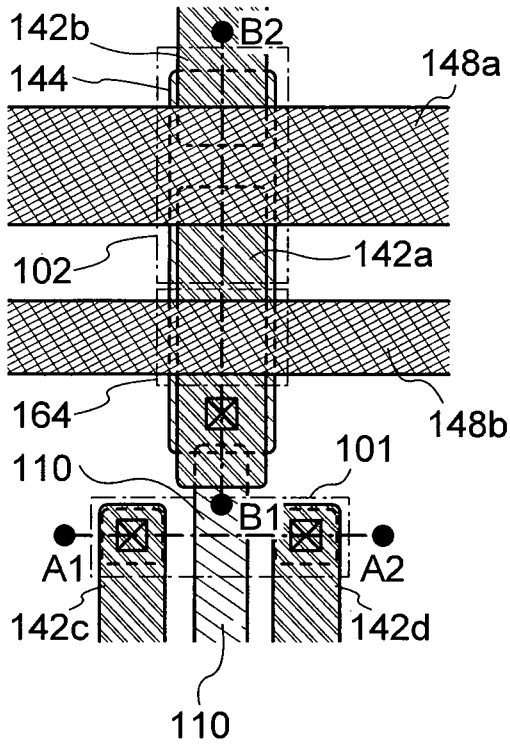


FIG. 13A

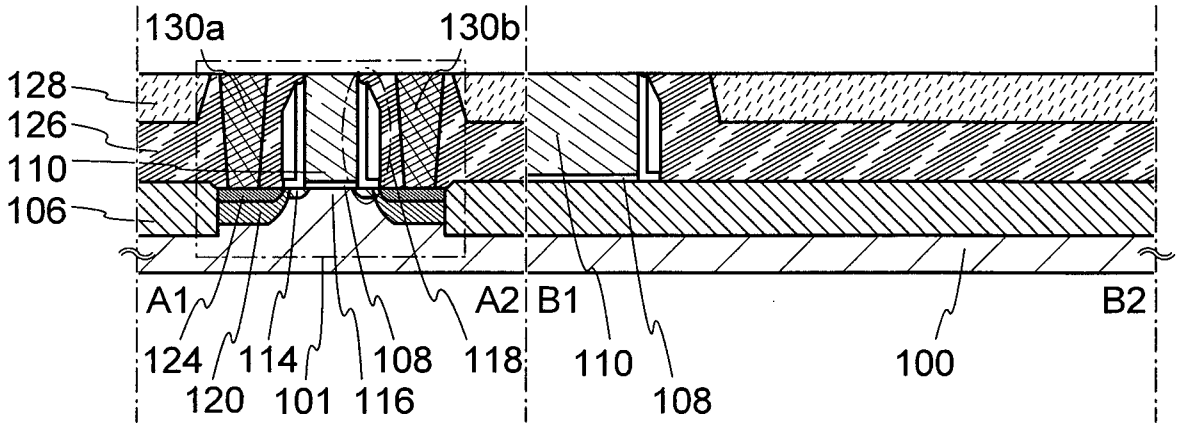


FIG. 13B

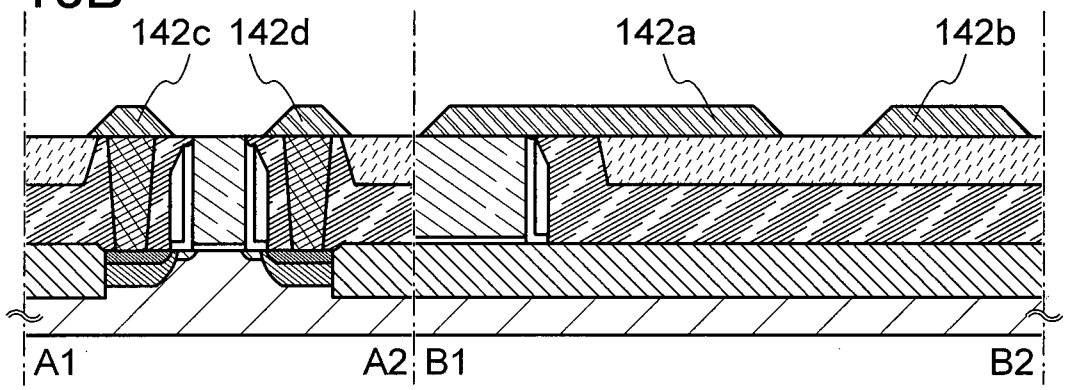


FIG. 13C

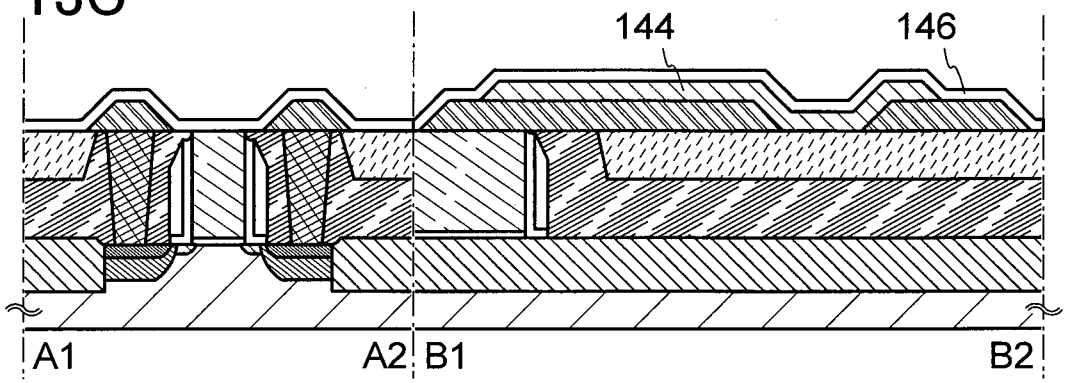


FIG. 13D

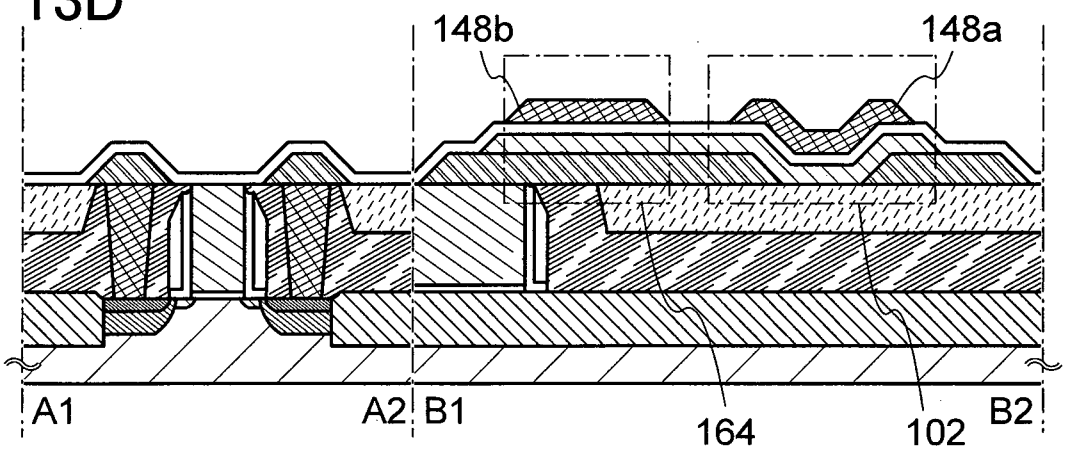


FIG. 14A

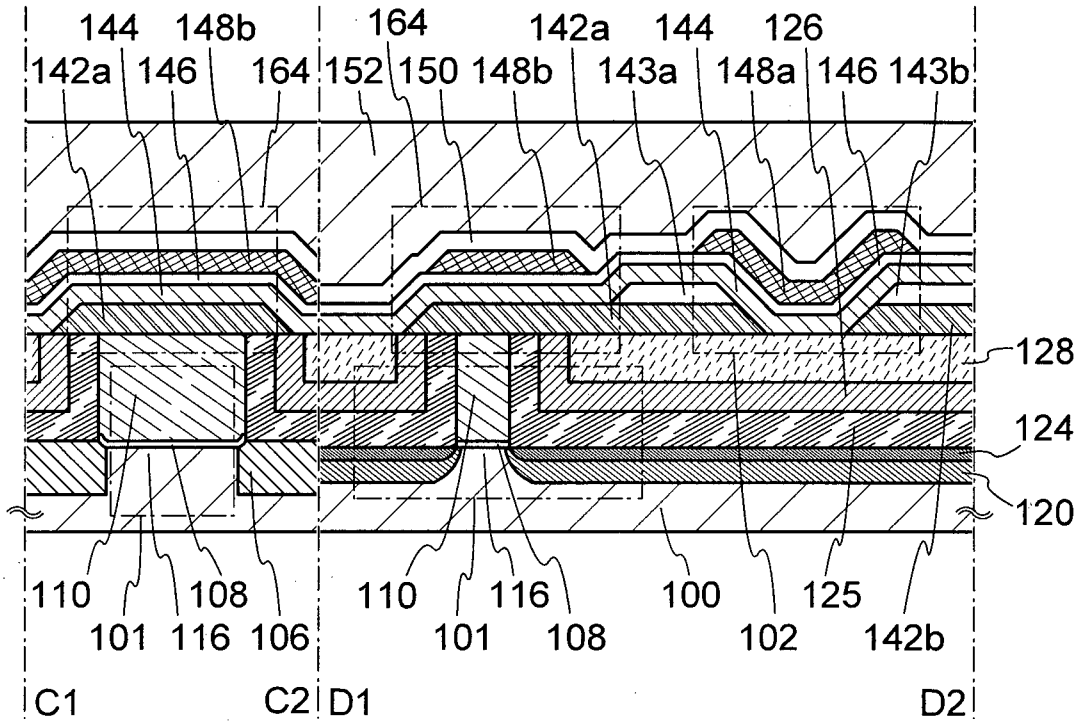


FIG. 14B

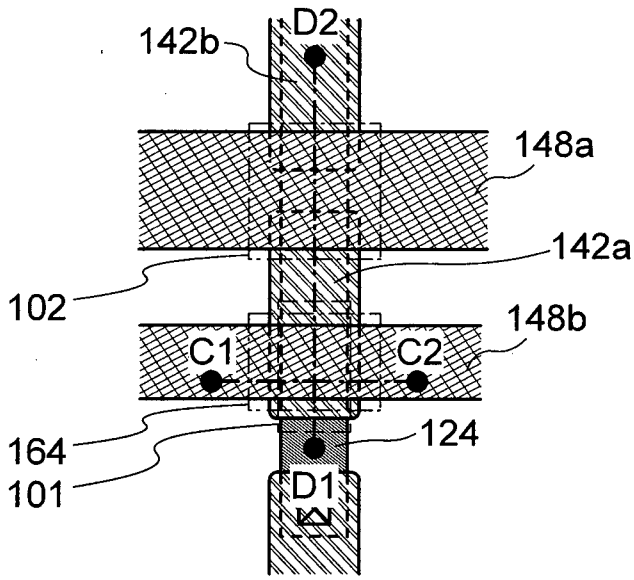


FIG. 15A

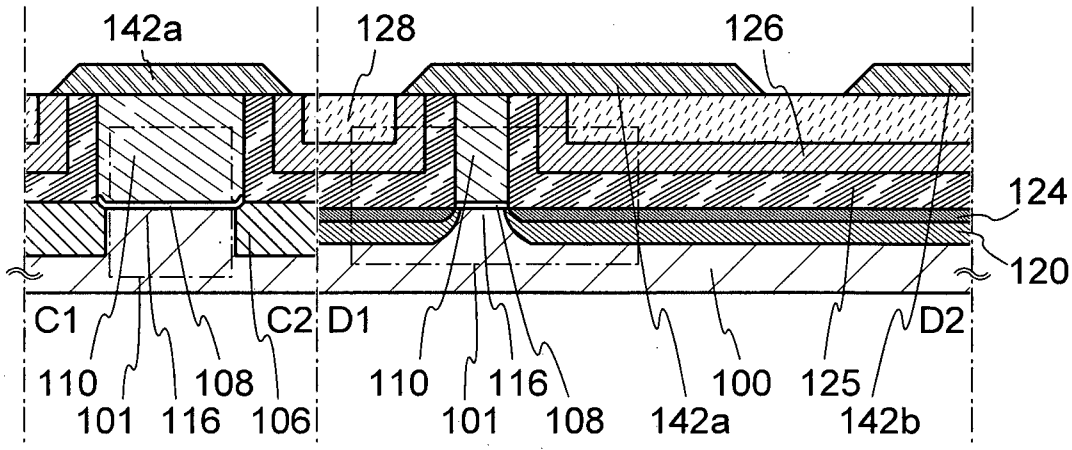


FIG. 15B

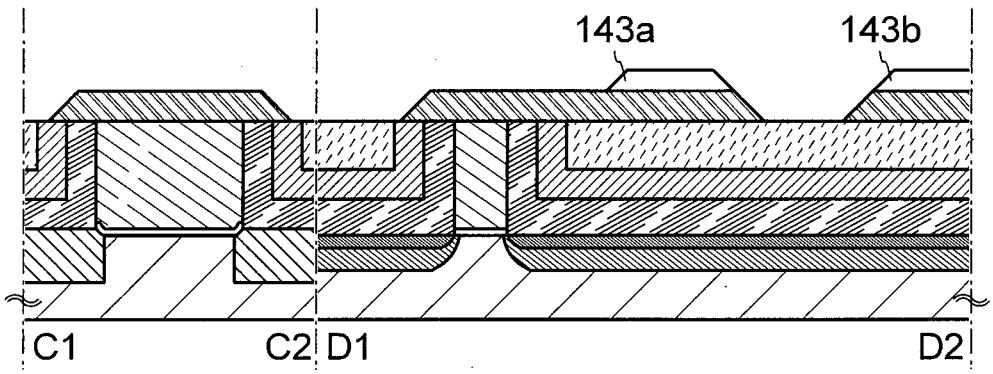


FIG. 15C

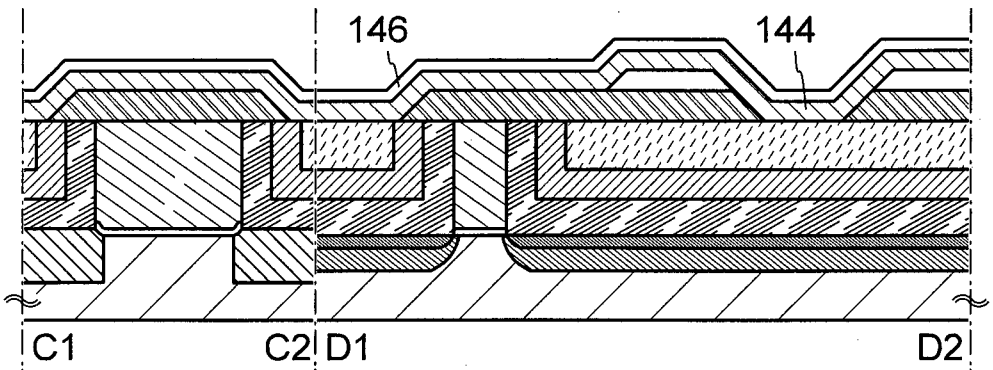


FIG. 16A

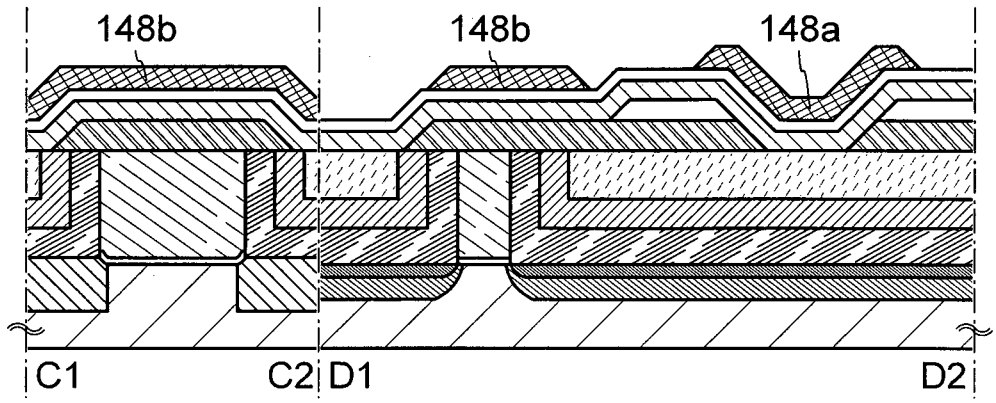


FIG. 16B

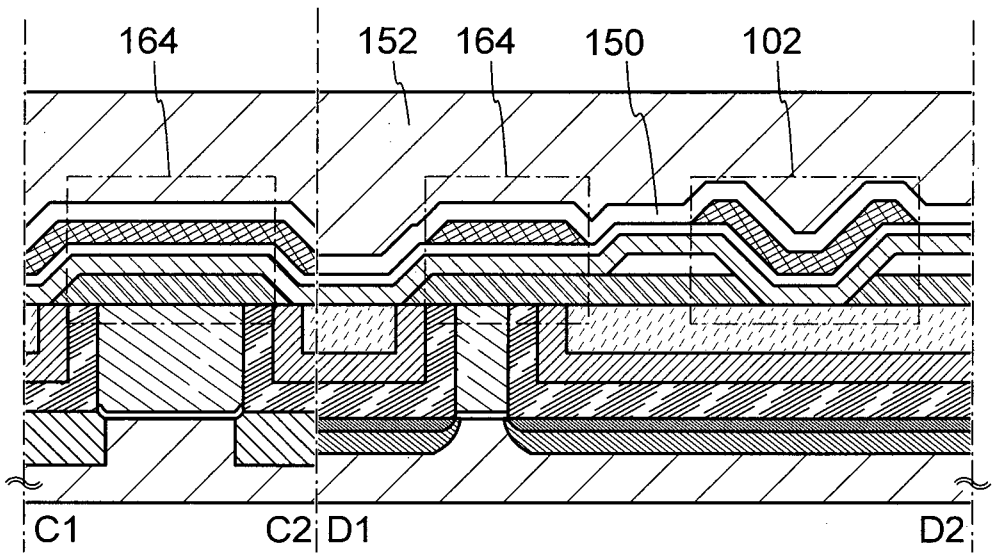


FIG. 17A

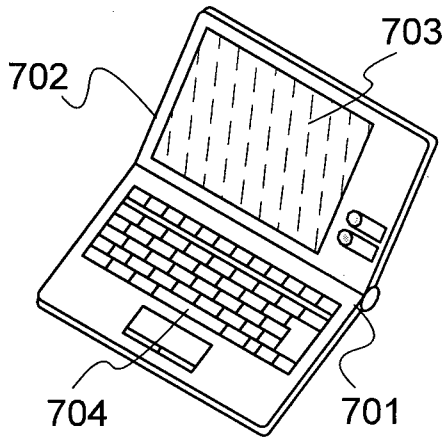


FIG. 17B

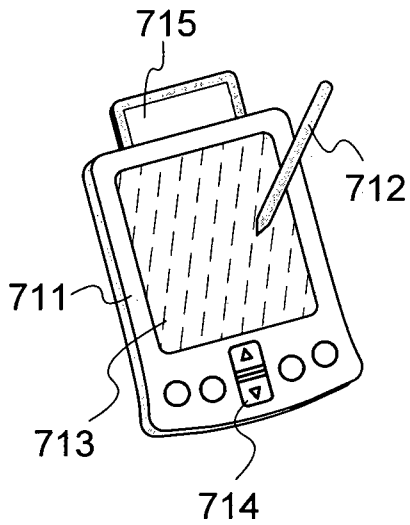


FIG. 17C

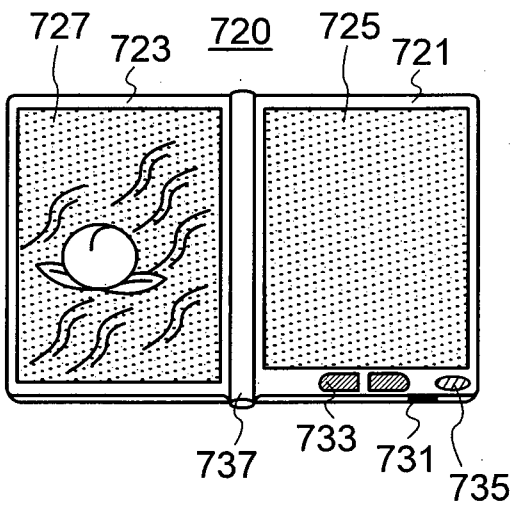


FIG. 17D

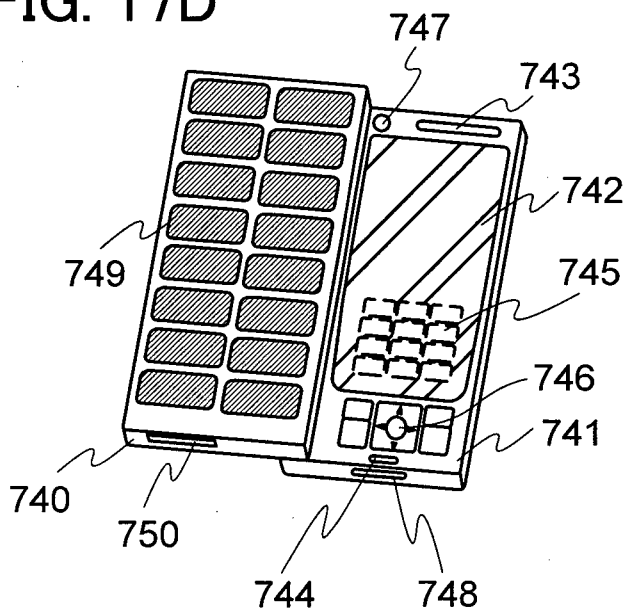


FIG. 17E

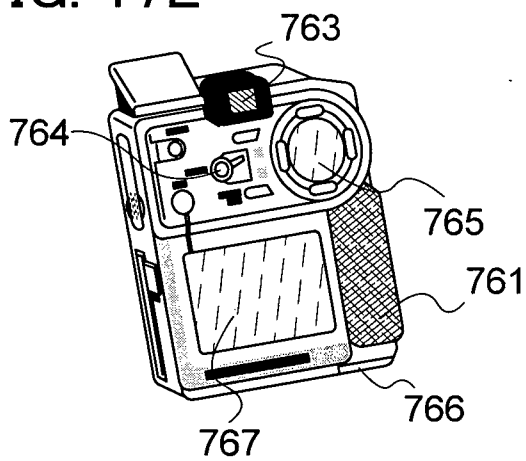


FIG. 17F

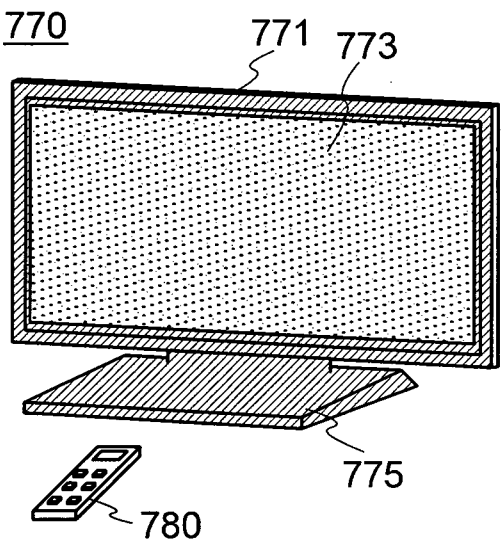


FIG. 18

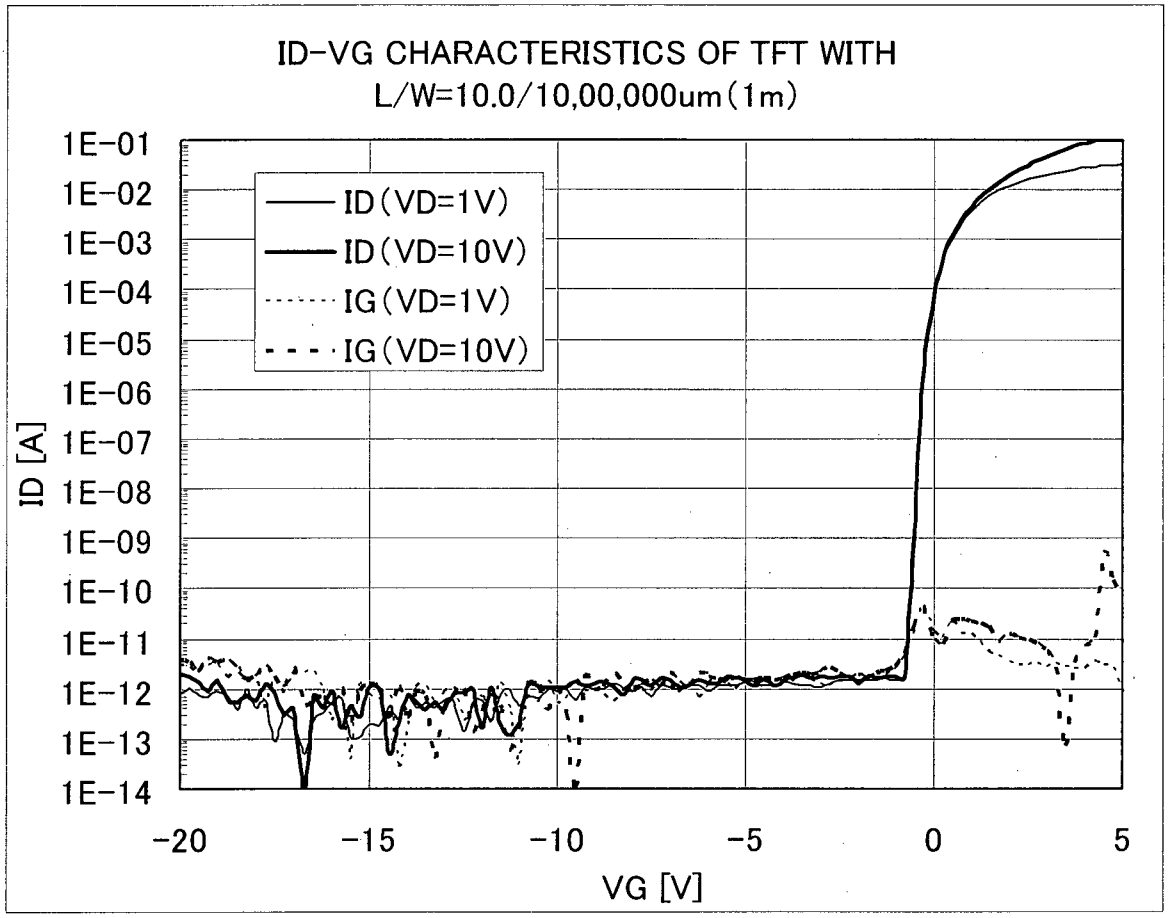

ID-VG CHARACTERISTICS OF TFT WITH
L/W=10.0/10,00,000um(1m)
ID(VD=1V)
ID(VD=10V)
IG(VD=1V)
IG(VD=10V)
ID [A]
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
1E-14
-20
-15
-10
-5
0
5
VG [V]

FIG. 19

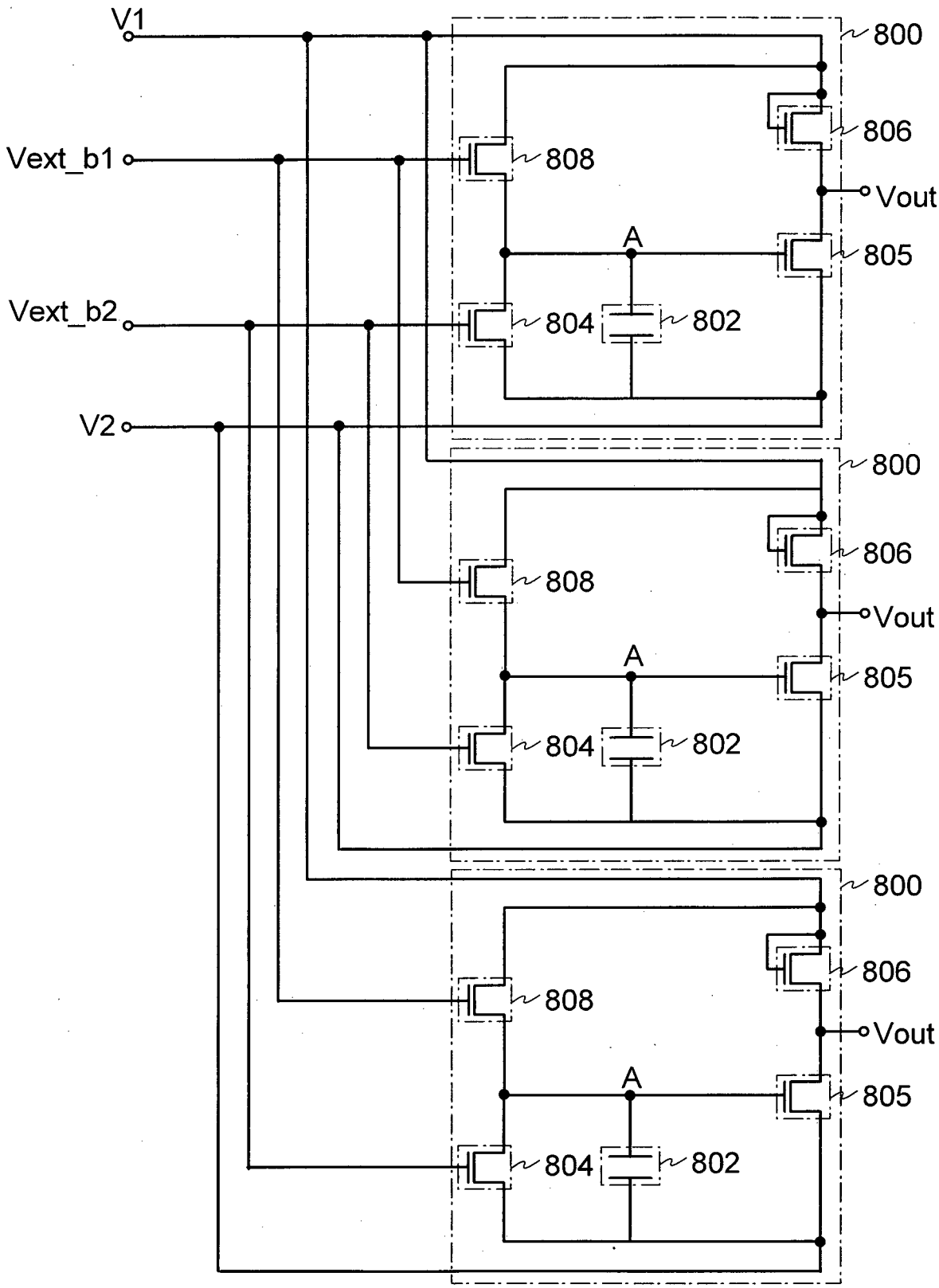

V1
Vext_b1
Vext_b2
V2
800
806
808
Vout
A
805
804
802
800
806
808
Vout
A
805
804
802
800
806
808
Vout
A
805
804
802

FIG. 20

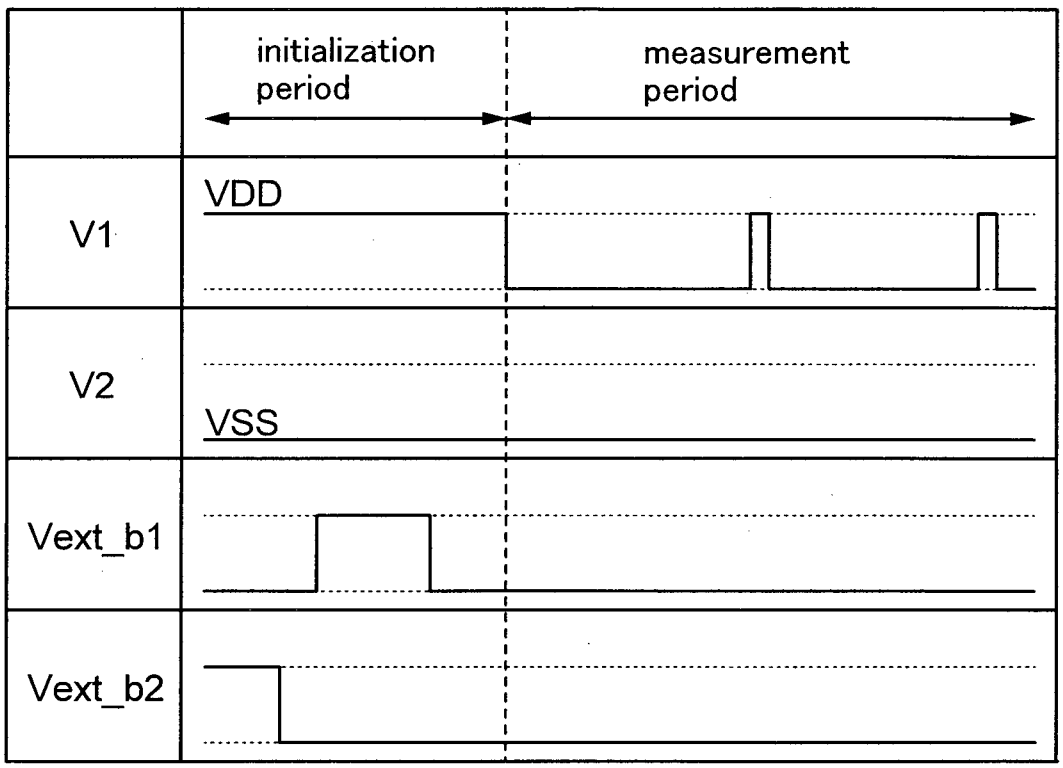

initialization period
measurement period
V1
VDD
V2
VSS
Vext_b1
Vext_b2

FIG. 21

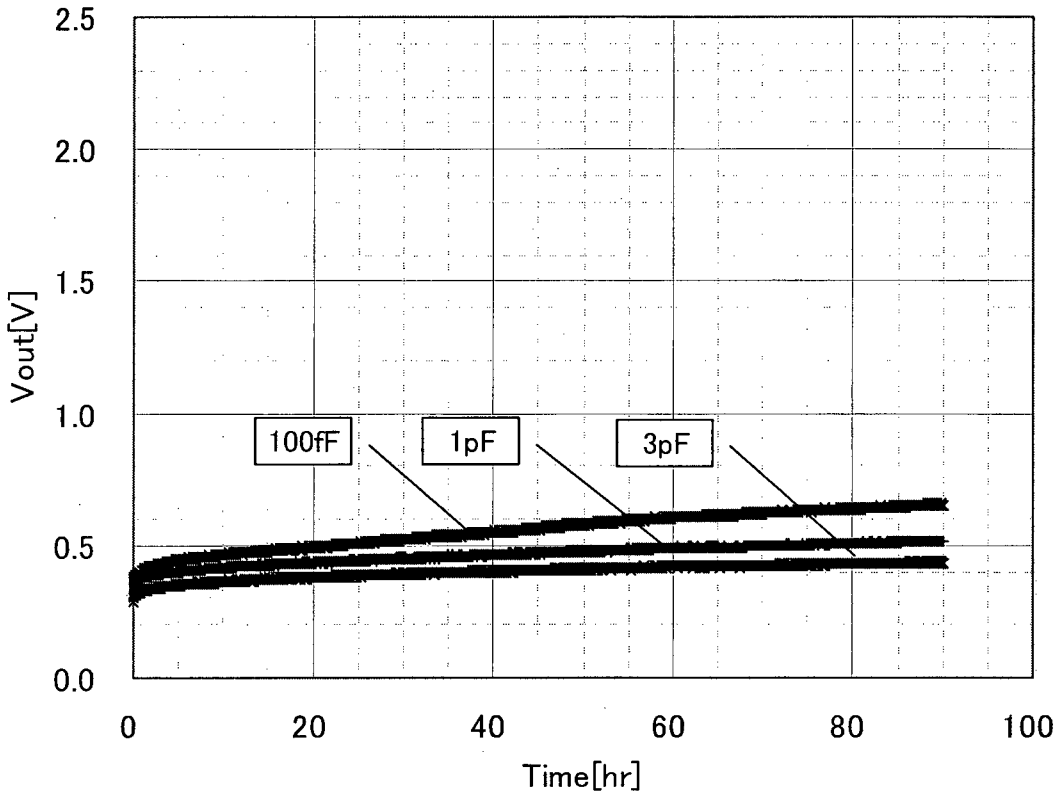
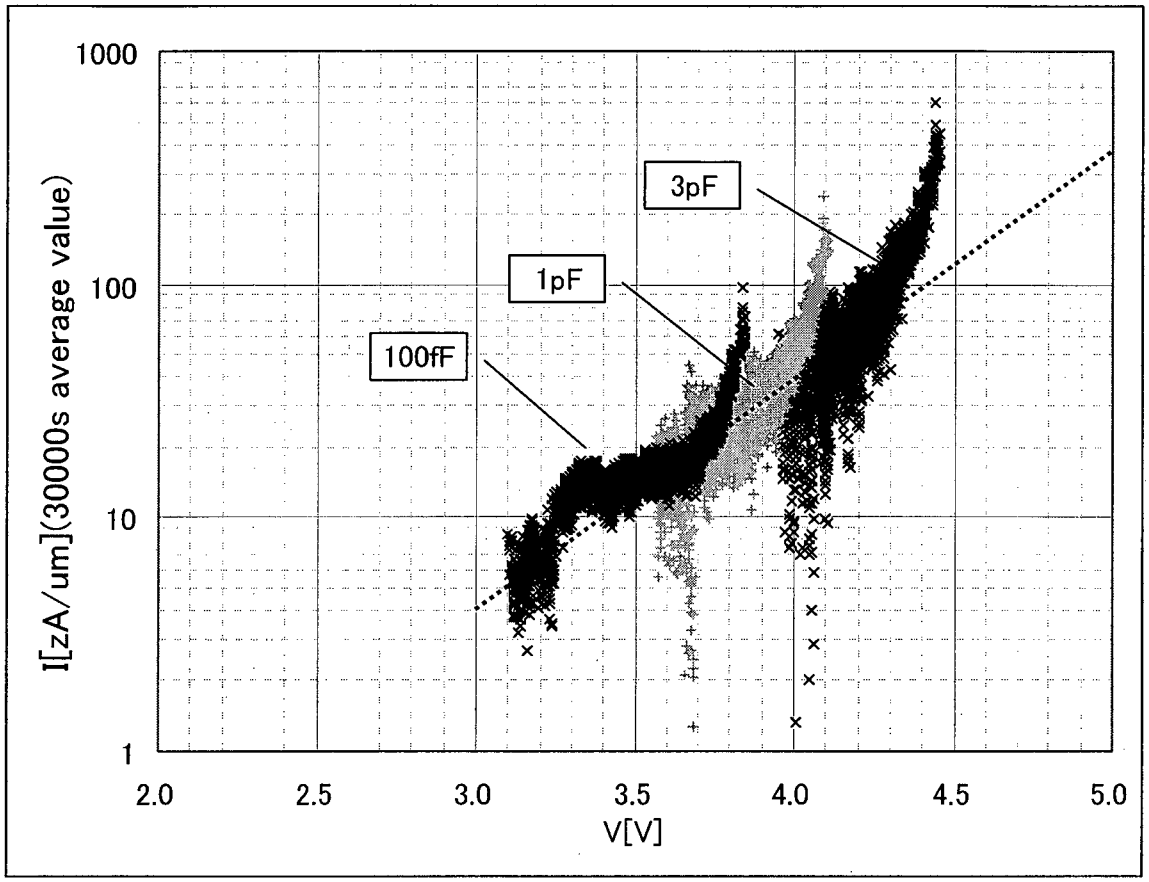


FIG.22


1000
100
10
1
I[zA/um](30000s average value)
2.0
2.5
3.0
3.5
4.0
4.5
5.0
V[V]
3pF
1pF
100fF

EXPLANATION OF REFERENCE

100: substrate, 101: transistor, 102: transistor, 104: semiconductor region, 105: protective layer, 106: element isolation insulating layer, 108: gate insulating layer, 110: gate electrode, 112: insulating layer, 114: impurity region, 116: channel formation region, 118: sidewall insulating layer, 120: high-concentration impurity region, 122: metal layer, 124: metal compound region, 125: interlayer insulating layer, 126: interlayer insulating layer, 128: interlayer insulating layer, 144: oxide semiconductor layer, 146: gate insulating layer, 150: interlayer insulating layer, 152: interlayer insulating layer, 164: capacitor, 200: memory cell, 201: transistor, 202: transistor, 211: wiring, 212: wiring, 213: wiring, 221: wiring, 240: memory cell, 250: memory cell, 264: capacitor, 281: node, 290: memory cell, 701: housing, 702: housing, 703: display portion, 704: keyboard, 711: main body, 712: stylus, 713: display portion, 714: operation button, 715: external interface, 720: e-book reader, 721: housing, 723: housing, 725: display portion, 727: display portion, 731: power supply, 733: operation key, 735: speaker, 737: hinge portion, 740: housing, 741: housing, 742: display panel, 743: speaker, 744: microphone, 745: touch panel, 746: pointing device, 747: camera lens, 748: external connection terminal, 749: solar cell, 750: external memory slot, 761: main body, 763: eyepiece, 764: operation switch, 765: display portion, 766: battery, 767: display portion, 770: television set, 771: housing, 773: display portion, 775: stand, 780: remote controller, 800: measurement system, 802: capacitor, 804: transistor, 805: transistor, 806: transistor, 808: transistor, 1200: memory cell, 1201: transistor, 1202: transistor, 1211: driver circuit, 1212: driver circuit, 1213: driver circuit, 1250: memory cell, 1264: capacitor, 130a: source or drain electrode,

130b: source or drain electrode, 130c: electrode, 142a: source or drain electrode, 142b: source or drain electrode, 142c: wiring, 142d: wiring, 143a: insulating layer, 143b: insulating layer, 148a: gate electrode, 148b: electrode, 802a: capacitor, 802b: capacitor, 802c: capacitor.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/050614

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G11C11/405(2006.01)i, G11C11/401(2006.01)i, H01L21/8242(2006.01)i, H01L27/108(2006.01)i, H01L29/786(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G11C11/405, G11C11/401, H01L21/8242, H01L27/108, H01L29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6314017 B1 (SONY CORPORATION) 2001.11.06, column 16, line 53 to column 19, line 5, Figs.12, 16 & JP 2001-93988 A & KR 10-2001-0015418 A	13-16 1-8, 9-12
Y	JP 54-142031 A (NEC CORPORATION) 1979.11.05, column 3, line 4 to column 4, line 2, Fig.2 (Family: None)	1-8, 9-12
Y	JP 2002-368226 A (SHARP KABUSHIKI KAISHA) 2002.12.20, Paragraphs 0045-0054, Fig.8 (Family: None)	2-4, 10-12
Y	US 2006/0113565 A1 (CANON KABUSHIKI KAISHA) 2006.06.01, Paragraphs 0289-0325, Figs.17-47 & JP 2006-165532 A	2-4, 10-12

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search	Date of mailing of the international search report
12.04.2011	19.04.2011

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/050614

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0194379 A1 (JAPAN SCIENCE AND TECHNOLOGY) 2007.08.23, the whole document & EP 1737044 A1 & WO 2005/088726 A1 & KR 10-2006-0123765 A	1-16
A	US 2002/0096702 A1 (Tomoyuki ISHII) 2002.07.25, the whole document & JP 2002-94029 A & KR 10-2002-0021310 A	1-16