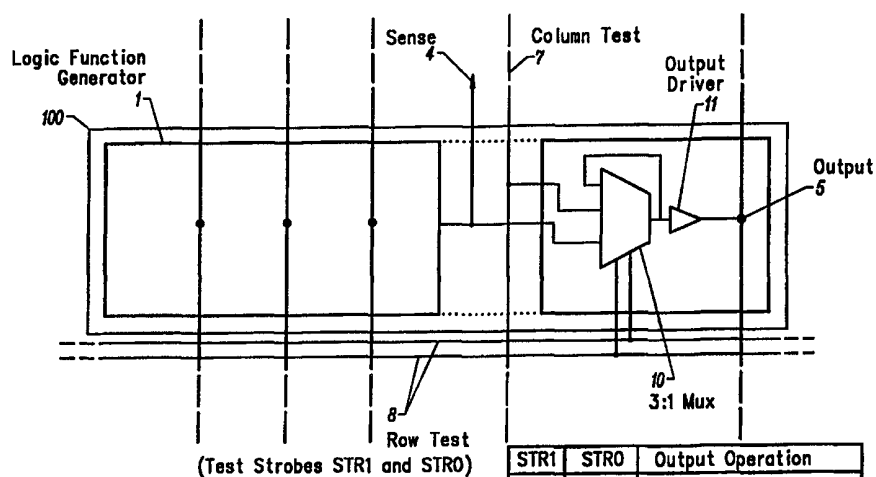




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(21) International Application Number: PCT/US98/06567 (22) International Filing Date: 2 April 1998 (02.04.98) (71) Applicant: LIGHTSPEED SEMICONDUCTOR CORPORATION [US/US]; 1151 Sonora Court, Sunnyvale, CA 94086 (US). (72) Inventor: OSANN, Robert, Jr.; 328 Costello Court, Los Altos, CA 94024 (US). (74) Agents: FLIESLER, Martin, C. et al.; Fliesler, Dubb, Meyer & Lovejoy LLP, Four Embarcadero Center, Suite 400, San Francisco, CA 94111-4156 (US).		(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: INTEGRATED CIRCUIT ARCHITECTURE HAVING AN ARRAY OF TEST CELLS PROVIDING FULL CONTROLLABILITY FOR AUTOMATIC CIRCUIT VERIFICATION



STR1	STR0	Output Operation
0	0	Normal
0	1	Latch Closed
1	1	Latch Open

Table 1. Interpretation of test Strobes STR1 and STR0

(57) Abstract

A new circuit architecture is provided for testing digital integrated circuits which allows one to arbitrarily force any combination of logic values to be simultaneously driven onto any combination of internal nets. This allows all of the connections to each internal logic cell, and the logic cell itself, to be verified by applying a set of test patterns to each logic cell individually. In this way, the integrity of the entire device can be verified without having knowledge of the operation of the circuit as a whole.

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5 Integrated Circuit Architecture
 Having an Array of Test Cells Providing
 Full Controllability for Automatic Circuit Verification

FIELD OF THE INVENTION

10 This invention relates to imbedded test structures for integrated circuits, and in particular to structures for testing those devices known as Application Specific Integrated Circuits or ASICs.

BACKGROUND OF THE INVENTION

This invention addresses the problem of testing complex digital integrated circuits. Many families of integrated circuits fall into the category known as ASICs. The most prolific of these is known as Gate Arrays. Gate Arrays are usually prefabricated up to a certain stage (typically through all steps except metalization). The metal patterns are then configured according to the needs of the user's application. For these types of ASICs, it is necessary to test the circuit after the fabrication process is completed to insure the integrity of the circuit.

Today, virtually all such testing is done by applying a stream of test vectors to the integrated circuit device. A test vector is a pattern of signal values, some of which are applied to the integrated circuit device, and some of which represent an expected response from the integrated circuit device.

25 The important point is that these vectors are applied to the periphery of the

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integrated circuit device, in a sequence which corresponds to a proper operational sequence of the integrated circuit device's internal circuitry. Most important is that this stream of vectors must be created and that the burden of this tedious task almost always falls on the user himself.

5 There have been many attempts to provide software which creates these vectors automatically. Unfortunately, none of these attempts have produced a solution which works for the majority of user applications. Automated solutions which functionally exercise a circuit work best when the user's application is implemented in regular, synchronous circuits. To further
10 automate the testing of such synchronous designs, engineers have often added test circuitry to integrated circuits which is known as "scan test" circuitry, also known as "LSSD" and "boundary scan" circuitry. Examples of this type of test circuit are many, and include U.S. Patents No.4,488,259 to Mercy, No.4,441,075 to McMahon, No.4,780,874 to Lenoski, and No.4,682,329 to
15 Kluth, among others.

 Scan test structures rely on stages of registers placed between blocks of combinatorial logic where extra circuitry has been added to allow the register contents to be shifted either in or out to allow the initialization or observation of logic states during testing. Unfortunately, a great many engineers don't
20 design fully synchronous circuits where this type of structure can be used.

 Attempts have also been made to add various forms of imbedded test circuitry aimed at testing integrated circuits regardless of what design style was employed by the designer. One of these is shown in U.S. Pat No. 4,739,250 to Tanizawa where a gate array comprised of logic cells has a
25 separate access circuit attached to an input of each logic cell, this access

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circuit being able to force a specific logic value at the output of the logic cell under control of row and column selection wires. This scheme can test every logic cell and connection, but only if they are of the simple NAND or NOR variety. It cannot arbitrarily apply any pattern to the inputs of all logic cells
5 due to the limitation of the row and column addressing which controls the access circuits which, in turn, drive the test input of each logic cell. While it is possible to construct a gate array which uses simple NAND or NOR gates as the logic cell, a more complex logic cell is generally more effective when test circuitry is to be added on a per-cell basis.

10 Another test circuit which is intended for integrated circuits which may use either synchronous or non-synchronous designs is shown in U.S. Pat No. 4,749,947 to Gheewala. This approach adds a row and column grid which connects to transistor pass-gates to selectively observe or drive a net in the user's circuit. This circuit is intended primarily to provide complete
15 observability when used in conjunction with automatic test vector generation software. It has a limited ability to drive signals in the circuit, again due to limitations inherent in row and column addressing. As with the previous example, this test architecture cannot arbitrarily apply any pattern to the inputs of all logic cells.

20 Yet another example of prior art test circuits is U.S. Pat No. 4,752,729 to Jackson. Although this circuit appears to be intended mostly for applying patterns useful for life-testing a device, its technique has some application in general circuit test. Here, interface circuits are inserted at various points within an integrated circuit. Each interface circuit controls the
25 value of the logic signal which passes through the particular net under control of test signals which come from the exterior of the device and are connected

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in common to all interface circuits. Interface circuits can allow a signal simply to pass through or alternately to be forced to a logic "1" or "0" value. It is important to note that since all interface circuits follow the same test signals, it is impossible to use this scheme for applying any arbitrary pattern to any logic circuit within the integrated circuit.

Each of the imbedded test circuits in the last three examples has some ability to test an integrated circuit device regardless of whether the designer chose synchronous or asynchronous design techniques. However, none of these can fully control all the inputs of an internal circuit simultaneously and thus test that circuit by applying any arbitrary pattern to its inputs. It is this controllability that has been lacking and thus prevented an integrated circuit to be fully tested for all possible design implementations, using an imbedded test circuit.

SUMMARY OF THE INVENTION

The object of the present invention is to provide, in an integrated circuit device containing multiple logic cells, imbedded test circuitry which does not require a particular design technique on the part of the user, or a particular logic cell structure (in other words, the designer may use synchronous or asynchronous design techniques). This imbedded test circuitry can also verify the integrity of the entire device without any knowledge of the operation of the implemented circuit as a whole. To accomplish this, a new architecture is disclosed which provides the ability to arbitrarily force any combination of logic values to be simultaneously driven onto any combination of internal nets. This allows all of the connections to each logic cell, and the logic cell itself, to be verified by applying a set of arbitrary test patterns to all of the inputs of each logic cell individually.

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To apply any arbitrary test pattern to the inputs of a logic cell, the present invention provides test storage elements which are distributed throughout the integrated circuit device and control test circuits which determine the logic state on selected logic cell outputs within the integrated circuit device. These test circuits which allow any logic value to be forced on a logic cell output are inserted into each logic cell just before the logic cell output. As the addition of these circuits in series with the logic cells adds some delay to any logic signal passing through a logic cell, it is a further object of this invention to combine the test storage elements and added test circuits so as to minimize any added delay or additional numbers of transistors due to the presence of the imbedded test circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a portion of the logic cell based array of an integrated circuit utilizing the present invention.

Fig. 2 shows an expanded view of one logic cell of the present invention showing the Logic Function Generator along with the Output Driver and Test Latch.

Fig. 3 shows an expanded view of an alternative embodiment of one logic cell having greater flexibility.

Table 1 shows how the value encoded in the Test Strobe bits of the circuit implementation of Fig. 2 affect the operation of that circuit.

Table 2 shows how the value encoded in the Test Data bits of the

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circuit implementation of Fig. 3 affect the operation of that circuit.

DETAILED DESCRIPTION

The present invention requires a logic cell based array approach as shown in Fig. 1. In accordance with the invention, each logic cell 100 is made up of two parts, the Logic Function Generator 1 and the Output Driver and Test Latch 2, which is inserted between the outputs of any driven circuitry (i.e., the logic function generator) and the logic cell output which would otherwise be connected to the logic function generator. There may be any number of inputs 3 to Logic Function Generator 1. The output of the Logic Function Generator 1 is connected to both the input of the Output Driver and Test Latch 2 and a sensing circuit (not shown). Many structures of sensing circuitry are known in the art and are therefore not mentioned here. The sensing circuit must be able to pass a logic value from the sense signal 4 to an external pin of the integrated circuit device. The output 5 of the Output Driver and Test Latch 2 may be connected to any number of inputs of other logic cells by way of routing tracks 6.

Output Driver and Test Latch 2 has a plurality of additional test inputs which are dedicated to the purpose of testing the device. These test inputs include the Row Test bits 8 and the Column Test bits 7. These groups of test bits are driven along the rows and columns formed by the logic cells 100. Which group is chosen to drive the rows, and which the columns, is arbitrary. In the configuration shown, each Column Test bit 7 is applied to all the logic cells 100 in a column, and the Row Test bits 8 (each one common to all logic cells 100 in a row) are applied to the rows.

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As shown in Table 1, in the example embodiment of Fig. 2 there are two Row Test bits 8, here named Test Strobes STR0 and STR1, which define three modes of operation: Normal, Latch Open (where a new test condition is entered by allowing a new Test Data value to be incorporated), and Latch
5 Closed (where the test condition is frozen).

One embodiment for Output Driver and Test Latch 2 is shown in Fig. 2. Here, in Fig. 2, the test storage element is implemented with a latch made from a 3-to-1 Mux 10. This Test Latch then feeds the logic cell's Output Driver 11. It is important to note that, by combining in the same Mux 10, the
10 test circuit which selects normal or test data as well as the Test Latch, fewer transistors will be necessary to implement the imbedded test function while any extra delay for logic signals passing through the Test Latch during normal operation is minimized.

Of course, other types of circuitry may be used for the test storage
15 element which is here, in Fig. 2, implemented by a Test Latch. In addition to edge-triggered devices such as flip-flops, it is also acceptable to use dynamic storage elements where stored information may be lost after some time period has passed. Dynamic storage elements are acceptable when the number of nets which must be driven to test one particular logic cell is relatively small.
20 Here, the test cycle time is relatively small compared with the retention time of the dynamic storage elements.

One alternative embodiment is shown in Figure 3. Here, a test command is applied to all of the logic cells 100 in a row via row Test bits 8 (here named Test Data bits CMD0 and CMD1) and subsequently, Column
25 Test 7, or Test Strobes, are applied to those logic cells 100 where it is

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desired that the test command take effect. This allows some logic cells in a row to be placed in a test condition (e.g., drive a high or low test value), while other logic cells in the same row are left in a normal condition where the output of Logic Function Generator 1 is passed to the Output Driver 11.

5 To accomplish this, 2-to-1 Mux 14 stores whether the logic cell 100 will be placed in a normal or test condition. The output of Mux 14 controls another Mux 15 which selects either the output of the Logic Function Generator 1 or the output of Mux 17, which stores a test value (a high or low value).

The embodiment shown in Fig. 3 provides a more flexible

10 implementation than that of Fig. 2 in that a first logic cell can pass through the logic value generated by its Logic Function Generator to some driven logic cell. Meanwhile, other logic cells provide test values to control both the first logic cell and any driven logic cells. This logic value from the first logic cell can then be passed through to the output of the Logic Function Generator

15 1 of the driven logic cell where it is observed by a sensing circuit. In this way, the path from logic cell inputs 3 to the outputs 5 of Output Driver and Test Latch 2 can be tested. This is important since, during the testing of a single logic cell, the output logic value is available at the Sense signal 4 before it is applied to output selection Mux 15.

20 Even though imbedded test circuitry for a logic cell based array is not specifically shown with tri-state output circuits to implement the outputs of the Output Driver and Test Latch circuits, such a configuration is easily tested by the embodiment of Fig. 3, as a logic cell output which controls a particular tri-state output can also be forced to any desired logic value in the same

25 manner. To verify that an output with tri-state capability of a logic cell under test has entered a high impedance condition, it is necessary to provide a pull-

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up resistor through which the output 5 of the Output Driver and Test Latch can connect to a known logic value so that the output 5 will be pulled to that known value when placed in a high impedance condition.

5 While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modification as fall within the true spirit and scope of this invention.

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What is claimed is:

1. An integrated circuit, comprising:
a prefabricated array of logic cells, couplable to form an arbitrary circuit, wherein a plurality of logic cells in said array each includes:
 - 5 a cell output;
 - a logic function generator;
 - a test circuit, operably coupled to said cell output and to said logic function generator, said test circuit operable in a first mode of operation to pass a test logic value to said cell output and operable in a
10 second mode of operation to pass a generated logic value from said logic function generator to said cell output, said test circuit included in each of said plurality of logic cells in said prefabricated array of logic cells prior to coupling said prefabricated array of logic cells to form said arbitrary circuit and regardless of the arbitrary circuit to be
15 ultimately formed by coupling said prefabricated array of logic cells.
2. The integrated circuit of claim 1, wherein the test circuit in some logic cells in said array of logic cells is operable in said first mode of operation while simultaneously the test circuit in other logic cells in said array of logic cells is operable in said second mode of operation.
- 20 3. The integrated circuit of claim 1, wherein each logic cell in said array further includes a sense output, coupled to said logic function generator, to carry said generated logic value.
4. The integrated circuit of claim 3, wherein said sense output carries said generated logic value when said test circuit is operating in said first mode of

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operation and when the test circuit is operating in said second mode of operation.

5. The integrated circuit of claim 1, wherein said first mode of operation includes holding said test logic value on said cell output.

5 6. The integrated circuit of claim 1, wherein each of said plurality of logic cells in said array further includes:

a first test input coupled to said test circuit; and

a second test input coupled to said test circuit.

7. The integrated circuit of claim 6, wherein the mode of operation of
10 said test circuit is determined by at least one of a signal carried on said first test input and a signal carried on said second test input.

8. The integrated circuit of claim 7, wherein said first test input is a row test input and said second test input is a column test input.

9. The integrated circuit of claim 1, wherein, when said logic cells are
15 coupled to form said arbitrary circuit, the logic function generator in some of said logic cells in said array of logic cells implements a synchronous function while the logic function generator in other of said logic cells in said array of logic cells implements an asynchronous function.

10. The integrated circuit of claim 1, wherein said test circuit includes a
20 multiplexor.

11. The integrated circuit of claim 10, wherein said test circuit includes a

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plurality of multiplexors.

12. The integrated circuit of claim 11, wherein at least two of said plurality of multiplexors are each configured to be operable as a latch.

13. The integrated circuit of claim 10, wherein said test circuit includes
5 only said multiplexor.

14. The integrated circuit of claim 13, wherein said multiplexor is configured to be operable as a latch.

15. The integrated circuit of claim 1, wherein said test circuit includes a storage unit.

10 16. The integrated circuit of claim 15, wherein said storage unit includes a latch.

17. The integrated circuit of claim 16, wherein said test circuit includes only said latch.

18. The integrated circuit of claim 15, wherein said storage unit includes a
15 dynamic storage element.

19. The integrated circuit of claim 1, wherein said cell output in each of said plurality of logic cells is coupled to a driver.

20. The integrated circuit of claim 1, wherein:
said cell output is a tri-state output; and

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said logic cell further includes a pull-up resistor coupled to said cell output.

21. An integrated circuit, comprising:

5 a prefabricated array of logic cells, couplable to form any one of a plurality of circuits, wherein a plurality of logic cells in said array each includes:

a first test input;

a second test input;

a cell output circuit having a cell output;

10 a logic function generator having a generator output for carrying a generated logic value;

a test circuit, coupled to said cell output circuit, coupled to said generator output, and coupled to said first test input and said second test input, said test circuit operable in a first mode of operation to pass a test logic value to said cell output and operable in a second mode of operation to pass said generated logic value to said cell output, wherein the mode of operation of said test circuit is determined by at least one of a signal carried on said first test input and a signal carried on said second test input, said test circuit included in each of said plurality of logic cells regardless of the function to be performed by said logic function generator when said prefabricated array of logic cells is coupled to form one of said plurality of circuits; and

15

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wherein the test circuits in some logic cells in said array of logic cells are operable in said first mode of operation while simultaneously the test circuits in other logic cells in said array of logic cells are operable in said second mode of operation.

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22. The integrated circuit of claim 21, wherein each logic cell in said plurality of logic cells includes a sense output, coupled to said generator output, to carry said generated logic value.

5 23. The integrated circuit of claim 21, wherein said first mode of operation includes holding said test logic value on said cell output.

24. The integrated circuit of claim 21, wherein each logic cell in said plurality of logic cells further includes a third test input coupled to said test circuit, wherein said first test input is for carrying said test logic value, and said second test input and said third test input are for carrying signals to select
10 said mode of operation of said test circuit.

25. The integrated circuit of claim 21, wherein, when said prefabricated array of logic cells is coupled to form one of said plurality of circuits, the logic function generator in some of said logic cells in said array of logic cells implements a synchronous function while the logic function generator in other
15 of said logic cells in said array of logic cells implements an asynchronous function.

26. The integrated circuit of claim 21, wherein said first input is a column test input and said second input is a row test input.

27. The integrated circuit of claim 21, wherein said test circuit includes a
20 storage unit.

28. The integrated circuit of claim 27, wherein said storage unit includes a multiplexor.

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29. The integrated circuit of claim 28, wherein said multiplexor is configured to be operable as a latch.

30. An integrated circuit, comprising:

5 a prefabricated array of logic cells, couplable to form any one of a plurality of circuits, wherein, regardless of which one of said plurality of circuits said array of logic cells is ultimately coupled to form, each logic cell in said array includes:

- a row test input;
- a column test input;
- 10 a cell output circuit having a cell output;
- a logic function generator having a generator output for carrying a generated logic value;
- a test circuit, including a one-bit test storage unit having an input and an output, said one-bit test storage unit input coupled to said
- 15 generator output, said one-bit test storage unit output coupled to said cell output circuit, and said one-bit test storage unit coupled to said row test input and to said column test input, said one-bit test storage unit operable in a first mode of operation to pass said test logic value to said cell output and hold said test logic value on said cell output,
- 20 and said one-bit test storage unit operable in a second mode of operation to pass said generated logic value to said cell output, wherein the mode of operation of said one-bit test storage unit is determined by at least one of a signal carried on said row test input and a signal carried on said column test input;
- 25 wherein the one-bit test storage unit in some logic cells in said array of logic cells are operable in said first mode of operation while simultaneously the one-bit test storage unit in other logic cells in said array of logic cells are

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operable in said second mode of operation.

31. The integrated circuit of claim 30, wherein each logic cell in said array further includes a sense output coupled to said generator output, to carry said generated logic value.

5 32. The integrated circuit of claim 30, wherein each logic cell further includes a second row test input coupled to said test circuit for carrying a second row test signal, and wherein said mode of operation is determined by said row test signal and said second row test signal.

10 33. The integrated circuit of claim 32, wherein said test circuit includes one and only one one-bit storage unit.

34. The integrated circuit of claim 33, wherein said one-bit test storage unit includes a multiplexor configured to be operable as a latch, wherein:
a first input of said multiplexor is coupled to said generator output;
a second input of said multiplexor is coupled to receive said test logic
15 value;
a third input of said multiplexor is coupled to the output of said multiplexor;
a first select input of said multiplexor is coupled to said row test input;
and
20 a second select input of said multiplexor is coupled to said second row test input.

35. A method of manufacturing an integrated circuit, comprising the sequential steps of:

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forming an array of logic cells, wherein each logic cell has a cell output, a logic function generator, and a test circuit operably coupled to said logic function generator and said cell output and operable in a first mode of operation to pass a test logic value to said cell output and operable in a second
5 mode of operation to pass a generated logic value from said logic function generator to said cell output; and

forming any one of a plurality of circuits by coupling some of said logic cells in said array of logic cells to other logic cells in said array of logic cells.

10 36. The method of claim 35, wherein said step of forming an array of logic cells includes forming the test circuit in each logic cell such that the test circuits in some of said array of logic cells are operable in said first mode of operation while simultaneously the test circuits in other logic cells in said array of logic cells are operable in said second mode of operation.

15 37. The method of claim 35, wherein said step of forming an array of logic cells includes forming in each logic cell a sense output, coupled to said generator output, to carry said generated logic value.

38. The method of claim 35, wherein said step of forming an array of logic cells includes forming said array of logic cells wherein each logic cell
20 further includes a first input and a second input, both said first input and said second input coupled to said test circuit.

39. The method of claim 38, wherein said step of forming an array of logic cells includes forming said array of logic cells wherein each logic cell further includes a third input coupled to said test circuit, wherein said first

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input is for carrying said test logic value, and said second input and said third input are for carrying signals to select said mode of operation of said test circuit.

5 40. The method of claim 39, wherein said first input is a column test input and said second input and said third input are formed as row test inputs.

41. The method of claim 35, wherein, after said step of forming any one of a plurality of circuits, the logic function generator in some of said logic cells in said array of logic cells implements a synchronous function while the logic function generator in other of said logic cells in said array of logic cells
10 implements an asynchronous function.

42. The method of claim 35, wherein said step of forming said array of logic cells includes forming said test circuit to include a storage unit.

43. The method of claim 42, wherein said storage unit includes a multiplexor.

15 44. The method of claim 43, wherein said multiplexor is configured to be operable as a latch.

45. A method of testing an integrated circuit having an array of logic cells, said array of logic cells coupled to form any one of a plurality of circuits, wherein each logic cell in said array includes a first input, a second input, a cell output, a logic function generator, and a test circuit operably coupled to
20 said logic function generator, said cell output, said first input, and said second input, comprising the steps of:

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applying a first mode selection signal to said first input of a first logic cell in said array of logic cells to select a test mode of operation for said test circuit in said first logic cell;

applying a test value to said second input of said first logic cell;

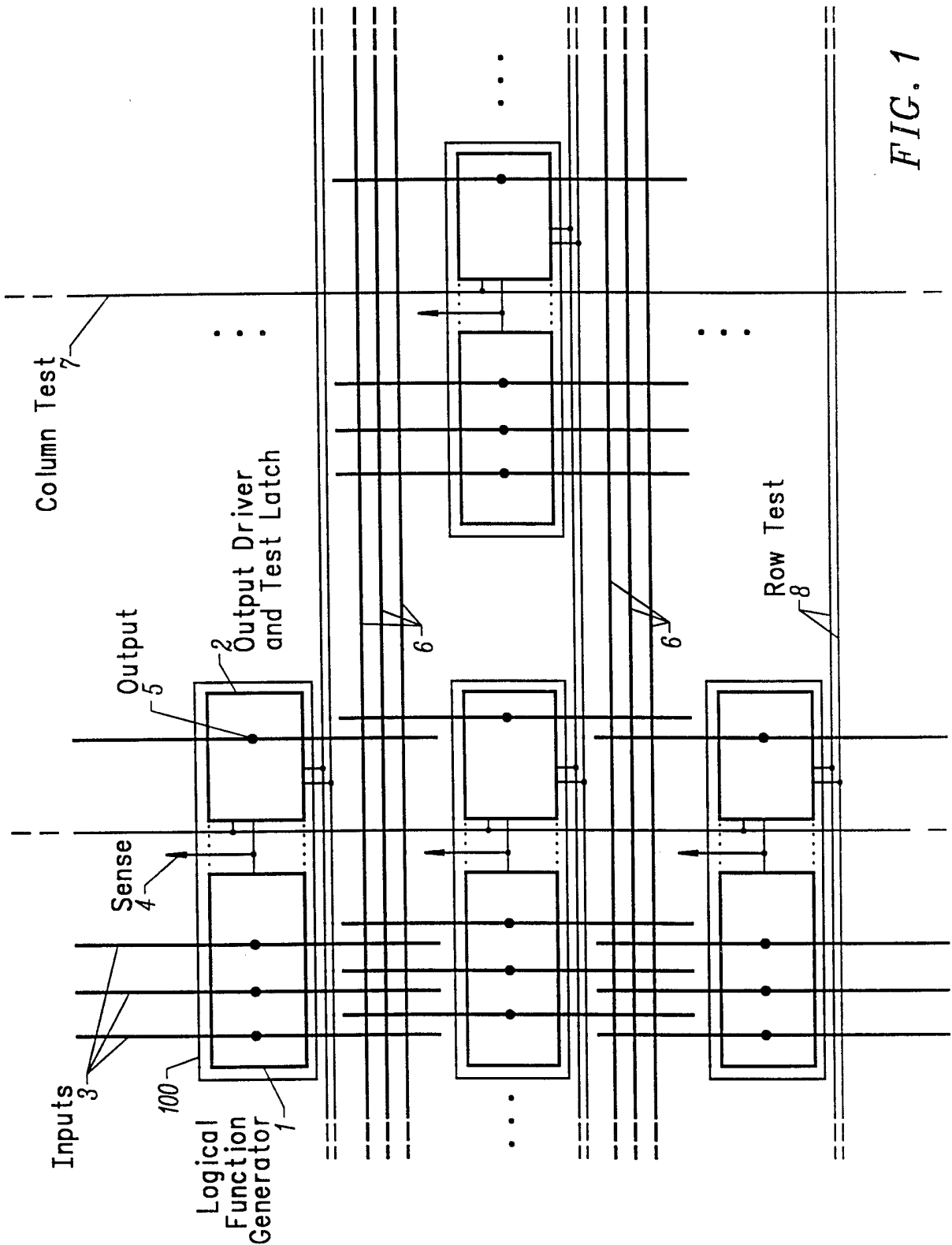
5 passing, by said test circuit of said first logic cell, said test value to said cell output of said first logic cell;

holding, by said test circuit of said first logic cell, said test value on said cell output of said first logic cell;

10 applying, while said first logic cell is in said test mode of operation, a second mode selection signal to said first input of a second logic cell to select a pass-through mode of operation for said test circuit of said second logic cell to pass a generated logic value from said logic function generator of said second logic cell to said cell output of said second logic cell.

15 46. The method of claim 45, wherein said step of applying a test value to said second input of said first logic cell precedes said step of applying a first selection signal to said first input of said first logic cell.

20 47. The method of claim 45, further including the step of
 applying a third selection signal to said first input of said first logic cell to select a pass-through mode of operation for said test circuit of said first logic cell to pass said generated logic value of said first logic cell to said cell output of said first logic cell.



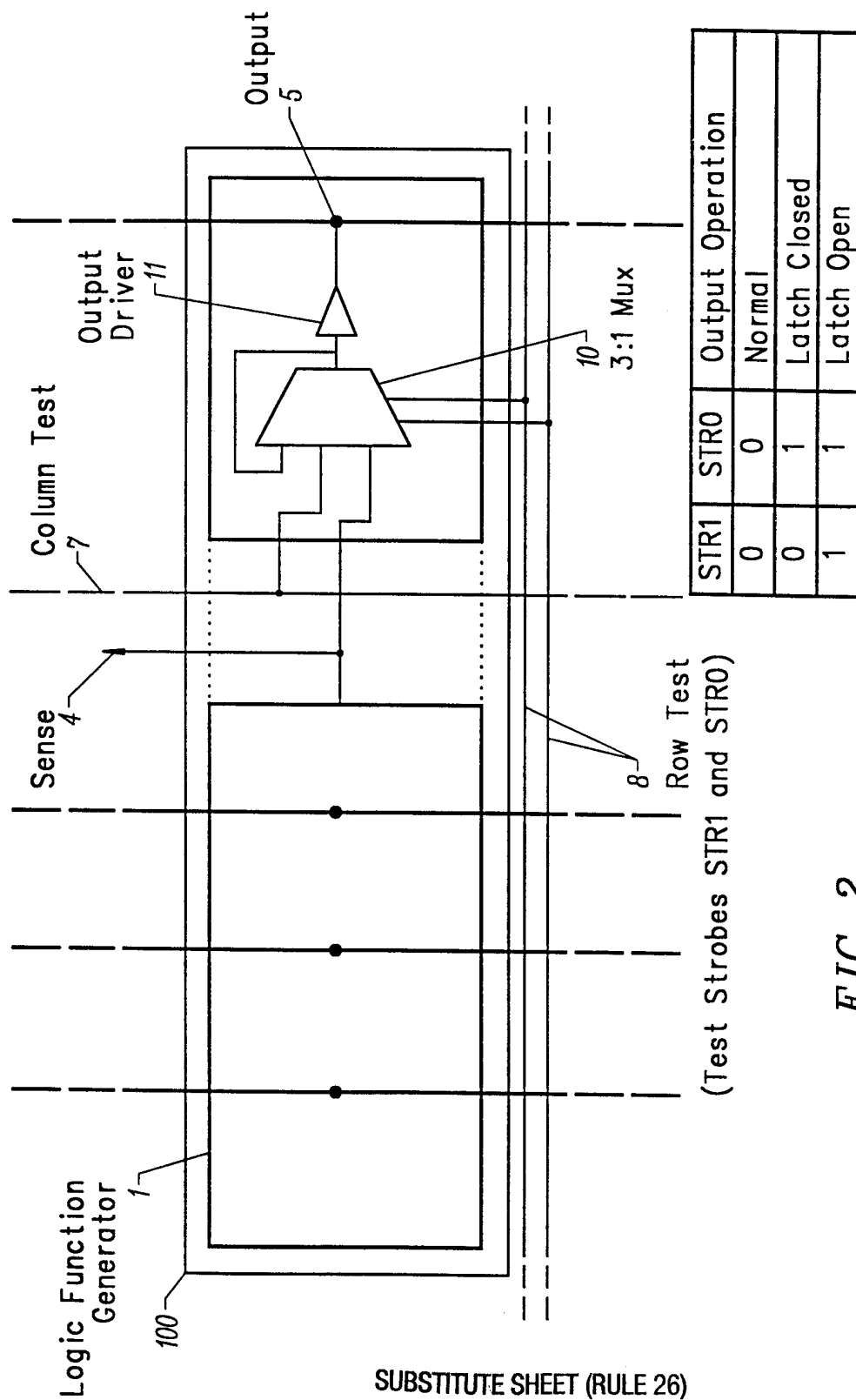


FIG. 2

Table 1. Interpretation of test Strobes STR1 and STR0

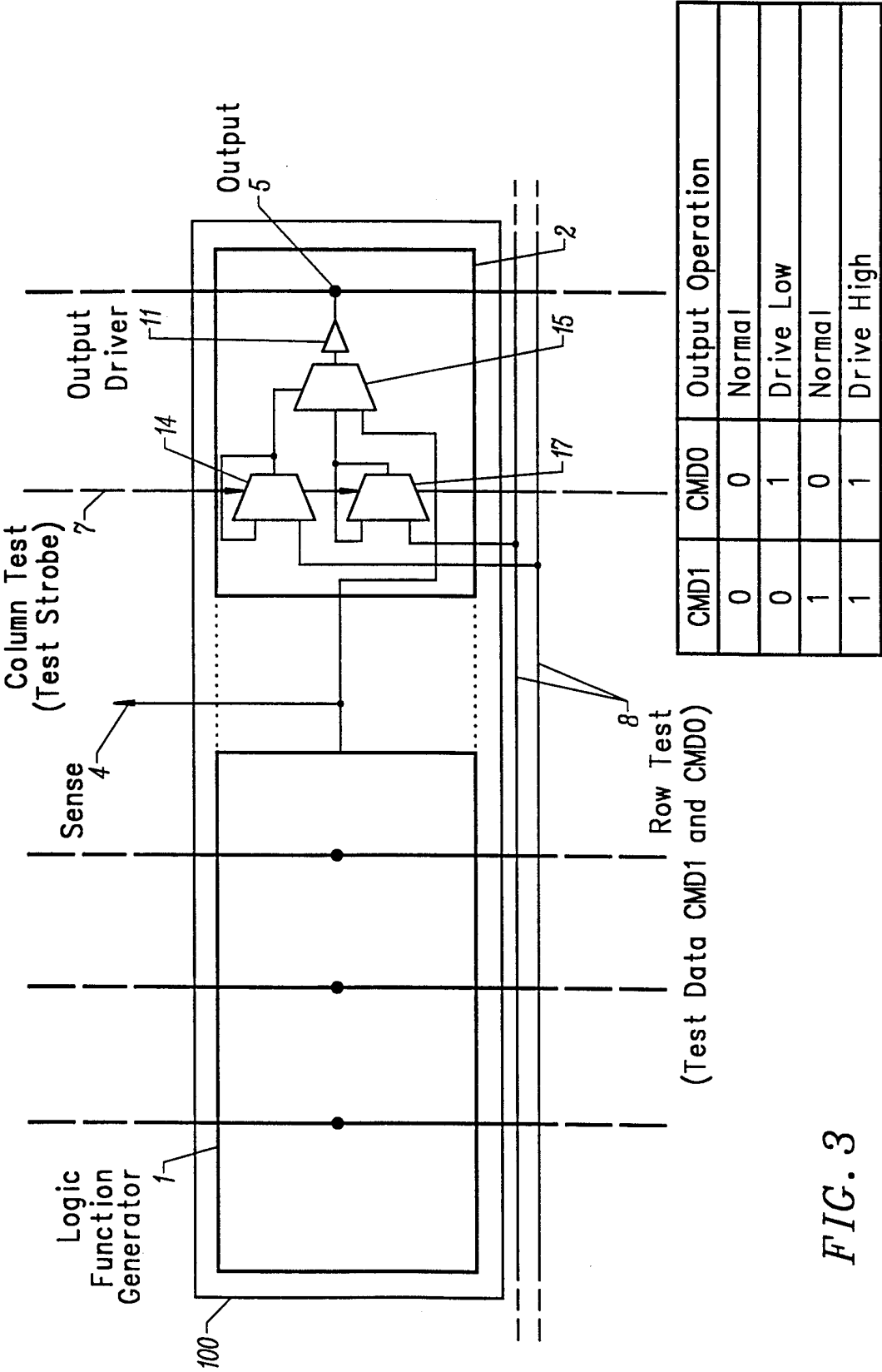


FIG. 3

Table 2. Interpretation of Test Data CMD1 and CMD0

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 98/06567

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 G06F11/267

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 528 600 A (EL AYAT KHALED ET AL) 18 June 1996	1,2, 5-11,15, 16,19, 21, 23-27, 30,35, 36, 38-42, 45-47
A	see column 8, line 55 - column 9, line 30; figure 4A	3,4, 12-14, 17,18, 20,22, 28,29, 31-34, 37,43,44
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 98/06567

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
A	<p>FRAKE S O ET AL: "A SCAN-TESTABLE MASK PROGRAMMABLE GATE ARRAY FOR CONVERSION OF FPGA DESIGNS"</p> <p>PROCEEDINGS OF THE CUSTOM INTEGRATED CIRCUITS CONFERENCE, BOSTON, MAY 3 - 6, 1992,</p> <p>no. CONF. 14, 3 May 1992, pages 27.3.1-27.3.4, XP000340969</p> <p>INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS</p> <p>see page 27.3.3, left-hand column, line 40 - page 27.3.4, right-hand column, line 8; figure 1</p> <p style="text-align: center;">----</p>	1-47
A	<p>JP 06 109816 A (HITACHI LTD) 22 April 1994 & US 5 809 039 A (TAKAHASHI ET AL.)</p> <p>15 September 1998</p> <p>see abstract</p> <p style="text-align: center;">-----</p>	1-47

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5528600 A	18-06-1996	US 5614818 A	25-03-1997
		US 5804960 A	08-09-1998
JP 06109816 A	22-04-1994	US 5809039 A	15-09-1998