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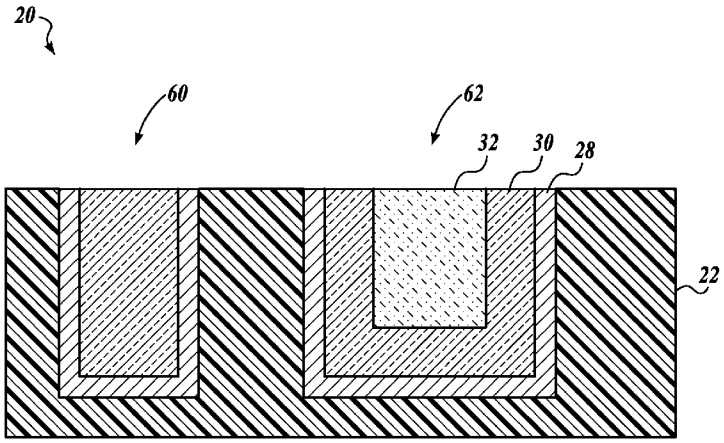

FIG. 1F

(57) Abstract: In one embodiment of the present disclosure, a method for depositing metal in a feature on a workpiece is provided. The method includes electrochemically depositing a second metal layer on a first metal layer on a workpiece having at least two features of two different sizes in a dielectric layer, wherein the second metal layer is a copper layer and wherein the first metal layer includes a metal selected from the group consisting of cobalt and nickel, wherein the first metal layer completely fills the smallest feature but does not completely fill the largest feature.

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CO OR NI AND CU INTEGRATION FOR SMALL AND LARGE FEATURES IN INTEGRATED CIRCUITS

BACKGROUND

Integrated circuits (IC) include various semiconductor devices formed within or on layers of dielectric material that overlay a substrate. The devices formed in or on the dielectric layers may include MRS transistors, bipolar transistors, diodes, and diffused resistors. Other devices formed in or on the dielectric material may include thin film resistors and capacitors. Metal lines interconnect the semiconductor devices to power the devices and enable the devices to share and exchange information. Interconnects may extend horizontally between devices within a dielectric layer as well as vertically between dielectric layers. These metal lines are connected to each other by a series of interconnects. The electrical interconnects or metal lines are first patterned into the dielectric layers to form vertical and horizontal recessed features (vias and trenches) that are subsequently filled with metal. The resulting layer containing metal-filled lines residing in a dielectric is referred to as a metallization layer.

A long-standing objective in the advancement of IC technology has been the scaling down of IC dimensions. Scaling-down of IC dimensions is critical to obtaining higher speed performance of ICs. An increase in IC performance is normally accompanied by a decrease in device area and/or an increase in device density. An increase in device density results in a decrease in via and trench dimensions (widths) used to form interconnects. However, as feature dimensions on wafers decrease, negative consequences may occur. For example, reduced-size features may result in less reliable interconnects.

Copper interconnects are typically used in ICs. However, drawbacks of copper interconnects in small features include performance as a result of, for example, voids formed during deposition, electromigration tendencies of copper, line resistance, and via resistance. Therefore, there exists a need for the integration of copper and non-copper interconnects, the metal for a feature being selected depending on the size of the feature. Embodiments of the present disclosure are directed to an integration scheme for Cu and other metal interconnects to solve these and other problems.

SUMMARY

This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This summary is not intended to identify key features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

In accordance with one embodiment of the present disclosure, a method for depositing metal in a feature on a workpiece is provided. The method includes electrochemically depositing a second metal layer on a first metal layer on a workpiece having at least two features of two different sizes in a dielectric layer, wherein the second metal layer is a copper layer and wherein the first metal layer includes a metal selected from the group consisting of cobalt and nickel, wherein the first metal layer completely fills the smallest feature but does not completely fill the largest feature.

In accordance with another embodiment of the present disclosure, a microfeature workpiece includes a dielectric having at least two features, wherein the critical dimension of the first feature is less than or equal to 17 nm and is filled with cobalt or nickel, and wherein the critical dimension of the second feature is greater than 20 nm and is filled with a stack layer of cobalt or nickel and copper.

In any of the embodiments described herein, the first feature may have a critical dimension of less than or equal to 17 nm.

In any of the embodiments described herein, the second feature may have a critical dimension of greater than 20 nm.

In any of the embodiments described herein, a method may further include heat treating the workpiece after deposition of the second metal layer.

In any of the embodiments described herein, the temperature for heat treating the workpiece may be in the temperature range of 150 degrees C to 400 degrees C.

In any of the embodiments described herein, heat treating the workpiece may anneal the first and second metal layers.

In any of the embodiments described herein, heat treating the workpiece may reflow the second metal layer to at least partially fill the largest feature.

In any of the embodiments described herein, a method may further include plasma treating the first metal layer using hydrogen plasma or hydrogen radicals (H*) prior to electrochemically depositing the second metal layer.

In any of the embodiments described herein, a method may further include heat treating the first metal layer before depositing the second metal layer.

In any of the embodiments described herein, heat treating the first metal layer may be in the temperature range of 200 degrees C to 400 degrees C.

In any of the embodiments described herein, the second metal layer may be a conformal, superconformal, or bottom-up fill layer.

In any of the embodiments described herein, the second metal layer may include an overburden.

In any of the embodiments described herein, the second metal layer may at least partially fill the largest feature without depositing an overburden on the workpiece.

In any of the embodiments described herein, a method may further include electrochemically depositing a third metal layer on the second metal layer.

In any of the embodiments described herein, the third metal layer may be an overburden, a cap, a fill layer, a conformal conductive layer, or a superconformal conductive layer.

In any of the embodiments described herein, a method may further include CMP.

In any of the embodiments described herein, a method may further include heat treating the workpiece after CMP.

In any of the embodiments described herein, the first metal layer may be a first seed layer.

In any of the embodiments described herein, the first seed layer may be deposited by a process selected from the group consisting of physical vapor deposition, chemical vapor deposition, atomic layer deposition, and electro-less deposition.

In any of the embodiments described herein, a method may further include a second seed layer on the first seed layer prior to deposition of the second metal layer.

In any of the embodiments described herein, the second seed layer may be different in metal composition from the first seed layer.

In any of the embodiments described herein, the second seed layer may be a copper seed layer.

In any of the embodiments described herein, the second seed layer may be deposited by a process selected from the group consisting of physical vapor deposition, chemical vapor deposition, atomic layer deposition, and electro-less deposition.

In any of the embodiments described herein, the workpiece may include an adhesion or barrier layer deposited in the feature prior to deposition of the seed layer.

In any of the embodiments described herein, the second metal layer may be deposited over the entire surface of the seed layer.

wherein the workpiece includes an adhesion or barrier layer deposited in the features prior to deposition of the cobalt or nickel layer.

DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this disclosure will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURES 1A-1F are a series of schematic illustrations of a method of forming a interconnects in accordance with one embodiment of the present disclosure;

FIGURES 2A-2C are a series of schematic illustrations of a method of forming a interconnects in accordance with another embodiment of the present disclosure;

FIGURES 3A-3D are a series of schematic illustrations of a method of forming a interconnects in accordance with another embodiment of the present disclosure;

FIGURES 4 and 5 are flow diagrams depicting exemplary processes in accordance with embodiments of the present disclosure;

FIGURE 6 is an SEM image showing fill of small features with cobalt and large features with copper, in accordance with one embodiment of the present disclosure;

FIGURE 7 is a three-dimensional schematic illustration depicting an exemplary workpiece in accordance with one embodiment of the present disclosure;

FIGURES 8A-8C are a series of schematic illustrations of a method of removing oxides and/or other contaminants from a seed layer in accordance with embodiments of the present disclosure;

FIGURE 9 schematically illustrates a hydrogen ion plasma chamber for use with methods in accordance with embodiments of the present disclosure; and

FIGURE 10 schematically illustrates an electrochemical deposition plating tool for use with methods in accordance with another embodiment of the present disclosure.

DETAILED DESCRIPTION

The present disclosure relates to methods and integration for hybrid non-copper (such as cobalt and nickel) and copper metallization layers in some larger features (such

as trenches, particularly in Damascene applications) of a microelectronic workpiece and non-copper metallization layers in other smaller features (such as vias, particularly in Damascene applications) of a microelectronic workpiece.

In one exemplary embodiment, one small feature on a workpiece having a critical dimension of less than or equal to 17 nm is filled with cobalt or nickel metallization, and another feature on a workpiece having a critical dimension of greater than 20 nm is filled with a hybrid of cobalt or nickel and copper metallization. In another exemplary embodiment, one small feature on a workpiece having a critical dimension of less than or equal to 15 nm is filled with cobalt or nickel metallization, and another feature on a workpiece having a critical dimension of greater than 20 nm is filled with a hybrid of cobalt or nickel and copper metallization.

Embodiments of the present disclosure are directed to workpieces, such as semiconductor wafers, devices or processing assemblies for processing workpieces, and methods of processing the same. The terms "workpiece," "wafer," and "semiconductor wafer" means any flat media or article, including semiconductor wafers and other substrates or wafers, glass, mask, and optical or memory media, MEMS substrates, or any other workpiece having micro-electric, micro-mechanical, or microelectro-mechanical devices.

Methods described herein are to be used for metal or metal alloy deposition in features of workpieces, including trenches and vias. In one embodiment of the present disclosure, the process may be used in "small" features, for example, features having a feature critical dimension of less than 20 nm. The dimension sizes discussed in the present application may be post-etching feature dimensions at the top opening of the feature. In one embodiment of the present disclosure, small Damascene features may have a minimum dimension size of less than or equal to 17 nm. In another embodiment, small Damascene features may have a minimum dimension size of less than or equal to 15 nm.

In other embodiments, "large" Damascene features as described in the present disclosure may have a minimum dimension size of greater than 20 nm.

The processes described herein may be applied to various forms of cobalt, nickel, copper, and alloys, for example, in Damascene applications.

The descriptive terms "micro-feature workpiece" and "workpiece" as used herein may include all structures and layers previously deposited and formed at a given point in

the processing, and is not limited to just those structures and layers as depicted in the figures. For example, larger features may be present on the workpieces in accordance with standard semiconductor procedure and manufacture.

Although generally described as metal deposition in the present application, the term "metal" also contemplates metal alloys and co-deposited metals. Such metals, metal alloys, and co-deposited metals may be used to form seed layers or to fully or partially fill the feature. As a non-limiting example in co-deposited metals and metal alloys, the alloy composition ratio may be in the range of about 0.5% to about 6% secondary alloy metal.

With reference to FIGURES 1A-1F, an integration scheme for filling one or more features using cobalt and copper to form exemplary interconnects will now be described. As a non-limiting example, the series of layers in a workpiece 20 typically include a dielectric layer 22 (see FIGURE 1A), an optional adhesion layer 28 (see FIGURE 1B), a first metal layer 30, for example a seed layer (see FIGURE 1C), and a second metal layer 32, for example, a conformal electrochemically deposited metallization layer (see FIGURE 1D).

The integration scheme is illustrated for two features of two different sizes in the dielectric layer 22, shown as a first small feature 60 and a second larger feature 62 (see FIGURE 1A). Although only illustrated as including two features, a workpiece having any number of features is within the scope of the present disclosure, so long as there is at least one small feature 60 and at least one large feature 62.

Referring to FIGURE 1B, an optional adhesion (or barrier) layer 28 on the dielectric material may include, for example, titanium (Ti), tantalum (Ta), titanium nitride (TiN), tantalum nitride (TaN), etc. As a non-limiting example, the adhesion layer may be a TiN layer formed by a CVD or an ALD process. In some applications, an adhesion layer may not be needed.

Referring to FIGURE 1C, the first metal layer 30 is a seed layer deposited on the adhesion layer 28, or directly on the dielectric layer 22 if there is no adhesion layer. In accordance with embodiments of the present disclosure, the seed layer is, for example, formed from Co or Ni by a CVD process. Although commonly formed by a CVD process, the seed layer may also be formed by using other deposition techniques, such as ALD, PVD, or electro-less deposition. The first metal layer 30 may also be a stack film including a seed layer and a liner layer (not shown).

In the illustrated embodiment, the first metal layer 30 fills the smaller feature 60, but does not fill the larger feature 62. As can be seen in FIGURE 1C, the thickness of the first metal layer 30 may be equal to or greater than the ½ opening after deposition of the barrier or liner layer 28 in the small feature 60 on the workpiece 20. In the illustrated embodiment, a seam 64 is formed in the small feature 60 where the two sides of the conformal first metal layer 30 come together. The first metal layer 30 may have a film thickness of half the width of the feature 60 to fill an opening having that critical dimension, for example, in the range of about 5 nm to about 50 nm.

In another embodiment of the present disclosure, the first metal layer 30 may be thin enough to leave all features open and not filling even the small feature 60 on the workpiece. In another embodiment of the present disclosure, the first metal layer 30 may fill all the features (large and small) on the workpiece.

In the illustrated embodiment of FIGURES 1A-1F, the first metal layer 30 is not annealed immediately following deposition. However, in other embodiments, the first metal layer 30 may be optionally annealed following deposition, as described in greater detail below. Such annealing may be advantageous for healing the seam 64 (see FIGURE 1C), sealing micro-voids, stabilizing the film, densifying the film, lowering the resistivity of the film, and promoting crystal growth.

In some cases, annealing of a first metal layer 30 may be at a suitable temperature to cause a reflow of the first metal layer 30. In other cases, the anneal may be performed at a lower temperature without reflowing the first metal layer 30.

In some cases, the first metal layer 30 may be annealed to lower sheet resistance prior to ECD deposition of the second metal layer 32.

After annealing, the thickness of the first metal layer 30 may be reduced, for example, in the range of about 2 nm to about 35 nm.

Annealing conditions for the first metal layer 30 may be in a temperature range of 200 C to 400 C, and a pressure between 1 mTorr and 1 atm. In addition, a vacuum anneal is also within the scope of the present disclosure. The annealing environment may be hydrogen, a hydrogen/helium mix (e.g., 4% hydrogen, 96% helium), or a hydrogen/nitrogen mix (e.g., 4% hydrogen, 96% nitrogen).

After deposition (and optional anneal) of the first metal layer 30, a second metal layer 32 is electrochemically deposited, as seen in FIGURE 1D. In one embodiment of

the present disclosure, the second metal layer 32 is an ECD Cu layer. The ECD Cu layer may have a film thickness in the range of about 50 nm and about 500 nm.

Thin seed layers or seed layers made from metals other than copper tend to have high sheet resistance, which can lead to overheating of the workpiece where electrical connection is made during the electrochemical deposition process. Therefore, the second metal layer 32, for example, an ECD Cu layer, may be plated using contacts immersed in the plating solution and thus, the second metal layer 32 is deposited on a first metal layer 30 (or seed layer) over the entire surface of the workpiece...

In the illustrated embodiment of FIGURE 1D, the second metal layer 32 is a conformal layer. However, the ECD second metal layer 32 may be a conformal layer, a super-conformal layer, or a bottom-up fill layer, for example, deposited using conventional acid chemistry.

In one non-limiting example, the second metal layer 32 is an ECD Cu layer is deposited using an alkaline chemistry including a very dilute copper ethylenediamine (EDA) complex. ECD copper may also be deposited using other copper complexes, such as citrate, tartrate, glycine, ethylenediaminetetraacetic acid (EDTA), urea, etc., and may be deposited in a pH range of about 2 to about 11, about 3 to about 10, about 4 to about 10, or in a pH range of about 6 to about 10. In one embodiment of the present disclosure, the ECD copper alkaline chemistry may have a mildly acidic, neutral, or alkaline pH, for example in the range of about 6.5 to 9.3. In addition, the copper electrolyte includes a source of copper ions, such as copper chloride or copper sulfate, and may include a complexing agent, such as glycine or EDA.

In another non-limiting example, the electrolyte may include one or more components, such as organic additives and/or complexing agents, and a pH range of about 6 to about 13 to achieve super-conformal fill.

Conventional ECD copper acid chemistry may include, for example, copper sulfate, sulfuric acid, methane sulfonic acid, hydrochloric acid, and organic additives (such as accelerators, suppressors, and levelers). ECD deposition provides a substantially bottom up (e.g., nonconformal) metal fill. Acid chemistry may dissolve some of the cobalt seed layer (up to 40 Angstroms). Therefore, the use of conventional ECD copper acid chemistry includes consideration of the potential dissolution.

In some exemplary embodiments of the present disclosure, deposition current density for ECD can range from 1 mA/cm^2 to 6 mA/cm^2 for dilute chemistry or from

1 mA/cm2 to 30 mA/cm2 for more concentrated chemistry. The waveform for applied current during deposition can be either direct current or pulsed current. Temperature during ECD can range between 15 to 40 degrees Celsius.

As seen in comparing FIGURE 1D with FIGURE 1E, the workpiece 20 may be optionally heat treated or annealed after deposition of the second metal layer 32. As mentioned above, annealing can provide one or more of the advantageous effects of healing the seam 64 of the first metal layer 30 in the small feature 60, sealing micro-voids, stabilizing the film, densifying the film, lowering the resistivity of the film, and promoting crystal growth.

As a not limiting example, resistivity for a cobalt seed layer as a first metal layer 30 may be in the range of about 8 to about 12 μΩ·cm post anneal. In contrast, the bulk resistivity for a copper layer as the second metal layer 32 may be about 25% of cobalt resistivity. However, in narrow features, copper resistivity may exceed the resistivity of cobalt. Annealing may help to reduce the resistivity of the first and/or second layers 30 and 32. In some cases, annealing may cause a reflow of the first and/or second metal layers 30 and 32, for example, as seen in the larger feature 62 of FIGURE 1E. Reflow of the second metal layer 32 may cause partial or full fill of the larger feature 62.

Annealing conditions for the workpiece 20 after deposition of the second metal layer 32 may be in a temperature range of 150 C to 400 C, and a pressure between 1 mTorr and 1 atm. In addition, a vacuum anneal is also within the scope of the present disclosure. The annealing environment may be hydrogen, a hydrogen/helium mix (e.g., 4% hydrogen, 96% helium), or a hydrogen/nitrogen mix (e.g., 4% hydrogen, 96% nitrogen). The time for the annealing process may be in the range of about 1 to about 60 minutes.

If the line is wide, cobalt and nickel are not effective metal conductors because of resistance. Instead, a copper conductor is needed to carry the current in the wide line. If the line or the via is narrow and short, for example, having a width of less than or equal to 17 nm and a length of less than 3 microns, cobalt or nickel will be an effective, low resistance metal conductor. Therefore, the inventors have found features having a critical dimension of less than 17 nm or narrower have better performance if the conductor is made of Co or Ni, and not Cu. Still yet, features wider than 20 nm perform better if the

conductor is made of Cu. Therefore, embodiments of the present disclosure are directed to an integration scheme for Co and/or Ni and Cu features on a single workpiece.

In the illustrated embodiment of FIGURES 1A-1F, the ECD Cu process completely fills all features (small and large) leaving an overburden on the field. Therefore, the post plating anneal process in FIGURE 1E anneals the overburden metal in addition to the metal filling the feature, which may promote crystal growth, stabilize and lower the resistivity of the films, and seal any remaining microvoids and seams.

In accordance with embodiments of the present disclosure, an ECD electrolyte for conformal or super-conformal fill or a conventional acidic ECD electrolyte for bottom up can be used for either full or partial fill of some of the features, or overburden deposition, or both, in one or two deposition steps or more, as needed. For example, a third metal layer (not shown), may be deposited to fill the large feature 62 or to deposit an overburden on the workpiece.

As a non-limiting example, the thickness of the ECD Cu metallization layer in an exemplary first metallization step may be in the range of about 10 nm to about 50 nm. Further as a non-limiting example, the thickness of the ECD Cu metallization layer in an exemplary second metallization and/or overburden step may be in the range of about 100 nm to about 500 nm.

Referring to FIGURE 1F, the workpiece is then subjected to a chemical-mechanical planarization (CMP) process to fabricate the device.

In accordance with embodiments of the present disclosure, the processes described herein may include a post-CMP anneal to promote crystal growth, to stabilize and lower the resistivity of the films, and to seal any remaining microvoids and seams.

In one exemplary embodiment of FIGURES 1A-1F, the small feature is completely filled with CVD cobalt or nickel and the larger feature includes a CVD cobalt or nickel seed, but is filled with ECD copper. Referring to an exemplary process in the EXAMPLE below, an SEM image in FIGURE 6 showing several features of different sizes on a workpiece, cobalt or nickel fills the smaller features (e.g., less than or equal to 17 nm) and a cobalt/nickel and copper stack fills the larger features (e.g., greater than 20 nm).

Referring to FIGURE 4, an exemplary process in accordance with one embodiment of the present disclosure includes obtaining a workpiece having a small feature (critical dimension less than or equal to 17 nm) and a large feature (critical

dimension greater than 20 nm). The process includes optionally depositing an adhesion layer in the features. The process includes depositing a Co or Ni layer in the features, wherein the Co or Ni layer completely fills the small feature but does not fill the large feature. The process includes optionally annealing the Co or Ni layer. The process includes electrochemically depositing Cu on the Co or Ni layer, and optionally annealing the workpiece after ECD deposition. After the large feature has been filled, the process includes CMP.

In another exemplary process in accordance with one embodiment of the present disclosure, the process includes electrochemically depositing a second metal layer (Cu) on a first metal layer (Co or Ni) on a workpiece having at least two features of two different sizes in a dielectric layer, wherein the first metal layer completely fills the smallest feature but does not completely fill the largest feature.

One advantageous effect of a workpiece including hybrid Co or Ni and Cu metallization is reduced resistance of Co/Ni interconnects as compared to Cu interconnects in smaller features, which results in improved IC performance. The hybrid use of Co or Ni and Cu metallization also provides a means for extending the use of Cu metallization as IC dimensions continue to scale down.

Another advantageous effect is a Co/Ni and Cu stack in the larger features may mitigate the expected high resistance in large and long lines that are filled with only Co or Ni metal.

Another advantageous effect is the use of a Co/Ni and Cu stack may reduce via resistance, an advantage for high speed devices. Moreover, cobalt can use a thinner liner layer than copper, thus reducing the thickness of a TaN liner (or cladding) in the vias and trenches. Referring to an exemplary workpiece 120 in FIGURE 6, an integration of CVD Co in narrow lines 150 and ECD Cu in wide lines 152 is illustrated.

Referring to alternate method in accordance with embodiments of the present disclosure in FIGURES 2A-2C, the larger feature is filled with bottom-up copper metallization 42 (see FIGURE 2A), instead of conformal fill as illustrated in FIGURE 1D. Bottom-up fill may be achieved with conventional ECD fill and cap techniques in the feature, for example, using an acid deposition chemistry. Conventional ECD copper acid chemistry may include, for example, copper sulfate, sulfuric acid, methane sulfonic acid, hydrochloric acid, and organic additives (such as accelerators, suppressors, and levelers). Electrochemical deposition of copper has been found to be the

most cost effective manner by which to deposit a copper metallization layer. In addition to being economically viable, ECD deposition techniques provide a substantially bottom up (e.g., nonconformal) metal fill that is mechanically and electrically suitable for interconnect structures.

Referring to FIGURE 2B, the workpiece 20 may be annealed in accordance with methods described above. Such annealing may heal seam 64. With bottom-up or super-conformal fill, annealing of the second metallization layer 42 at temperatures for reflow of the layer 42 to partially or fully fill the second larger feature 62 may not be needed.

Referring to FIGURE 2C, the workpiece 20 is subjected to a chemical-mechanical planarization (CMP) process to fabricate the device.

Referring to FIGURES 3A-3C another alternate method in accordance with embodiments of the present disclosure is provided. Referring to FIGURE 3A, a copper seed layer 52 is deposited on a cobalt or nickel seed layer 30. The copper seed layer may be deposited by a process selected from the group consisting of physical vapor deposition, chemical vapor deposition, atomic layer deposition, and electro-less deposition

Referring to FIGURE 3B, the larger feature 62 is filled with bottom-up copper metallization 54. However, in accordance with other embodiments of the present disclosure, the larger feature 62 may be fully or partially filled with conformal or superconformal copper metallization by an electrochemical deposition process.

Referring to FIGURE 3C, the workpiece 20 may be annealed in accordance with methods described above. Such annealing may heal seam 64 and meld the first copper seed layer 52 and the second copper metallization layer 54 into one copper layer 56.

Referring to FIGURE 3D, the workpiece 22 is then subjected to a chemical-mechanical planarization (CMP) process to fabricate the device.

Referring to FIGURE 3A-3C and the flow diagram of FIGURE 5, an exemplary process in accordance with one embodiment of the present disclosure includes obtaining a workpiece having a small feature (critical dimension less than or equal to 17 nm) and a large feature (critical dimension greater than 20 nm). The process includes optionally depositing an adhesion layer in the features. The process includes depositing a Co or Ni seed layer in the features, wherein the Co or Ni layer completely fills the small feature but does not fill the large feature. The process includes depositing a Cu seed layer on the Co or Ni seed layer. The process includes optionally annealing the seed layers. The

process includes electrochemically depositing Cu on the Cu seed layer, and optionally annealing the workpiece after ECD deposition. After the large feature has been filled, the process includes CMP.

In another exemplary process in accordance with one embodiment of the present disclosure, the process includes electrochemically depositing on second metal layer (Cu) on a seed layer stack of a first seed layer (Co or Ni) and a second seed layer (Cu) on a workpiece having at least two features of two different sizes in a dielectric layer, wherein the first seed layer completely fills the smallest feature but does not completely fill the largest feature.

Referring to FIGURE 7, a three-dimensional schematic of a workpiece 120 in accordance with embodiments of the present disclosure is illustrated. The workpiece 100 includes a substrate 122. A second metal layer 132 (Cu) is deposited on a first metal layer 130 (Co or Ni) on a workpiece having at least two features of two different sizes in a dielectric layer, wherein the first seed layer completely fills the smallest feature 160 but does not completely fill the largest feature 162.

EXAMPLE

Two wafers were obtained. On the wafer 30Å of PVD TaN and 100 Å of CVD Co were deposited. The wafers were annealed at 400°C for 5 minutes. The wafers were transferred to a nitrogen-purged FOUP to mitigate oxidation of the Co layer. The wafers plated using ECD Cu Seed chemistry at a pH of 9.3. A two-step plating process was used at 2 Amin and annealed at 250°C for 1 minute. FIGURE 4 is flow diagram for the process described in this example. An SEM cross-section in FIGURE 6 shows Co fill of the small features and Co/Cu stack in the large features.

TREATMENT WITH HYDROGEN PLASMA

Seed layers have a tendency to oxidize, and such oxidation may degrade subsequent metal deposition on the seed layer. In addition, an oxidized surface tends to increase defects and may degrade the reliability of the interconnect. A high temperature anneal of the seed layer in a reducing atmosphere tends to reduce such oxides. The oxides can be further reduced prior to metal deposition, for example, by plasma treatment either before, or during, or after the high-temperature anneal. In accordance with embodiments of the present disclosure, anneal and plasma treatment steps may be

performed in different chambers or in the same chamber, either simultaneously or in sequence.

In accordance with embodiments of the present disclosure, surface treatment can be achieved using a low temperature surface treatment method so as to maintain the integrity and continuity of the deposited seed layer and minimize damage to the seed layer. Referring to FIGURES 8A-8C, in one embodiment of the present disclosure, the seed layer 30 is treated with hydrogen radicals H*. The hydrogen radicals H* is used to reduce metal oxides back to metal and covert the oxides to water. The hydrogen radical H* can also be used to clean contaminants from the seed layer surface, such as carbon.

In accordance with embodiments of the present disclosure, the hydrogen radicals H* may be generated using a plasma chamber, using a hot-filament radical source, or a combination of both. The hydrogen radicals H* can be used to uniformly reduce oxides 40 and clean the seed layer surface 30 in the feature.

Advantageous effects of hydrogen radical H* surface treatment in accordance with embodiments of the present disclosure include reduced agglomeration of the conductor layers and/or reduced changes to the intrinsic properties of the seed layer were typically caused by high temperature treatments in previously developed processes. Another advantageous effect of surface treatment includes enhances nucleation of the plated conductor as a result of the surface treatment to reduce oxygen and other contaminants.

After surface treatment by hydrogen radicals H*, a short processing window between surface treatment and electrochemical deposition, re-oxidation of the seed layer surface 30 is significantly reduced. Accordingly, in some embodiments of the present disclosure, the time range between seed layer surface treatment and metallization layer deposition is less than 60 seconds. In other embodiments, the time range may be less than 30 seconds. In some embodiments, re-oxidation of the seed layer may be mitigated by storing the workpiece in a nitrogen environment (or another inert environment) before plasma surface treatment, after plasma surface treatment, or during other intervals in workpiece processing.

In some embodiments of the present disclosure, a wet process is used to reduce the oxide layer and further clean the surface of the seed, prior to plating. The wet process typically takes place in the plating bath, between wafer immersion in the bath and the initiation of plating. The wet process may be used with or without the plasma treatment

described above. In some embodiments the wet clean process is performed without the preceding plasma treatment, and in those embodiments all oxides and surface contaminants are removed during the wet process. In other embodiments, a plasma treatment precedes the wet clean. In other non-limiting embodiments only plasma treatment is used and plating commences during immersion or immediately afterwards.

In comparison, a typical plating window after a seed deposition process is in the range of about 6-24 hours, generally considered by the industry to be an acceptable time period for plating metal on a seed layer. Moreover, cobalt seed layer surface treatment in accordance with the processing methods described herein may have the effect of improving adhesion, reducing defects, improving interconnect reliability, and other properties for subsequent cobalt metallization layers.

Referring to FIGURE 9, an exemplary a hydrogen ion plasma chamber for use with methods in accordance with embodiments of the present disclosure is shown.

To achieve the short processing window, advances have been made to the plating tool. Referring to FIGURE 10 an exemplary plating tool for use with methods described herein in shown, commonly known as the MUSTANG® tool manufactured by APPLIED Materials, Inc. The tool of FIGURE 10 includes modules or subsystems within an enclosure 322. Wafer or substrate containers 324, such as FOUP (front opening unified pod) containers, may be docked at a load/unload station 326 at the front of the enclosure 322. The subsystems used may vary with the specific manufacturing processes performed by the system 320. In the illustrated embodiment, the system 320 includes a front interface 328 which may provide temporary storage for wafers to be moved into or out of the system 320, as well as optionally providing other functions. As non-limiting examples, the system 320 may include an anneal module 330, a hydrogen radical H* generation chamber, a rinse/dry module 332, a ring module 340, and electroplating chambers 342, which may be sequentially arranged within the enclosure 322 behind the front interface 328. Robots move the wafers between the subsystems.

In some embodiments of the present disclosure, the tool may have an ambient air environment between chambers. In other embodiments, the tool may have a nitrogen environment in the enclosure between chambers to mitigate oxidation of the seed layer before plasma surface treatment, after plasma surface treatment, or during other intervals in workpiece processing.

In some embodiments of the present disclosure, the tool may include separate annealing and hydrogen radical H* generation chambers. In other embodiments of the present disclosure, the hydrogen radical H* generation may occur in the same chamber as is used for an annealing process. Although the same chamber may be used for both processes, the processes will occur separately in the workpiece manufacturing process, and not at the same time. To accommodate both processes, the chamber will have both hydrogen radical H* generation capabilities and annealing capabilities. In one embodiment, the chamber accommodates a temperature range from room temperature to 300°C or room temperature to 400°C.

The combination of hydrogen radical H* generation and annealing in one processing chamber reduces that manufacturing site foot print of the tool and provides for annealing at high temperature and high vacuum, which may prove to be of benefit to the seed layer.

The metal options of the seed and metallization layers are described above. Embodiments of the present disclosure include, for example, a cobalt or nickel seed layer and a copper metallization layer.

While illustrative embodiments have been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the disclosure.

CLAIMS

The embodiments of the disclosure in which an exclusive property or privilege is claimed are defined as follows:

1. A method for depositing metal in a feature on a workpiece, the method comprising:

electrochemically depositing a second metal layer on a first metal layer on a workpiece having at least two features of two different sizes in a dielectric layer, wherein the second metal layer is a copper layer and wherein the first metal layer includes a metal selected from the group consisting of cobalt and nickel, wherein the first metal layer completely fills the smallest feature but does not completely fill the largest feature.

2. The method of Claim 1, wherein the first feature has a critical dimension of less than or equal to 17 nm.

3. The method of Claim 1, wherein the second feature has a critical dimension of greater than 20 nm.

4. The method of Claim 1, further comprising heat treating the workpiece after deposition of the second metal layer.

5. The method of Claim 4, wherein the temperature for heat treating the workpiece is in the temperature range of 150 degrees C to 400 degrees C.

6. The method of Claim 4, wherein heat treating the workpiece anneals the first and second metal layers.

7. The method of Claim 4, wherein heat treating the workpiece reflows the second metal layer to at least partially fill the largest feature.

8. The method of Claim 4, further comprising plasma treating the first metal layer using hydrogen plasma or hydrogen radicals (H*) prior to electrochemically depositing the second metal layer.

9. The method of Claim 1, further comprising heat treating the first metal layer before depositing the second metal layer.

10. The method of Claim 9, wherein heat treating the first metal layer is in the temperature range of 200 degrees C to 400 degrees C.

11. The method of Claim 1, wherein the second metal layer is a conformal, superconformal, or bottom-up fill layer.

12. The method of Claim 1, wherein the second metal layer includes an overburden.

13. The method of Claim 1, wherein the second metal layer at least partially fills the largest feature without depositing an overburden on the workpiece.

14. The method of Claim 1, further comprising electrochemically depositing a third metal layer on the second metal layer.

15. The method of Claim 14, wherein the third metal layer is an overburden, a cap, a fill layer, a conformal conductive layer, or a superconformal conductive layer.

16. The method of Claim 1, further comprising CMP.

17. The method of Claim 16, further comprising heat treating the workpiece after CMP.

18. The method of Claim 1, wherein the first metal layer is a first seed layer.

19. The method of Claim 18, wherein the first seed layer is deposited by a process selected from the group consisting of physical vapor deposition, chemical vapor deposition, atomic layer deposition, and electro-less deposition.

20. The method of Claim 18, further comprising a second seed layer on the first seed layer prior to deposition of the second metal layer.

21. The method of Claim 20, wherein the second seed layer is different in metal composition from the first seed layer.

22. The method of Claim 20, wherein the second seed layer is a copper seed layer.

23. The method of Claim 20, wherein the second seed layer is deposited by a process selected from the group consisting of physical vapor deposition, chemical vapor deposition, atomic layer deposition, and electro-less deposition.

24. The method of Claim 1, wherein the workpiece includes an adhesion or barrier layer deposited in the feature prior to deposition of the seed layer.

25. The method of Claim 1, wherein the second metal layer is deposited over the entire surface of the seed layer.

26. A microfeature workpiece, comprising:

a dielectric having at least two features, wherein the critical dimension of the first feature is less than or equal to 17 nm and is filled with cobalt or nickel, and wherein the critical dimension of the second feature is greater than 20 nm and is filled with a stack layer of cobalt or nickel and copper.

27. The workpiece of Claim 26, wherein the workpiece includes an adhesion or barrier layer deposited in the features prior to deposition of the cobalt or nickel layer.

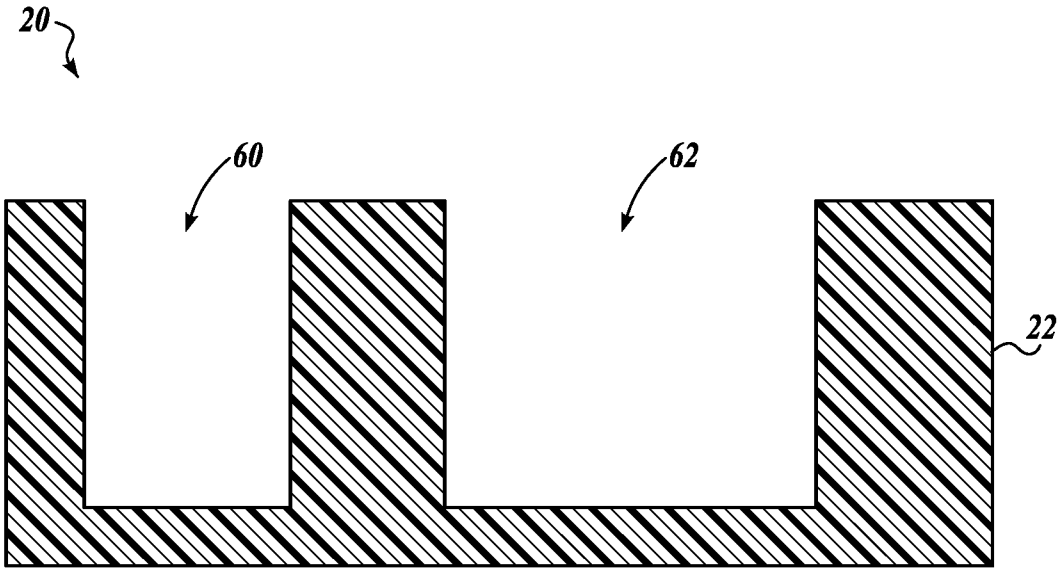

FIG. 1A

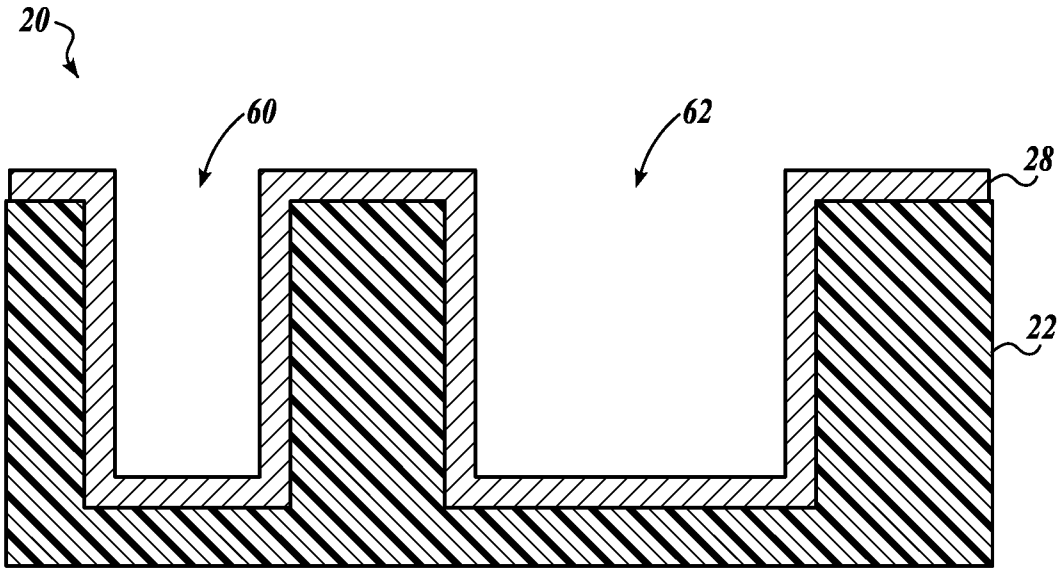

FIG. 1B

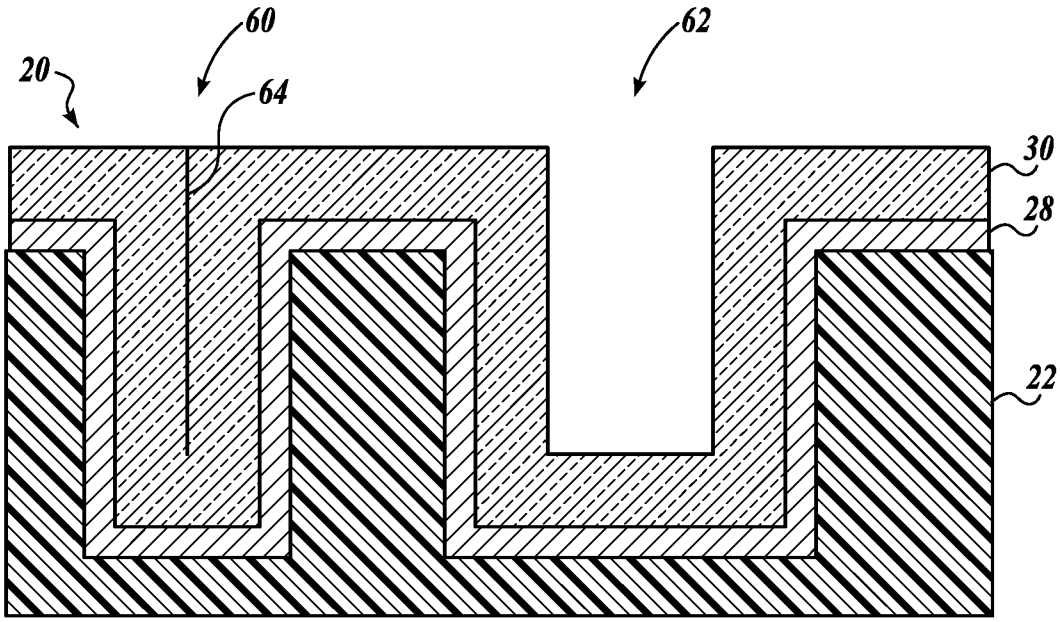

FIG. 1C

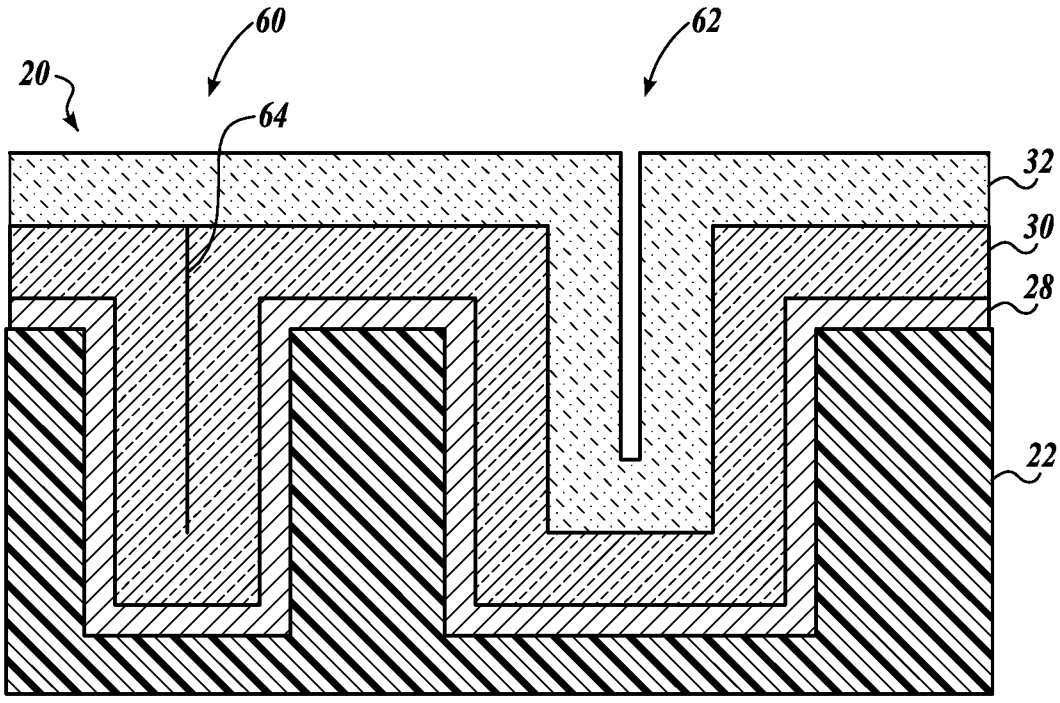

FIG. 1D

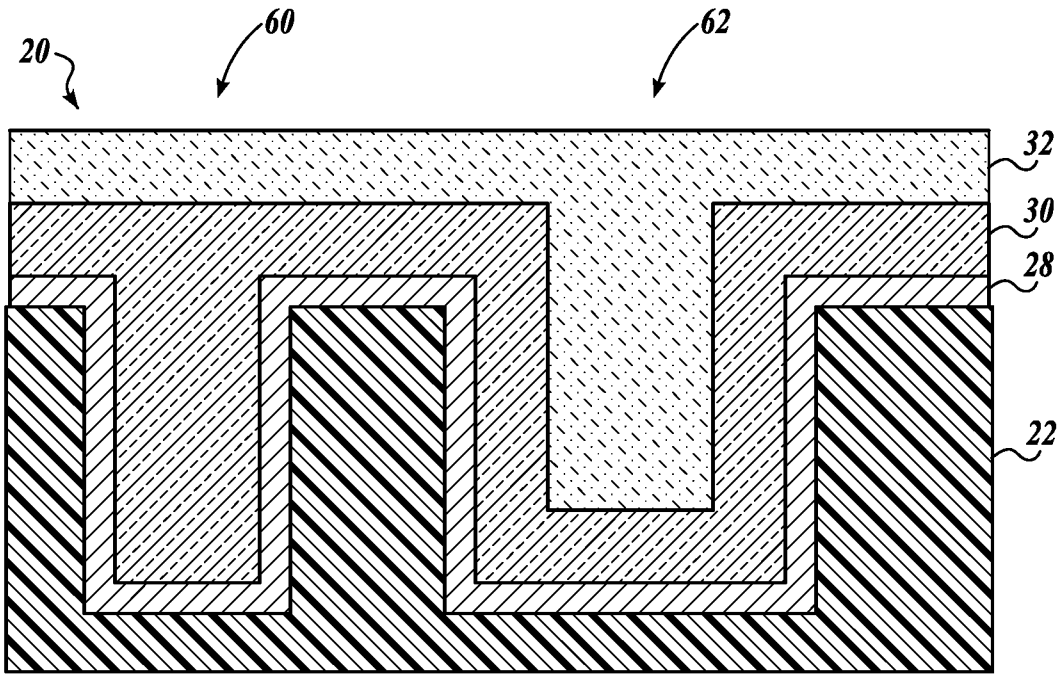

FIG. 1E

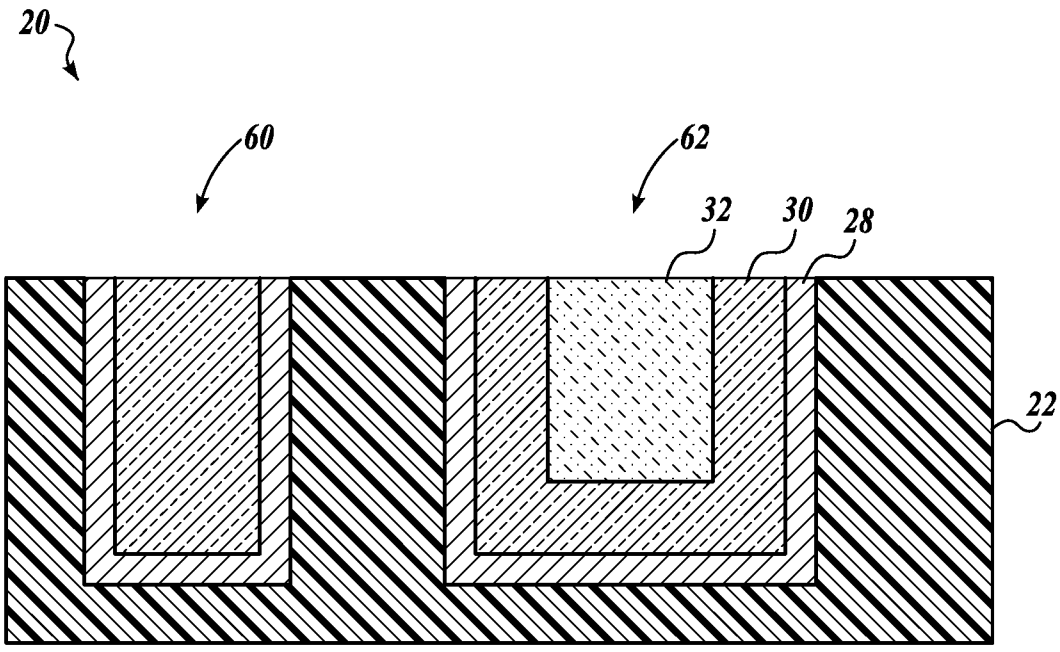

FIG. 1F

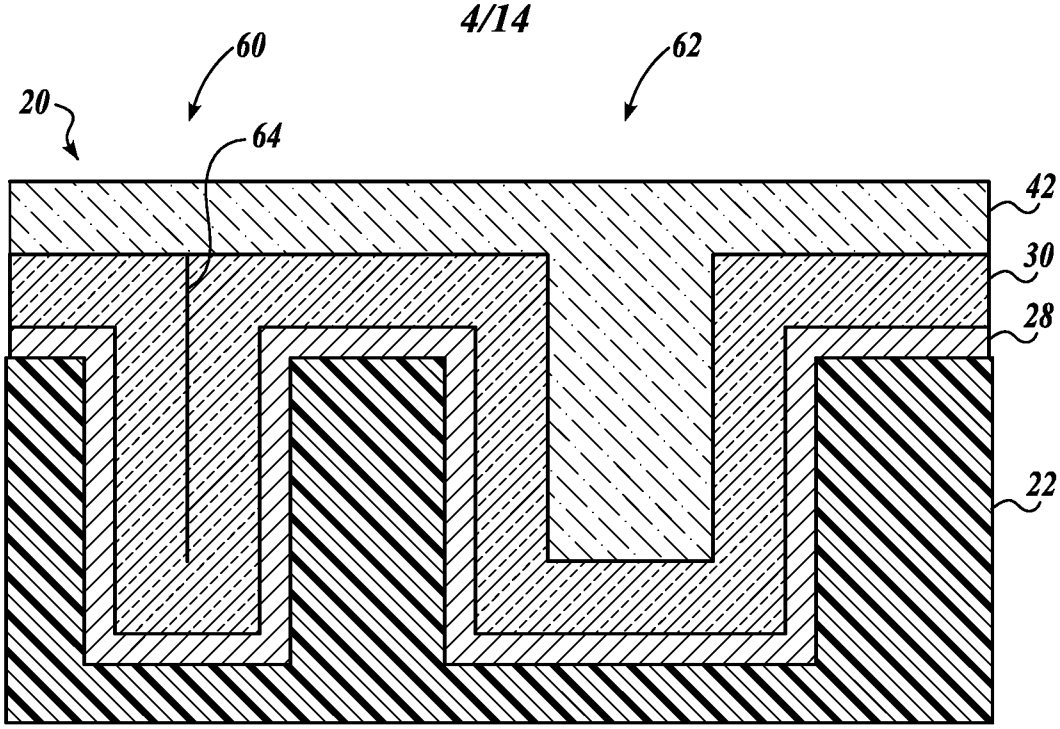

FIG. 2A

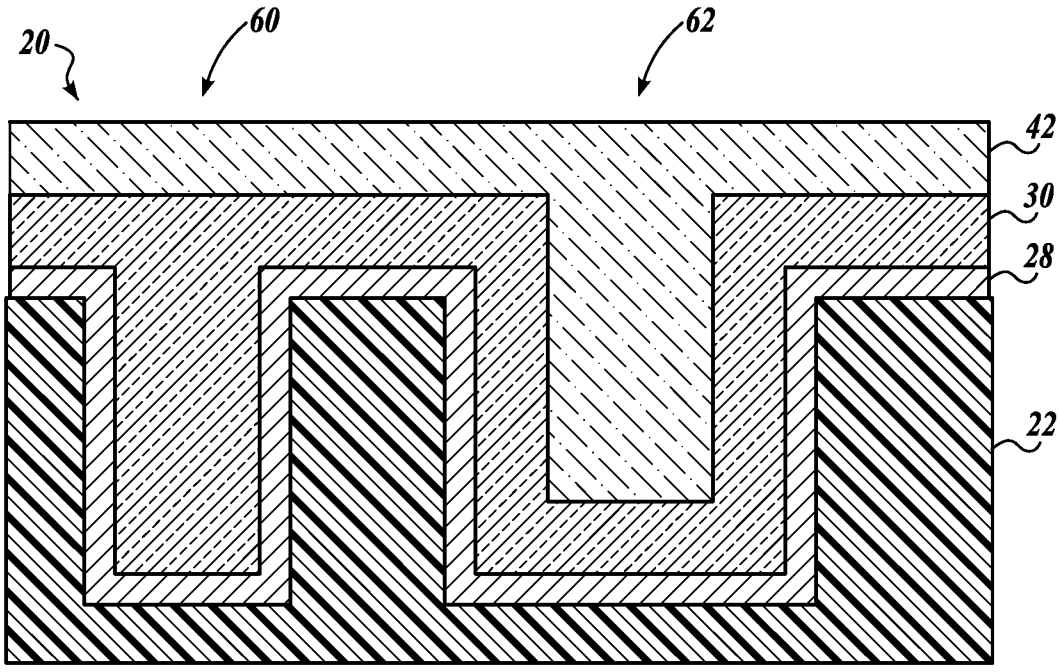

FIG. 2B

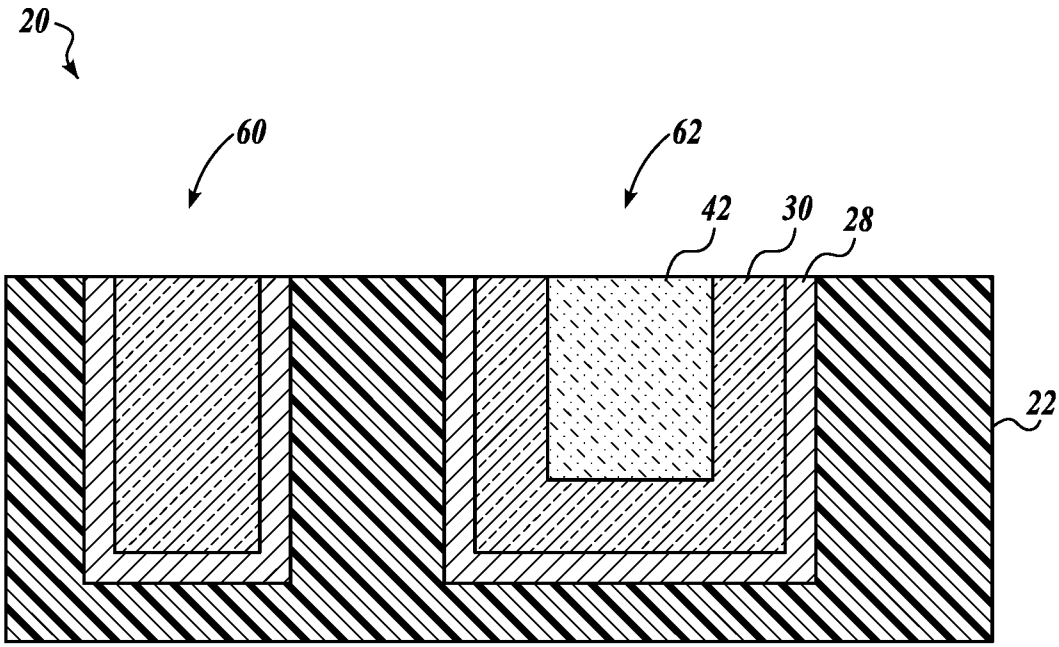

FIG. 2C

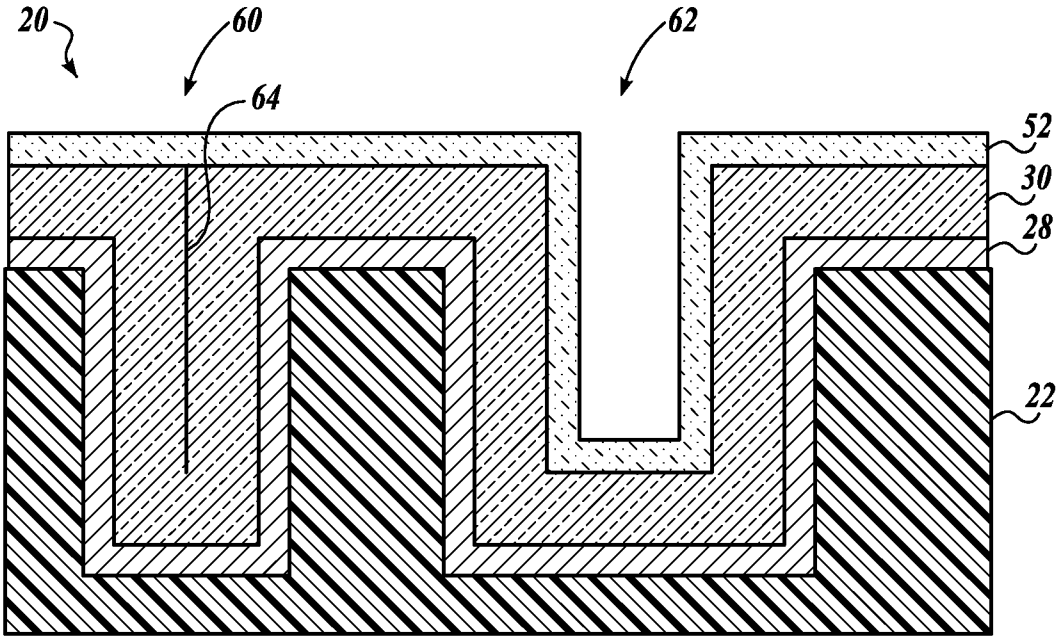

FIG. 3A

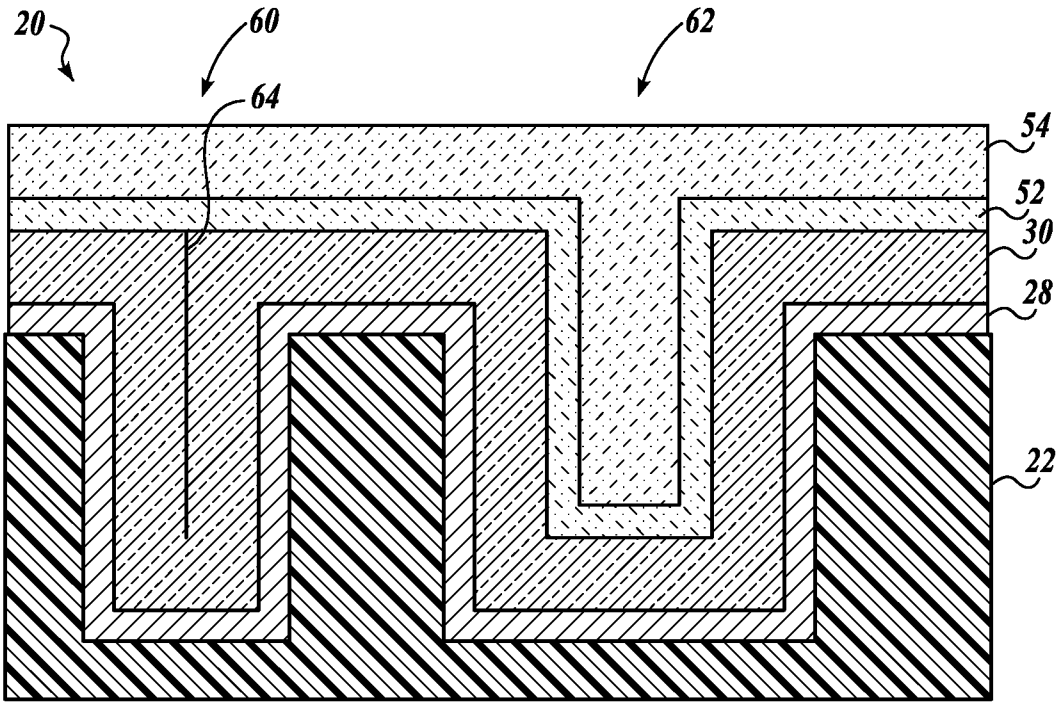

FIG. 3B

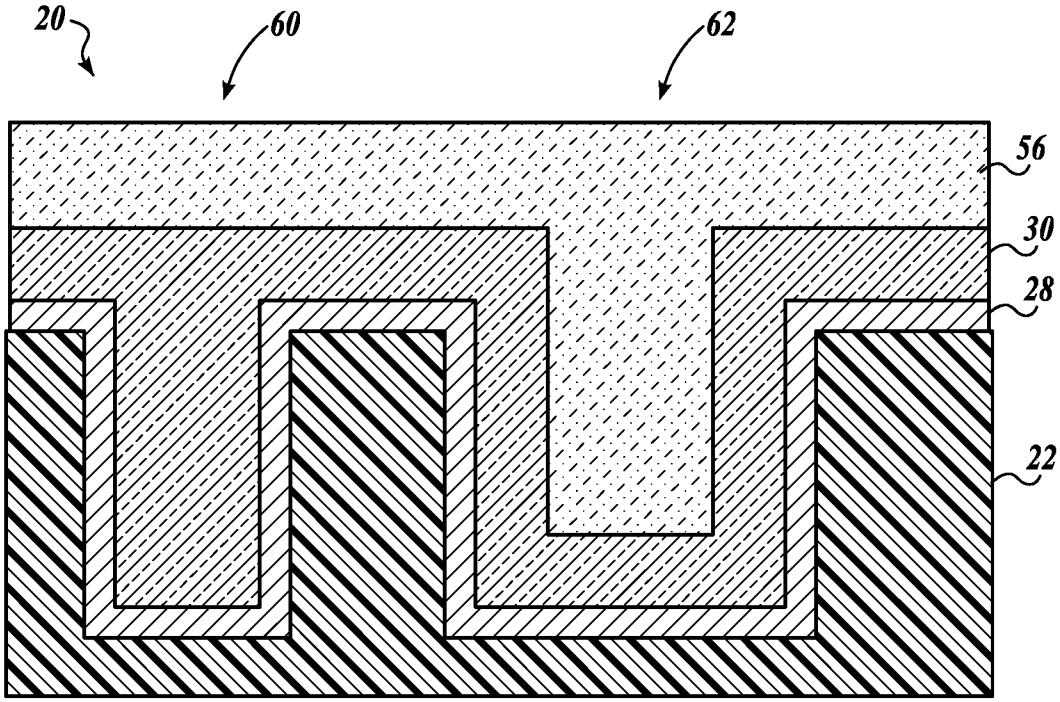

FIG. 3C

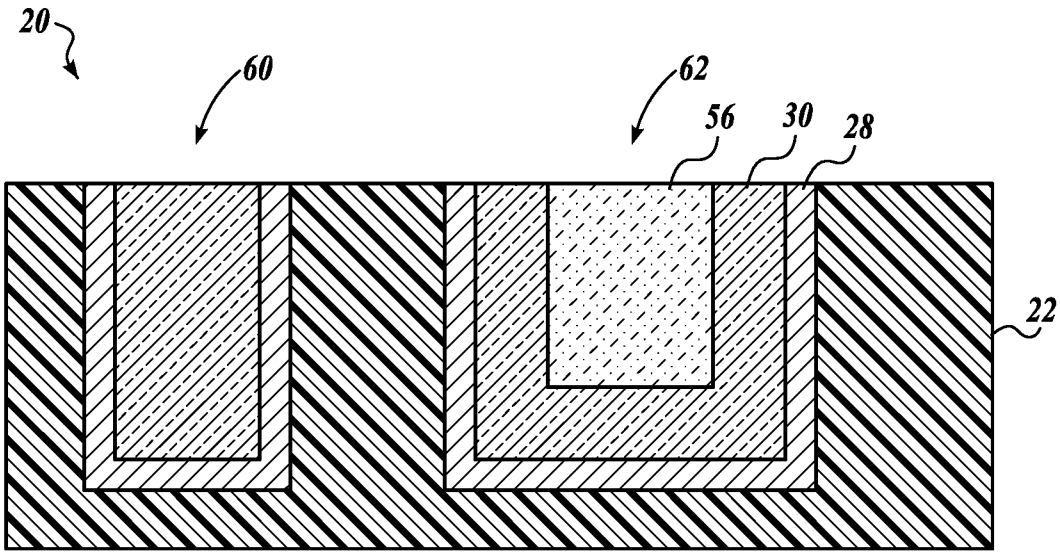

FIG. 3D

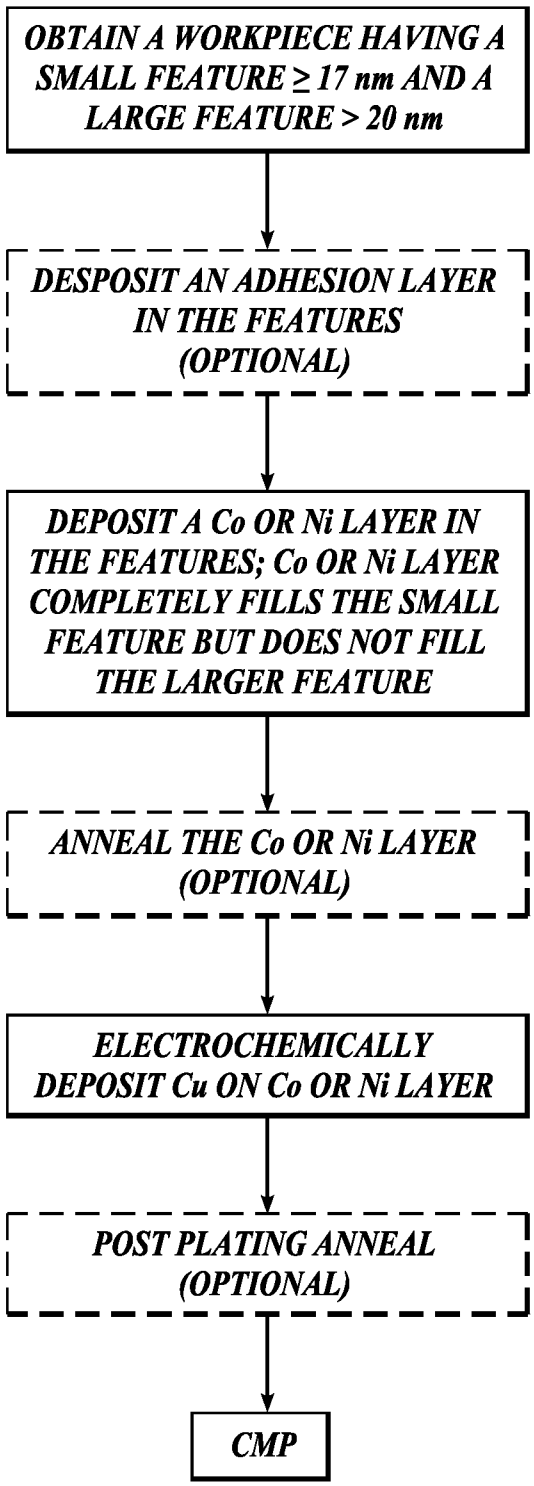
OBTAIN A WORKPIECE HAVING A SMALL FEATURE ≥ 17 nm AND A LARGE FEATURE > 20 nm
DESPOSIT AN ADHESION LAYER IN THE FEATURES (OPTIONAL)
DEPOSIT A Co OR Ni LAYER IN THE FEATURES; Co OR Ni LAYER COMPLETELY FILLS THE SMALL FEATURE BUT DOES NOT FILL THE LARGER FEATURE
ANNEAL THE Co OR Ni LAYER (OPTIONAL)
ELECTROCHEMICALLY DEPOSIT Cu ON Co OR Ni LAYER
POST PLATING ANNEAL (OPTIONAL)
CMP

FIG. 4

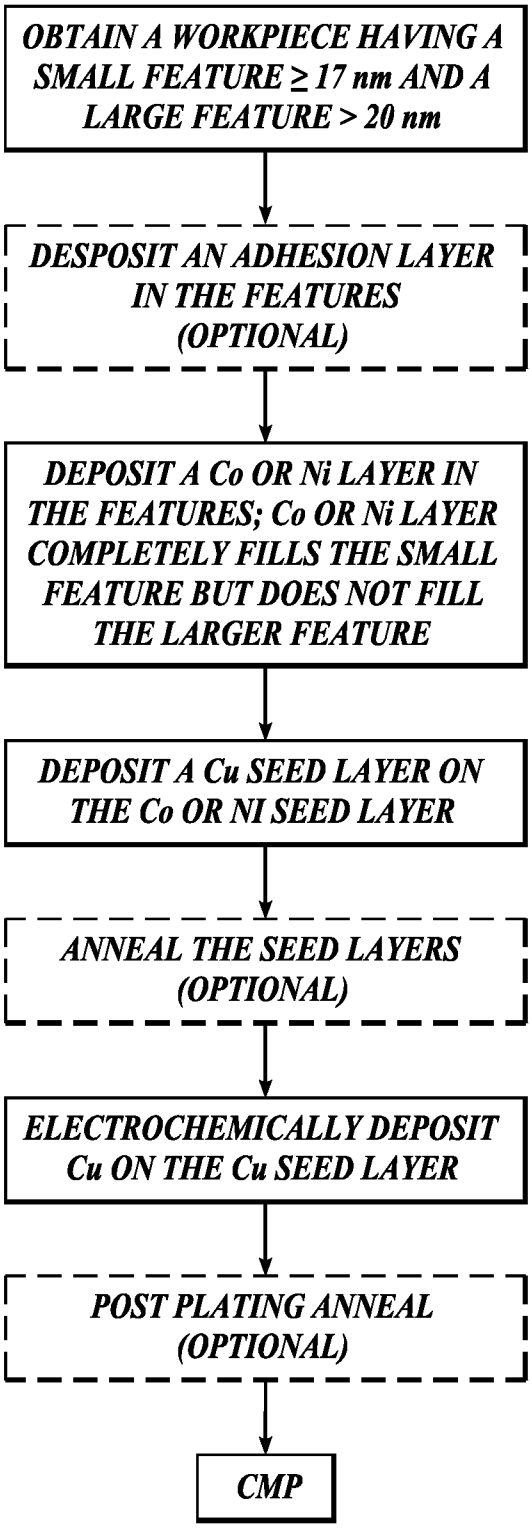
OBTAIN A WORKPIECE HAVING A SMALL FEATURE ≥ 17 nm AND A LARGE FEATURE > 20 nm
DESPOSIT AN ADHESION LAYER IN THE FEATURES (OPTIONAL)
DEPOSIT A Co OR Ni LAYER IN THE FEATURES; Co OR Ni LAYER COMPLETELY FILLS THE SMALL FEATURE BUT DOES NOT FILL THE LARGER FEATURE
DEPOSIT A Cu SEED LAYER ON THE Co OR NI SEED LAYER
ANNEAL THE SEED LAYERS (OPTIONAL)
ELECTROCHEMICALLY DEPOSIT Cu ON THE Cu SEED LAYER
POST PLATING ANNEAL (OPTIONAL)
CMP

FIG. 5

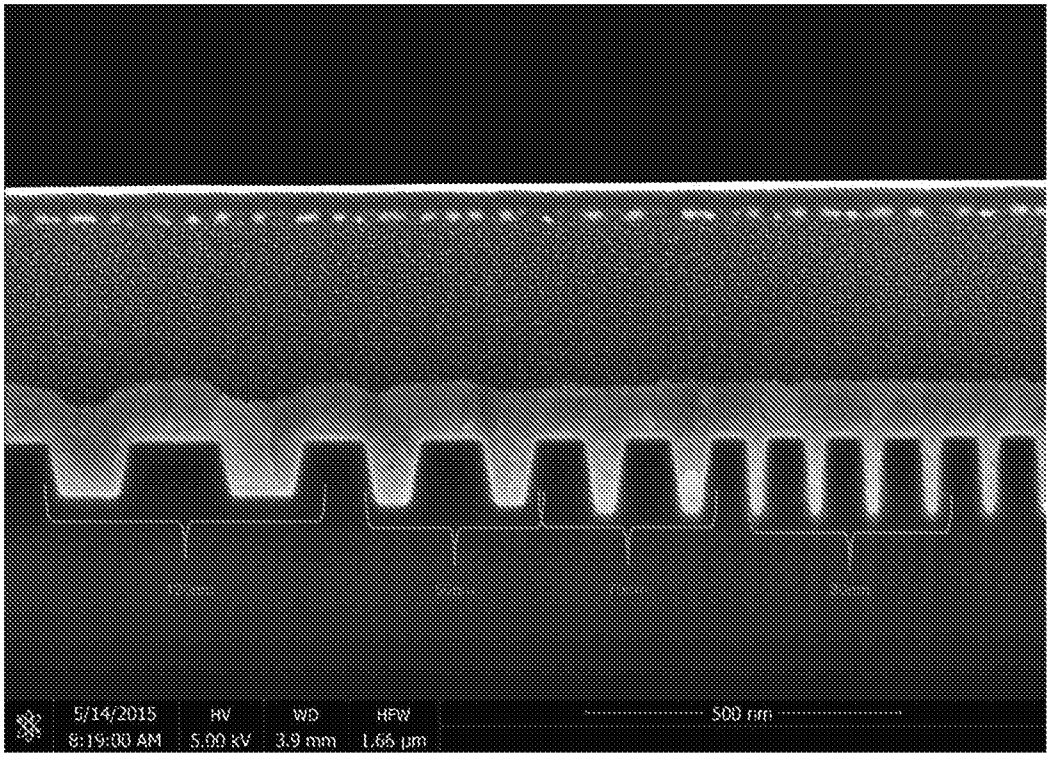

FIG. 6

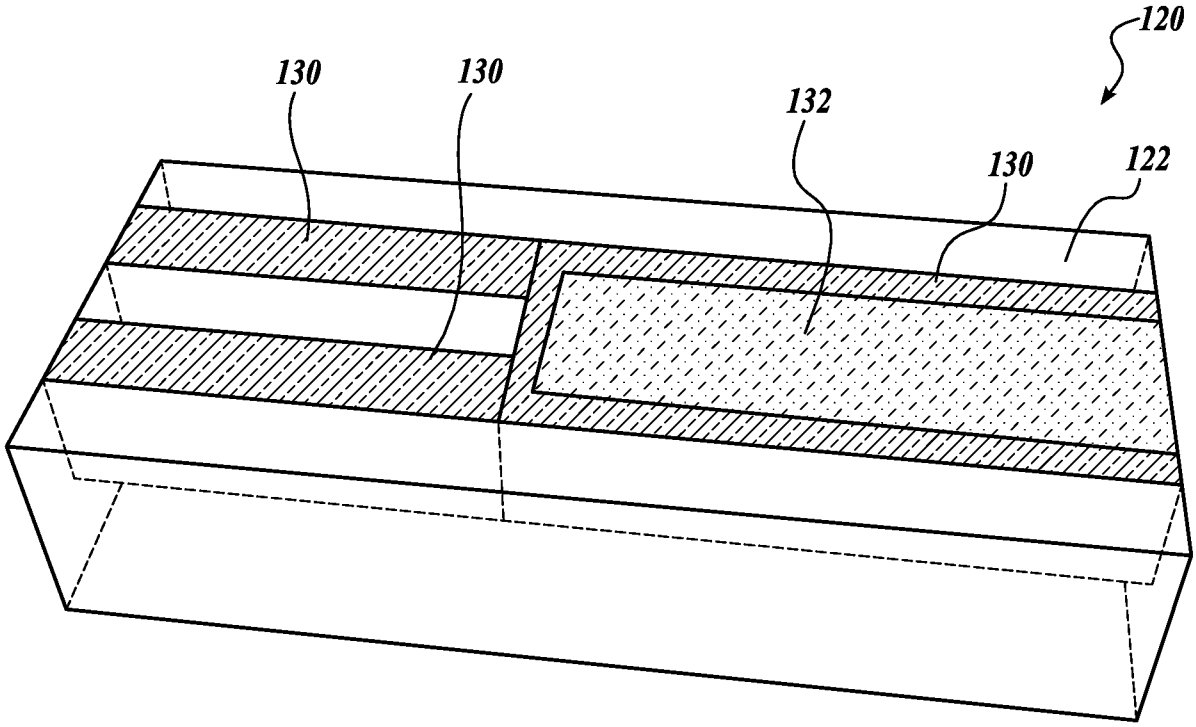

FIG. 7

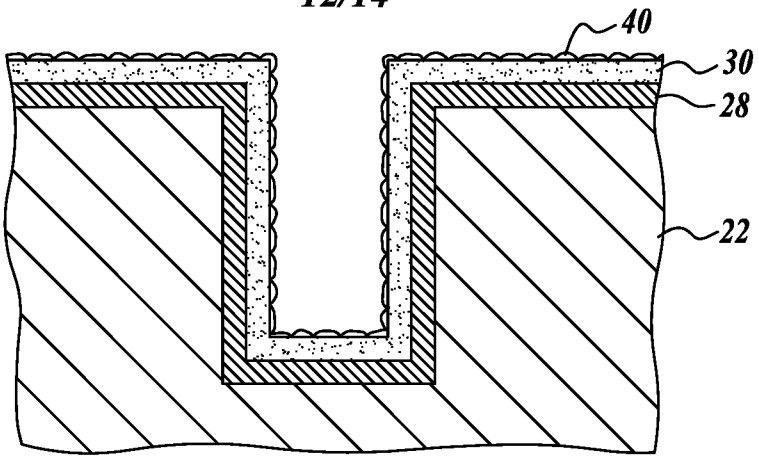

FIG. 8A

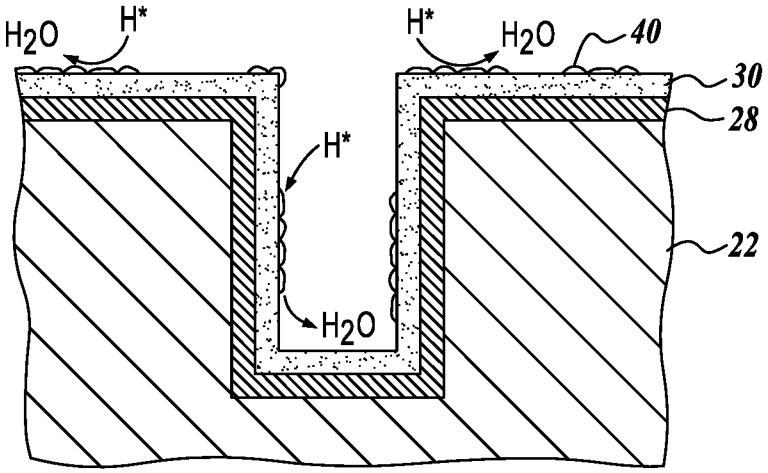

FIG. 8B

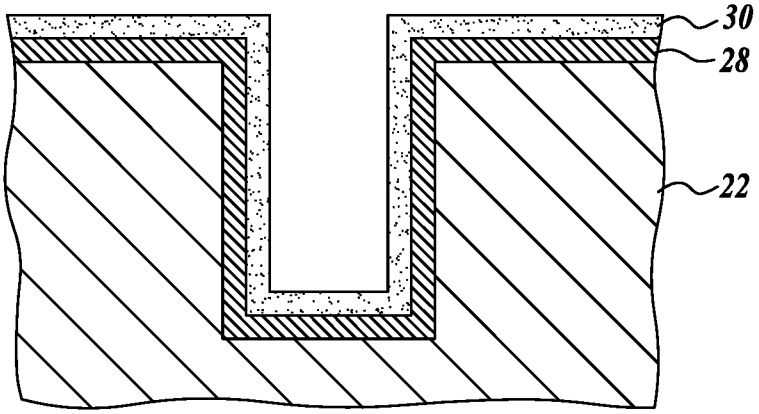

FIG.8C

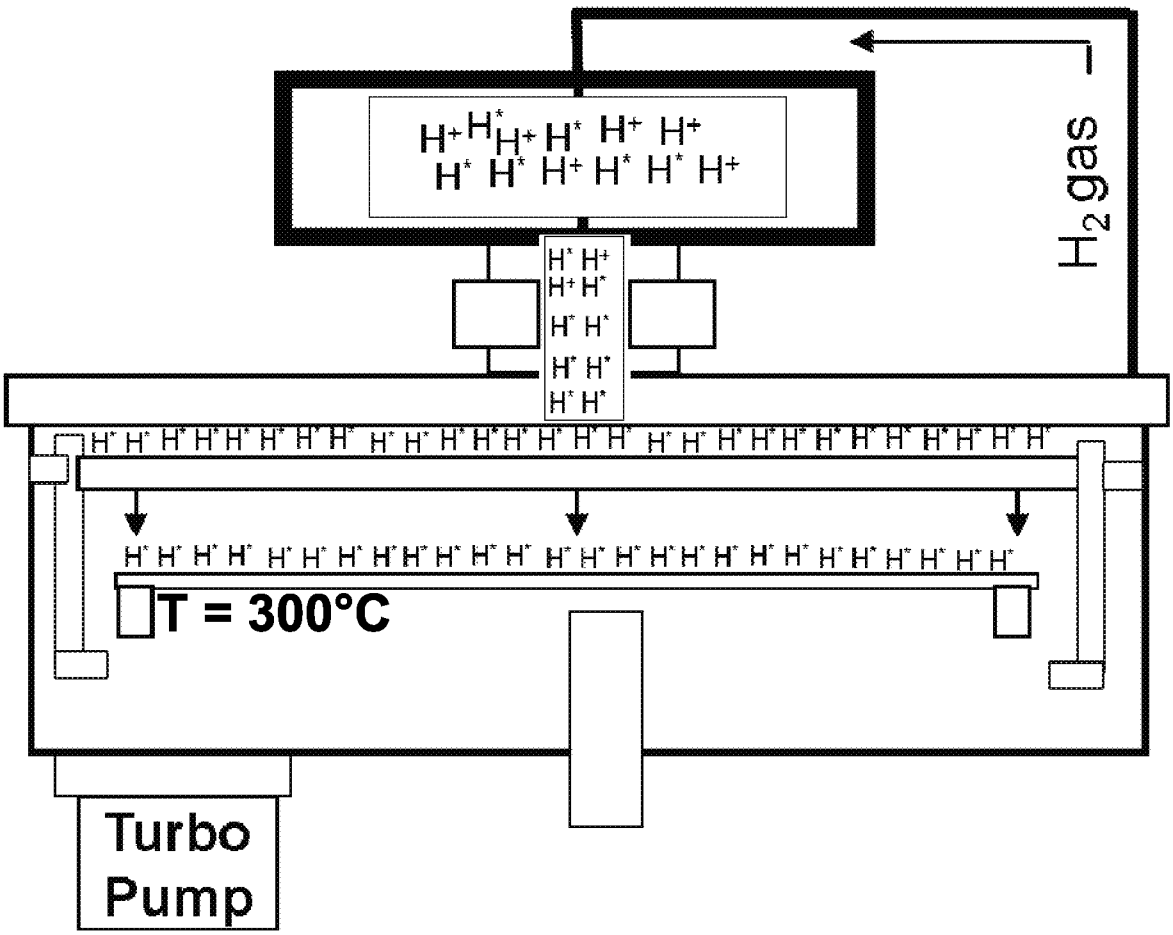

FIG. 9

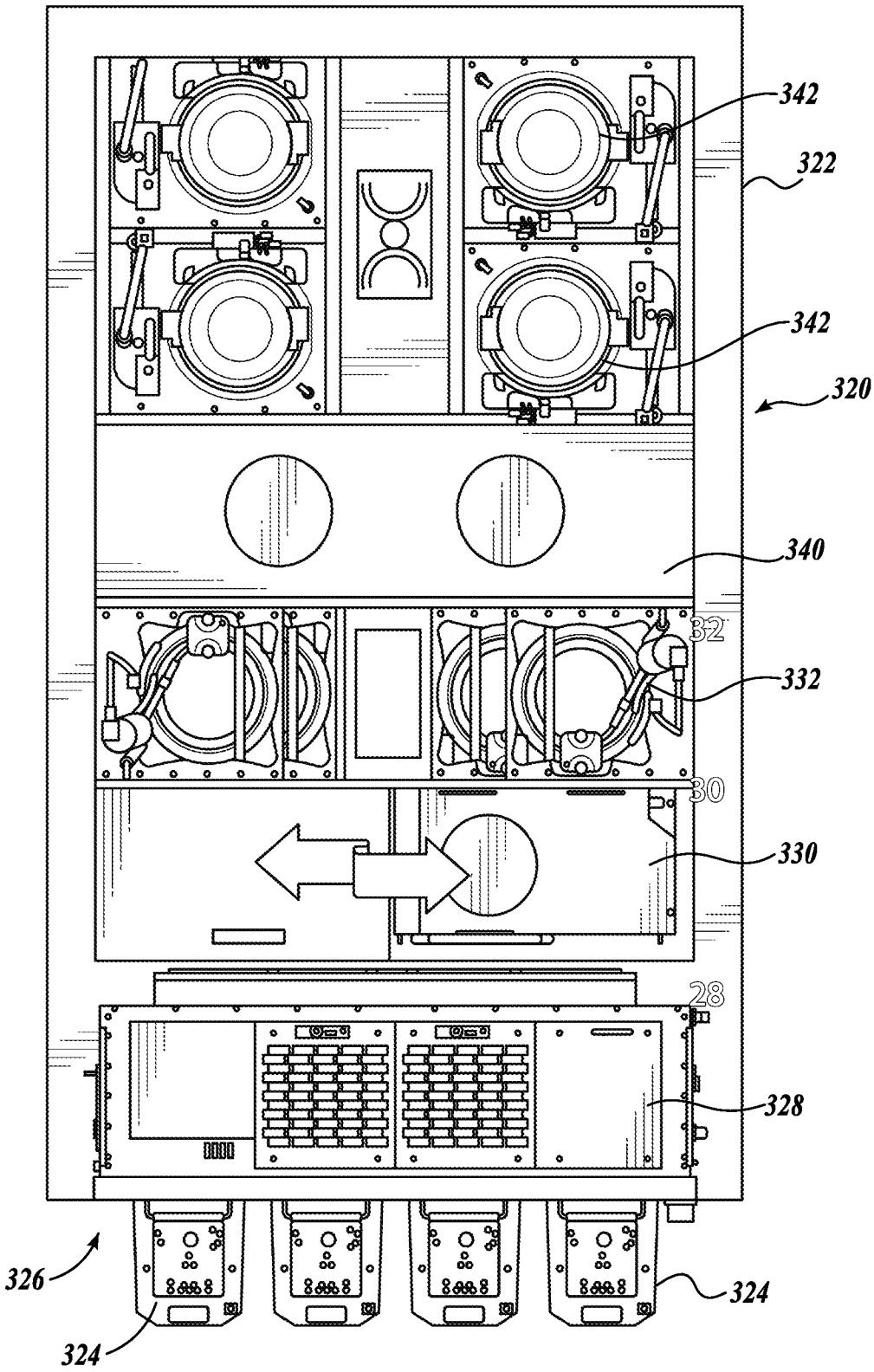

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/062583

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/285(2006.01)i, H01L 21/28(2006.01)i, H01L 21/02(2006.01)i, H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/285; H01L 23/52; G06F 17/50; H05H 1/24; B32B 15/04; H05K 3/00; H01L 23/538; H01L 21/3205; H01L 21/44; C23C 16/00; H01L 21/02; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: interconnect, cobalt, nickel, copper, trench, via, fill layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004-0087148 A1 (KAISER H. WONG) 06 May 2004 See paragraphs [0008]-[0012] and figures 1, 7-9.	1-27
Y	US 2012-0091593 A1 (KANGGUO CHENG et al.) 19 April 2012 See paragraphs [0016]-[0022] and figures 1-6.	1-27
Y	US 2009-0017227 A1 (XINYU FU et al.) 15 January 2009 See paragraphs [0016]-[0025] and figure 2.	8
A	JP 2010-212601 A (TOKYO ELECTRON LTD.) 24 September 2010 See the whole document.	1-27
A	US 2008-0280151 A1 (NICOLAS JOURDAN et al.) 13 November 2008 See paragraphs [0022]-[0032] and figures 1A-1F.	1-27

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 April 2017 (19.04.2017)	**20 April 2017 (20.04.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/062583

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