

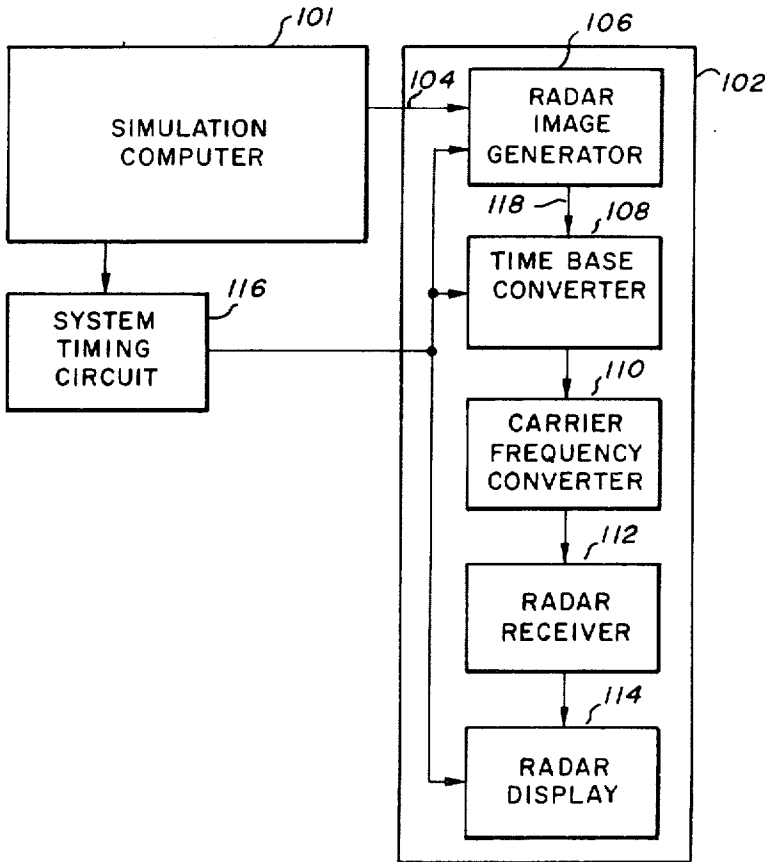
[54] SIGNAL CONVERSION SYSTEM
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[21] Appl. No.: 337,225
[52] U.S. Cl. 35/10.4
[51] Int. Cl. G09b 9/00
[58] Field of Search..... 35/10.4

[56] References Cited
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3,764,719 10/1973 Dell 35/10.4
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Primary Examiner—T. H. Tubbesing
Attorney, Agent, or Firm—Paul M. Hentzel; William
Grobman

[57] ABSTRACT
A signal conversion system which employs a random access memory for storing signals, and further including means for generating a first address for storing the signals and a second address for retrieving the stored signals is disclosed in this specification. The first set of addresses is generated in accordance with a first mathematical function, and the second set of addresses is generated in accordance with a second mathematical function. The input signal is periodically sampled, and an analog-to-digital converter is provided for converting the input signal from an analog form to a digital form for storage in the memory in accordance with the first set of addresses. A digital-to-analog converter is provided for converting the digital signals retrieved from the memory in accordance with the second set of addresses into an analog form. Control signals are generated for generating the first and second sets of addresses and for synchronizing the operation of the individual constituent circuits.

26 Claims, 23 Drawing Figures



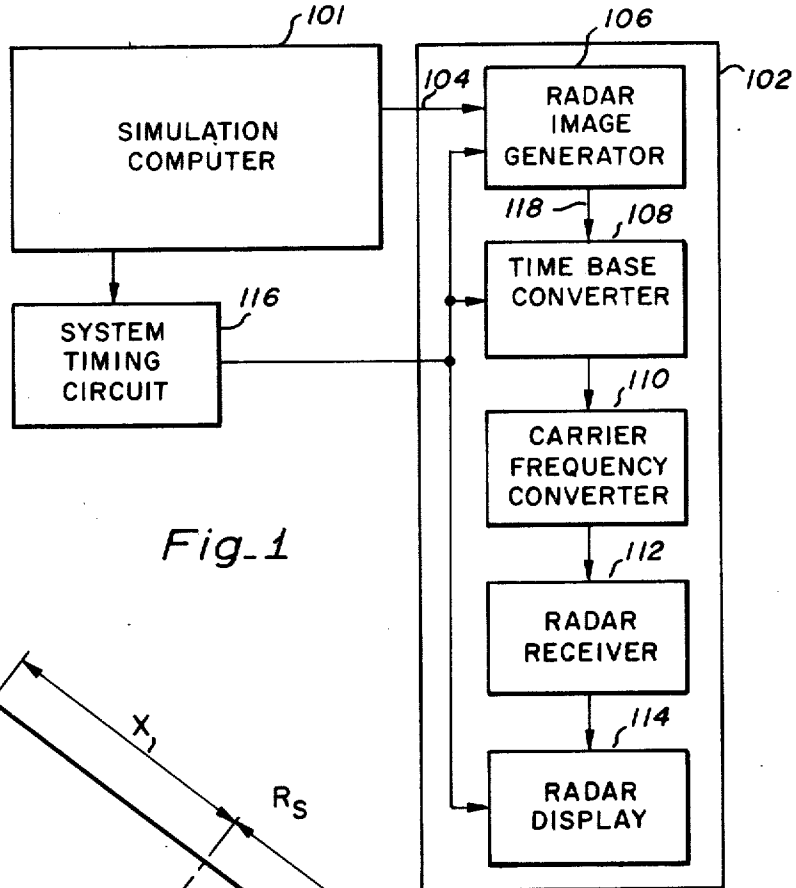


Fig-1

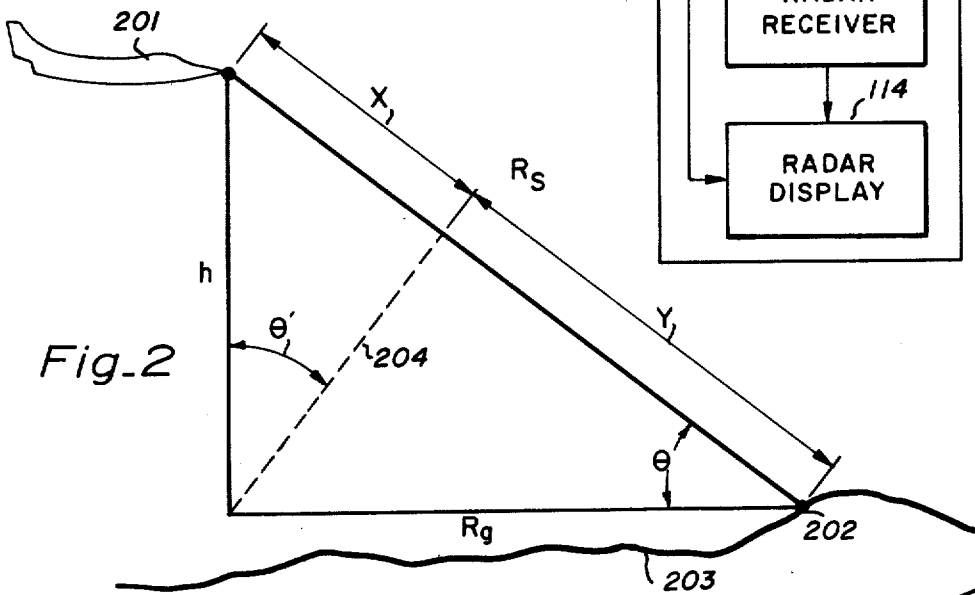


Fig-2

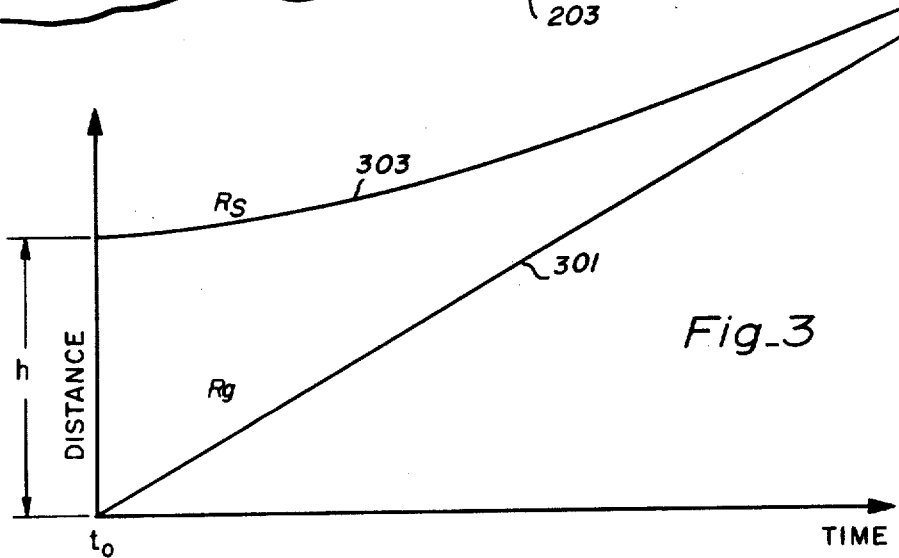
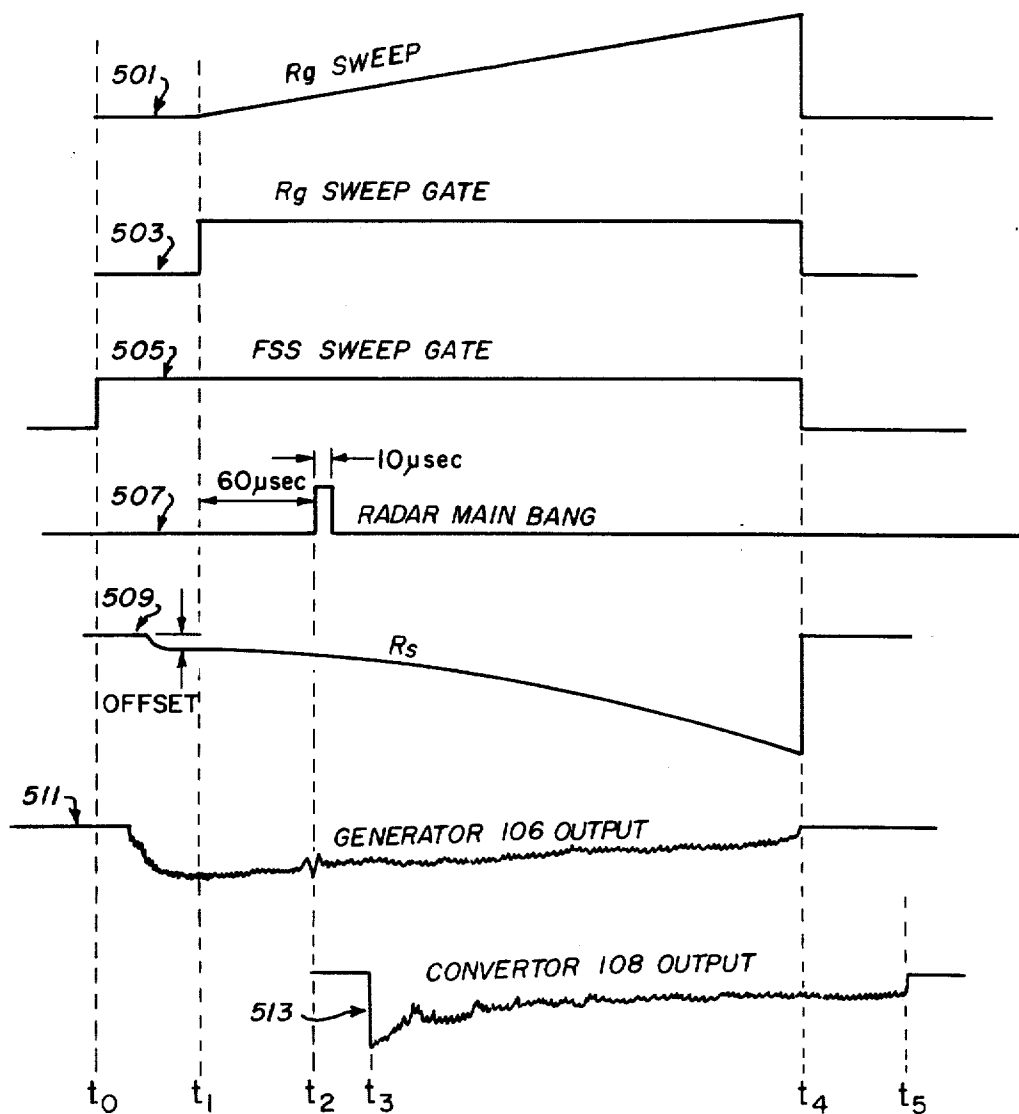
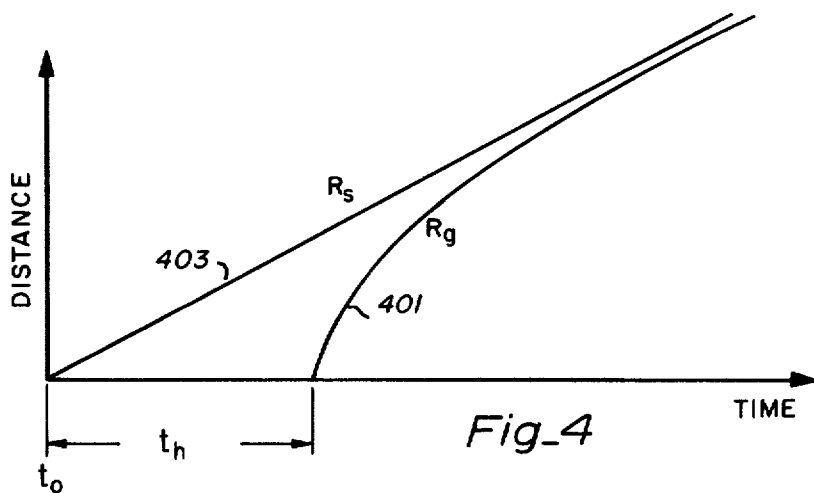


Fig-3



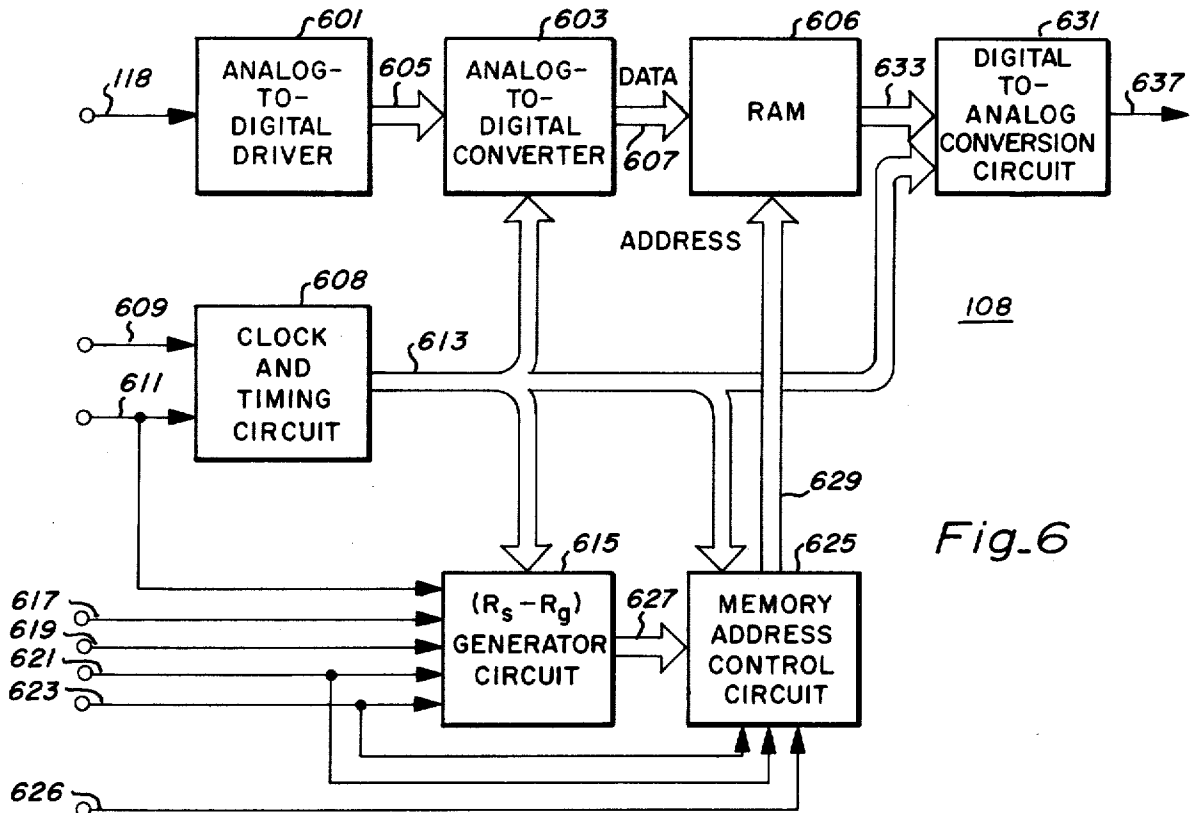


Fig. 6

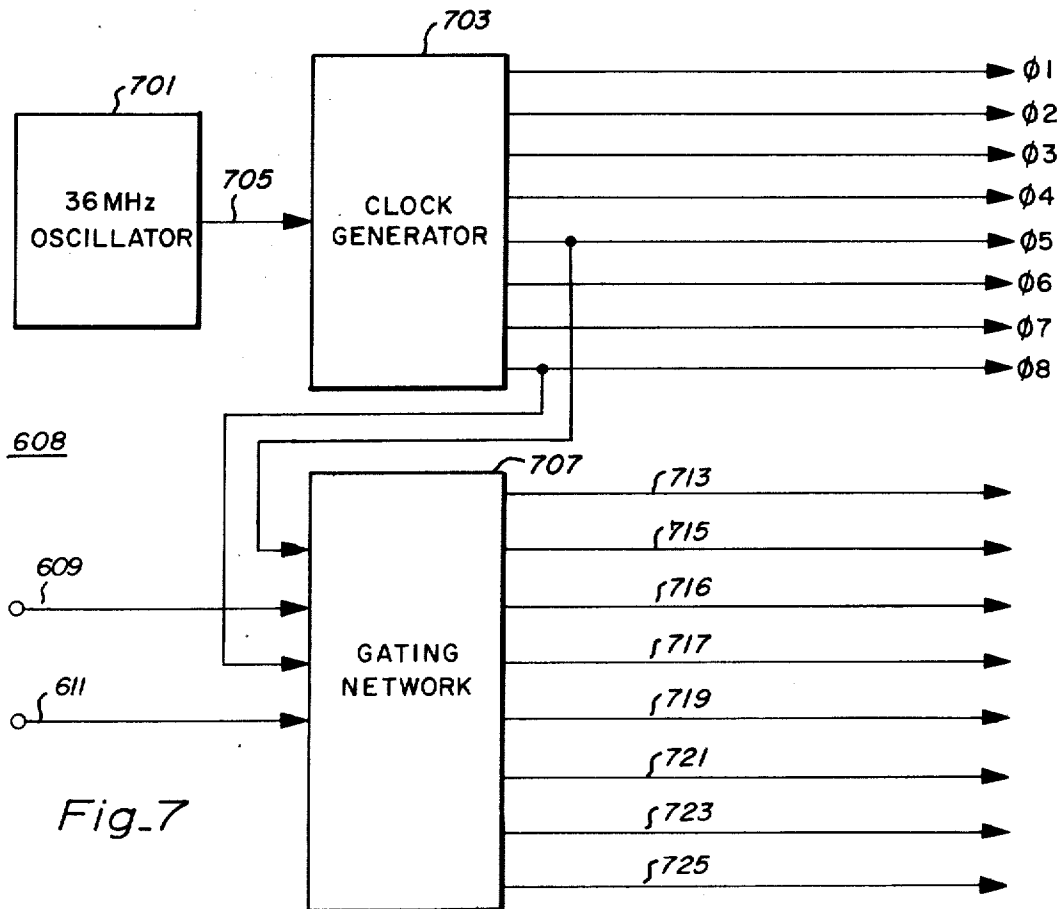
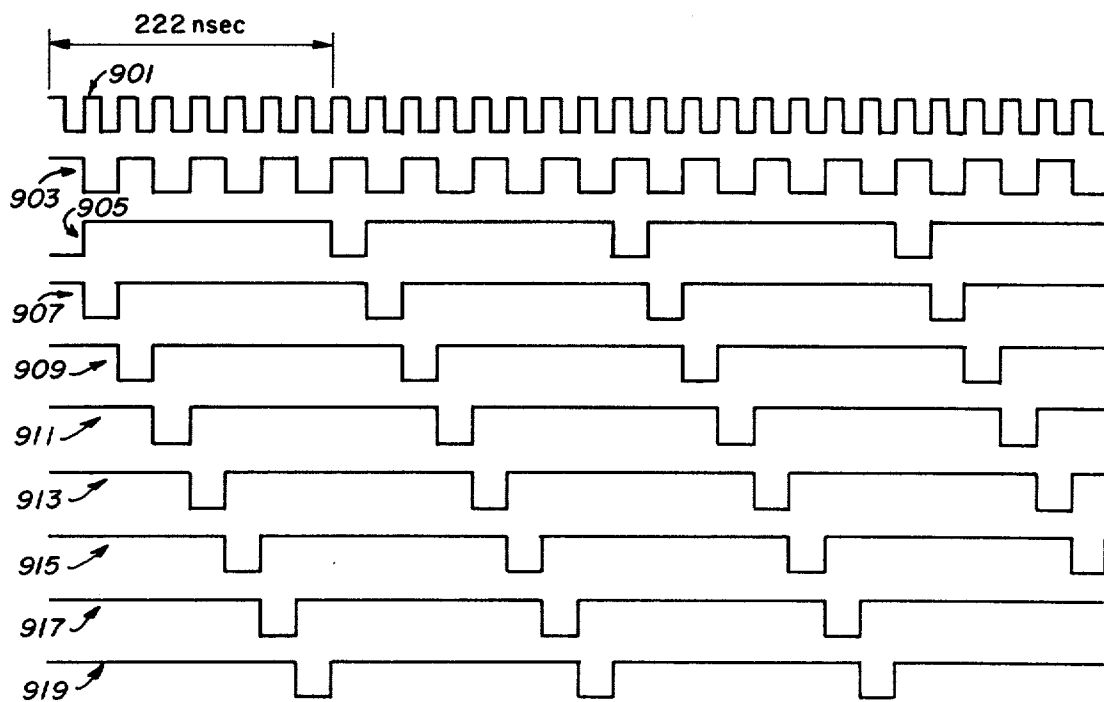
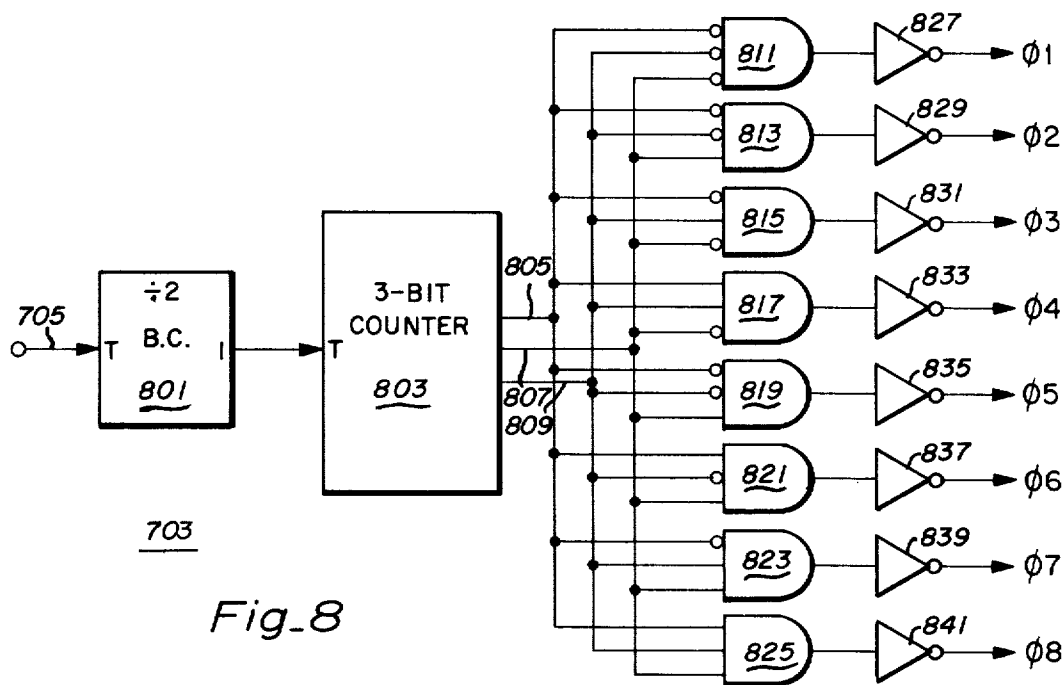


Fig. 7



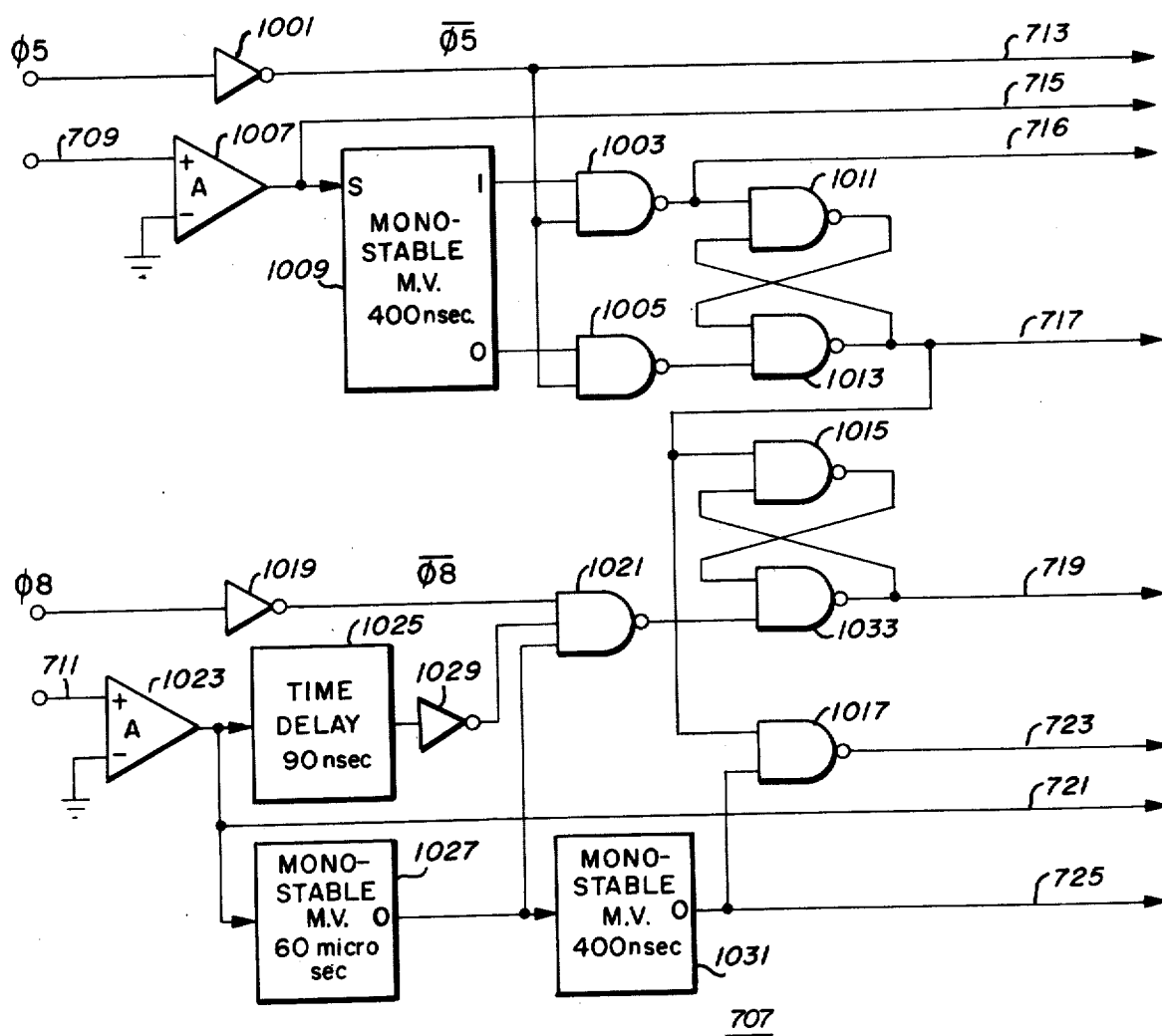


Fig. 10

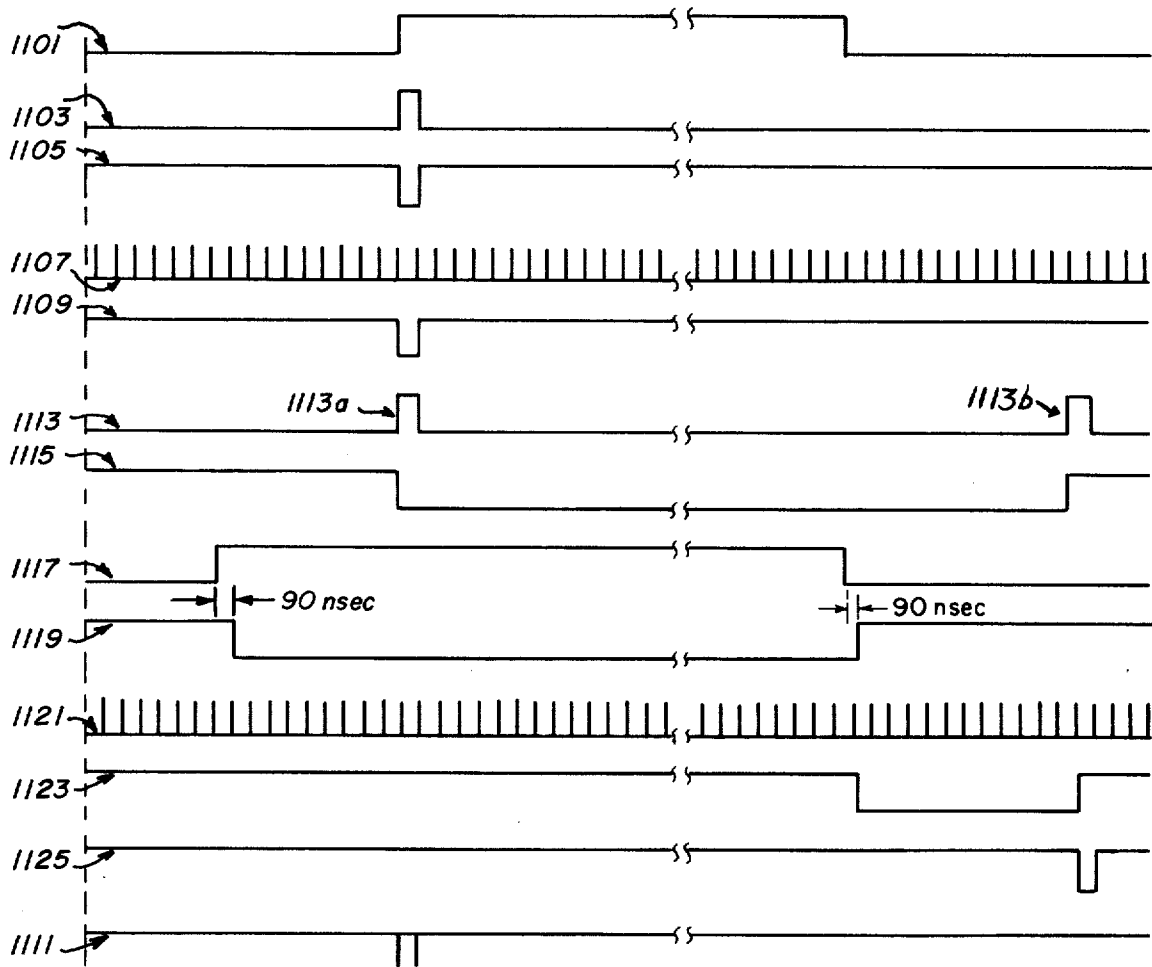


Fig. 11

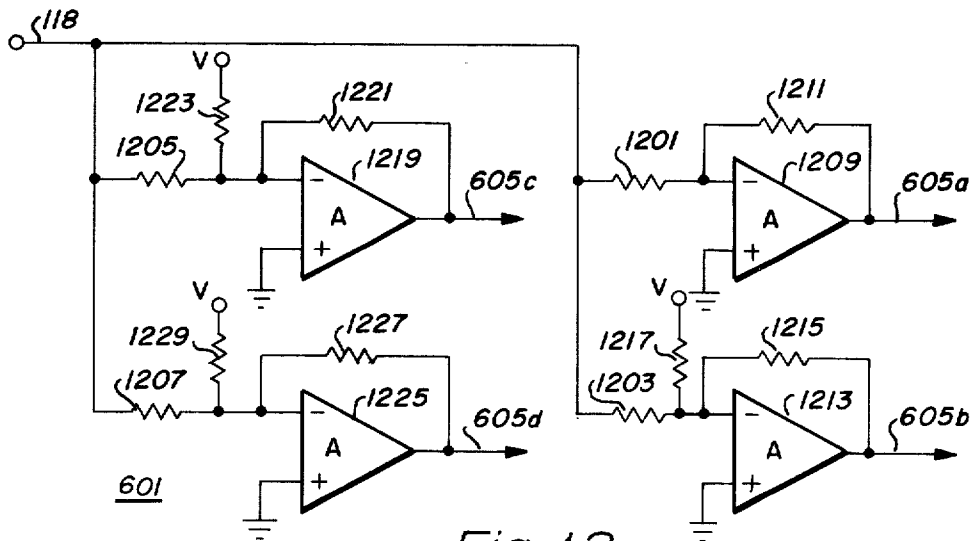


Fig. 12

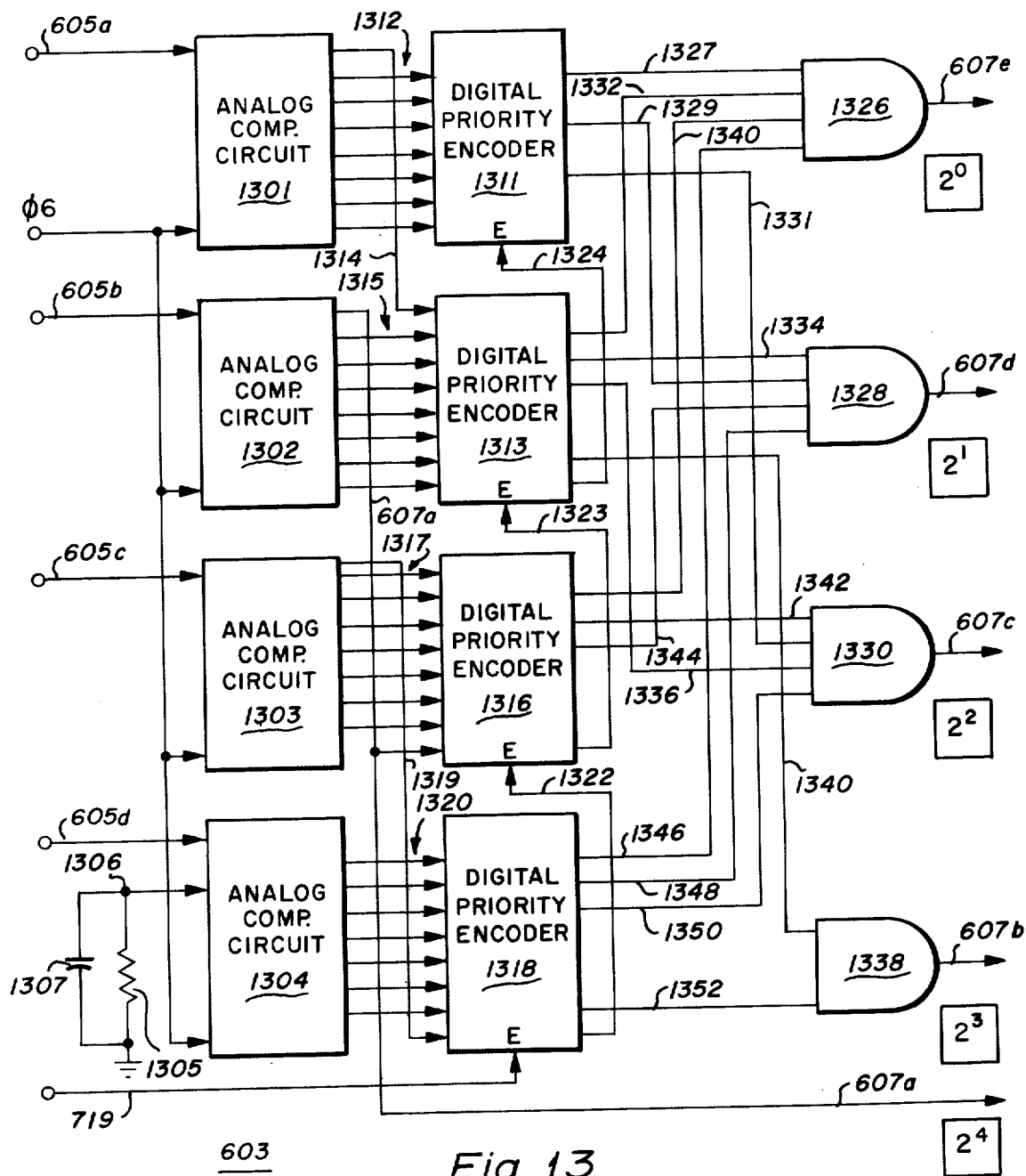
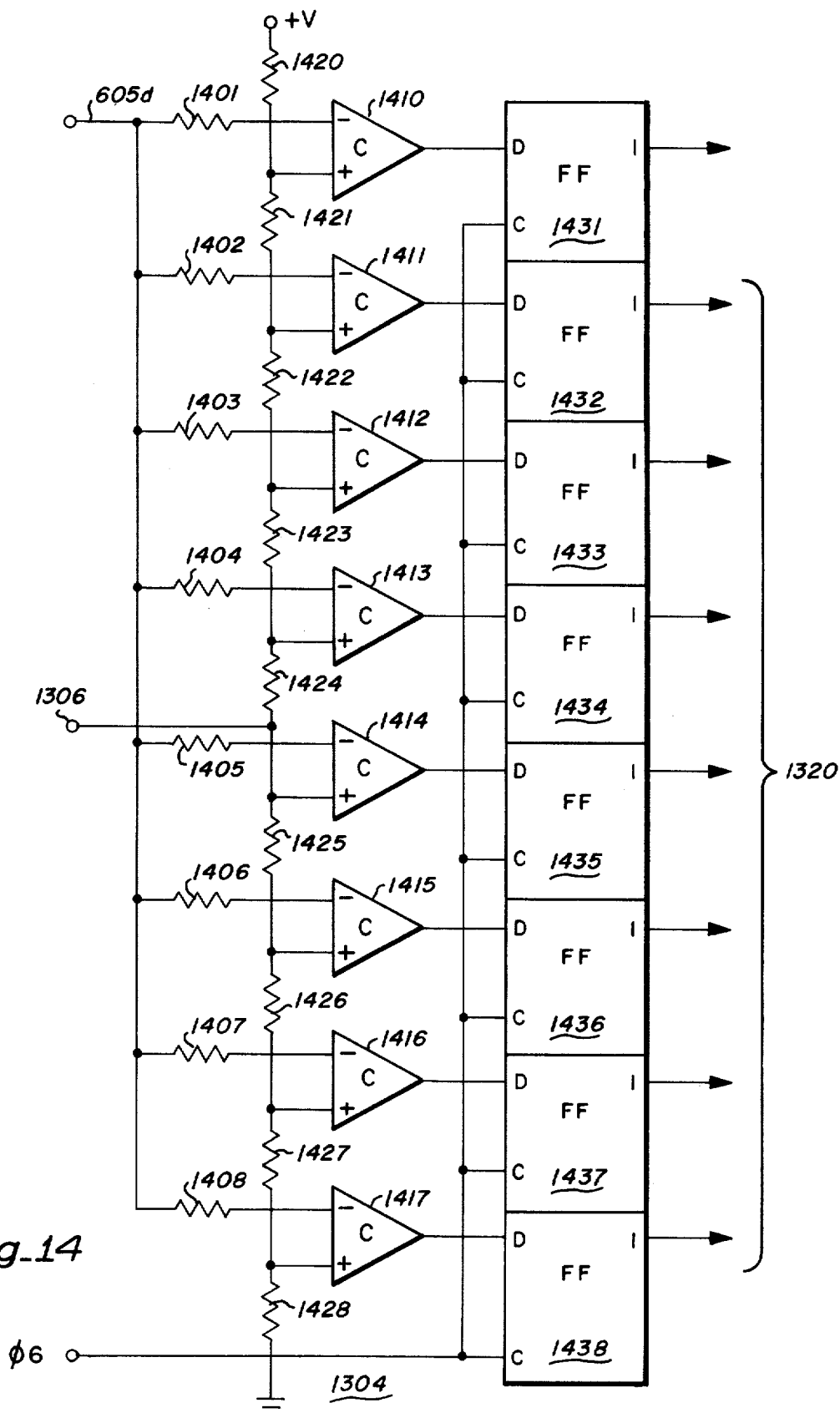


Fig. 13



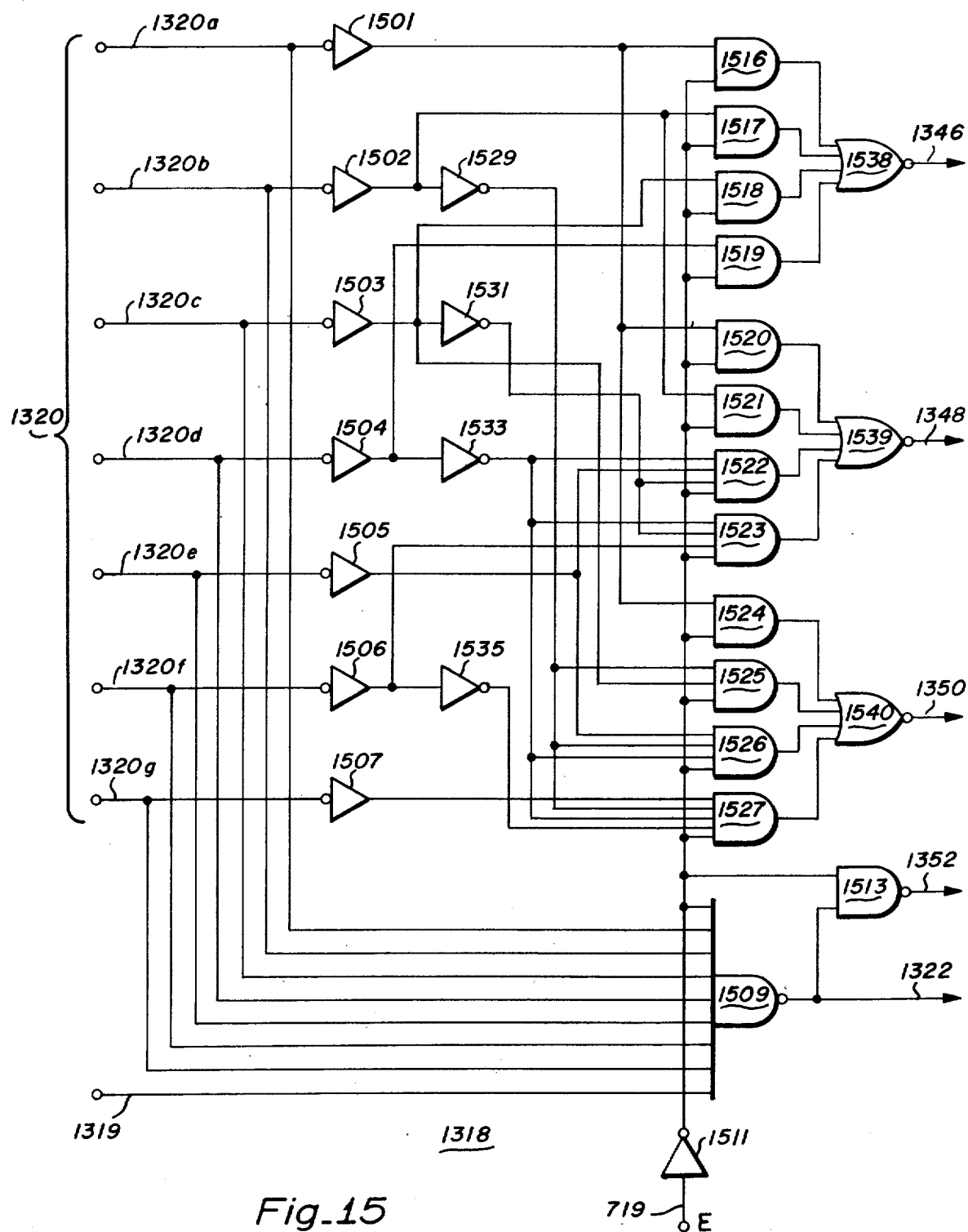
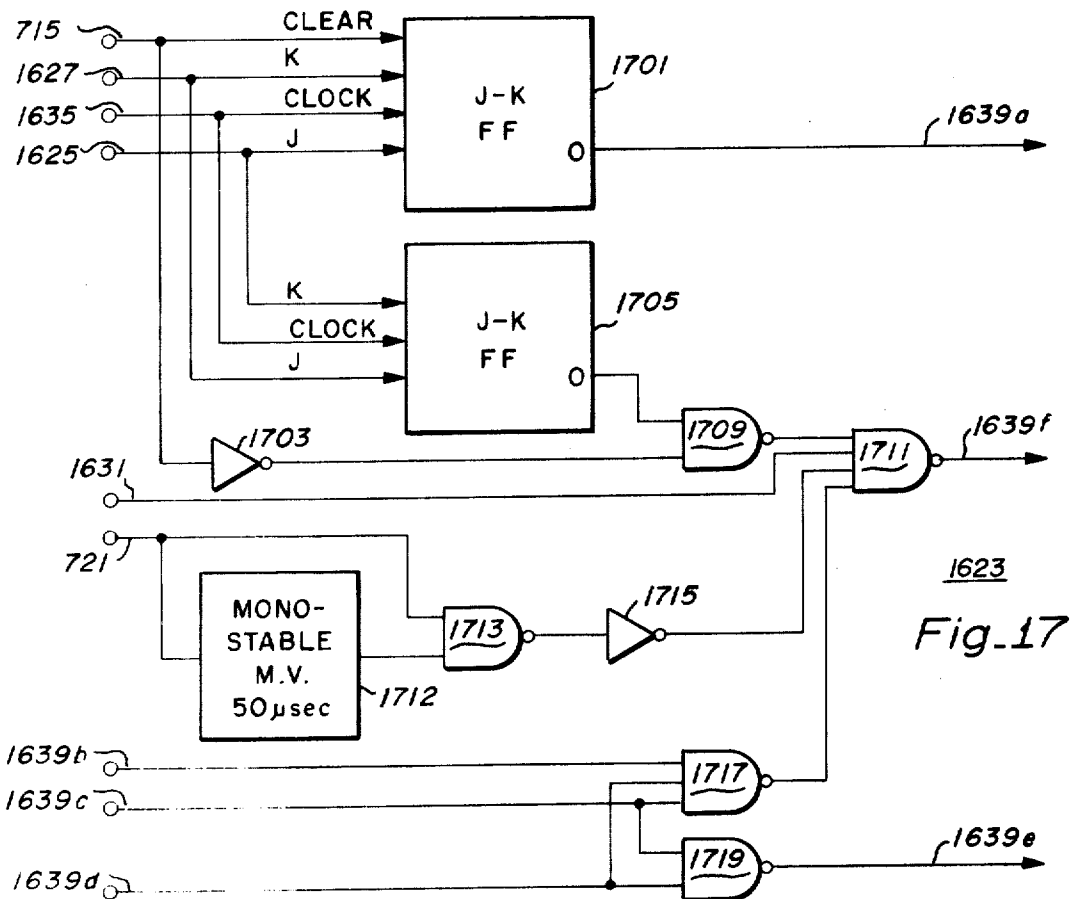
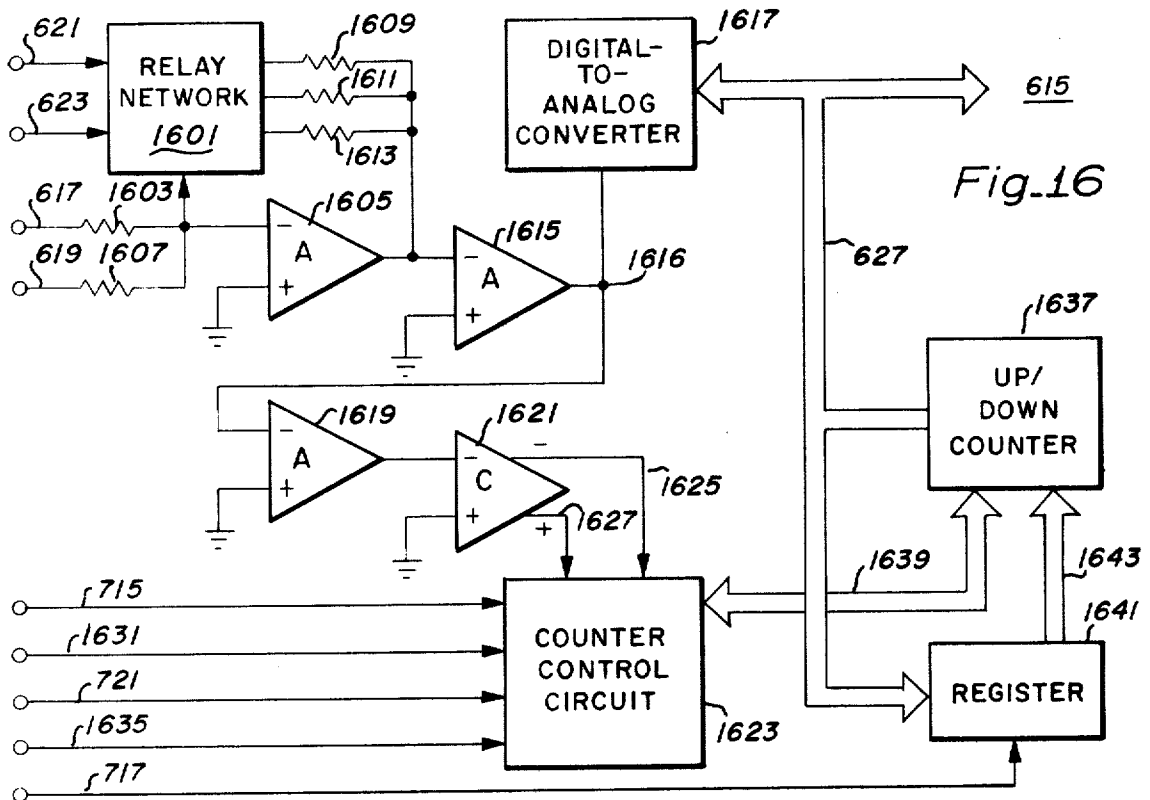


Fig. 15



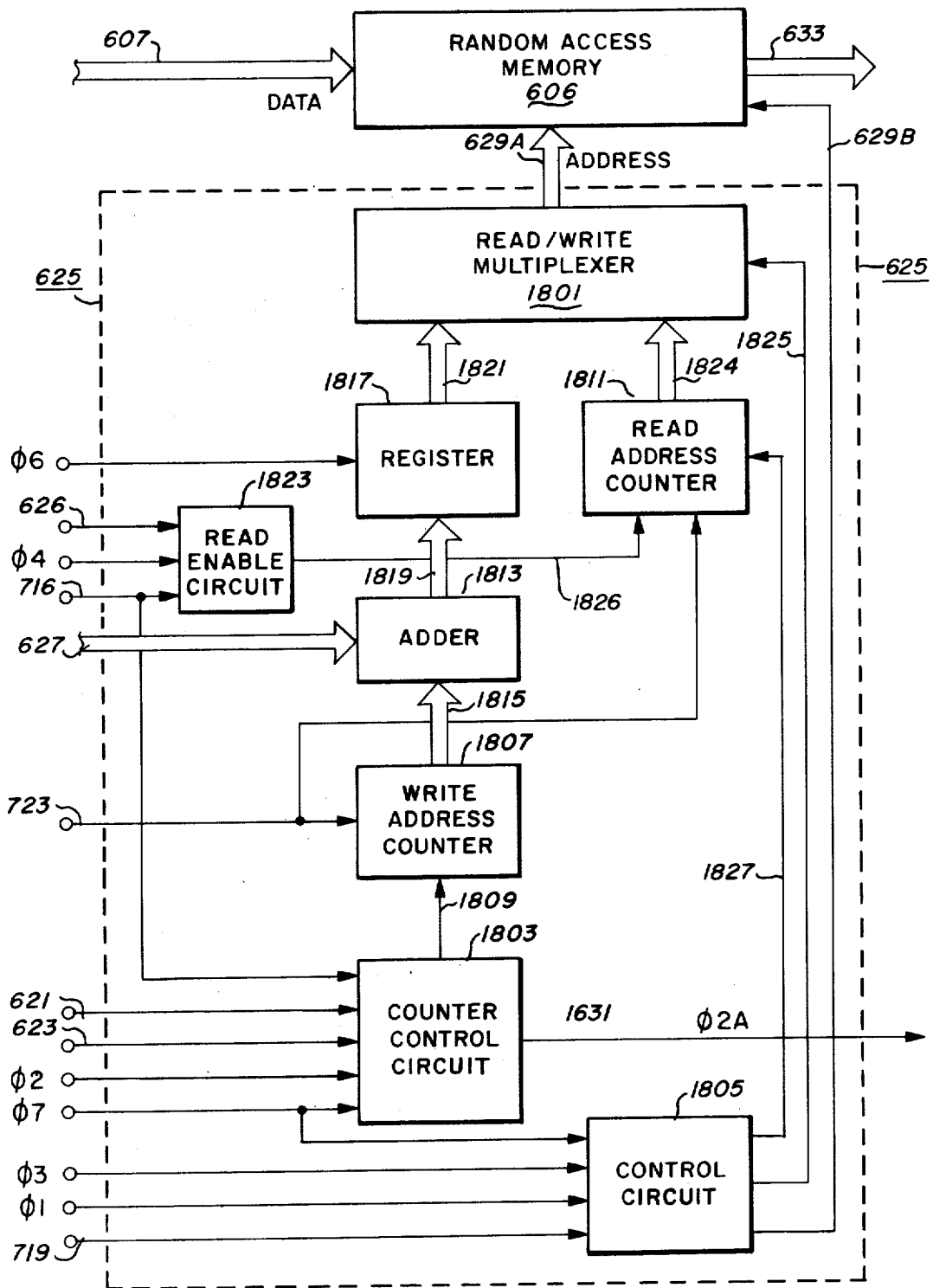


Fig_18

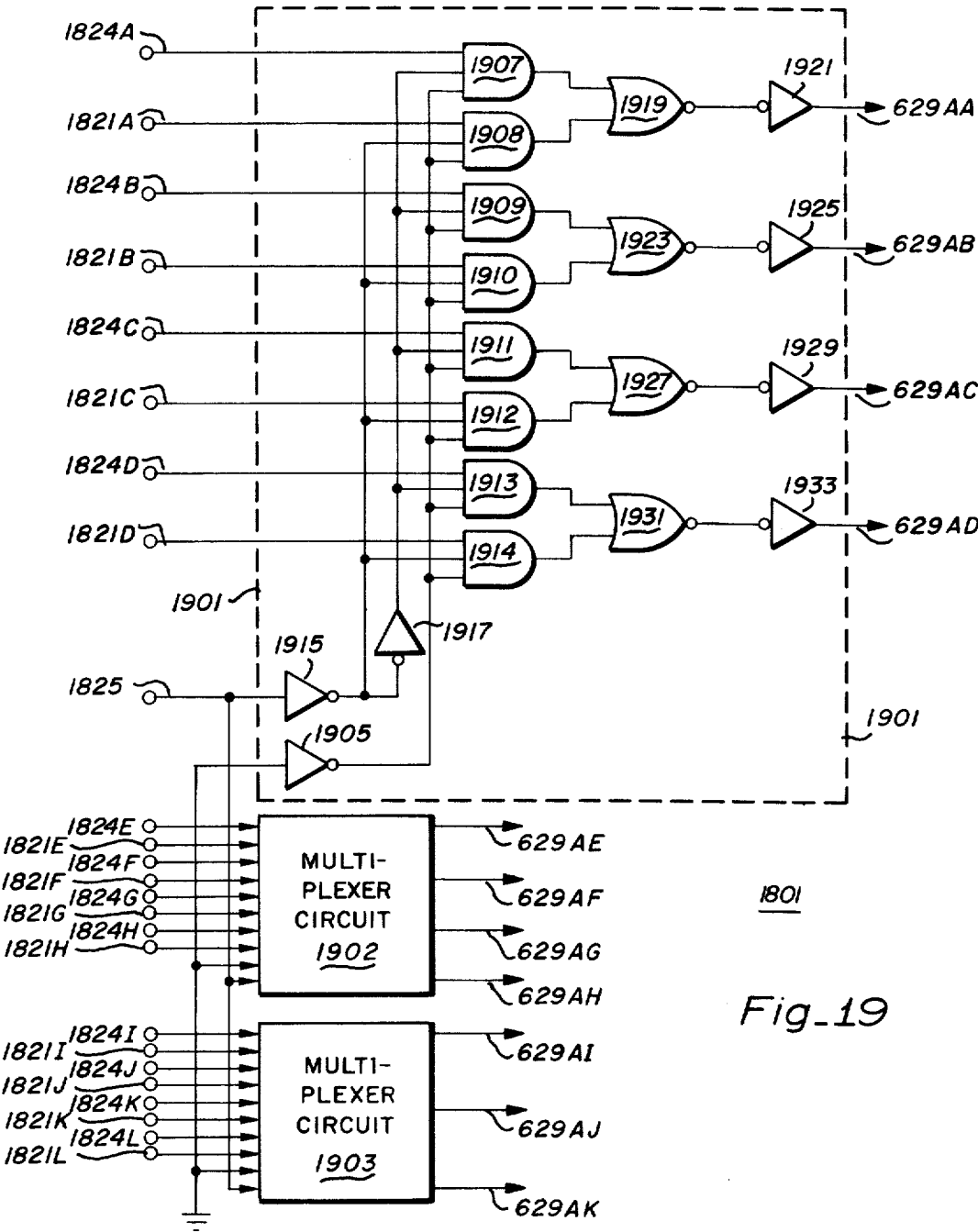


Fig-19

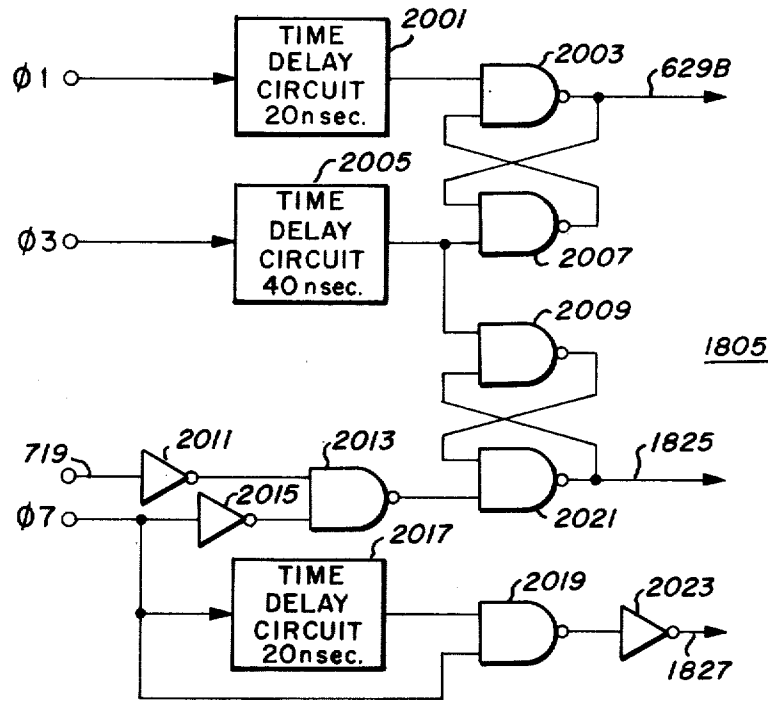
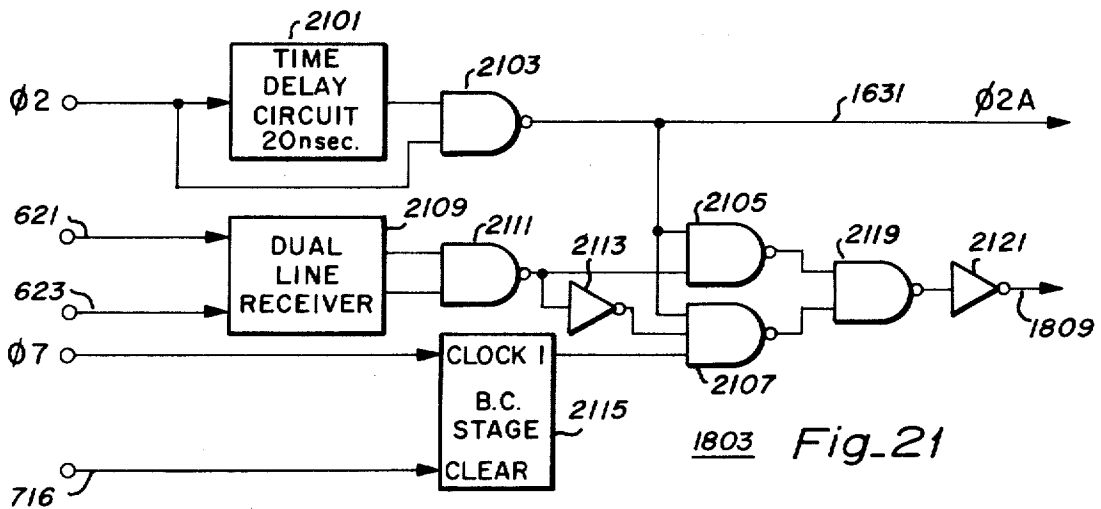


Fig_20



1803 Fig_21

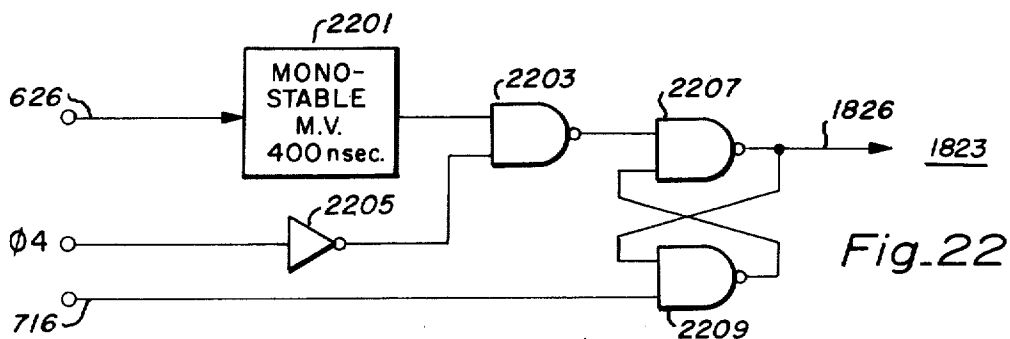


Fig. 22

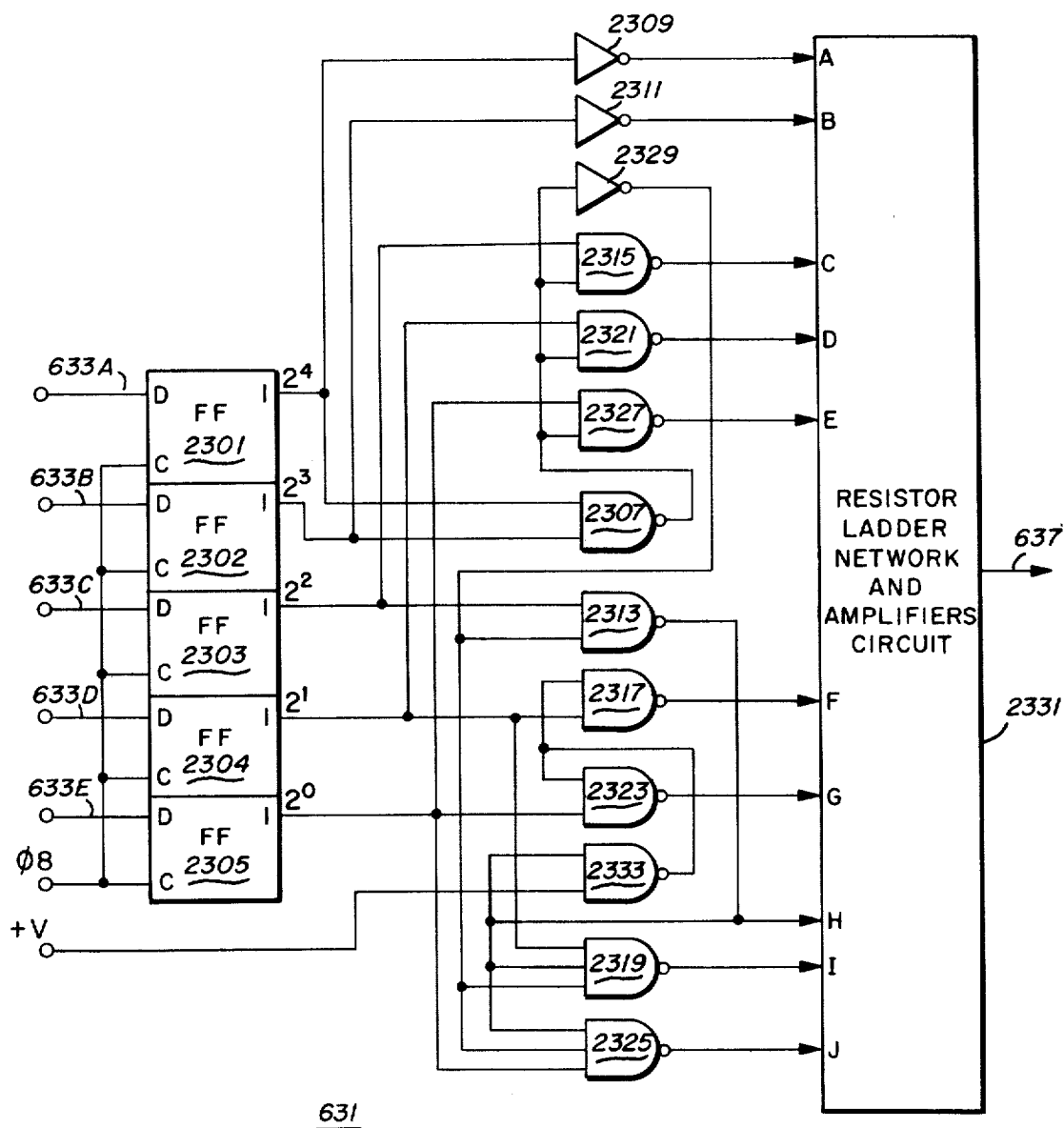


Fig. 23

SIGNAL CONVERSION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to simulators for training personnel in the operation of aircraft radar equipment, and more particularly to an improved apparatus for realistically simulating images displayed by radar equipment employed in aircraft flight simulators.

2. Description of the Prior Art

In the past, aircraft flight simulators have employed auxiliary devices for generating synthetic representations of the environment which would typically surround such simulated aircraft in flight; and for generating signals to operate instruments and indicators which are typically employed in such simulated aircraft. One such auxiliary device is an aircraft radar simulator.

Aircraft radar equipment normally includes a transmitter of very high frequency electromagnetic energy pulsed at a predetermined rate and a receiver which responds to the portion of the transmitted energy reflected from an object of the terrain. The output of the radar receiver is coupled to a cathode ray tube (CRT) which is employed as the radar display means. The electron beam of the CRT scans radial lines from an initial point representing the position of the aircraft itself, and light blips or spots representing objects or targets will appear on the CRT at radial distances from the initial point corresponding to the range or distance that the actual objects or terrain features bear with respect to the aircraft. A plurality of the radial lines are rapidly scanned in a sequence, and the light blips or spots are combined by the radar equipment in order that a map-like display be provided on the CRT with various terrain features and other objects appearing as light spots in scaled relation with the aircraft's location. The range or distance is representative of the slant range from the aircraft to the terrain features and other objects.

The simulation of actual aircraft radar equipment is often accomplished by employing at least one flying-spot scanner (FSS) or other light source to synchronously scan a pair of photographic transparencies, wherein various shades of gray on the first of the transparencies is encoded to represent radar reflectance information, and a second of the transparencies is encoded to represent elevation information. The modulated light passing through the transparencies is thereafter converted into video signals and operated upon to provide input signals for the radar display means. An example of this type of simulator is disclosed in U.S. Pat. Nos.: 3,031,774; 3,067,526; 3,100,328; 3,113,989; and 3,291,884.

Another type of radar simulator presently being used employs a single FSS and a transparency containing both elevation and reflectance information color-coded onto the transparency. The modulated light passing through the transparency is collected and decoded into a plurality of discrete signals, and these signals are operated upon to provide a combined video signal for the simulated radar CRT.

These radar simulators generate radar video signals by radially scanning the transparencies with the FSS from a point indicative of aircraft ground position to objects on the terrain. The radar video signal thus generated is linear with respect to a ground range time base. Since the actual aircraft radar video is linear with

respect to a slant range time base, the synthetically generated video signal from the radar simulator must be converted to a video signal linear with respect to slant range time base.

One such device presently available on the market for converting radar video from a linear ground range time base to a linear slant range time base is a dual electron beam scan-converting vacuum tube, or a storage tube. This scan-converting tube employs two opposing electron guns disposed coaxially with an electron charge-storage screen located between the two electron guns. The electron beam from a first of these two electron guns is directed toward one side of the charge-storage screen, and the electron beam from the second electron gun is directed toward the second side of the charge-storage screen. A separate deflection means is provided for each electron beam. In general operation, the first electron beam is deflected in a predetermined pattern, and the beam is further modulated to cause disruptions in the electron charges on the charge-storage screen. A pattern of the disrupted charges is thereby made on the charge-storage screen. The second electron beam may be deflected in the same or a different pattern to detect, with a secondary collector electrode, the pattern of disrupted charges made by the first electron beam. This type of scan-converting tube, or storage tube, is described in greater detail in "Television" by V. K. Zworykin and G. A. Morton, Second Edition, on pages 377 and 378.

As used in radar simulators, the first electron beam of the scan-converting tube is deflected by a non-linear signal representative of the simulated aircraft's slant range, which signal is derived from the linear ground range time base of the radar simulator in combination with the aircraft altitude above the terrain. The first electron beam is modulated by the synthetic video from the radar simulator. The pattern of disrupted charges produced on the charge-storage screen, as a result of the deflection and modulation, is representative of a spatial distribution of the slant range video signal. The second electron beam scans the charge-storage screen and the resulting analog signal produced at the secondary collector electrode is representative of video linear with respect to the slant range time base. However, it is pointed out that the second electron beam is delayed in time from the scanning operation of the first electron beam for an amount of time sufficient to preclude simultaneous production of charge-storage by the first electron beam and the scanning of the charge-storage from the same element on the screen by the second electron beam.

The prior art scan-converting tube is not reliable over any reasonable period of time in that it requires frequent and precise realignment as a result of serious short-term drift, and in that the tube must be replaced periodically as a result of a relatively short life expectancy.

SUMMARY OF THE INVENTION

According to the present invention, a storage means is disposed for randomly storing discrete manifestations of the video information from an FSS of a radar simulator. Video information is entered into the memory at an address whose numerical value is proportional to the instantaneous difference between the radar slant range distance and the radar ground range distance. The video information is retrieved sequentially from the

storage means. Electronic circuits are provided for generating an address for retrieving video information from the memory; and for controlling the timing of all circuitry.

A general object of this invention is the provision of a novel apparatus for converting radar simulator video signals into a realistic representation of the simulated operation of aircraft radar equipment.

Another object is the provision of a new and improved solid-state electronic circuit for converting radar simulator video signals which are generated linearly with respect to a ground range time base into radar video signals which are linear with respect to a slant range time base.

Another object is the provision of an improved means for converting radar simulator video signals from one time base to another time base, which means employs a high-speed random access memory.

A further object is the provision of a radar simulator video time base converter which, in comparison to those previously known, is simpler in construction, lower in cost, and more reliable in operation.

A primary advantage of the present invention over similar devices of the prior art is that solid-state electronic circuitry is employed, which circuitry improves the reliability of operation.

These and other objects and advantages of the present invention will become clear to one normally skilled in the art from perusal of the appended specification when taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a simulator system in which the apparatus of the present invention may be used;

FIG. 2 is a diagram of the geometric relationship between ground range R_g , slant range R_s , and altitude h ;

FIG. 3 is a diagram illustrating the distance-to-time relationship of R_g , R_s , and h prior to a time base conversion by the present apparatus;

FIG. 4 is a diagram illustrating the distance-to-time relationship of R_g , R_s , and h following a time base conversion by the present apparatus;

FIG. 5 is a timing diagram of the signals supplied to the present apparatus and the video signal provided at the output following a time base conversion;

FIG. 6 is a block diagram of one form of the apparatus of the present invention;

FIG. 7 is a block diagram of the clock and timing circuit;

FIG. 8 is a logic-block diagram of the clock generator of FIG. 7;

FIG. 9 is a timing diagram for the circuit of FIG. 8;

FIG. 10 is a logic diagram of the gating network of FIG. 7;

FIG. 11 is a timing diagram for the circuitry shown in FIG. 10;

FIG. 12 is a schematic-block diagram of the analog-to-digital driver circuit;

FIG. 13 is a logic-block diagram of the analog-to-digital converter;

FIG. 14 is a schematic-logic diagram of the analog comparator circuit of FIG. 13;

FIG. 15 is a logic diagram of the encoder of FIG. 13;

FIG. 16 is a schematic-block diagram of the $R_s - R_g$ generator;

FIG. 17 is a logic diagram of the conditioning logic and count limiter circuit of FIG. 16;

FIG. 18 is a block diagram of the memory address control circuit;

FIG. 19 is a logic-block diagram of the read/write multiplexer of FIG. 18;

FIG. 20 is a logic diagram of the control logic for the read address counter, multiplexer, and random access memory of FIG. 18;

FIG. 21 is a logic diagram of the write address control logic of FIG. 18;

FIG. 22 is a logic diagram of the read enable logic of FIG. 18; and

FIG. 23 is a logic-block diagram of the digital-to-analog converter circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings in detail, and to FIG. 1 in particular, the reference character 101 designates a simulation computer which may, for example, comprise a conventional digital computer programmed for simulating aircraft. Data is supplied from computer 101 to a radar simulator 102 via a line 104. This output data is indicative of such things as simulated aircraft position, altitude, etc. Radar simulator 102 comprises a radar image generator 106 which receives the information from the computer 101 and has its output connected to an input of a time base converter 108 whose output is connected to the input of a carrier frequency converter 110 which feeds a portion of a radar receiver 112 and a radar display 114 connected to the output of the receiver 112. Simulation computer 101 also supplied data to a system timing circuit 116. The timing circuit generates a plurality of waveforms for controlling the radar simulator 102. More particularly, timing signals from circuit 116 are supplied as inputs to radar image generator 106, time base converter 108, and the radar display 114.

The radar image generator 106 generates synthetic radar video by scanning one or more transparencies containing information representative of terrain elevation and reflectance information. The scanning is usually performed by a beam of light, such as generated by a flying spot scanner, moving in a prescribed pattern, and then the light, which is modulated by its passage through the transparencies is converted into electrical signals. The output of radar image generator 106 is supplied to the input of the time base converter 108 via line 118. The time base converter 108, which constitutes the apparatus of the present invention, converts the video signals, generated linearly with respect to ground range, to video signals which are linear with respect to slant range. The frequency converter 110 modulates a carrier frequency (for example, 30 MHz) with the video converted by converter 108. Only a portion of receiver 112 is used, and the carrier modulated with the radar video from converter 110 is connected directly to the intermediate frequency (I.F.) portion of receiver 112. The output of receiver 112 activates radar display 114 to display the synthetic video generated by scanning the transparency(s). The operation of the FSS within the radar image generator 106 is synchronized with the sweep circuitry of the radar display 114 by the timing signals supplied from circuit 116. Also, as will be shown in greater detail hereinbelow, the operation of the time base converter 108 is operated in

synchronization with the same timing signals supplied from circuit 116.

In FIG. 2 the relationship is shown between the ground range and the slant range of the radar beam from the aircraft 201 to an object 202 on the ground. A triangle is formed by the slant range R_s , the ground range R_g and the altitude of the aircraft 201. The altitude of the aircraft 201 is computed from the actual altitude of the aircraft 201 above sea level less the elevation of the object 202. The ground range is the horizontal distance from the point of intersection of a vertical from the aircraft with the ground and the object 202. These values are computed by the computer 101 in accordance with information originally stored therein or supplied from the transparencies mentioned above.

The angle formed by sides R_s and R_g is designated hereafter as angle θ . A line 204 drawn perpendicular to slant range side R_s , and intersecting the right angle formed between sides h and R_g , forms an angle θ' between line 204 and side h . In accordance with the laws of geometry, angle θ' is equal to the angle θ .

Hypotenuse R_s is divided by the point of intersection with the line 204 into portions x and y . The portion x is equal to the distance between the aircraft 201 and this point of intersection, and the portion y is equal to the distance between object 202 and the intersection of line 204 with hypotenuse R_s . It may be readily seen from the diagram of FIG. 2 that R_s is equal to the sum of x and y . In accordance with the laws of trigonometry, the portion x is equal to $h \sin \theta'$; and the portion y is equal to $R_g \cos \theta$. This relationship is expressed mathematically as follows:

$$R_s = h \sin \theta' + R_g \cos \theta$$

[1]

The value for angle θ ranges from a maximum of 90° when the radar is sweeping beneath the aircraft, to a minimum angle when the radar is sweeping ahead of the aircraft. At the beginning of the radar sweep, angle θ is equal to 90° , and R_s is thereby equal to h since $\sin 90^\circ$ equals 1 and $\cos 90^\circ$ is equal to zero. As time progresses angle θ becomes very small, and R_s is approximately equal to R_g since the Sine of a small angle is very small and the Cos of the same angle approaches 1. This relationship may be more fully understood from the diagram of FIG. 3 illustrating both the relationship of R_g and R_s in a plot of distance versus time.

With reference to FIG. 3, curve 301 represents the linear relationship of R_g for distance versus time, and curve 303 represents the relationship of R_s (as a function of R_g and h) versus time. The vertical axis represents distance and the horizontal axis represents time. In particular, time t_0 represents the beginning of R_g sweep time, and also corresponds to the beginning of a single sweep by the FSS within the radar image generator 106. As stated hereinabove, the FSS scans from a point on the transparency corresponding to the aircraft ground position to points on the transparency which would be ahead of and in the direction of the radar line of sight. The scanning operation of the FSS is linear; and, therefore, the plot of R_g for distance versus time is linear as represented by curve 301.

Curve 303 is a mathematical plot of equation [1] given hereinabove. Curve 303 intersects the vertical (or "distance") axis at a value equal to h , since the value for R_s is equal to h when angle θ is equal to 90° .

As time t increases, angle θ decreases, and the value for R_s approaches the value for R_g . This is represented in FIG. 3 by curve 303 approaching curve 301 asymptotically as time t increases. That is, the value for R_s approaches the value for R_g as angle θ approaches 0° . With reference to the prior art scan-converting device described hereinabove, curve 303 is representative of the shape of the deflecting signal employed in the scan-converting tube for deflecting the first electron beam.

The apparatus of the present invention performs the time base conversion by delaying discrete samples of the video signal from generator 106 for an amount of time proportional to the instantaneous difference between the values for R_s and R_g . In particular, the amount of this time delay for any given time t (measured on the horizontal time axis) is equal to the vertical difference between curve 303 and curve 301 multiplied by a constant proportionately K , wherein K is equal to 1 microsecond per 500 feet.

FIG. 4 illustrates the distance versus time relationship of R_s and R_g following a time base conversion by the apparatus of the present invention. The vertical axis represents distance and the horizontal axis represents time. Curve 401 illustrates ground range R_g , and curve 403 represents slant range R_s . Note that curve 403 is linear and represents the desired time base for displaying the radar simulator video on the CRT. Curve 401 represents the nonlinear variation of ground range following the conversion to a linear slant range. The point at which curve 401 intersects the horizontal (or "time") axis represents a time delay (t_n) proportional to altitude h . It is pointed out that the horizontal incremental difference between curves 403 and 401 represent the amount of time delay to be applied to each discrete sample of video from image generator 106. As will be shown in greater detail hereinbelow, the amount of time delay is effected by the use of a random access memory which stores data randomly at address locations proportional to the instantaneous horizontal difference between curves 403 and 401, and retrieves data from the RAM sequentially at an address location represented by curve 403.

Referring now to FIG. 5, the timing signals from circuit 116, and the video signals from both the image generator 106 and the time base converter 108 are illustrated with the timing relationship therebetween. Waveform 501 illustrates the linear R_g SWEEP signal indicative of the linear sweeping relationship of terrain objects and features from a transparency by the FSS. Waveform 503 illustrates the R_g SWEEP GATE signal, which signal is at a high level during the time that waveform 501 is linearly increasing in magnitude. Waveforms 501 and 503 both begin positive transitions at time t_1 , wherein t_1 represents the time at which a given simulated radar sweep begins.

Waveform 505 is the FSS SWEEP GATE signal, which signal is indicative of the operation of the FSS for the sweeping of a single line on the transparency. Waveform 505 begins a positive transition at time t_0 , wherein time t_0 represents the beginning of operation of the FSS for a given simulated radar sweep. The time interval between time t_0 and time t_1 is provided to allow sufficient time for the FSS to turn on and stabilize operation prior to the given simulated radar sweep beginning at time t_1 .

Waveform 507 represents the RADAR MAIN BANG signal, which signal is representative of the beginning of the simulated operation of the radar equipment dur-

ing the given radar sweep. The positive transition of the RADAR MAIN BANG signal is approximately 10 microseconds in time duration, and occurs approximately 60 microseconds after time t_1 . The 60 microsecond time delay is nominal, and prevents the two electron beams of the dual beam storage tube from simultaneously operating on the same point of the storage screen.

Waveform 509 represents slant range R_s as a function of R_g and h during a given radar sweep. The shape of this waveform between times t_1 and t_2 is identical to that of curve 303, and is employed in the prior art scan-conversion tube as the first electron beam deflection signal. As will be shown in greater detail hereinbelow, this waveform is employed in the apparatus of the present invention in conjunction with waveform 501 to generate instantaneous differences between slant range R_s and ground range R_g . The instantaneous differences between these two waveforms is used for providing a memory address for entering information into the memory.

Waveform 511 represents the radar video signal generated in generator 106 for a single sweep by the FSS, which signal is linear with respect to the ground range time base. Waveform 513 represents the video signal provided at the output of the digital time base converter 108, which signal has been converted to a video signal linear with respect to slant range time base. The video signal shown by waveform 513 between times t_3 and t_5 is the video signal shown by waveform 511 between times t_1 and t_4 which has been converted to a linear slant range time base. Time t_1 is analogous to the nadir point of the given radar scan as generated by the radar simulator. Time t_3 is analogous to the nadir point of the given radar sweep of the video signal to be displayed on the simulator CRT. It is also pointed out that the time delay between times t_1 and t_2 is the same as the time delay between times t_4 and t_5 . That is, the delay of the RADAR MAIN BANG signal affects a similar delay in the resultant video signal supplied from the time base converter 108. It is also pointed out that the time delay between times t_2 and t_3 is the same amount of time delay as represented by the horizontal distance between curves 403 and 401 along the time axis of the diagram of FIG. 4.

The time base converter 108 is shown in greater detail in FIG. 6. An input line 118 to an analog-to-digital driver 601 is connected to the output of the radar image generator 106 as shown in FIG. 1. The output from the A/D driver 601 is applied to the input of an analog-to-digital converter 603, throughout a line 605 is connected to the input of a read-only memory (RAM) 606 through a line 607. Another input to the converter 603 comes from the output 613 of a timing and synchronization circuit 608. The output of the RAM 606 is applied to the input of a digital-to-analog conversion circuit 631. In addition to the input from the A/D converter 603, the RAM 606 also receives an input from the output 629 of a memory address control circuit 625, whose input is supplied by a difference generating circuit 615 at output 627. The timing and synchronizing circuit 608 supplies signals to time and synchronize the RAM 606, the D/A converter 631, the difference generating circuit 615 and the memory address control circuit 625 also, all through a line 613. The difference generating circuit 615 receives interface input signals on lines 617, 619, 621, and 623 from image gen-

erator 108. Line 617 has the ground range (R_g) sweep signals (waveform 501) applied to it; the negative slant range ($-R_s$) sweep signal (waveform 509) is applied to line 619; and two image controlling signals are applied to the lines 621 and 623 for determining the operating range of the simulated radar. The lines 621 and 623 are also connected as inputs to the memory address control circuit 625.

The signal applied to the line 621 selects the 80 mile range (for example) of the radar set to be displayed, and the signal on the line 623 selects the 200 mile range. When neither of the lines 621 and 623 carries a signal, the system selects the 40 mile range.

Binary numbers retrieved from RAM 606, which numbers are a binary manifestation of the video signal linear with respect to slant range time base, are supplied to the input of a digital-to-analog conversion circuit 631 via lines 633. Circuit 631 is controlled by one of the timing signals on lines 613. The output of circuit 631 is an analog signal representative of video which has been converted to a linear slant range time base, and is supplied to the frequency converter 110 (FIG. 1) via line 637. The signal supplied at the output of converter 110 is a high frequency carrier signal which has been modulated by the video signal supplied on line 637. The output signal from converter 110 is supplied to the I.F. strip of the radar receiver 112.

In operation, the video signal which is linear with respect to ground range time base, and is supplied at the output of radar image generator 106 is supplied to the input of driver 601 via line 118. A plurality of analog signal comparator circuits are employed within driver 601 to separate the video signal on line 118 into four discrete bands of analog signals. These four bands of analog signals are supplied to converter 603 via lines 605. Converter 603 converts the four bands of analog signals supplied thereto into a binary number having a value proportional to the magnitude of the input analog signals. Additionally, converter 603 has provisions for scaling the binary numbers into weighted values in accordance with fine, medium, and coarse transitions of the input video signal on line 118.

Control and synchronization of the operation of the circuitry of the time base converter 108 is supplied by the circuit 608. A plurality of clock timing signals are generated by the circuit 608 to control individual steps of the time base conversion during a given sweep of the FSS. The timing signals supplied on lines 609 (R_g SWEEP GATE) and 611 (FSS SWEEP GATE) are employed in circuit 608 to generate additional control signals to effect the synchronization of operation of time base converter 108 to the remaining circuitry of the radar simulator. These signals will be explained in greater detail hereinbelow.

Generator 615 generates the instantaneous algebraic sum of the varying values of the $-R_s$ SWEEP signal and the R_g SWEEP signal supplied on lines 617 and 619. A binary number is provided at the output of circuit 615 which is indicative of this instantaneous sum between $-R_s$ and R_g . The binary number representative of the instantaneous sum between $-R_s$ and R_g is supplied to circuit 625 via lines 627.

It is the function of circuit 625 to supply an address to RAM 606 via lines 629 during a first time interval for entering data into the memory via lines 607, and for retrieving data from the RAM 606 on lines 633 during a second time interval. The binary numbers retrieved

from the RAM 606 are supplied to conversion circuit 631 via lines 633.

Conversion circuit 631 converts the binary numbers retrieved from the RAM into an analog signal representative of the video signal which is linear with respect to slant range time base. This signal is supplied on line 637 to frequency converter 110.

In summary, the operation of the time base converter 108 is to sample the video signals supplied on line 118 periodically; store this sample of the video signal into the RAM 606 at an address proportional to the instantaneous difference between $-R_s$ and R_o ; to sequentially retrieve the stored information from the RAM 606; and, convert the information retrieved from the RAM 606 back into an analog signal representative of a video signal linear with respect to slant range time base.

Referring now to FIG. 7, the clock and timing circuit 608 is illustrated in block diagram form. A 36 Megahertz oscillator 701 supplies an oscillatory voltage to a clock generator 703 via a line 705. Oscillator 701 may comprise, for example, a conventional free-running multivibrator. Clock generator 703 uses the clock pulses supplied on line 705 to produce eight subclock signals which will be referred to hereinafter as 01 through 08. Subclock signals 01 through 08 are employed for timing other circuitry of this invention, as will be explained in greater detail hereinbelow.

The 05 and the 08 subclock signals are supplied as inputs to a gating network 707. The R_o SWEEP GATE signal generated in timing circuit 116, and represented by waveform 503, is supplied as an input to gating network 707 via line 609. Also, the FSS SWEEP GATE signal supplied from timing circuit 116, and represented by waveform 505, is supplied as an input to gating network 707 via line 611. The signals provided at the output of gating network 707 are defined as follows: an inversion of the 05 signal on line 713; a BUFFERED R_o SWEEP GATE signal on line 715; a CLOCKED R_o SWEEP GATE signal on line 716; a $(R_s - R_o)$ GENERATOR REGISTER ENABLE signal on line 717; a MASTER ZERO signal on line 719; a BUFFERED FSS SWEEP GATE signal on line 721; a MASTER CLEAR signal on line 723; and, an ALTITUDE h DATA TRANSFER signal on line 725. The generation and detailed explanation of these signals will be described in greater detail hereinbelow. Also, the operation of the clock and timing circuit 608 will be explained in greater detail following a description of the circuitry comprising generator 703 and network 707.

Referring now to FIG. 8, clock generator 703 is illustrated in greater detail. The 36 Megahertz oscillatory signal from oscillator 701 is supplied to the toggle input of a binary counter stage 801. The oscillatory signal at the output of counter stage 801 is an 18 Megahertz oscillatory signal, which is supplied to the count input of a 3-bit counter 803. Counter 803 may comprise any conventional binary counter however, it is preferred that counter 803 be a closed-ring counter. That is, when the contents of the counter 803 reaches the counter capacity, it resets to a count of zero. The signals at the output of counter 803 represent the binary value of the contents of the counter. The signal supplied on an output line 805 represents a binary count of 2^0 ; the signal supplied on an output line 807 represents a binary count of 2^1 ; and, the signal supplied on an output line 809 is representative of a binary count

of 2^2 . Line 805 is connected to an inverting input of an AND gate 811; an inverting input of an AND gate 813; an inverting input of an AND gate 815; a direct input of AND gate 817; an inverting input of an AND gate 819; a direct input of an AND gate 821; an inverting input of an AND gate 823; and, a direct input of an AND gate 825. Line 807 is connected to an inverting input of the AND gate 811; a direct input of the AND gate 813; an inverting input of the AND gate 815; an inverting input of the AND gate 817; a direct input of the AND gate 819; a direct input of the AND gate 821; a direct input of the AND gate 823; and, a direct input of the AND gate 825. The line 809 is connected to an inverting input of the AND gate 811; an inverting input of the AND gate 813; a direct input of the AND gate 815; a direct input of the AND gate 817; an inverting input of the AND gate 819; an inverting input of the AND gate 821; a direct input of the AND gate 823; and, a direct input of the AND gate 825. The output of the AND gate 811 is connected to an input of inverter 827, and the output of inverter 827 constitutes the 01 signal. The output of the AND gate 813 is connected to an input of an inverter 829, and the output of inverter 829 constitutes the 02 signal. The output of the AND gate 815 is connected to an input of inverter 831, and the output of inverter 831 constitutes the 03 signal. The output of the AND gate 817 is connected to an input of inverter 833, and the output of inverter 833 constitutes the 04 signal. The output of the AND gate 819 is connected to an input of inverter 835, and the output of inverter 835 constitutes the 05 signal. The output of the AND gate 821 is connected to an input of inverter 837, and the output of inverter 837 constitutes the 06 signal. The output of the AND gate 823 is connected to an input of inverter 839, and the output of inverter 839 constitutes the 07 signal. The output of the AND gate 825 is connected to an input of inverter 841, and the output of inverter 841 constitutes the 08 signal.

In operation, the 36 Megahertz oscillatory signal supplied at the input to binary counter stage 801 is effectively divided by two since only positive transitions of the signal supplied to the input of the stage will cause a change in state at the 1 output of the counter stage. The 18 Megahertz signal supplied to the count input of counter 803 increments the counter from a count of 000 to a count of 111, wherein the counter 803 is again reset to a count of 000. This operation continues in this manner independently without interruption from external circuitry. When the contents of counter 803 are 000, the AND gate 811 is enabled and a high-level signal is supplied to the input of inverter 827. The signal at the output of inverter 827 is at a low level when the signal from the output of the AND gate 811 is at a high level. Similarly, when the contents of counter 803 are 111, the AND gate 825 is enabled and the output of the inverter 841 goes to a low level. Each of the AND gates 813 through 823 are enabled in response to unique binary values within the counter 803. The relationship of the 01 through 08 subclock signals, and the oscillatory voltage supplied on line 705 may be more fully understood from the description of the timing diagram hereinbelow.

With reference to FIG. 9, waveform 901 represents the 36 Megahertz oscillatory signal supplied on line 705 from oscillator 701. Waveform 903 represents the 18 Megahertz signal provided at the output of counter

stage 801. Waveform 905 represents the 01 signal provided at the output of inverter 827; waveform 907 represents the 02 signal provided at the output of inverter 829; waveform 909 represents the 03 signal provided at the output of inverter 831; waveform 911 represents the 04 signal provided at the output of inverter 833; waveform 913 represents the 05 signal provided at the output of inverter 835; waveform 915 represents the 06 signal provided at the output of inverter 837; waveform 917 represents the 07 signal provided at the output of inverter 839; and, waveform 919 represents the 08 signal provided at the output of inverter 841. It is to be noted at this juncture of the description that the time between subsequent negative transitions on each of the subclock signals is equal to 222 nanoseconds.

Referring now to FIG. 10, gating network 707 is illustrated in greater detail. The 05 subclock signal from generator 703 is supplied to the input of inverter 1001. The output of inverter 1001 is connected to line 713. Line 713 is further connected to an input of a NAND gate 1003 and an input of a NAND gate 1005. Line 709, which supplies the R_0 SWEEP GATE signal, is connected to the noninverting input of an amplifier 1007. The output of amplifier 1007 is connected to the set input of a monostable multivibrator 1009 for one-shot, which has a time delay of 400 nanoseconds. The output of amplifier 1007 is also connected to line 715. The 1 output of multivibrator 1009 is connected to a second input of the NAND gate 1003; and the zero output of multivibrator 1009 is connected to a second input of the NAND gate 1005. The output of NAND gate 1003 is connected to the line 716, and is further connected to an input of a NAND gate 1011. The output of NAND gate 1005 is connected to an input of a NAND gate 1013. The output of NAND gate 1013 is connected to the other input of NAND gate 1011, and the output of NAND gate 1011 is connected to the other input of NAND gate 1013. The output of NAND gate 1013 also is connected to line 717, which is further connected to an input of a NAND gate 1015 and to an input of a NAND gate 1017.

The 08 subclock signal is connected to the input of an inverter 1019, and the output thereof is connected to an input of a NAND gate 1021. Line 711, which supplies the FSS SWEEP GATE signal, is connected to the noninverting input of an amplifier 1023. The output of amplifier 1023 is connected to the input of a 90 nanosecond time-delay circuit 1025, to line 721, and to the input of a monostable multivibrator 1027 which has a time delay of 60 microseconds. The output of time delay circuit 1025 is connected to an input of an inverter 1029, and the output thereof is connected to a second input of NAND gate 1021. The output of multivibrator 1027 is connected to a third input of NAND gate 1021, and is also connected to the input of a monostable multivibrator 1031 which has a time delay of 400 nanoseconds.

The output of NAND gate 1021 is connected to a first input of a NAND gate 1033. The output of NAND gate 1033 is connected to line 719, which is also connected to the second input of NAND gate 1015. The output of NAND gate 1015 is connected to the second input of the NAND gate 1033.

The output of multivibrator 1031 is connected to line 725, and is also connected to the second input of NAND gate 1017. The output of NAND gate 1017 is

connected to line 723 for supplying the MASTER CLEAR signal to external circuitry.

In operation, the 05 subclock signal is inverted by inverter 1001, and the signal appearing on line 713 is the inverse of the signal illustrated by waveform 913. The inverter 05 subclock signal is also supplied to inputs of the NAND gates 1003 and 1005. It is to be noted that the subclock signals are continuously running and, therefore, the inverted 05 subclock signal is repeatedly present on line 713 and at inputs of the NAND gates 1003 and 1005. However, the effect of the 05 subclock signal on the circuitry illustrated in FIG. 10 is dependent upon the state of multivibrator 1009.

A positive transition of the BUFFERED R_0 SWEEP GATE signal causes the multivibrator 1009 to change state for a period of time equal to 400 nanoseconds. That is, the multivibrator 1009 is in a reset state prior to the application of the positive transition of the BUFFERED R_0 SWEEP GATE signal, wherein the 1 output of the multivibrator is at a low level and the zero output is at a high level. Under these conditions the output of the NAND gate 1005 is periodically (at the rate of the 05 subclock signal) at a low level; and the output of the NAND gate 1003 is at a continuous high level. Likewise under these conditions the signal on lines 715 and 717 are both at a high level. The buffered SWEEP GATE signals are the constant level signals produced when the sweep ramp is applied to a saturating amplifier.

When the R_0 SWEEP GATE signal, which is supplied on line 709, makes a positive transition the multivibrator 1009 will change to a set state. That is, the one output of the multivibrator 1009 will change to a high level, and the zero output thereof will change to a low level. The output of the NAND gate 1003 will periodically (at the rate of the 05 subclock signal) change to a low level. The output of the NAND gate 1005 will change to a high level which will, in turn, cause the output of NAND gate 1013 to go to a low level. After a 400 nanosecond time delay, the multivibrator 1009 will return to a reset state; and the signals on lines 716 and 717 will return to high level states.

The positive transition of the BUFFERED FSS SWEEP GATE signal from amplifier 1023 actuates the time delay circuit 1025 and the multivibrator 1027. The output signal from the time delay circuit 1025 is a high level until 90 nanoseconds after the positive transition of the input signal is applied thereto, whereupon the output signal of circuit 1025 makes a negative transition. The negative transition at the output of circuit 1025 causes the output of inverter 1029 to go to a high level. The output of the multivibrator 1027 is normally at a high level and goes to a low-level state for a time duration of 60 microseconds following the application of the positive transition of the BUFFERED FSS SWEEP GATE signal at the input thereto. When the output of the multivibrator 1027 returns to a high-level state following the 60 microsecond time delay, the NAND gate 1021 is enabled to supply a low-level signal at the output thereof.

The low-level signal at the output of NAND gate 1021 will cause the output of NAND gate 1033 to go to a high level which will, in turn, cause the output of the NAND gate 1015 to go to a low level. The state of the NAND gates 1015 and 1033 will remain as described hereinabove until the signal on line 717 goes to

a low-level state, whereupon the signal on line 719 will return to a low-level state.

The low-level signal at the output of multivibrator 1027, which is 60 microseconds in time duration, is also applied to the input of the multivibrator 1031. However, multivibrator 1031 will not be activated until the output signal from multivibrator 1027 makes a positive transition following the 60 microsecond time delay. When this positive transition is made, the output of multivibrator 1031 will go to a low-level state for a time duration of 400 nanoseconds. The output of the multivibrator 1031, which is supplied on line 725 constitutes the ALTITUDE *h* DATA TRANSFER signal referred to hereinabove. It is pointed out at this juncture of the description that the output of the NAND gate 1017 will be at a low-level state during the time at which the signal on lines 717 and 725 are at a high-level state. However, when the signal at the output of the multivibrator 1031 changes to a low-level state for the 400 nanosecond time period, the signal present at the output of the NAND gate 1017 on line 723 will change to a high-level state. The operation and time relationship of the circuitry illustrated in FIG. 10 and described hereinabove will be more fully understood from a description of the timing diagram illustrated in FIG. 11.

Referring now to FIG. 11, waveform 1101 represents the BUFFERED R_s SWEEP GATE signal supplied on line 715 from the output of the amplifier 1007. The positive transition on waveform 1101 occurs at the beginning of the R_s SWEEP GATE signal as represented by waveform 503 hereinabove. Waveform 1103 represents the state of the 1 output of the multivibrator 1009. The positive transition of waveform 1103 occurs simultaneously with the positive transition of waveform 1101 and is 400 nanoseconds in time duration. Waveform 1105 represents the state of the zero output of the multivibrator 1009. The positive transition of waveform 1105 occurs simultaneously with the negative transition of waveform 1101 and is 400 nanoseconds in time duration. Waveform 1107 represents the inverter 05 subclock signal provided at the output of the inverter 1001. The time delays between consecutive positive transitions of waveform 1107 is equal to 222 nanoseconds. Waveform 1109 represents the $(R_s - R_0)$ GENERATOR REGISTER ENABLE signal provided at the output of the NAND gate 1013 on line 717. The negative transition of waveform 1109 occurs at a time when waveform 1105 is in a negative state and when a positive transition is made by waveform 1107. The time duration of the negative transition of waveform 1109 may vary from a minimum of 222 nanoseconds to a maximum of 444 nanoseconds. Waveform 1111 represents the CLOCKED R_0 SWEET GATE signal which is supplied on line 716. The two negative transitions are effected by the inverted 05 subclock signals which pass through the NAND gate 1003 during the time at which the "one" output of the multivibrator 1009 is at a high-level state.

Waveform 1113 represents the MASTER CLEAR signal which is supplied on line 723. The first positive transition 1113a of waveform 1113 occurs during the time at which waveform 1109 is at a low-level state and varies in time duration from 222 nanoseconds to 444 nanoseconds. The second positive transition 1113b of waveform 1113 occurs when the output of the multivibrator 1031 is at a low-level state and is 400 nanoseconds in time duration. Waveform 1115 represents the

MASTER ZERO signal supplied on line 719. The negative transition occurs at the same time waveform 1109 makes a negative transition as a result of the signal supplied on line 717 causing the NAND gate 1015 and 1033 to change state. The positive transition of waveform 1115 occurs when the output of the NAND gate 1021 causes the NAND gates 1015 and 1033 again to change state.

Waveform 1117 represents the BUFFERED FSS SWEEP GATE signal supplied on line 721 from the output of the amplifier 1023. The positive and negative transitions of waveform 1117 occur at the same time as the respective positive and negative transitions of the FSS SWEEP GATE signal as represented by waveform 503 hereinabove. Waveform 1119 represents the signal appearing at the output of inverter 1029 in response to the BUFFERED FSS SWEEP GATE signal delayed for 90 nanoseconds by time delay circuit 1025. The negative transition of waveform 1119 occurs 90 nanoseconds after the positive transition of waveform 1117. The positive transition of waveform 1119 occurs 90 nanoseconds after the negative transition of waveform 1117. Waveform 1121 represents the 08 subclock signal which has been inverted by the inverter 1019. Waveform 1123 represents the signal appearing at the output of multivibrator 1027, wherein the time duration of the negative portion of this waveform is 60 microseconds. Waveform 1121 represents the signal appearing at the first input of the NAND gate 1021; waveform 1119 represents the signal appearing at the second input of the NAND gate, 1021; and waveform 1123 represents the signal at the third input of the NAND gate 1021. Therefore, when the signals represented by waveforms 1119, 1121, and 1123 are all simultaneously at a high-level state, the output of the NAND gate 1021 will change to a low-level state which will, in turn, change the state of the NAND gates 1015 and 1023 to change the signal appearing on line 719. Waveform 1125 represents the ALTITUDE *h* DATA TRANSFER signal which is supplied on line 725 from the output of multivibrator 103. The negative transition of waveform 1125 occurs at the time waveform 1123 makes a positive transition following the 60 microsecond time delay. The time duration of the negative transition of waveform 1125 is 400 nanoseconds.

Referring not to FIG. 12, the analog-to-digital driver 601 is illustrated in greater detail. Line 118, from radar image generator 106, is connected to one terminal of each of resistors 1201, 1203, 1205, and 1207. The second terminal of resistor 1201 is connected to the inverting input of an amplifier 1209. The noninverting input of amplifier 1209 is connected to ground potential. The output of the amplifier 1209 is connected to line 605a, which is one of the output lines 605 from driver 601. Feedback resistor 1211 is connected across amplifier 1209, and in particular one terminal of resistor 1211 is connected to the inverting input of the amplifier and the second terminal thereof is connected to the output of the amplifier.

The second terminal of resistor 1203 is connected to the inverting input of an amplifier 1213, the noninverting input of which is connected to ground potential. The output of the amplifier 1213 is connected to line 605b. One terminal of a feedback resistor 1215 is connected to the inverting input of the amplifier 1213, and the second terminal of the resistor 1215 is connected to the output of the amplifier 1213. One terminal of a

biasing resistor 1217 is connected to the inverting input of the amplifier 1213, and the second terminal of biasing resistor is connected to a source of positive voltage.

The second terminal of the resistor 1205 is connected to the inverting input of an amplifier 1219. The noninverting input of the amplifier 1219 is connected to ground potential. The output of the amplifier 1219 is connected to line 605c. One terminal of a feedback resistor 1221 is connected to the inverting input of the amplifier 1219, and the second terminal of the feedback resistor is connected to the output of the amplifier 1219. One terminal of a biasing resistor 1223 is connected to the inverting input of the amplifier 1219, and the second terminal of the biasing resistor is connected to a source of positive voltage.

The second terminal of the resistor 1207 is connected to the inverting input of an amplifier 1225. The noninverting input of the amplifier 1225 is connected to ground potential. The output of amplifier 1225 is connected to line 605d. One terminal of a feedback resistor 1227 is connected to the inverting input of the amplifier 1225, and the second terminal of the feedback resistor is connected to the output of the amplifier 1225. One terminal of a biasing resistor 1229 is connected to the inverting input of the amplifier 1225, and the second terminal of the biasing resistor is connected to a source of positive voltage.

As stated hereinabove, it is the function of the driver circuit 601 to divide the input video signal supplied on line 118 into four separate bands of analog signals. Hereinafter, the four bands of analog signals will be referred to as BAND 1 VIDEO, BAND 2 VIDEO, BAND 3 VIDEO, and BAND 4 VIDEO. The video signal supplied on line 118 may have, for example, a range of voltage values from 0 volts to -10 volts, and the range of voltage values for each band of analog signals would be, say, from 0 volts to +4 volts. The division of the video signal into the four separate bands of analog signals is effected by not biasing BAND 1 VIDEO amplifier 1209, and by biasing each of the remaining amplifiers 1213, 1219, and 1225 at different voltage level points. In accordance with a preferred embodiment no biasing resistor is employed for the BAND 1 VIDEO amplifier 1209 since the initial operating point for this amplifier is 0 volts. The remaining three amplifiers are biased at selected voltage level points of the input video signal. In particular, BAND 2 VIDEO amplifier 1213 is biased to operate at an initial input video signal value of -1.6 volts; BAND 3 VIDEO amplifier 1219 is biased to operate at an initial input video signal value of -3.2 volts; and, BAND 4 VIDEO amplifier 1225 is biased to operate at an initial input video signal value of -4.8 volts.

The amplifiers 1209, 1213, and 1219 are each set for a gain of 2.5 by the use of feedback resistors 1211, 1215, and 1221, respectively. The gain of amplifier 1225 is set at 0.77 by the use of feedback resistor 1227.

In the operation of the circuit with the values given as examples, as the input video signal decreases in value from 0 volts to a negative value of -1.6 volts the amplifier 1209 supplies to BAND 1 VIDEO signal on line 605a ranging from 0 volts to +4 volts. As the input video signal decreases further in value, the output of amplifier 1209 remains at +4 volts. As the video signal further decreases in value from -1.6 volts to -3.2 volts, the amplifier 1213 supplies the BAND 2 VIDEO signal on line 605b ranging from +0.5 volts to +4 volts. As the

video signal further decreases in value from the output of both amplifiers 1209 and 1213 remain at +4 volts. A further decrease in the voltage value of the input video signal from -3.2 volts to -4.8 volts causes amplifier 1219 to supply the BAND 3 VIDEO signal on line 605c range from +0.5 volts to +4 volts. As the magnitude of the input video signal further decreases, the output of amplifiers 1209, 1312, and 1219 remain at +4 volts each. Further decreases in the magnitude of the input video signal from -4.8 volts to -10 volts will cause amplifier 1225 to supply the BAND 4 VIDEO signal on line 605d ranging from +0.308 volts to +4 volts.

The operation as described hereinabove may be more fully understood from the table of voltage values hereinbelow.

TABLE 1

LEVEL	INPUT VIDEO	BAND 1 VIDEO	BAND 2 VIDEO	BAND 3 VIDEO	BAND 4 VIDEO
0	OV	OV	OV	OV	OV
1	-0.2	+0.5	.	.	.
2	-0.4	+1.0	.	.	.
3	-0.6	+1.5	.	.	.
4	-0.8	+2.0	.	.	.
5	-1.0	+2.5	.	.	.
6	-1.2	+3.0	.	.	.
7	-1.4	+3.5	.	.	.
8	-1.6	+4.0	OV	OV	OV
9	-1.8	+4.0	+0.5	OV	OV
10	-2.0	.	+1.0	.	.
11	-2.2	.	+1.5	.	.
12	-2.4	.	+2.0	.	.
13	-2.6	.	+2.5	.	.
14	-2.8	.	+3.0	.	.
15	-3.0	.	+3.5	.	.
16	-3.2	+4.0	+4.0	OV	OV
17	-3.4	+4.0	+4.0	+0.5	OV
18	-3.6	.	.	+1.0	.
19	-3.8	.	.	+1.5	.
20	-4.0	.	.	+2.0	.
21	-4.2	.	.	+2.5	.
22	-4.4	.	.	+3.0	.
23	-4.6	.	.	+3.5	.
24	-4.8	+4.0	+4.0	+4.0	OV
25	-5.2	+4.0	+4.0	+4.0	+0.308
26	-5.6	.	.	.	+0.616
27	-6.0	.	.	.	+0.924
28	-6.4	.	.	.	+1.23
29	-7.6	.	.	.	+2.16
30	-8.8	.	.	.	+3.08
31	-10.0	+4.0	+4.0	+4.0	+4.00

The analog-to-digital converter 603 is shown in greater detail in block form in FIG. 13. In addition, FIGS. 14 and 15 illustrate in greater detail portion of the analog comparator circuit and digital priority encoder which comprise FIG. 13. FIG. 13 comprises a first group of circuits called the analog comparator circuits 1301, 1302, 1303, and 1304, and a second group of circuits called "digital priority encoders" 1311, 1313, 1316, and 1318. The output 605a from the analog-to-digital drivers shown in FIG. 12 is applied as an input to the analog comparator circuit 1301, a second output 605b from the analog to digital drivers of FIG. 12 is applied as an input to the analog comparator circuit 1302, and similarly the output 605c is applied to analog comparator circuit 1303 and 605d is applied to the input of analog comparator circuit 1304 circuit 1304 is provided on line 1306 with a noise filter capacitor 1307 and a weighting resistor 1305. In addition, a clock pulse is applied to a second input of each of these analog comparator circuits 1301-1304. The particular clock pulse is 06 subclock pulse from the output of the clock generator shown in detail in FIG. 8. Each of the

comparator circuits 1301, 1302, 1303, and 1304 has eight output lines. Four digital priority encoders 1311, 1313, 1316, and 1318 are provided. Seven of the output lines from the analog circuit 1301 are applied as inputs to the encoder circuit 1311; seven of the output lines from the comparator circuit 1302 are applied as inputs to the encoder circuit 1313; seven of the output lines from the comparator circuit 1303 are applied as inputs to the digital priority encoder 1316; and the eight output lines from the comparator circuit 1304 are applied as inputs to the encoder circuit 1318. In addition, the eighth output of the circuit 1301 is applied as an input to the encoder 1313; the eighth output from the comparator circuit 1302 is applied as an input to the encoder 1316 and the eighth output from the comparator circuit 1303 is applied as an input to the encoder 1318. The eighth output from the circuit 1302 is also provided as an output line 607a. Summarizing the above, a first group of four comparator circuits 1301-1304 are provided, and a group of four encoders 1311-1318 are also provided. The outputs from the circuit 1301 are applied to the circuit 1311, the output of the circuit 1302 are applied as inputs to the encoder 1313, the outputs of the comparator circuit 1303 are provided as inputs to the encoder 1316 and the outputs of the comparator 1304 are provided as inputs to the encoder 1318 with one input from the circuits 1301, 1302, and 1303 each going to the next higher numbered encoder circuit. An input 719, which is the MASTER ZERO from FIG. 10, is applied as an enable input to the encoder 1318. An output 1322 from the encoder 1318 is applied to the next lower numbered enable input of the encoder 1316. In a similar manner an output 1323 from the encoder 1316 is connected to the enable input of the encoder 1313, and an output 1324 from the encoder 1313 is applied to the enable input of the encoder 1311. Encoder 1311 has three outputs, and encoder 1316 has three additional outputs, whereas the two encoders 1313 and 1318 each have four additional outputs. The AND gate 1326 is connected to the uppermost output from each of the encoder circuits 1311, 1313, 1316, and 1318. The AND gate 1328 receives the next outputs from each of the four encoders, the AND gate 1330 receives next to the lowest output from the four encoders, and the AND gate 1338 receives the lowest output from the two encoders 1313 and 1318. The outputs from the gates 1326, 1328, 1330, and 1338 are the outputs from the analog-to-digital converter.

Before the operation of FIG. 13 can be understood readily some sort of the description of FIG. 14 should be encountered. FIG. 14 is a sample circuit of the analog comparator 1304. The device comprises a plurality of clocked flip-flops 1431, 1432, 1433, 1434, 1435, 1436, 1437, and 1438. These eight flip-flops comprise the output circuits which energize the eight output lines of each of the comparator circuits 1301-1304. Each flip-flop has its clock input connected to the line which supplies the clock pulses. This means that every time a 06 clock pulse is received, the flip-flops are all simultaneously clocked and the signals which are at their inputs are entered. The set inputs to the flip-flops 1431-1438 are each connected to the output of an individual differential amplifier 1410, 1411, 1412, 1413, 1414, 1415, 1416, and 1417. The output of the amplifier 1410 is connected to the set input of the flip-flop 1431; the output of the amplifier 1411 is connected to

the set input of the flip-flop 1432; the output of the amplifier 1412 is connected to the set input of the flip-flop 1433; and so forth. Each of the differential amplifiers 1410-1417 has two inputs: a sum input and a difference input. The sum inputs of all of the amplifiers 1410-1417 are connected to junction points on a voltage divider formed of a series connection of resistors 1420, 1421, 1422, 1423, 1424, 1425, 1426, 1427, and 1428. The free end of resistor 1420 at one end of the resistor string is connected to a source of positive potential and the free end of the resistor 1428 at the other end of the resistor string is connected to ground or to the negative terminal of the source of potential. The middle of the resistor string is connected to input 1306 between resistors 1424 and 1425. The current flowing through the resistors 1420-1428 from the positive source to ground provides a voltage at each junction point which is different from but related to the voltage at each of the other junction points. Thus, the amplifier 1410 has the highest positive voltage applied to its positive input and the amplifier 1417 has the lowest voltage applied to its positive input. The negative or difference inputs of the individual amplifiers 1410-1417 are connected through individual resistors 1401, 1402, 1403, 1404, 1405, 1406, 1407, and 1408 to a junction point which is connected to the input line 605. The resistor 1401 is connected between the line 605 and the negative input of the amplifier 1410; the resistor 1402 is connected between the line 605 and a negative input of the amplifier 1411; the resistor 1403 is connected between the line 605 and a negative input of the amplifier 1412; and so forth, with the resistor 1408 connecting the negative input to the amplifier 1417 with line 605.

In operation each of the amplifiers 1410-1417 is biased to a particular level by the voltage applied to its positive input from the resistor voltage divider. With no input signal applied to the line 605d all of the flip-flops have positive potentials applied to their set inputs by the outputs of the amplifiers 1410-1417. Thus, whenever 06 clock pulse arrives, the positive input signal is entered into the individual flip-flops 1431-1438. When a signal appears on the input line 605d, it is applied simultaneously to all of the amplifier negative inputs. The input signal is sufficiently high to drive at least some of the amplifiers to cut off so that they have low outputs. Since the lower amplifiers 1417, 1416, etc. are biased the least, they are the first to have their biases overcome and to be turned off. The first is 1417, the second is 1416, the third is 1415, etc. When the next 06 clock pulse appears, the low inputs are entered into those flip-flops (1438, 1437, 1436 etc.) which have low voltage applied to their inputs, and they are restored. The other flip-flops remain in the set state. Thus, the amplitude of the incoming signal on line 605d results in a number of flip-flops 1431-1438 having set outputs and a number of the flip-flops having restored outputs.

Referring again to FIG. 13, each of the comparator circuits 1301-1304 operates as described above. Each circuit receives its own input signal on the inputs lines 605a, 605b, 605c, and 605d, and each generates output signals on its eight output lines in accordance with the description of FIG. 14. Actually, in FIG. 13, the comparator circuit 1304 is shown with a second voltage applied to the voltage divider by line 1306. The top portion of the comparator circuit has one voltage applied to the potential divider and the bottom half has a second voltage so applied. This enables two different reso-

TABLE II—Continued

lutions of conversion to take place. The lower portion of the circuit 1304 provides a rough resolution and the upper portion provides a medium resolution. This means that the bias voltages on the amplifiers 1410, 1411, 1412, and 1413 are closer in value to each other than the bias voltages applied to the amplifiers 1414-1417. In FIG. 13, the comparator circuits 1301, 1302, and 1303 provide a fine resolution of the incoming signal. By providing 6 times as many amplifiers as each of the portions of comparator 1304, the resolution can be that much finer.

In FIG. 15, a sample priority encoder 1318 is shown in detail. The seven output lines 1320 from the comparator circuit 1304 are individually provided with their own individual inverters 1501, 1502, 1503, 1504, 1505, 1506, and 1507. The outputs from the inverters 1501-1507 are applied in various combinations to the several inputs of AND gates 1516, 1517, 1518, 1519, 1520, 1521, 1522, 1523, 1524, 1525, 1526, 1527, and the inputs 1320a-1320g to inverters 1501-1507 plus input 1319 are applied to NAND gate 1509 to produce outputs which are combined in NOR gates 1538, 1539, 1540, and in NAND gate 1513. The enable signal on line 719 is applied through the inverter 1511 to an input of all of the AND gates 1516-1527 NAND gate 1509, and NAND gate 1513. To provide suitable input signals to the gates to decode the inputs from the lines 1320, some of the input signals are applied in both true and false forms to separate inputs of the AND gates. To accomplish this, the outputs from the inverters 1502, 1503, 1504, and 1506 are applied, also, through additional inverters 1529, 1531, 1533, and 1535, respectively. The inverters 1501-1507 are to provide the gates with positive input signals. If other logic is used, the inverters may not be needed. The inverters 1529-1535 are to provide negative signals for the gates. Each of the gates 1516-1519 passes one of the top four inputs to gate 1538 when an enable signal is present on line 719. These four signals are passed through the NOR gate 1538 and provide the output on line 1346. The first two signals are also passed through the gates 1520 and 1521. The gates have combinations of the following signals, counting signal 1 as the signal on the top line 1320a, 2 as the second line from the top 1320b etc.

TABLE II

GATE	SIGNALS	INVERTER
1516	1	1501
1517	2	1502
1518	3	1503
1519	4	1504
1520	1	1501
1521	2	1502
1522	3	1503
	4	1504
	5	1505
1523	3	1503
	4	1504
	6	1506
1524	1	1501
1525	2	1502
	3	1503

GATE	SIGNALS	INVERTER
1526	2	1529
	4	1533
	5	1505
1527	2	1529
	4	1533
	6	1535
	7	1507

With an understanding of the construction and operation of the comparator circuits 1301-1304 and of the encoder circuits 1311-1318, the analog-to-digital converter shown in FIG. 13 can be more readily understood. As described above, the four input lines 605a, 605b, 605c, and 605d carry different levels of the same analog signal. The signal was separated into four level bands in the analog-to-digital drivers shown in FIG. 12. These four levels are the signals applied to the inputs 605a-605d. The analog signals are applied to the inputs of the comparator circuits 1301-1304 which then produce digital output signals. Each of the comparator circuits 1301-1304 produces signals on eight output lines, some of which are low in accordance with the analog input. When the analog input to any of the comparator circuits exceeds four volts, all of the outputs from that circuit are low. The eight outputs from each of the comparator circuits are applied to one of the four encoder circuits 1311-1318 which comprise a plurality of AND gates arranged to decode the eight input signals. One such arrangement for a decoder has been shown in FIG. 15 and has been described, but others may be developed. In any case, the combinations of signals on the eight input lines are decoded by the application of selected combinations of these signals to individual gates so that one output line from the decoder is energized. That output line represents the voltage of the analog signal applied to the drivers of FIG. 12. In addition, the lowest decoder 1318 applies an enable signal to the next higher decoder 1317, and so forth up the line. This means that unless a lower order decoder develops an output signal representing a maximum input, the next higher decoder will not be enabled. In this way, false outputs are prevented. Similarly, the highest order comparator circuit 1301 applies an output signal from its highest position to the lowest input of the next lower order comparator in the manner of a carry, so that all of the outputs may be taken into account. The final output signal from the analog to digital converter shown in FIG. 13 is a digital word comprising five digits appearing on lines 607a, 607b, 607c, 607d, and 607e, with the line 607e representing 2⁰, line 607d representing 2¹, and so forth to line 607a representing 2⁴. Table III illustrates the original analog video voltage; the manner in which the original voltage is sampled at a fixed resolution through the top 24 levels and how the resolution changes in band 4; the four bands produced by the drivers 1219, 1209, 1225, and 1213; and the binary code produced by the encoder circuits and appearing on output lines 607a, 607b, 607c, 607d, and 607e. The values of the voltages are, of course only exemplary.

TABLE III

Level	Analog Video Voltage	Output From Drivers	Binary Video From Encoders				
			607a	607b	607c	607d	607e
0	0	0	1	1	1	1	1
1	-0.2	+0.5	1	1	1	1	0
2	-0.4	+1.0	1	1	1	0	1

TABLE III - Continued

Level	Analog Video Voltage	Output From Drivers	Binary Video From Encoders					
			607a	607b	607c	607d	607e	
3	-0.6	Band 1 Offset 0V	+1.5	1	1	1	0	0
4	-0.8		+2.0	1	1	0	1	1
5	-1.0		+2.5	1	1	0	1	0
6	-1.2		+3.0	1	1	0	0	1
7	-1.4		+3.5	1	1	0	0	0
8	-1.6	Band 2 Offset 1.6V	+4.0	1	0	1	1	1
9	-1.8		+0.5	1	0	1	1	0
10	-2.0		+1.0	1	0	1	0	1
11	-2.2		+1.5	1	0	1	0	0
12	-2.4		+2.0	1	0	0	1	1
13	-2.6	Band 3 Offset 3.2V	+2.5	1	0	0	1	0
14	-2.8		+3.0	1	0	0	0	1
15	-3.0		+3.5	1	0	0	0	0
16	-3.2		+4.0	0	1	1	1	1
17	-3.4		+0.5	0	1	1	1	0
18	-3.6	Band 4 Offset 4.8V	+1.0	0	1	1	0	1
19	-3.8		+1.5	0	1	1	0	0
20	-4.0		+2.0	0	1	0	1	1
21	-4.2		+2.5	0	1	0	1	0
22	-4.4		+3.0	0	1	0	0	1
23	-4.6		+3.5	0	1	0	0	0
24	-4.8		+4.0	0	0	1	1	1
25	-5.2		+0.308	0	0	1	1	0
26	-5.6		+0.616	0	0	1	0	1
27	-6.0		+0.924	0	0	1	0	0
28	-6.4		+1.23	0	0	0	1	1
29	-7.6		+2.16	0	0	0	1	0
30	-8.8		+3.08	0	0	0	0	1
31	-10.0		+4.00	0	0	0	0	0

Referring now to FIG. 16, the ($R_s - R_g$) generator 615 is illustrated in greater detail. Line 621, which supplies the 80 mile range selection signal, is connected to a first control input of a relay network 1601. Line 623, which supplies the 200 mile range selection signal, is connected to a second control input of the relay network 1601. Relay network 1601 may comprise conventional well-known electromagnetic relays with the associated operating, normally-open, and normally-closed contacts, or electronic relays, as desired.

Line 617, which supplies the R_g SWEEP signal (waveform 501), is connected to a first terminal of a resistor 1603. The second terminal of the resistor 1603 is connected to the operating terminal of the relay network 1601, and to the inverting input of an amplifier 1605. Line 619, which supplies the R_s SWEEP signal (waveform 509), is connected to the first terminal of a resistor 1607. The second terminal of the resistor 1607 is connected to the operating terminal of the relay network 1601, and to the inverting input of the amplifier 1605. The non-inverting input terminal of the amplifier 1605 is connected to ground potential. A first output of the relay network 1601 is connected to a first terminal of a resistor 1609; a second output terminal from the relay network is connected to a first terminal of a resistor 1611; and, a third output from the relay network is connected to a first terminal of a resistor 1613. The second terminal of resistors 1609, 1611, and 1613 are connected together and to the output of the amplifier 1605 which is also connected to the inverting input of an amplifier 1615. The non-inverting input of the amplifier 1615 is connected to ground potential. The output of the amplifier 1615 is connected to a summing junction 1616 which is connected to the output of a digital-to-analog converter 1617 and to the inverting input of an amplifier 1619. The non-inverting terminal of the amplifier 1619 is connected to ground potential.

The output of the amplifier 1619 is connected to the inverting input terminal of a dual-output comparator 1621. The non-inverting input terminal of the comparator 1621 is connected to ground potential, and its inverting output terminal is connected to a counter control circuit 1623 via a line 1625. The non-inverting out-

put terminal of the comparator 1621 is connected via a line 1627 to the circuit 1623 which has several inputs. The BUFFERED R_g SWEEP GATE signal, as illustrated by waveform 1101, is supplied to the circuit 1623 via a line 715. The 02 sub-clock signal, which has been delayed in time and is hereinafter designated 02A sub-clock signal, is supplied to circuit 1623 via a line 1631. The derivation of the 02A sub-clock signal will be explained in greater detail hereinbelow. The BUFFERED FSS SWEEP GATE signal, as illustrated by waveform 1117, is supplied to circuit 1623 via a line 721. The 05 sub-clock signal is supplied to circuit 1623 via line 1635. The output signals from circuit 1623 are supplied to an up/down counter 1637 via a first portion of lines 1639, and the status of the counter 1637 is supplied as an input to circuit 1623 via a second portion of the lines 1639.

The contents of the counter 1637 are supplied to the digital-to-analog converter 1617 via the lines 627. The output from counter 1637 constitutes $R_s - R_g$ generator circuit 615. The lines 627 are also supplied to the data input of an initialization register 1641, and the output from the register 1641 is supplied to the inputs of the counter 1637 via lines 1643. The ($R_s - R_g$) GENERATOR REGISTER ENABLE signal, as illustrated by waveform 1109, is supplied to the control input of the register 1641 via the line 717. Register 1641 stores the previous $R_s - R_g$ value for initializing up/down counter 1637 and eliminating the slew-up period which would normally be required by counter 1637.

It is the function of the ($R_s - R_g$) generator circuit 615 to derive a binary number representative of the instantaneous difference between the R_s SWEEP signal (waveform 509) and the R_g SWEEP signal (waveform 501). The value of the feedback resistance for the amplifier 1605 is determined by the relay network 1601 as a function of the state of the range selection signals supplied on lines 621 and 623. Register 1609 is selected when a signal is supplied on line 621; resistor 1611 is selected when a signal is supplied on line 623; and resistor 1613 is selected when no signal is present on either line 621 or 623. The algebraic sum of the R_s SWEEP signal and the R_g SWEEP signal is provided at

the output of the amplifier 1605. Amplifier 1615 inverts the signal from amplifier 1605. The output of the amplifier 1615 is summed with the output of converter 1617 at summing junction 1616, and this summed signal is supplied to the inverting input of the amplifier 1619. It is the function of the digital-to-analog converter 1617 to convert the binary number supplied on lines 627 into an analog signal which is supplied to the summing junction 1616 as a feedback voltage.

The amplifier 1619 generates an error signal proportional to the magnitude of the summed signals at the junction 1616, which error signal activates the comparator 1621. At the same time the output signals from the dual-output comparator 1621 select the direction of count for counter 1637 via lines 1625 and 1627, circuit 1623, and lines 1639. When the error signal at the output of the amplifier 1619 is of a first polarity, counter 1637 is incremented; and, when the error signal at the output of the amplifier 1619 is of a second polarity, counter 1637 is decremented. When the value content within the counter 1637 is approximately equal to the difference between R_s and R_o , the error signal supplied to junction 1616 is small; and, when the amplitude of the error signal at the output of the amplifier 1619 is sufficiently small, the incrementing/decrementing clock pulses to the counter 1637 are inhibited. During this condition, the contents of the counter 1637 is the binary equivalent of the analog voltage representing $(R_s - R_o)$. The counter control circuit 1623 will be explained in greater detail hereinbelow.

Referring now to FIG. 17, the counter control circuit 1623 is illustrated in greater detail. Line 715, which supplies the BUFFERED R_o SWEEP GATE signal, is connected to the clear input of a J-K flip-flop 1701 and to the input of an inverter 1703. Line 1627, which supplies the positive output from the comparator 1621, is connected to the K input of the flip-flop 1701, and to the J input of a J-K flip-flop 1705. The line 1635, which supplies the 05 sub-clock signal to circuit 1623, is connected to the clock input of the flip-flops 1701 and 1705. The line 1625, which supplies the negative output from the comparator 1621, is connected to the J input of the flip-flop 1701, and the K input of the flip-flop 1705.

The zero or restore output of the flip-flop 1701 is supplied on line 1639a to counter 1637 to constitute the up/down selection for the counter 1637. The zero output from the flip-flop 1705 is connected to one of two inputs of a NAND gate 1709, the second input to which is the output of the inverter 1703. The output of the NAND gate 1709 is connected to one of four inputs of a NAND gate 1711. The line 1631, which supplies the 02A sub-clock signal, is connected to the second input of the NAND gate 1711.

The line 721, which supplies the BUFFERED FSS SWEEP GATE signal, is connected to the input of a monostable or one-shot multivibrator 1712 having a time delay set at 50 microseconds. Line 721 is also connected to one of two inputs of a NAND gate 1713. The output of the multivibrator 1712 is connected to the second input of the NAND gate 1713 whose output is connected to the input of an inverter 1715. The output of the inverter 1715 is connected to the third input of the NAND gate 1711.

Lines 1639b and 1639c are connected to two of three inputs of a NAND gate 1717. In addition, line 1639c is connected to one of two inputs of a NAND gate 1719.

Line 1639d is connected to the second input of the NAND gate 1719, and to the third input of the NAND gate 1717. The output of the NAND gate 1719 is supplied on line 1639e to the counter 1637 of FIG. 16, while the output of the NAND gate 1717 is connected to the fourth input of the NAND gate 1711. The output of the NAND gate 1711 is supplied on line 1639f to the counter 1637. Lines 1639b, 1639c, and 1639d supply signals indicative of the status of the carry outputs of the counter 1637 to the circuit 1623. Line 1639e supplies a counter enable signal to the counter 1637, and line 1639f supplies the clock signal to the counter 1637.

The counter control circuit 1623 controls the operation of the counter 1637 in response to the system timing signals, the sub-clock signals, the amplitude of the feedback voltage at the summing junction 1616, and the status of the counter itself. When the output of the comparator 1621 is positive, a positive potential is applied to the K input of the flip-flop 1701 and to the J input of the flip-flop 1705. At the next 05 sub-clock signal, the flip-flop 1701 is driven into its set state and the flip-flop 1705 is driven into its restore state. The output of the flip-flop 1701 is low and the signal applied by line 1639a to the counter 1637 causes it to decrement. At the same time the output from the counter 1705 is high and this supplies a high signal to the input of gate 1709. During this time the R_o GATE signal is present as a high signal which is inverted by the inverter 1703 to provide the second input of the gate 1709 with a low signal. This insures that the output from the gate 1709 is high only when the R_o signal is present. In this manner, the output from the gate 1709 applies a high conditioning signal at the input of the gate 1711 only so long as the R_o GATE signal is present. The lines 1639b, 1639c, and 1639d are supplied with carries from the counter 1637. Another conditioning signal on the gate 1711 comes from the output of the gate 1717. So long as any of the three carries on the lines 1639b, c, and d are low, the output of the gate 1717 will be high. The FSS GATE signal is applied directly to one input of gate 1713 and also to the input of the multivibrator 1712 to drive that circuit into its unstable state. During the 50 microseconds that the multivibrator 1712 is in its unstable state, the gate 1713 has two high signals applied to its input and it generates a low output signal. This low signal is inverted to a high signal by the inverter 1715 to provide a third conditioning signal to the gate 1711. The fourth conditioning signal to the gate 1711 is a 02A sub-clock signal. When all of the other three inputs to the gate 1711 are high, it passes the 02A sub-clock signal to the counter 1637 to be counted. It should be noted that two clock signals are used. The 05 sub-clock signal is used to enter the polarity of the comparator 1621 into the flip-flop 1705. The following 02A sub-clock signal passes through the gate 1711 to actually clock the counter. This insures that the clock pulse which is applied to the counter is not interrupted at an inconvenient time.

Referring now to FIG. 18, the memory address control circuit 625 is shown in greater detail with connections to the RAM 606. The portion of the block diagram enclosed within the dashed line comprises the memory address control circuit 625. Binary numbers generated in the analog-to-digital converter 603, which binary numbers are indicative of the magnitude of samples of the video input signal, are supplied to the DATA

input of the RAM on lines 607. The address to the RAM 606 is supplied on lines 629A from a read-write multiplexer 1801 contained within circuit 625, and the WRITE ENABLE signal for the RAM is supplied on line 629B.

A counter control circuit 1803 has several inputs which include the 80 mile range selection signal supplied on line 621, the 200 mile range selection signal supplied on line 623, the 02 sub-clock signal, and the 07 sub-clock signal which is also supplied to an input of control circuit 1805. A first output of the circuit 1803 is connected to the clock input of a write address counter 1807 via a line 1809 and a second output supplied the 02A sub-clock signal from the circuit 1803 via a line 1631. The line 723, which supplies the MASTER CLEAR signal, is connected to the reset input of the counter 1807, and the reset input of a read address counter 1811. The output of the counter 1807 is supplied to a first set of add inputs of a binary adder 1813 via lines 1815. The line 627, which supplies the binary number from the circuit 615, is connected to a second set of add inputs of the binary adder 1813. The sum outputs from the adder 1813 are supplied to a register 1817 via lines 1819. The output of the register 1817 is supplied to a first set of inputs of the multiplexer 1801 via lines 1821. The 06 sub-clock signal is supplied to the clock input of the register 1817.

The line 626, which supplies the RADAR MAIN BANG signal, is connected to an input of a read enable circuit 1823. The 04 sub-clock signal is applied to an input of the circuit 1823. The line 716, which supplies the CLOCKED R_s SWEEP GATE signal, is connected to a third input of the circuit 1823, and to an input of the circuit 1803. The output of the circuit 1823 is connected to an enable input of the counter 1811 via a line 1826. The output of the counter 1811 is supplied to a second set of inputs of the multiplexer 1801 via lines 1824.

The 03 sub-clock signal is supplied to an input of the circuit 1805. The 01 sub-clock signal is supplied to one input, and line 719, which supplies the MASTER ZERO signal, is connected to a second input of the control circuit 1805. One of the three outputs of the control circuit 1805 is connected to line 629B. A second output of the circuit 1805 is connected to a control input of the multiplexer 1801 via a line 1825. The third output from the circuit 1805 is connected to the clock input of the counter 1811 via a line 1827. The structure and operation of the circuits 1803, 1805, and 1823 will be explained in greater detail hereinbelow.

The memory address control circuit 625 generates the address and the WRITE ENABLE signal for the memory 606. The address for entering data is supplied to the RAM 606 during a first time interval, and the address for retrieving data from the memory is supplied during a second time interval. The write address (address for the data entry operation) is generated by the write address counter 1807 and the adder 1813. More particularly, the write address counter is incremented by signals from the control circuit 1803, and the binary number produced in the $(R_s - R_d)$ generator circuit 615 (which binary number is supplied on lines 627) is added to the binary number supplied from the counter 1807 on lines 1815. The sum of the binary numbers supplied on lines 627 and lines 1815 is supplied to the register 1817 via the lines 1819. When the 06 sub-clock signal is applied to the clock input of the register 1817,

the sum of the binary numbers is supplied to the multiplexer 1801 via the lines 1821. A first state of the signal supplied to the multiplexer 1801 via the line 1825 will enable the multiplexer to supply the binary number on lines 1821 to the address input of the RAM 606 via lines 629A. At this time, the WRITE ENABLE signal is supplied to the RAM 606 via the line 629B which signal will cause the entry of the binary data supplied on the lines 607 at a location corresponding to the address supplied on lines 629A.

The read address (address for the data retrieval operation) is generated by the read address counter 1811. The counter 1811 is incremented, at a constant rate, by clock signals supplied from the read enable circuit 1823. Both the write address counter 1807 and the read address counter 1811 are reset by the MASTER CLEAR signal supplied on line 723.

At this juncture of the description, it is again pointed out that data is randomly entered into the RAM 606, and data is retrieved from the RAM sequentially. More particularly, the write address is generated by adding the binary number from the $(R_s - R_d)$ generator circuit 615 (which binary number is proportional to the instantaneous difference between the values for R_s and R_d) to a binary number from the counter 1807 (which binary number is increasing in value at a constant rate). The read address is generated by incrementing the counter 1811 at a constant rate.

Referring now to FIG. 19, the read/write multiplexer 1801 is illustrated in greater detail. Initially, it is pointed out that the multiplexer 1801 is any conventional multiplexing circuit as, for example, Model No. 9322 as manufactured by Fairchild Semiconductor of Mountain View, Calif.

The multiplexer 1801 is shown as comprising three individual multiplexer components for the preferred embodiment of the present invention for ease of description, but it could comprise any number of individual modules as desired. A single multiplexer circuit is illustrated in logic diagram form within dashed line 1901, and two additional identical multiplexer circuits are represented by blocks 1902 and 1903. Ground potential is connected to the input of an inverter 1905 of circuit 1901, and similar inverters in circuits 1902 and 1903. The output of the inverter 1905 is connected to one of three inputs of AND gates 1907 through 1914.

Line 1825, which supplies the control signal generated in circuit 1805, is connected to the input of an inverter 1915, and to similar inverters in circuits 1902 and 1903. The output of inverter 1915 is connected to an inverting input of an inverter 1917, and to the second input of the even numbered AND gates 1908, 1910, 1912, and 1914. The output of the inverter 1917 is connected to the second input of the odd numbered AND gates 1907, 1909, 1911, and 1913.

Line 1824A, from counter 1811, is connected to the third input of the AND gate 1907. Line 1821A, which is connected to the output of register 1817, is connected to the third input of the AND gate 1908. The line 1824B is connected to the third input of the AND gate 1909. The line 1821B is connected to the third input of the AND gate 1910. The line 1824C is connected to the third input of the AND gate 1911. The line 1821C is connected to the third input of the AND gate 1912. The line 1824D is connected to the third input of the AND gate 1913. Line 1821D is connected to the third input of the AND gate 1914. The line

1824E through 1824L, and the lines 1821E through 1821L are connected to inputs of the multiplexors 1902 and 1903 in the same manner as lines 1824A through 1824D and lines 1821A through 1821D, respectively.

The output of the AND gate 1907 is connected to one of two inputs of a NOR gate 1919, and the output of the AND gate 1908 is connected to the second input of the NOR gate 1919. The output of the NOR gate 1919 is connected to the inverting input of an inverter 1921, the output of which is connected to a line 629AA. The output of the AND gate 1909 is connected to one of two inputs of a NOR gate 1923, and output of the AND gate 1910 is connected to the second input of the NOR gate 1923. The output of the NOR gate 1923 is connected to the inverting input of an inverter 1925, the output of which is connected to a line 629AB. The output of the AND gate 1911 is connected to one of two inputs of a NOR gate 1927, and the output of the gate 1912 is connected to the second input of the gate 1927. The output of the NOR gate 1927 is connected to the inverting input of an inverter 1929, the output of which is connected to the line 629AC. The output of the AND gate 1913 is connected to one of two inputs of a NOR gate 1931, and the output of the AND gate 1914 is connected to the second input of the NOR gate 1931. The output of the NOR gate 1931 is connected to the inverting input of an inverter 1933, the output of which is connected to a line 629AD. The outputs from circuit 1902 are connected to lines 629AE through 629AH, and the outputs from the circuit 1903 are connected to lines 629AI through 629AK.

FIG. 19 illustrates a typical multiplexer circuit. The multiplexer 1801 of FIG. 18 is used to switch the outputs from the register 1817 and the address counter 1811 alternately to the RAM 606. The gates 1907 through 1914 are used to accomplish the switching. When a control signal from the control circuit 1805 is applied to the line 1825, it inhibits the even numbered gates and enables the odd numbered gates. This is accomplished by the transmission of the positive going control signal through the two inverters 1915 and 1917. With a positive going control signal, the output of the inverter 1915 is low and the output of the inverter 1917 is high. Since the input to the inverter 1905 is grounded, its output is always high. Thus, the application of a positive control signal to the line 1825 applies the outputs of the address counter 1811 to the input of the memory 606, and the absence of positive going control signal enables the even numbered gates and applies the output of the register 1817 to the memory 606. The OR gates 1919, 1923, 1927, and 1931 are used to transmit the same odd outputs from the register 1817 and the counter 1811 to the appropriate outputs lines. As mentioned above, the construction and the operation of the multiplexer circuits 1902 and 1903 are identical to that explained above in connection with the circuit 1901.

Referring now to FIG. 20, the control circuit 1805 is illustrated in greater detail. The 01 sub-clock signal is supplied to the input of a 20 nanosecond time delay circuit 2001 whose output is connected to one of two inputs of a NAND gate 2003. The 03 sub-clock signal is supplied to the input of a 40 nanosecond time delay circuit 2005 whose output is connected to one of two inputs of a NAND gate 2007, and one of two inputs of a

NAND gate 2009. The output of the NAND gate 2007 is connected to the second input of the NAND gate 2003, and the output of the NAND gate 2003 is connected to line 629B which is also connected to the second input of the NAND gate 2007.

The line 719, which supplies the MASTER ZERO signal, is connected to the input of an inverter 2011 whose output is connected to one of two inputs of a NAND gate 2013. The 07 subclock signal is connected to the input of an inverter 2015, the input of a 20 nanosecond time delay circuit 2017, and to one of two inputs of a NAND gate 2019. The output of the inverter 2015 is connected to the second input of the NAND gate 2013 whose output is connected to one of two inputs of a NAND gate 2021. The output of the NAND gate 2021 is connected to the line 1825, and is also connected to the second input of the NAND gate 2009. The output of the NAND gate 2019 is connected to the input of an inverter 2023, and the output of this inverter is connected to the line 1827.

The circuits shown in FIG. 20 are designed to adjust the time of the pulses applied to the multiplexer and counter of FIG. 18. Each of the sub-clock pulses has a width of 27.8 nanoseconds. Assuming that 01 appears at the input of the delay 2001 at time 0, then 03 will appear at the delay at time 55.6 and 07 will appear at the input to delay 2017 at time 166.7. These numbers represent elapsed time in nanoseconds. Then gate 2003 will receive one low input circuit 2001 from time 20 to 47.8, and it will receive a second low input from gate 2007 from time 0 to 123.3. Thus, the output of gate 2003 will go low from time 20 to 47.8. The gate 2009 receives one high input from delay 2005 from time 27.8 to 125, and a second high input from gate 2021 from time 166.7 to 194.4, during the time that 07 exists. The output from gate 2021 remains high during time 123.3 to 166.7 and remains low from time 166.7 to 194.4.

Gate 2019 receives on high input from time 166.7 to 194.4 and another high input from time 186.7 to 214.4. Thus, the output on line 1827 goes high from time 186.7 to 194.4.

Referring now to FIG. 21, the counter control circuit 1803 is illustrated in greater detail. The 02 sub-clock signal is supplied to the input of a 20 nanosecond time delay circuit 2101, and to one of two inputs of a NAND gate 2103. The output of the circuit 2101 is connected to the second input of the NAND gate 2103. The output of the NAND gate 2103 is connected to the line 1631. The line 1631 is connected to one of two inputs of a NAND gate 2105, and one of three inputs of a NAND gate 2107. It is pointed out at this juncture of the description that the signal generated by circuit 2101 and the NAND gate 2103 is the 02A sub-clock signal as alluded to hereinabove.

The line 621, which supplies the 80 mile range selection signal, is connected to a first input of a dual line receiver 2109. The line 623, which supplies the 200 mile range selection signal, is connected to the second input of the dual line receiver 2109. The two outputs of the line receiver 2109 are connected to two inputs of a NAND gate 2111, whose output is connected to the second input of the NAND gate 2105, and is also connected to an input of an inverter 2113. The output of the inverter 2113 is connected to the second input of the NAND gate 2107.

The 07 sub-clock signal is connected to the count input of a binary counter stage 2115. The line 716,

which supplies the CLOCKED R_s SWEEP GATE signal, is connected to the clear input of the counter stage 2115, and its output is connected to the third input of the NAND gate 2107. The output of the NAND gate 2107 is connected to one of two inputs of a NAND gate 2119. The output of the NAND gate 2105 is connected to the second input of the NAND gate 2119. The output of the NAND gate 2119 is connected to the input of an inverter 2121. The output of the inverter 2121 is connected to the line 1809.

The 02 sub-clock pulse is applied to the inputs of the delay 2101 and the gate 2103 at the same time. Twenty nanoseconds later, the output from the delay 2101 applies the second input to the gate 2103, opening the gate and passing the 02A sub-clock signal. Using the timing set forth above, the 02 pulse is applied to the gate 2103 from 27.8 to 55.6 and the output from the delay 2101 is applied to the gate 2103 from 47.8 to 75.6. The output on line 1631 exists from 47.8 to 55.6, or a length of 7.8 nanoseconds. The dual-line receiver 2109 is little more than two coupling circuits in the same box. They match impedances, voltages, etc. The two inputs to the gate 2111 are the 80 mile and the 200 mile range selection signals. When either of these signals is not present, the output of the gate 2111 is high. When signals are present on both of lines 621 and 623, the output of gate 2111 is low, gate 2105 receives an inhibiting signal and gate 2107 receives a conditioning signal. The counter stage 2115 generates an output for every other 07 pulse it receives. Thus, when a 02A pulse is received at the same time that signals are present on lines 621 and 623 and the counter stage 2115 is in the one state, gate 2107 output goes low, driving the output of gate 2119 high. Line 1809 goes low. When the output of gate 2113 is high, gate 2105 output goes low with the same end result. In between 02A pulses, the outputs of gates 2105 and 2107 are both high, the output of gate 2119 is low, and line 1809 is high.

Referring now to FIG. 22, the read enable circuit 1823 is illustrated in greater detail. The line 626, which supplies the RADAR MAIN BANG signal, is connected to the input of a monostable multivibrator 2201 which is set for a 400 nanosecond time delay. The output of the monostable multivibrator 2201 is connected to one of two inputs of a NAND gate 2203. The 04 sub-clock signal is connected to the input of an inverter 2205, and the output of this inverter is connected to the second input of the NAND gate 2203. The output of the NAND gate 2203 is connected to one of two inputs of a NAND gate 2207, the output of which is connected to the line 1826 and to one of two inputs of a NAND gate 2209. Line 716, which supplies the CLOCKED R_s SWEEP GATE signal, is connected to the second input of the NAND gate 2209, the output of which is connected to the second input of the NAND gate 2207.

In operation, the output of the gate 2203 is high except when the multivibrator 2201 is in its unstable condition and 04 pulse is not present. The multivibrator 2201 applies a high input to gate 2203 from time 0-400, and the inverter 2205 applies a high input to gate 2203 except when 04 pulse is present from time 84.4 to 112.2. Thus, the output of the gate 2203 is high from time 0-83.4 and from 111.2-400. The high output from gate 2203 applies a second high input to gate 2207 which drives line 1826 low from time 0-83.4 and from 111.2-400. Line 1826 is high from 83.4-111.2

and when the R_s SWEEP GATE is present on line 716.

Referring now to FIG. 23, the digital-to-analog conversion circuit 631 is illustrated in greater detail. Lines 633a through 633e, which supply the binary numbers recovered from the RAM 606, are connected to the DATA (D) inputs of flip-flops 2301 through 2305, respectively. The 08 sub-clock signal is connected to the CLOCK (C) inputs of the flip-flops 2301 through 2305.

The 1 output of the flip-flop 2301 is connected to one of two inputs of a NAND gate 2307, and to the input of an inverter 2309. The 1 output of the flip-flop 2302 is connected to the second input of the NAND gate 2307, and to the input of an inverter 2311. The 1 output of the flip-flop 2302 is connected to one of two inputs of a NAND gate 2313, and to one of two inputs of a NAND gate 2315. The 1 output of the flip-flop 2304 is connected to one of two inputs of a NAND gate 2317, and to one of three inputs of a NAND gate 2319, and to one of two inputs of a NAND gate 2321. The 1 output of the flip-flop 2305 is connected to one of two inputs of a NAND gate 2323, to one of three inputs of a NAND gate 2325, and to one of two inputs of a NAND gate 2327.

The output of the NAND gate 2307 is connected to the second input of the NAND gates 2327, 2321, and 2315, and is also connected to the input of an inverter 2329. The output of the inverter 2329 is connected to the second input of the NAND gates 2313, 2319, and 2325.

The output of the inverter 2309 is connected to an input, designated hereinafter A, of a resistor ladder network and amplifier circuit 2331. The circuit 2331 is a conventional circuit employed in performing digital-to-analog conversions, and is well known in the electronics art. In accordance with the preferred embodiment, circuit 2331 is adapted for receiving ten individual binary input signals (hereafter designated inputs A through J), and generating an analog voltage at a single output of the line 637. The output of the inverter 2311 is connected to the B input of the circuit 2331. The output of the NAND gate 2315 is connected to the C input of the circuit 2331. The output of the NAND gate 2321 is connected to the D input of the circuit 2331. The output of the NAND gate 2327 is connected to the E input of the circuit 2331. The output of the NAND gate 2317 is connected to the F input of the circuit 2331. The output of the NAND gate 2323 is connected to the G input of the circuit 2331. The output of the NAND gate 2313 is connected to the H input of the circuit 2331, to one of two inputs of a NAND gate 2333, and to the third input of the NAND gates 2319 and 2325. The output of the NAND gate 2333 is connected to the second input of the NAND gates 2317 and 2323 and the other input to NAND gate 2333 is connected to voltage +V. The output of the NAND gate 2319 is connected to the I input of the circuit 2331, and the output of the NAND gate 2325 is connected to the J input of the circuit 2331.

When a 08 sub-clock signal appears, the data applied to the inputs of the flip-flops 2301 through 2305 is transferred into those flip-flops which comprise a clocked register. The outputs of the register are combined with each other and a positive potential in gates 2307, 2313, 2315, 2317, 2319, 2321, 2323, 2325, 2327, and 2333 to decode the digital signals. The following table shows the connections of the gates with the outputs. For this discussion the output of flip-flop

2305 is the 2^0 term, the output of flip-flop **2301** is the 2^4 terms, and the other flip-flop outputs represent the intervening terms.

TABLE IV

Gate (Inverter)	Inputs	Output
2309	2^4	A
2311	2^3	B
2329	2307	C
2315	2307	
	2^2	D
2321	2307	
	2^1	E
2327	2307	
	2^0	H
2307	2^4	
	2^3	F
2313	2^2	
	2329	G
2317	2^1	
	2333	I
2323	2^0	
	2333	J
2333	2313	
	+V	
2319	2^1	
	2313	
2325	2329	
	2313	
	2329	
	2^0	

The resistor ladder network **2331** is organized to operate in a manner opposite to the ladder shown and described in FIG. 14. The converter of FIG. 14 varied in the resolution with which the signal was represented in digital form at different voltage levels. The ladder **2331** receives the inputs from the decoding gates with the resolution represented by each and converts that input to a prescribed voltage level. As an input line to the ladder **2331** is energized, the ladder provides line **637** with a predetermined voltage level. An integrator, either within the block **2331** or without it, molds the changing voltages on line **637** into a smooth curve which represents the original input video signal into a corrected video signal which has been modified in a prescribed manner.

Accordingly, an exemplary new and improved solid-state circuit has been described hereinabove for converting signals which are generated in accordance with a first mathematical function into signals in accordance with a second mathematical function. The invention contemplated herein is the provision of a simple solid-state memory system and controls therefor in lieu of earlier devices such as scan-conversion tubes for performing similar signal conversions.

In review of the structure and operation described hereinabove, reference is again made to FIG. 6. The radar simulator video signal, which is generated linear with respect to a ground range time base (first mathematical function), is supplied on the line **118** to the input of the analog-to-digital driver **601**, and the output of the driver is supplied to the input of the analog-to-digital converter **603**. The converter **603** converts the video signal from an analog form into a digital form, and the digital form of the video signal is supplied to the data input of the RAM **606** for storage in the RAM.

The memory control circuit **625** supplies an address during a first time interval to the RAM **606** for selecting the location at which the digital form of the video signal is to be stored. Also, the circuit **625** supplies an address during a second time interval to the RAM **606** for selecting the location from which the digital form

of the video signal is to be retrieved. The address supplied during the first time interval is generated as a function of the instantaneous difference between the values for the R_s and R_o signals, and the address supplied during the second time interval is generated uniformly.

The instantaneous difference between the values for the R_s and R_o signals is generated within the $(R_s - R_o)$ generator circuit **615**, and the value for this difference is supplied, in digital form, to the memory address control circuit **615** via the lines **627**.

The digital form of the video signals retrieved from the RAM **606** are supplied on the lines **633** to the input of the digital-to-analog conversion circuit **631**. The circuit **631** converts the digital form of the video signal into an analog form of the video signal and supplies this analog signal on line **637** to the carrier frequency converter **110** (as shown in FIG. 1).

It readily may be appreciated from the discussion hereinabove that the signal conversion is performed by addressing the RAM **606** with two separate address values. The write address valve is generated for randomly storing the video signal at a location proportional to the instantaneous difference between the values for R_s and R_o , and the read address value is generated for sequentially retrieving the video signals from the RAM.

While a specific embodiment of the present invention has been disclosed hereinabove, it is meant to be exemplary only. Those having skill in the related art of the present invention may modify and depart from the spirit of the disclosed embodiment, and it is therefore intended that an exclusive property right be granted within the breadth and scope as defined by the claims appended hereinbelow.

What is claimed is:

1. A method for converting a first signal which varies in accordance with a first mathematical function into a second signal which varies in accordance with a second mathematical function, said method comprising the steps of:

- a. sampling said first signal;
- b. generating a first address in accordance with the instantaneous difference between said first and second mathematical function;
- c. utilizing said first address for storing manifestations of said first signal samples in a storage means during a first time interval;
- d. generating a second address proportional to said second mathematical function; and
- e. utilizing said second address for retrieving said stored manifestations from said storage means during a second time interval, wherein said retrieved manifestations correspond to said second signal in accordance with said second mathematical function.

2. The method as defined in claim 1, wherein the step of generating said first address further comprises the steps of:

- a. deriving a first number representative of the instantaneous difference between said first mathematical function and said second mathematical function;
- b. generating a second number uniformly increasing in value; and
- c. combining said first number with said second number to produce said first address.

3. The method as defined in claim 2, wherein the step of generating said second address further comprises the step of generating a third number uniformly increasing in value to produce said second address.

4. The method as defined in claim 2, wherein said deriving step includes the steps of:

- a. algebraically summing a first signal proportional to said first mathematical function with a second signal proportional to said second mathematical function to generate a third signal varying in amplitude;
- b. comparing the amplitude of said third signal with a reference potential to produce first and second composite signals each of which represents a polarity of the difference between said third signal and said reference potential;
- c. incrementing a digital counter in response to said first composite signal representative of one polarity of said difference;
- d. decrementing said digital counter in response to said second composite signal representative of the other polarity of said difference;
- e. converting said first number derived by incrementing said digital counter into an analog form; and
- f. modifying the amplitude of said third signal with the amplitude of said analog form of said first number to maintain proportionality between the amplitude of said third signal and the value of said first member.

5. The method as defined in claim 1, wherein the step of sampling said first signal in accordance with said first mathematical function includes the steps of:

- a. producing from each of said samples a plurality of individual amplitudes which together represent the value of the sample;
- b. converting all of said amplitudes into a digital number which represents said value with each of said amplitudes being converted at its own digital resolution; and
- c. encoding said digital number into manifestations of said sampled signal.

6. A system for converting a first signal which varies in accordance with a first mathematical function into a second signal which varies in accordance with a second mathematical function, said system comprising:

- a. means for sampling the first signal in accordance with said first mathematical function;
- b. means having a data input coupled to the output of said sampling means for storing manifestations of the sampled signal;
- c. means having an output coupled to an address input of said storage means to generate a first address for storing said manifestations in said storage means;
- d. means having an output coupled to the address input of said storage means to generate a second address for retrieving said stored manifestations from said storage means;
- e. means for utilizing said first address for storing said manifestations in said storage means during a first time interval and for utilizing said second address for retrieving said manifestations from said storage means during a second time interval, wherein said retrieved manifestations are representative of the first signal in accordance with said second mathematical function; and
- f. means for controlling said sampling means, said storage means, and said first and said second ad-

dress generating means for coordinated synchronous operation.

7. The system as defined in claim 6, wherein said first address generating means comprises:

- a. means for deriving values representative of instantaneous differences between said first mathematical function and said second mathematical function;
- b. a first counting means disposed for providing a uniformly increasing output value;
- c. an adding means having a first set of adding inputs coupled to the output of said counting means and having a second set of adding inputs coupled to the output of said deriving means; and
- d. means coupling the output of said adding means to the address input of said storage means.

8. The system as defined in claim 7 wherein said second address generating means comprises:

- a. a second counting means disposed for providing a uniformly increasing output value; and
- b. means for coupling the output of said second counting means to an address input of said storage means.

9. The system as defined in claim 8 wherein said means for sampling the signal comprises:

- a. means for producing a plurality of component signals which together represent the value of said signal samples;
- b. means for converting said component signals individually into digital components with each component signal being converted at its own resolution; and
- c. means for encoding said digital components into a single digital word which represents the value of said signal sample.

10. The system as defined in claim 7, wherein said deriving means includes:

- a. means for algebraically subtracting a first signal proportional to said first mathematical function from a second signal proportional to said second mathematical function to produce a third signal which varies in amplitude;
- b. means for comparing the amplitude of said third signal with a reference potential to produce composite signals each of which represent a first and second polarity;
- c. a digital counter coupled to said comparing means and adapted to increment in response to said first polarity representative of one of said composite signals, and adapted to decrement in response to said second polarity of another one of said composite signals, wherein the contents of said counter is said value representative of the instantaneous differences between said first mathematical function and said second mathematical function;
- d. means for converting the output of said digital counter into an analog signal which varies in amplitude in accordance with the output of said counter;
- e. means for comparing the analog output of said counter with said third signal to generate an error signal proportional to the difference therebetween; and
- f. means for adjusting the contents of said counter to reduce said error signal to zero.

11. The system as defined in claim 6 wherein said second address generating means comprises:

- a. a second counting means disposed for providing a uniformly increasing output value; and
- b. means for coupling the output of said second counting means to an address input of said means.

12. The system as defined in claim 6 wherein said means for sampling the signal comprises:

- a. means for producing a plurality of component signals which together represent the value of said signal samples;
- b. means for converting said component signals individually into digital components with each component signal being converted at its own resolution; and
- c. means for encoding said digital components into a single digital word which represents the value of said signal sample.

13. The system as defined in claim 6 wherein said storage means comprises a random access memory.

14. The system as defined in claim 6 wherein said means for controlling comprises:

- a. a source of clock pulses;
- b. means for generating sub-clock pulses which exist for equally spaced time intervals between said clock pulses;
- c. means for applying at least one of said sub-clock pulses to said sampling means;
- d. means utilizing said clock pulses for generating control signals; and
- e. means for applying said control signals to said storage means and said first and second address generating means.

15. Apparatus for converting a signal represented in accordance with a first mathematical function into the same signal represented in accordance with a second mathematical function, said apparatus comprising:

- a. means for periodically sampling a varying input signal;
- b. an information storage means having a plurality of addressable storage locations;
- c. means for generating in a first sequence which represents a third mathematical function a first set of addresses of said locations;
- d. means for writing representations of the values of the samples of said input signal into the storage means locations of said first set of addresses;
- e. means for generating a second set of addresses for said locations in a linear sequence;
- f. means for reading said stored representations of said samples from said storage means in accordance with said second sequence of addresses; and
- g. means for constructing a smooth output signal from the samples read from said storage means.

16. The apparatus defined in claim 15 wherein said means for generating the first set of addresses comprises:

- a. a first counter;
- b. means for stepping said first counter for each sample of said input signal;
- c. means for generating a third mathematical function signal which follows the difference between said first and second mathematical functions; and
- d. means for combining the contents of said first counter with said third function signal to produce said first set of addresses.

17. The apparatus defined in claim 16 wherein said means for stepping said first counter comprises:

- a. means for synchronizing the operation of said apparatus, said synchronizing means including
- b. means for generating timing signals;
- c. means for applying timing signals from said generating means to said sampling means to control the time of sampling said input signal; and
- d. means for applying timing signals from said generating means to said first counter to cause said first counter to step.

18. The apparatus defined in claim 16 wherein said means for generating said second set of addresses comprises a second counter, and means for stepping said second counter each time said input is sampled to produce said second set of addresses.

19. The apparatus defined in claim 18 further including:

- a. means for synchronizing the operation of said apparatus, said synchronizing means including
- b. means for generating timing signals;
- c. means for applying timing signals from said generating means to said sampling means to control the time of sampling said input signal; and
- d. means for applying timing signals from said generating means individually to said first and second counters to cause them to step in synchronism with said sampling and with each other.

20. The apparatus defined in claim 18, wherein said means for stepping said second counter comprises:

- a. means for synchronizing the operation of said apparatus, said synchronizing means including
- b. means for generating timing signals;
- c. means for applying timing signals from said generating means to said sampling means to control the time of sampling said input signal; and
- d. means for applying timing signals from said generating means to said second counter to cause said second counter to step.

21. The apparatus defined in claim 15 wherein said means for sampling includes means for converting said samples of said input signal from a varying amplitude form into an equivalent digital form.

22. The apparatus defined in claim 21 wherein said means for converting said samples of said input signal includes means for producing several signals having amplitudes representative of the amplitudes of said samples with respect to fixed values, and means for generating digital values of said several signals with the resolution varying from signal to signal.

23. The apparatus defined in claim 15 wherein said means for constructing an output signal includes means for converting the information read from said storage means in digital form into an equivalent signal in varying amplitude form.

24. The apparatus defined in claim 15 wherein said means for generating said second set of addresses comprises a second counter, and means for stepping said second counter each time said input signal is sampled to produce said second set of addresses.

25. The apparatus defined in claim 15 wherein said information storage means comprises a random access memory.

26. A system for converting a first video signal which varies in accordance with radar ground range into a second video signal which varies in accordance with radar slant range, said system comprising:

- a. an analog-to-digital converter for periodically sampling said first video signal, and for converting said first video signal into digital numbers;
- b. a random access memory having a data input coupled to the output of said converter and disposed 5 for storing said digital numbers;
- c. means for generating a first digital number representative of the instantaneous differences between a first signal proportional to radar ground range and a second signal proportional to radar slant 10 range;
- d. first means for producing a second number uniformly increasing in value;
- e. means for combining said first number with said second number; 15
- f. means coupling the output of said combining means to the address input of said memory during a first time interval, wherein said combined first

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- and second numbers are utilized for addressing the memory for storing said digital numbers in said memory;
- g. second means for producing a third number uniformly increasing in value;
- h. means coupling the output of said second producing means to the address input of said memory during a second time interval, wherein said third number is utilized for addressing said memory for retrieving said digital numbers from said memory; and
- i. a digital-to-analog converter for converting the digital numbers retrieved from said memory into an analog form, wherein said analog form is said second video signal which varies in accordance with said second mathematical function.

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