

- (51) International Patent Classification:
H01L 33/00 (2010.01) H01L 33/40 (2010.01)
H01L 33/44 (2010.01)
- (21) International Application Number:
PCT/EP2024/071604
- (22) International Filing Date:
30 July 2024 (30.07.2024)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
10 2023 121 984.7
16 August 2023 (16.08.2023) DE
- (71) Applicant: AMS-OSRAM INTERNATIONAL GMBH
[DE/DE]; Leibnizstr. 4, 93055 Regensburg (DE).
- (72) Inventor: VON MALM, Norwin; Stockloher Str. 8, 93152
Thumhausen/Nittendorf (DE).
- (74) Agent: SJW PATENTANWÄLTE; Goethestraße 21,
80336 München (DE).
- (81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG,
KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY,

- MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA,
NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO,
RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,
TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, CV,
GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST,
SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ,
RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ,
DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT,
LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,
SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).
- Published:
— with international search report (Art. 21(3))

(54) Title: METHOD FOR PROCESSING AN OPTOELECTRONIC DEVICE AND ARRAY OF OPTOELECTRONIC DEVICES

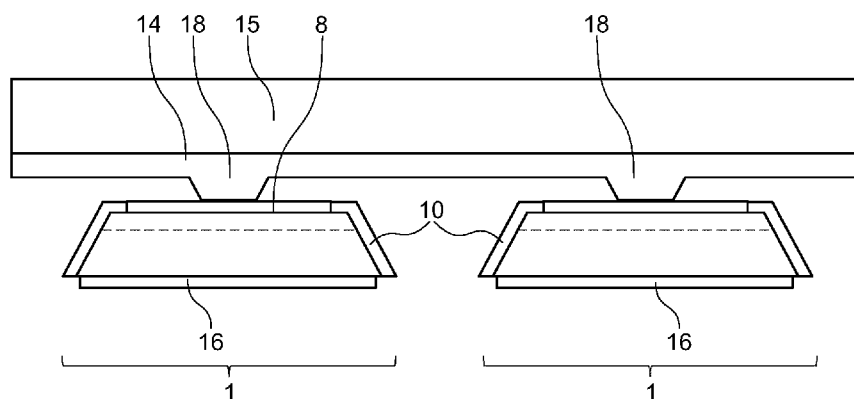


FIG. 12A

(57) Abstract: The invention concerns a method for processing an optoelectronic device, wherein a sacrificial layer is deposited covering the sidewalls of a mesa etched semiconductor layer stack. The sacrificial layer may comprise an organic material and is subsequently planarized and recessed are formed therein. A bond layer is deposited into the recess, the bond layer in particular comprising one of an organic material, a nitride-based material, a solder material and a gold alloy. A temporary carrier is attached to the bond layer and the growth substrate removed, thereby exposing portions of the sacrificial layer and the semiconductor layer stack.

**METHOD FOR PROCESSING AN OPTOELECTRONIC DEVICE AND ARRAY OF
OPTOELECTRONIC DEVICES**

The present application claims priority from German patent application
5 DE 10 2023 121 984.7 filed on August 16, 2023, the disclosure of which
is incorporated by way for reference in its entirety.

The present invention concerns a method for processing an
optoelectronic device, in particular μ LEDs. The present invention also
10 concerns an array of such optoelectronic devices arranged on a carrier.

BACKGROUND

μ LEDs are optoelectronic devices that comprise a lateral dimension in
15 the range from a few μm to about 40 μm . Such devices provide a variety
of different applications, including but not limited to displays.

They are usually processed in arrays of several thousands of devices,
and subsequently transferred from their growth substrate or an
20 intermediate carrier to a target substrate (e.g. display backplane).
The transfer process is delicate due to the small size and the effective
lack of rearrangement possibilities once the device has been placed.
Consequently, the optoelectronic devices are processed in such a way
that they are only fixed to a carrier at defined points by a holding
25 structure, also called tethers. These tethers are arranged and
configured such that they can easily break when the devices are being
mass-transferred, for example by stamping or another transfer method.
The tethers are usually formed by using a sacrificial layer, which is
dissolved at some stage, leaving the tether posts behind on which the
30 devices to be transferred are resting.

Various geometric arrangements and materials for such sacrificial
layers and tethers have been proposed. For example, references EP
1915774 B1 and US 7,622,367 B1 both describe tether structures, which
35 comprise a semiconductor post located below the semiconductor element.
They are formed by lateral undercutting of the semiconductor material.
When such devices are transferred, burrs and particles are formed on

the very surface that is to be connected to the target substrate. This not only complicates the bonding process with the target substrate, but can also contaminate or damage the stamp used for transfer.

5 Semiconductor tethers are also described in US 7,932,123 B2, in which the tether structure is located on the side of the component. The same reference describes holding structures that hold the devices partly from the side and partly from the top. In addition, a planar sacrificial layer is specified.

10 US 8,934,259 B2 shows holding structures made of a polymer, which hold the under-etched component from below. These types of tethers result from a process, in which an adhesive layer is exposed to a part-masked substrate in a patterned manner from the substrate side. The exposed
15 areas can be peeled out, while the unexposed areas form the retaining structures. Tethers and sacrificial layer are thus formed from an adhesive layer of identical material. However, this approach appears to be problematic, since either a pixel-precisely adjusted bonding of the partially masked substrate is required, or masking on the side of
20 the substrate facing away from the devices results in an exposure with insufficient lateral resolution.

It is therefore an object of the proposed principle to specify a geometry of tether structures and material selection with respect to
25 sacrificial layer and holding structures that overcome at least partially the above-mentioned disadvantages.

SUMMARY OF THE INVENTION

30 This and other objects are addressed by the subject matter of the independent claims. Features and further aspects of the proposed principles are outlined in the dependent claims.

The inventor proposes a method for processing optoelectronic devices,
35 that results in the devices being held from below, so there is no interference with the contact to a die or a carrier suitable for laser-induced forward transfer (LIFT). The holding structures made of a bond

material are also not broken but lose their mechanical contact to the semiconductor element during the transfer, specifically at an interface between the material of the holding structure and the material of the semiconductor element facing the holding structure.

5

In accordance with the proposed principle, the bond material of the holding structure is carefully selected and free of semiconductor component. It comprises an organic compound or a thin layer of solder material. Both approaches avoid the formation of particles or rupture and residues on the interface.

10

The transfer process leaves a defined surface on the underside of the optoelectronic device, the contact area or the surface of the device used for bonding to the target substrate.

15

During processing optoelectronic devices in accordance with the proposed principle, the inventor proposes a planarization step of a sacrificial layer material prior to bonding the device with a growth substrate to a carrier. This avoids the filling of areas on the sides of the semiconductor elements by bond material. The bond material is different from the material of the sacrificial layer, such that removal of the sacrificial layer is easily achievable using substances that do not affect the bond material or the device's surface.

20

The planar sacrificial layer with dedicated opening for the bond material of the holding structure attached to the optoelectronic device enables a maximum access area for the etchant used to remove the sacrificial layer in subsequent process steps. The planarization allows the openings in the sacrificial layer, which define the holding structures after filling with bond material, to be designed with lithographic precision.

30

This - in combination with the material selection for the bond material and surface of the optoelectronic device - is crucial to be able to control the adhesion force of the optoelectronic devices on the carrier for the transfer process. In addition, planarization of the sacrificial layer enables a particularly thin layer to be bonded to the substrate,

35

which means that metallic (thin-film) solders can be used as the material for the bond layer in addition to organic polymers. These are particularly resistant to the etching medium used for undercutting.

5 In some aspects, a proposed method for processing an optoelectronic device comprises the step of providing a growth substrate having a semiconductor layer stack epitaxially deposited thereupon. The semiconductor layer stack can for example be a layer stack of several semiconductor layers, such as for example a first layer of a first
10 conductivity type, a second layer of a second conductivity type as well as an active region between the first and second layer. A mesa etching process is conducted in a subsequent step to form sidewalls of the layer stack, said sidewalls covered by a material layer. The sidewall can be inclined and usually expose the active region, which is
15 subsequently covered by the material layer.

In accordance with the proposed principle, a sacrificial layer is deposited. The sacrificial layer covers the sidewalls of the material layer and extends above a top surface of the layer stack. In other
20 words, the sacrificial layer covers all surfaces of the layer stack being exposed, including any contact material on top. The sacrificial layer material is then planarized to form an even surface. Said sacrificial layer comprises one of a metal-oxide and an organic material.

25

In a subsequent step, the sacrificial layer is structured and at least one recess is formed therein, thereby exposing a portion of the material layer and/or the layer stack. The area of the semiconductor layer stack's surface being exposed is dependent on the location of the
30 recess. In some aspects, the exposed surface only contains one material. In some other aspects, the exposed surface can include two materials, i.e. a dielectric and a contact layer adjacent to it.

According to the proposed principle, a bond layer is deposited into
35 the recess, the bond material also extending above the recess and forming an even surface in some instances. The bond layer may comprise an organic material, a nitride-based material, a metallic alloy in

particular containing gold, or a metallic solder material. The composition of the bond layer is different from the sacrificial layer but selected such that any etchant used for removing the sacrificial layer does not affect the bond layer material or the surface of the layer stack.

A temporary carrier is attached to the bond layer. After the attachment of the carrier layer, the growth substrate as well as potential buffer layer can be removed to expose the backside of the layer stack and the semiconductor material. If needed, material of the layer stack is also removed until portions of the sacrificial layer are exposed. This will provide access to the sacrificial layer.

The proposed method provides several benefits. The method can be used for a plurality of semiconductor devices to be processed on their growth substrate by patterned etching from continuous semiconductor layer stack. The sacrificial layer fills the gap between the plurality of mesa structured layer stacks. The surface of the sacrificial layer facing away from the mesa structured semiconductor layer stacks (within experimental accuracy) is essentially co-planar with the growth substrate and comprises openings in the (lateral) regions of the semiconductor elements. The bond material fills the openings and mechanically bonds the semiconductor layer stack to the carrier.

The proposed method enables application of contacts and other elements like mirrors in a flexible way. For example, contacts and mirrors can be applied on both sides of the layer stack implementing a vertical μ LED, but also on the same side, thereby forming a horizontal μ LED. Both, the bonding layer and the sacrificial layer use materials that avoid undesired particle formation during transfer of the semiconductor devices, resulting in a high transfer yield. Various transfer processes are possible, further adding to the benefits of the proposed method.

The bonding layer does not obstruct the transfer process in any way, because no bond material is located at undesired places, for example between the optoelectronic devices. This enables the processing of elements with a very high density on the growth substrate, reducing

the overall costs. The holding structure, its shape, form and the chosen material provides a flexible yet precise control of the adhesive force between the devices and the holding structure.

5 As the sacrificial layer is exposed at a relatively large size, the etching process for removing the sacrificial layer can be shortened, which does not only increase process speed but also reduces possible effects of the etchant on the remaining portions, i.e. the semiconductor layer stack.

10 The proposed process is suitable for various and different kinds of devices including but not limited to μ LEDs, μ -photodetectors, μ -ICs and the like. Various material systems for the semiconductor layer stack are possible including, GaN, GaP, InGaN, InGaP, AlInGaN, InGaAlP, 15 InGaAlAs, InGaAlNAs and InGaAlSb. Likewise, various organic material combinations for the sacrificial layer and the bond material are possible, allowing for selective etching, selective undercutting and other dedicated process steps. Finally, the proposed method provides the possibility to deposit solder material on the layer stack and 20 contact thereof. This approach reduces complexity in later processing steps and enables a significantly simplified attachment process to a backplane.

In some aspects, the mesa etching process comprises the step of 25 depositing a structured mask, for example hard mask, on the semiconductor layer stack. The material of the mask can be suitable as a contact layer and may comprise transparent conductive oxides or another conductive material. By doing so, the structured mask material may remain on the top surface of the semiconductor layer stack after 30 the mesa etching step.

Generally, the etching process can be divided into several mesa etching steps, after each some cleaning or protecting the exposed surface may be conducted. In some aspects, a first mesa etch is conducted to a 35 depth smaller than a thickness of the semiconductor layer stack. Hence, a portion of the layer remains, and the mesa etch is stopped prior to

reaching a growth substrate or a buffer layer. In particular, the first mesa etch exposes the active region of the semiconductor layer stack.

Apart from Quantum well intermixing, the exposed sidewalls can also be regrown with a semiconductor material, SiO₂, Al₂O₃ and any other suitable material. In some instances, the regrown layer corresponds to the material layer, that is, it forms a portion of the outer surface of the device.

In some aspects, a second mesa etching step is conducted into remaining portions of the layer stack to a depth smaller than a thickness of the layer stack. Similar to the first mesa etch, any second or further etch will stop prior to reaching the growth substrate. Consequently, it is proposed in some aspects to have a continuous portion of the semiconductor layer stack remain on the growth substrate. The material layer may comprise a metal or a partially reflective material. In this regard, the material layer can also comprise various sublayers including dielectric and conductive layers.

Some aspects concern the selection of material for the sacrificial layer. Such selection should be based on a combination of the desired bond material as well as the material of the semiconductor layer stack, material for the sacrificial layer can be selected based on all layers that are in direct contact with the etchant used for removing the sacrificial layer.

In some aspects, the material of the sacrificial layer is selected to be ZnO if the material layer comprises SiO₂ or Si₃N₄, and a contact layer on the top surface of the semiconductor layer stack optionally comprises Au or Ag and in particular a solderable layer such as for example AuSn, InSn, AuInSn, NiInSn. Dissolving ZnO would be an inorganic implementation. However, ZnO is easily removed with diluted HCl that leaves SiO₂, Si₃N₄ or noble metals like Au, Pd, Pt and Ag unaffected.

As an alternative, one can use organic materials and compounds for the sacrificial layer. Polystyrene, particularly solute in Ethylacetate or

Toluol and is suitable if the material layer comprises SiO₂ or Si₃N₄ and a contact layer on the top surface of the semiconductor layer stack comprises Au or Ag and in particular a solderable layer such as for example AuSn, InSn, AuInSn, NiInSn. Polystyrene has the benefit that it is dissolvable in organic solvents, facilitating the later sacrificial layer removal.

Other forms of Polystyrene are possible, for example when melted and planarized by pressing if a contact layer on the top surface of the semiconductor layer stack comprises one of Au and Ag, an Au containing alloy, or a solderable layer such as for example AuSn, InSn, AuInSn, NiInSn. Polyvinylalcohol, PVA is also a suitable material if the material layer comprises SiO₂. It also has the benefit that it is dissolvable in H₂O. A similar material is Polyvinylacetate, PVAc, if the material layer comprises SiO₂ or Si₃N₄. It can be dissolved in Ethyl acetate. Finally, soft-baked photoresist can be used, if a contact layer on the top surface of the semiconductor layer stack comprises one of Au and Ag, an Au containing alloy, or a solderable layer such as for example AuSn, InSn, AuInSn, NiInSn. All organic materials as sacrificial layer material can also be removed by an oxygen-based plasma-etching process if a contact layer on the top surface of the semiconductor layer stack comprises one of Au, an Au containing alloy, or a solderable layer such as for example AuSn, InSn, AuInSn, NiInSn.

Some or all of the material of the sacrificial layer can be deposited by various means, further increasing the flexibility and optimizing the process. For example, deposition techniques include spinning the sacrificial layer material on a contact layer on the top surface of the semiconductor layer stack and/or the top surface of the semiconductor layer stack and/or the surface of the material layer, sputtering the sacrificial layer material on a contact layer on the top surface of the semiconductor layer stack and/or the top surface of the semiconductor layer stack and/or the surface of the material layer,, or spraying it on a contact layer on the top surface of the semiconductor layer stack and/or the top surface of the semiconductor layer stack and/or the surface of the material layer. In some aspects,

viscosity is adjusted by adding a suitable solvent. Consequently, some techniques are also used to planarize the sacrificial layer.

For example, sacrificial layer material together with a solvent is deposited using one of the above-mentioned techniques. The solvent is vaporized, leaving a substantially planar and even surface of sacrificial layer material. Other deposition techniques include melting sacrificial layer material on the surface or pressing molten and low viscous sacrificial layer material on the surface.

To planarize an uneven surface of the sacrificial layer, one can use CMP and other mechanical techniques, which are described further below in regard to planarizing the bond layer. In some further aspects, structuring the sacrificial layer comprises depositing a structured photo resist layer as to expose surface portions of the sacrificial layer. Then, the exposed portions of the sacrificial layer are wet etched or dry etched until a portion of the semiconductor layer stack's surface is exposed. The recess can be formed above the top surface of the layer stack and, for example, above a contact layer on the top surface of the semiconductor layer stack. The recess may also be formed in a sidewall portion of the layer stack and partially adjacent to a sidewall portion. The latter allows utilizing the bond material to connect to two adjacent optoelectronic devices.

Depositing the bond material on the sacrificial layer and the recess may include a vapor deposition of the bond layer material. In some aspects a thin film solder material based on a gold alloy like AuSn, AuInSn, but also InSn or NiInSn solder material is suitable. Alternatively, the bond layer material may be spun, sputtered or sprayed onto the sacrificial layer. In some aspects, the bond material comprises an organic compound. Consequently, the bond material may comprise a solvent to adjust its viscosity. This will provide an even surface after the solvent has evaporated.

Further deposition techniques may be used depending on the material. For example, one may use melting bond layer material on the surface or pressing molten or low viscous bond layer material on the surface.

Different bond layer materials are suitable, particular bond layer materials that are different in its etching characteristics from the material of the sacrificial layer. In some aspects, the bond layer material comprises one of Benzocyclobuthene or epoxy resin, that is at least partially cured at room temperature, particularly if the sacrificial layer comprises an organic compound and/or if the contact layer contains a solderable material stack. The bond layer material comprises in other aspects polystyrene if the sacrificial layer comprises PVA; or the bond layer material comprises epoxy resin or Benzocyclobuthene if the sacrificial layer comprises polystyrene. The various combinations are also stated further below.

In some aspects, the bond layer is cured after the temporary carrier is attached to the bond layer. For curing purposes, thermal or optical measures can be used. Of course, the curing process can be divided to fit the attachment and planarization process.

After attaching the temporary carrier, the layer stack can be freed of the growth substrate. The temporary carrier acts as a new substrate for such process steps. Various methods of removing the growth substrate are known in the art. This will expose the continuous portion of the semiconductor layer stack from the backside. This continuous portion is also removed to separate the individual optoelectronic devices embedded within the sacrificial layer. Removing the continuous portion of the semiconductor layer stack includes but is not limited to mechanical grinding, polishing, chemical mechanical polishing, CMP, wet or dry etching or combinations thereof.

The backside of the optoelectronic devices namely a bottom surface of the semiconductor layer stack opposite the top surface is then exposed and can be further structured. For example, a contact material can be deposited partially or fully on the bottom surface of the semiconductor layer stack. The contact material can be a conductive transparent oxide, ITO for example, also acting as an emission surface. This can be achieved by sputtering or physical vapor deposition (PVD). Another possibility to deposit a contact material would be plasma enhanced chemical vapor deposition (PECVD).

In addition, or as an alternative, the bottom surface of the semiconductor layer stack can be roughened or otherwise enhanced to facilitate the out coupling of light. For this purpose, optical structures can be provided on the bottom surface of the semiconductor layer stack. The bottom surface of the semiconductor layer stack or the contact material is structured. An optical element can also be attached onto or etched into the bottom surface of the semiconductor layer stack. These optical elements may comprise μ -Lenses and the like, but also photonic structures.

Finally, the proposed method may include removal of the sacrificial layer, in particular by one of dry-etching, wet-etching, plasma-etching, or dissolving in water or an organic solvent. Again, the selected removal process depends on the combination of the material of the semiconductor's surface, the material of the sacrificial layer and the bond material. The optoelectronic device is then held by the bond material, defining a specific adhesion force at the interface. This will allow an easy transfer process onto a target substrate or a carrier for a subsequent LIFT process using a stamp, for example.

Another aspect concerns an array of optoelectronic devices processed by the proposed method. In the array of optoelectronic devices, the sacrificial layer is removed, exposing bond layer material forming a holding structure comprising posts. Each respective post is attached to a respective optoelectronic device, wherein a surface of the optoelectronic device opposite the posts comprises one of a contact material and an optical element.

The bond material of the array comprises an organic compound, particularly including one of a at least partially cured epoxy resin, Benzocyclobuthene and Polystyrene. The array can be secured and transported to a different site for further processing.

SHORT DESCRIPTION OF THE DRAWINGS

Further aspects and embodiments in accordance with the proposed principle will become apparent in relation to the various embodiments

and examples described in detail in connection with the accompanying drawings in which

Fig. 1 to 12B show steps for processing an optoelectronic device in accordance with some aspects of the proposed principle;

Fig. 13A to 13C show embodiments of optoelectronic devices connected to a holding structure in accordance with some aspects of the proposed principle;

Fig. 14A to 14C shown further steps for processing an optoelectronic device in accordance with some aspects of the proposed principle;

Fig. 15 to 27 show steps of a further embodiment for processing an optoelectronic device in accordance with some aspects of the proposed principle; and

Fig. 28A to 28C each show an embodiment of an optoelectronic device connected to a holding structure in accordance with some aspects of the proposed principle.

DETAILED DESCRIPTION

The following embodiments and examples disclose various aspects and their combinations according to the proposed principle. The embodiments and examples are not always to scale. Likewise, different elements can be displayed enlarged or reduced in size to emphasize individual aspects. It goes without saying that the individual aspects of the embodiments and examples shown in the figures can be combined with each other without further ado, without this contradicting the principle according to the invention. Some aspects show a regular structure or form. It should be noted that in practice slight differences and deviations from the ideal form may occur without, however, contradicting the inventive idea.

In addition, the individual figures and aspects are not necessarily shown in the correct size, nor do the proportions between individual elements have to be essentially correct. Some aspects are highlighted by showing them enlarged. However, terms such as "above", "over", "below", "under", "larger", "smaller" and the like are correctly represented with regard to the elements in the figures. So it is possible to deduce such relations between the elements based on the figures.

Figures 1 to 12B show steps for processing an optoelectronic device in accordance with some aspects of the proposed principle.

In a first step, as shown in figure 1, a growth substrate 2 is provided with a semiconductor layer stack 3 epitaxially grown on top. The semiconductor layer stack comprises a first layer 4 of a first conductivity type, a second layer 5 of a second conductivity type as well as an active region 6 between the first and second layer 4, 5.

In a second step, as shown in figure 2, a structured first contact layer 7 is deposited on a top surface of the existing structure. The structured first contact layer 7 can for example form a structured mask which is suitable as a mask for a subsequent etching step but can also be deposited/grown on the semiconductor layer stack after a mesa etching of the semiconductor layer stack has been performed. In the embodiment shown, the first contact layer 7 is of a conductive and reflective material, such as for example a metal and can comprise for example a solder material or solder material layer on a surface facing away from the second layer 5. A solder material can for example comprise a metal layer stack consisting of AuSn, AuInSn, InSn, NiSn, NiInSn, SnAgCu. The first contact layer 7 can however also be of a transparent conductive material such a transparent conductive oxide (TCO), for example indium tin oxide (ITO).

In a further step, as shown in figure 3, a mesa etching step is performed. The mesa etching step structures the semiconductor layer stack 3, resulting in exposed portions of the semiconductor layer stack 3 that include a top surface 8 and inclined sidewalls 9. The etching

is performed such that the etching does not go through the whole first layer 4 but stops well before reaching the growth substrate 2. In particular the etching is performed to a depth d smaller than a thickness t of the semiconductor layer stack 3. However, depth d is larger than the sum of the thicknesses of layer 5 and 6. The exposed portions are thereby as shown in cross section in form of trapezoids arranged on a residue of the first layer 4.

In a following step, as shown in figure 4, a material layer 10 is provided on the mesa etched structure following the shape of the mesa etched structure. The material layer 10 can be provided such that it covers at least side walls 9. The material layer 10 can for example result from a Quantum well intermixing, or the exposed sidewalls can be regrown with a semiconductor material, SiO_2 , Al_2O_3 and any other suitable material. In the embodiment shown, the material layer 10 is a structured regrowth layer that forms a portion of the outer surface of the later optoelectronic device.

As shown in figure 5, a sacrificial layer 11 is then deposited on the semiconductor layer stack 3 and the material layer 10. The sacrificial layer 11 covers the sidewalls of the material layer 10 and extends onto the top surface 8 of the semiconductor layer stack 3 as well as onto the structured first contact layer 7. The sacrificial layer 11 in particular covers all exposed surfaces of the semiconductor layer stack 3 including the first contact layer 7 on top and in particular fills up completely all gaps between the mesa etched portions of the semiconductor layer stack 3 / the material layer 10. The sacrificial layer 11 thereby comprises one of a metal-oxide or an organic material.

The sacrificial layer 11 is then, as shown in figure 6, planarized to form an even surface 12. The even surface 12 of the sacrificial layer 11 facing away from the mesa structured semiconductor layer stack 3 (within experimental accuracy) is substantially co-planar with the growth substrate 2.

The deposition of the sacrificial layer 11 can for example comprise a spinning, sputtering, or spraying of the sacrificial layer material on

the exposed surface(s) of the semiconductor layer stack 3 and the material layer 10. The planarization of the sacrificial layer 11 can on the other hand comprise a mechanical planarization such as for example grinding and/or polishing, a chemical planarization using for example an etchant, a chemical mechanical polishing (CMP), or by melting and/or pressing molten or low viscous sacrificial layer material on the surface the exposed surface(s) of the semiconductor layer stack 3 and the material layer 10. In case of molten/liquid sacrificial layer material being deposited the exposed surface(s) of the semiconductor layer stack 3 and the material layer 10, the step of planarization can be dispensed with in such that the planarization can take place over time by itself as the molten sacrificial layer material levels itself over time.

The sacrificial layer 11 is then in a subsequent step structured, as shown in figure 7, to provide recesses 13 in the sacrificial layer 11. Due to structuring the sacrificial layer 11, thereby generating the recesses 13, a portion of the material layer 10 and/or a portion of the semiconductor layer stack 3 is exposed. The area of the material layer 10 and/or semiconductor layer stack 3 being exposed is dependent on the position where a holing structure is desired to be later provided. In the embodiment shown, only a portion of the top surface 8 is exposed, however it can also be conceivable to expose only a portion of the material layer 10 or a portion of both the material layer 10 and the semiconductor layer stack 3. Further embodiments regarding these aspects are explained later on with regard to figures 13A to 13C.

As shown in figure 8, a bond layer 14 is then provided on the sacrificial layer 11 and into the recesses 13. In the embodiment shown, the bond layer 14 forms an even surface opposite the semiconductor layer stack 3. The bond layer 14 can for example comprise an organic material, a gold alloy or can be a (thin film) solder material or combinations thereof. The composition of the bond layer 10 is however different from the sacrificial layer 11 and selected such that an etchant used for removing the sacrificial layer 11 does not or not substantially affect the bond layer 11, the first contact layer 7, the material layer 10 and any other exposed surface(s) of the semiconductor

layer stack 3. The bond layer 14 can for example be provided by means of a spin-on process or sputtering the material of the bond layer 14 onto the sacrificial layer 11 and into the recesses 13. The bond layer material within the recesses 13 contacting the exposed portion(s) of the material layer 10 and/or the semiconductor layer stack 3 together with the rest of the bond layer 14 forms a later holding structure 18 for the optoelectronic device(s).

A temporary carrier 15 is then attached to the bond layer 14 as shown in figure 9, for example by means of bonding. After the attachment of the temporary carrier 15, the growth substrate 2 as well as a potential buffer layer is removed, as shown in figure 10, to expose the backside of the semiconductor layer stack 2, in particular the first layer 4. The semiconductor layer stack 3, in particular the first layer 4 is then thinned to remove the connected residue of the first layer 4. By means of this, the semiconductor layer stack portions later forming an optoelectronic device are singulated and access to the sacrificial layer 11 is provided. The growth substrate removal and/or thinning can for example comprise LLO, grinding, dry etching, wet etching, CMP, or combinations thereof. After the step of thinning, portions of the semiconductor layer stack 3 are separated each exposing a bottom surface 17 of the semiconductor layer stack portions.

Figures 11A and 12A then show two possible subsequent steps for processing the optoelectronic devices, whereas figures 11B and 12B show two other possible subsequent steps of a further embodiment for processing the optoelectronic devices.

As shown in figure 11A, a structured second contact layer 16 is provided on the semiconductor layer stack 3, in particular on the bottom surfaces 17, electrically contacting the first layer 4 of the semiconductor layer stack portions. In the embodiment shown, the bottom surfaces 17 form a light emitting surface of the later optoelectronic devices, thus the second contact layer 16 is in particular to be of a transparent conductive material such as ITO.

As shown in figure 12A, the sacrificial layer 11 is then removed to expose the optoelectronic devices 1 attached to the holding structure 18. Due to the good accessibility of the sacrificial layer 11, also in the region between the bond layer 14 and the semiconductor layer stack 3, the sacrificial layer 11 can easily be removed. The removal of the sacrificial layer 11 can for example be done by one of dry-etching, wet-etching or plasma-etching. The selected removal process thereby depends on the combination of the material of the material layer 10, the first contact element 7 as well as the material of the bond layer 14. The optoelectronic device 1 is then held by the holding structure 18, defining a specific adhesion force at the interface between the holding structure 18 and the first contact element 7. This will allow an easy subsequent transfer process onto a target substrate.

As shown in figure 11B and 12B on the other hand, first the sacrificial layer 11 is removed before a structured second contact layer 16 is provided on the semiconductor layer stack 3, in particular on the bottom surfaces 17, electrically contacting the first layer 4 of the semiconductor layer stack portions. The removal of the sacrificial layer 11 exposes the optoelectronic devices 1 attached to the holding structure 18 and can be done by one of dry-etching, wet-etching, plasma-etching. Again the selected removal process depends on the combination of the material of the material of the material layer 10, the first contact element 7 as well as the material of the bond layer 14. Due to the sacrificial layer 11 already being removed, the deposition of the second contact layer 16 is self-structured, leading to residues of the second contact layer 16 remaining on the bond layer 14 between the optoelectronic devices 1, as shown in figure 12B.

Figures 13A to 13C show embodiments of optoelectronic devices 1 connected to different holding structures 18 in accordance with some aspects of the proposed principle. As indicated in figure 13A compared to figure 12A, the holding structure 18 can also be configured to be arranged contacting the material layer 10 at one, two or even more positions of the optoelectronic device 1. As indicated in figure 13B, the holding structure 18 can also be configured to be arranged contacting the material layer 10 at a side surface or at side surfaces

of the optoelectronic device 1. As indicated in figure 13C, the holding structure 18 can also be configured to be arranged contacting two or more optoelectronic devices 1 at a time for example contacting the material layer 10 at a side surface of the optoelectronic devices 1.

5 The shown embodiments are however only to be understood as exemplary and shall not be limiting in any way. The shown structures can for example be combined or changed in any possible way.

10 Figures 14A to 14C shown further steps of processing an optoelectronic device 1 as shown in figure 12A in accordance with some aspects of the proposed principle. Figures 14A to 14C show in particular possible embodiments of transferring the optoelectronic devices to for example a target substrate.

15 Figure 14A for example shows a transfer stamp 19, by means of which a single or several optoelectronic devices 1 can be picked and removed from the holding structure 18 to transfer the optoelectronic device(s) 1 to a target substrate. Therefore, a holding force of the transfer stamp 19 needs to be larger than a holding force of the interface
20 between the optoelectronic device(s) 1 and the holding structure 18.

Figure 14B on the other hand shows a transfer by lamination of the optoelectronic devices to a LIFT carrier 21 with a release layer 20 arranged on top. Therefore, the adhesiveness of the release needs to
25 be larger than the adhesiveness of the interface between the optoelectronic device(s) 1 and the holding structure 18.

As a third alternative figure 14C shows a direct transfer of the optoelectronic devices 1 onto solder pads 23 of a target substrate 22
30 by means of a LIFT process. Chosen optoelectronic devices 1, which are positioned above a respective solder pad 23, and in particular the holding structure 18 holding these optoelectronic devices 1 is therefore irradiated by laser light L, such that the holding structure 18 or at least the interface between the holding structure 18 and the
35 respective optoelectronic device 1 decomposes and the optoelectronic devices falls onto the solder pad 23. At least for this embodiment, it can for example be desired that the first contact layer 7 is of a

transparent conductive material, whereas the second contact layer 16 can for example comprise a solder material.

Figures 15 to 27 show steps of a further embodiment for processing an optoelectronic device in accordance with some aspects of the proposed principle. In difference to the embodiment already described for the previous figures, the resulting optoelectronic device is contactable as a flip chip and not, as shown in the previous figures as a vertical contactable optoelectronic device. Exemplary the processing is shown for only one optoelectronic device. It is however to be understood that more than one optoelectronic device can be processed in the described way.

The first two steps as shown in figures 15 and 16 are thereby comparable to the ones already described in figures 1 and 2. Figure 17 shows a step of mesa etching, as shown in figure 3 with the difference that the step is one of two mesa etching steps performed, wherein the first mesa etching step shown is performed such that the etching does not go through the whole first layer 4 but stops well before reaching the growth substrate 2. In particular the etching is performed to a first depth d_1 smaller than a thickness t of the semiconductor layer stack 3, wherein the first depth d_1 is chosen such that the first etching goes through the second layer 5 and the active region 6. The exposed portions are thereby as shown in cross section in form of trapezoids arranged on a residue of the first layer 4 and comprises besides the top surface 8 first side wall portions 9a.

In a following step, as shown in figure 18, a first material layer 10a is provided on the mesa etched structure following the shape of the mesa etched structure. The first material layer 10 is provided such that it covers at least partially the top surface 8, the first contact element 7 and the first side wall portions 9. The first material layer 10a is for example of SiO_2 and any other suitable material for providing an isolation/passivation of portions of the first contact element 7 and the first side wall portions 9a. Between the first material layer 10a and the first side wall portions 9a, for example a regrowth layer

can be arranged for enhancing the internal quantum efficiency within the later optoelectronic devices.

As shown in figure 19, a second mesa etching step is then performed into remaining portions of the semiconductor layer stack 3 to a second depth d_2 smaller than the thickness t of the semiconductor layer stack 3 but larger than the first depth d_1 . The first material layer 10a can for example act as a mask for the second etching step such that the etching results in second side wall portions 9b adjacent to the first side wall portions 9a. Similar to the first mesa etch, the second etch stops prior to reaching the growth substrate 2. Consequently, a continuous portion of the semiconductor layer stack 3 remains on the growth substrate 2. Prior of after the second mesa etch the first material layer 10a is structured to partially expose the first contact layer 7.

A second material layer 10b is then, as shown in figures 20A and 20B, provided on portions of the first material layer 10a and the second side wall portions 9b. The second material layer is in particular of a conductive material providing a bottom contact element for the optoelectronic devices. The second material layer 10b can for example, as shown in figure 20B and indicated by means of the circle, comprise material accumulation(s) contacting a top surface of the first layer 4 laterally adjacent to a first side wall portion 9a to reduce the contact resistance between the second material layer 10b and the first layer 4. It is however also conceivable that the second material layer 10b does not comprise material accumulation(s) but follows the underlaying shape with a constant thickness.

The steps shown in figures 21 to 25 are than again comparable to the steps described in figures 5 to 10, with depositing and planarizing the sacrificial layer 11, structuring the sacrificial layer 11 generating recess 13, providing bond layer 14 and temporary carrier layer 15, removing the growth substrate 2 and thinning the semiconductor layer stack 3.

Figure 26 further shows a step of providing an optical structure 24 on the bottom surface 17, to enhance a light extraction through the bottom surface 17 of the later optoelectronic device. On top of the optical structure 24, as shown in figure 27, the second contact layer in form of a transparent conductive material is provided electrically coupled to the first layer 4 and the second material layer 10b. The sacrificial layer 11 is then removed exposing the optoelectronic device 1 attached to the holding structure 18.

Figures 28A and 28B show two embodiments of possible arrangements of the holding structure 18. It is possible to choose an interface between the holding structure 18 and the second material layer 10b, as shown in figure 28A, to choose an interface between the holding structure 18 and the first material layer 10a, as shown in figure 28B, or, as not shown, to choose an interface between the holding structure 18 and the a contact material contacting the first contact layer 7 through the first material layer 10a. It is however to be understood that the holding structure 18 can also be formed according to the embodiments shown in figure 13A to 13C or variations thereof.

Figure 28C shows a further embodiment of a flip-chip configuration optoelectronic device which can be processed according to the proposed principle. The optoelectronic device comprises a recess through the semiconductor layer stack 3 to be able to provide a bottom contact element 25 at the top surface 8 contacting the first layer 4.

LIST OF REFERENCES

	1	optoelectronic device
	2	growth substrate
5	3	semiconductor layer stack
	4	first layer
	5	second layer
	6	active region
	7	contact layer
10	8	top surface
	9, 9a, 9b	side wall
	10, 10a, 10b	material layer
	11	sacrificial layer
	12	even surface
15	13	recess
	14	bond layer
	15	temporary carrier
	16	contact layer
	17	bottom surface
20	18	holding structure
	19	transfer stamp
	20	release layer
	21	LIFT carrier
	22	target substrate
25	23	bond pad
	24	optical structure
	25	bottom contact element
	L	laser radiation

CLAIMS

1. Method for processing an optoelectronic device, comprising the steps of:

- 5 - providing a growth substrate having a semiconductor layer stack epitaxially deposited thereupon;
- conducting a mesa etching process to form sidewalls of the layer stack, said sidewalls covered by a material layer;
- depositing a sacrificial layer covering the sidewalls of the
- 10 material layer and extending above a top surface of the semiconductor layer stack, said sacrificial layer comprising one of:
 - o a metal-oxide; and
 - o an organic material;
- 15 - planarizing the sacrificial layer to form an even surface above the top surface of the semiconductor layer stack;
- structuring the sacrificial layer to form a recess thereby exposing a portion of the material layer and/or the layer stack;
- depositing a bond layer into the recess, the bond layer in
- 20 particular comprising one of:
 - o an organic material;
 - o a nitride-based material;
 - o a gold alloy; and
 - o a metallic solder material;
- 25 - attaching a temporary carrier to the bond layer;
- removing the growth substrate, thereby exposing portions of the sacrificial layer and the semiconductor layer stack.

2. Method according to claim 1, wherein conducting a mesa etching

30 process comprises the steps of:

- Depositing a structured mask on the semiconductor layer stack, in particular of a material suitable as a contact layer;
- Conducting a first mesa etch to a depth smaller than a thickness of the semiconductor layer stack;
- 35 - Cleaning the sidewalls and depositing a first material on sidewalls, in particular regrowing a layer on the sidewalls, in particular depositing the material layer.

3. Method according to claim 2, further comprising the steps of
- conducting a second mesa etch into remaining portions of the layer stack to a depth smaller than a thickness of the semiconductor layer stack; and
 - 5 - cleaning the exposed sidewalls and depositing a second material on sidewalls, in particular depositing the material layer on the exposed sidewalls and the first material.
4. Method according to any of the preceding claims, wherein the
- 10 material layer covering sidewalls comprises at least partially a reflective material, in particular a metal.
5. Method according to any of the preceding claims, wherein the material of the sacrificial layer is selected from:
- 15 - ZnO if the material layer comprises SiO₂ and a contact layer on the top surface of the semiconductor layer stack optionally comprises Au or Ag;
 - Polystyrene, particularly solute in Ethylacetate or Toluol, if the material layer comprises SiO₂ and a contact layer on the top
 - 20 surface of the semiconductor layer stack comprises Au or Ag;
 - Polystyrene, particularly melted and planarized by pressing if a contact layer on the top surface of the semiconductor layer stack comprises one of Au and Ag or an Au containing alloy;
 - Polyvinylalcohol, PVA, if the material layer comprises SiO₂ or
 - 25 Si₃N₄;
 - Polyvinylacetate, PVAc, if the material layer comprises SiO₂ or Si₃N₄; and
 - Soft-baked photoresist, if a contact layer on the top surface of the semiconductor layer stack comprises one of Au and Ag or an
 - 30 Au containing alloy.
6. Method according to any of the preceding claims, wherein the step of depositing and planarizing the sacrificial layer comprises one of:
- 35 - spinning of the sacrificial layer material;
 - sputtering of the sacrificial layer material;
 - spraying of the sacrificial layer material; and

- melting of the sacrificial layer material;
 - pressing of molten or low viscous sacrificial layer material;
- wherein

optionally the step of planarizing the sacrificial layer to form an even surface above the top surface of the semiconductor layer stack is conducted by the selected deposition techniques.

7. Method according to any of the preceding claims, wherein structuring the sacrificial layer comprises:

- depositing a structured photo resist layer as to expose surface portions of the sacrificial layer; and
- etching, in particular one of wet or dry etching the exposed surface portions of sacrificial layer, wherein the recess is formed above at least one of
 - o the top surface of the semiconductor layer stack, in particular a contact layer or the material layer;
 - o a sidewall portion of the semiconductor layer stack or the material layer; and
 - o adjacent to a sidewall portion of the semiconductor layer stack.

8. Method according to any of the preceding claims, wherein the step of depositing a bond layer into the recess comprises one of:

- gas phase or vapor depositing of the bond layer material;
- spinning of the bond layer material;
- sputtering of the bond layer material;
- spraying of the bond layer material;
- melting of the bond layer material; and
- pressing of molten or low viscous bond layer material.

9. Method according to any of the preceding claims, wherein the bond layer material comprises one of an Benzocyclobuthene or an epoxy resin, that is at least partially cured at room temperature or slightly elevated temperature, particularly if the sacrificial layer comprises an organic compound.

10. Method according to any of the preceding claims, wherein

the bond layer material comprises polystyrene if the sacrificial layer comprises PVA; or

the bond layer material comprises epoxy resin or Benzocyclobuthene if the sacrificial layer comprises polystyrene.

5

11.Method according to any of the preceding claims, wherein the bond layer material comprises a solder material, in particular containing Gold, Tin or Indium.

10

12.Method according to any of the preceding claims, wherein the step of attaching a temporary carrier comprises the step of curing the bond layer using thermal or optical measures.

15

13.Method according to any of the preceding claims, wherein the step of removing the growth substrate comprises at least one of:

- grinding;
- polishing;
- chemical mechanical polishing;
- wet etching;
- dry etching;
- or combinations thereof

20

of the semiconductor material of the semiconductor layer stack.

25

14.Method according to any of the preceding claims, further comprising depositing, particular by one of sputtering, PVD, or PEVCD of a contact material, in particular a transparent conductive oxide onto a bottom surface of the semiconductor layer stack opposite the top surface.

30

15.Method according to any of the preceding claims, further comprising providing optical structures on a bottom surface of the semiconductor layer stack opposite the top surface or a contact material on a bottom surface of the semiconductor layer stack opposite the top surface by one of:

35

- o Structuring the bottom surface or the contact material; or
- o Attaching an optical element onto the bottom surface or the contact material.

16. Method according to any of the preceding claims, further comprising at least one of:

- removing the sacrificial layer, in particular by one of dry-etching, wet-etching, plasma-etching, or dissolving in water or an organic solvent; and
- transferring the optoelectronic device onto a target substrate or a carrier for a subsequent LIFT process.

17. Array of optoelectronic devices processed by a method according to any of the preceding claims,

wherein the sacrificial layer is removed exposing bond layer material forming posts;

wherein a respective post is attached to a respective optoelectronic device; and

wherein a bottom surface of the optoelectronic device opposite the posts comprises one of a contact material and an optical element.

18. The array of claim 17, wherein the bond layer material comprises an organic compound, particularly including one of a at least partially cured epoxy resin, Benzocyclobuthene and polystyrene.

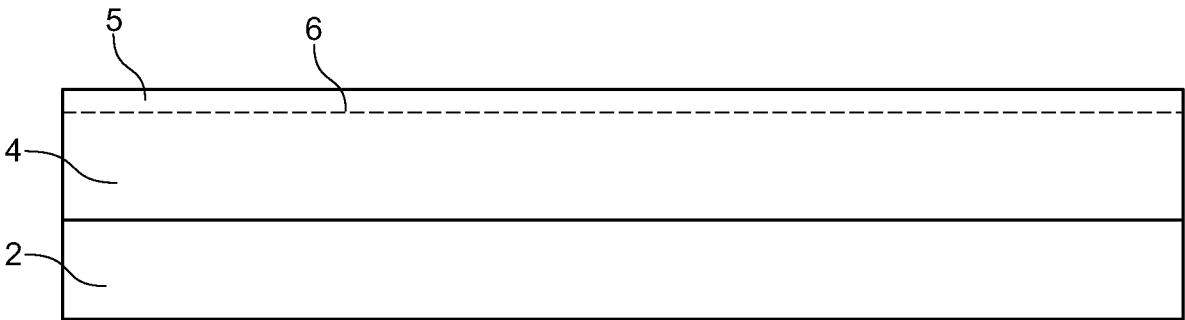


FIG. 1

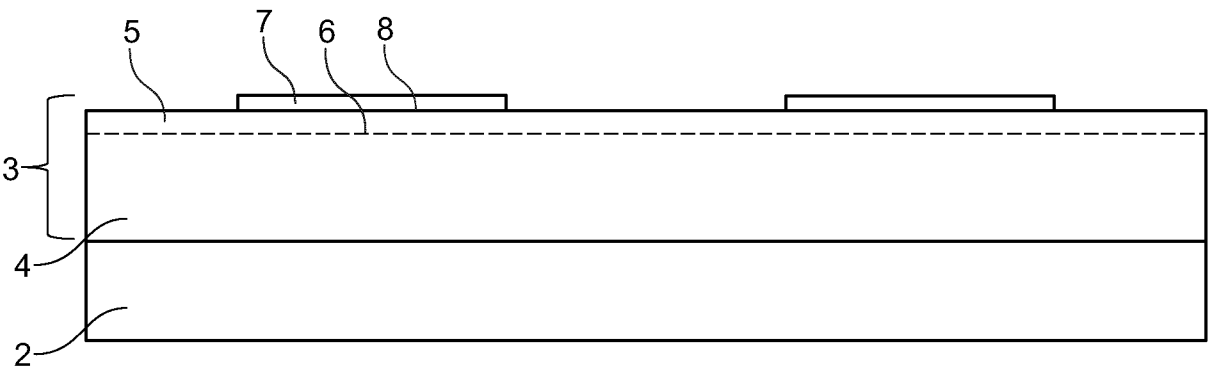


FIG. 2

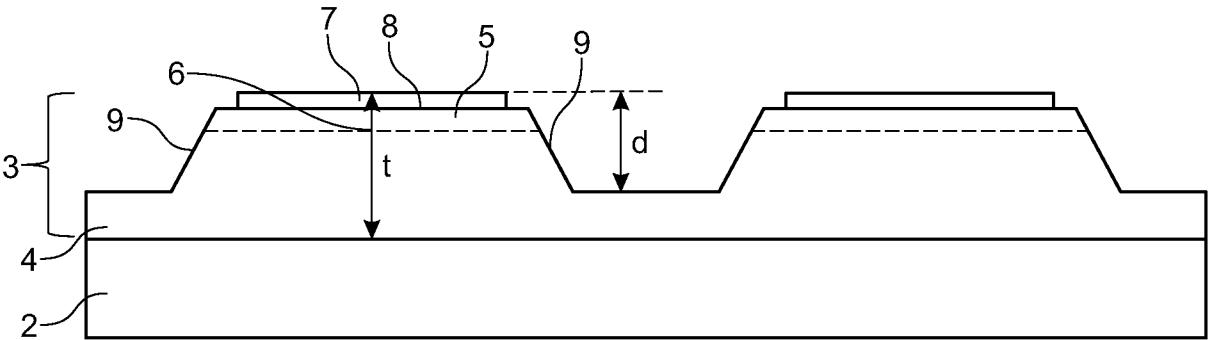


FIG. 3

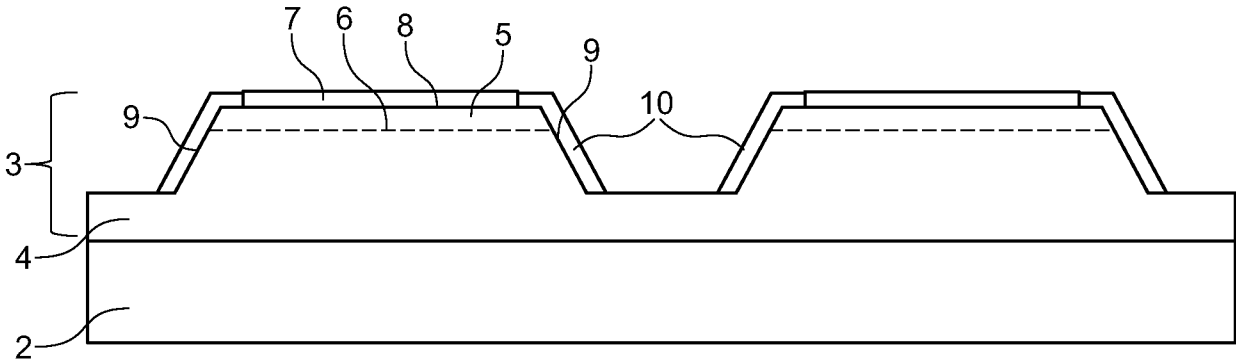


FIG. 4

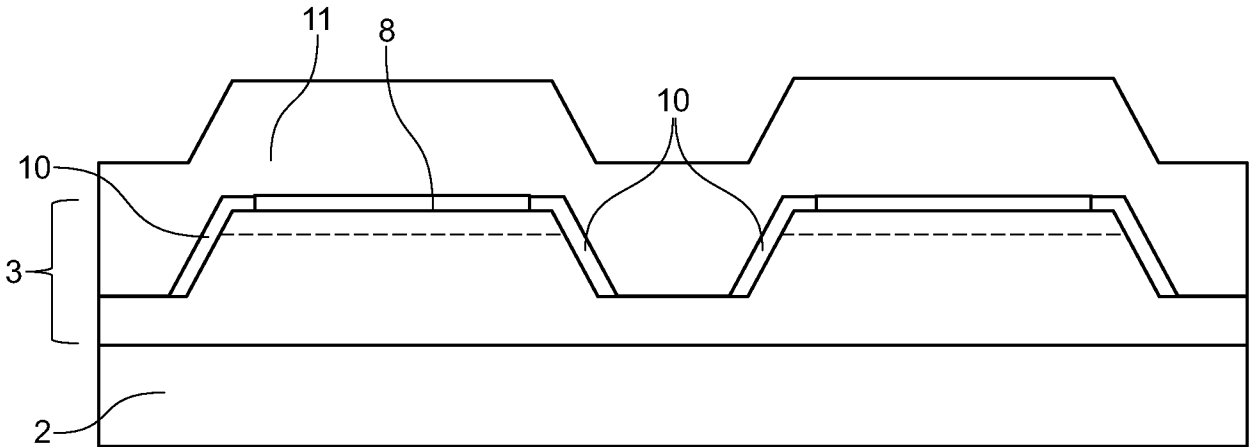


FIG. 5

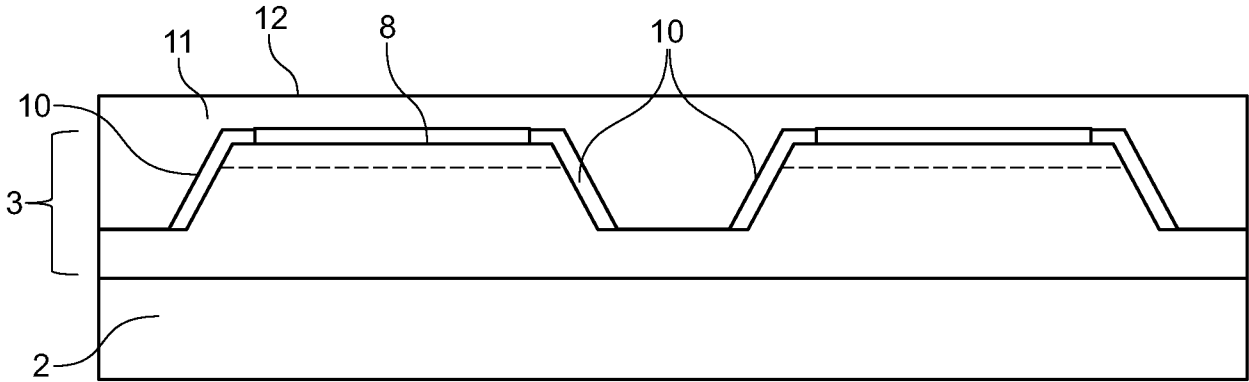


FIG. 6

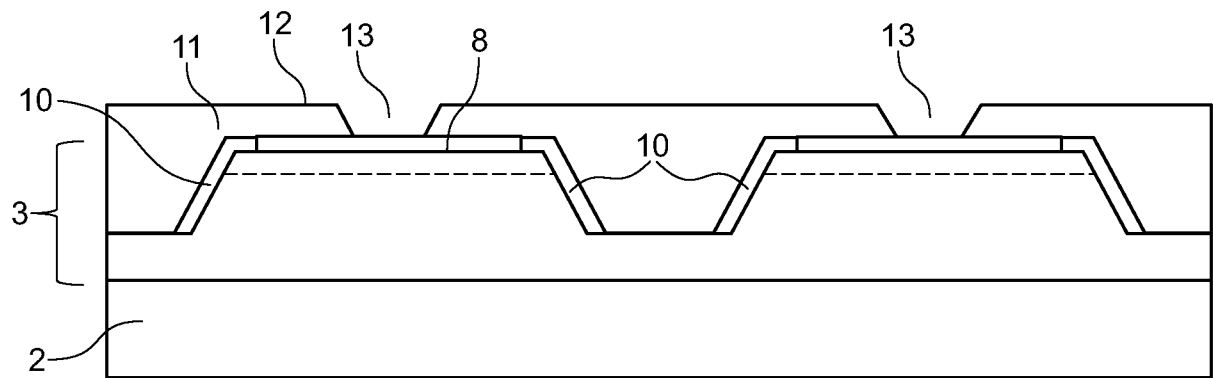


FIG. 7

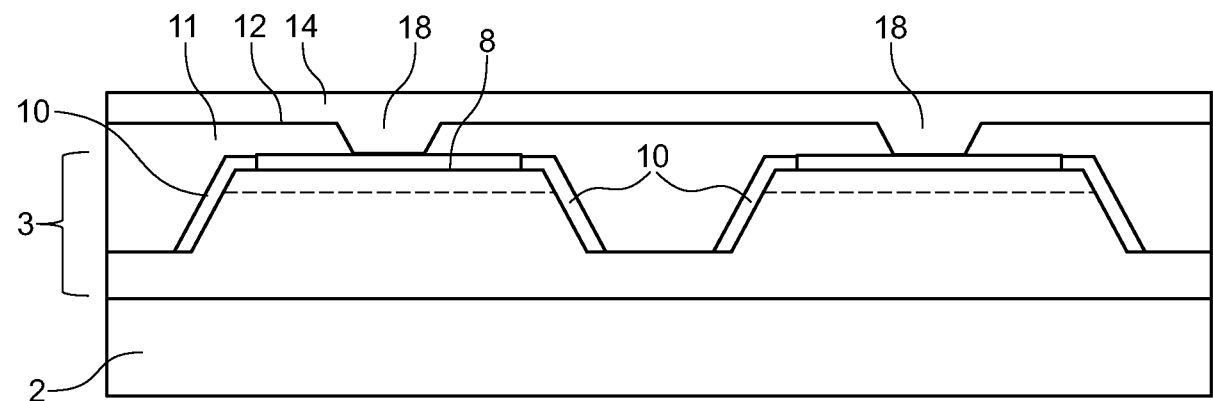


FIG. 8

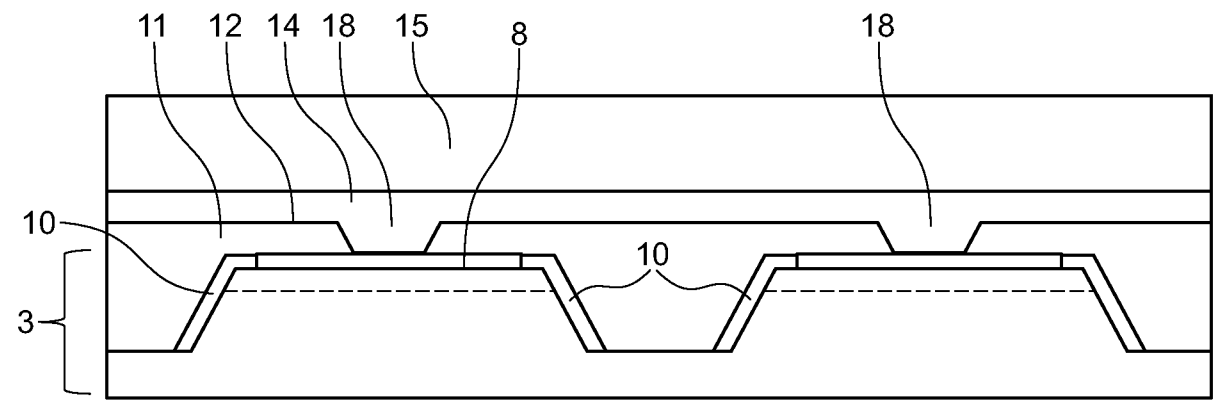


FIG. 9

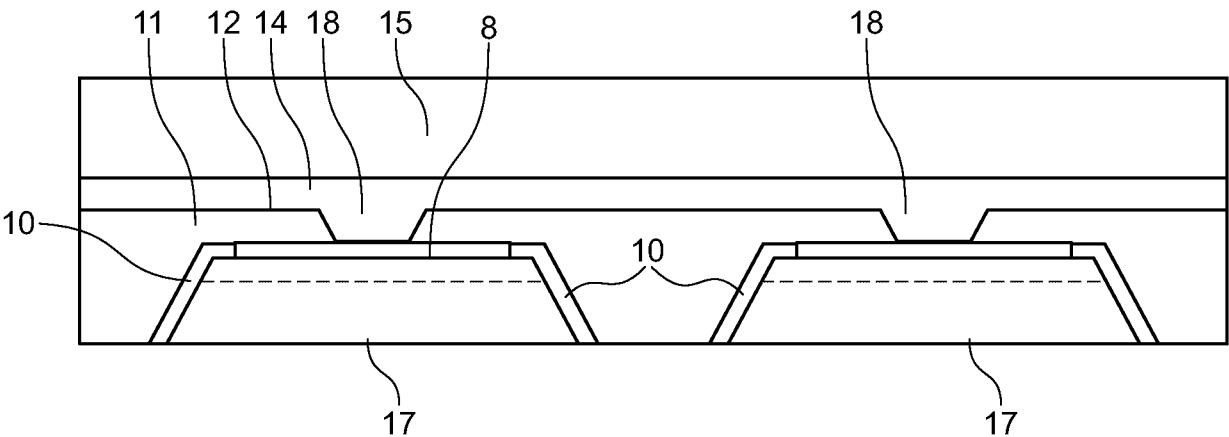


FIG. 10

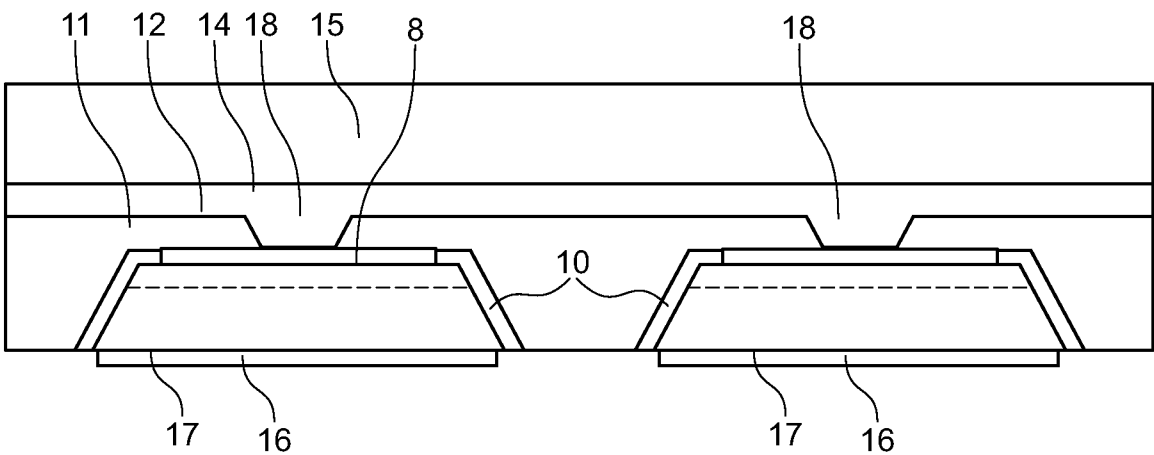


FIG. 11A

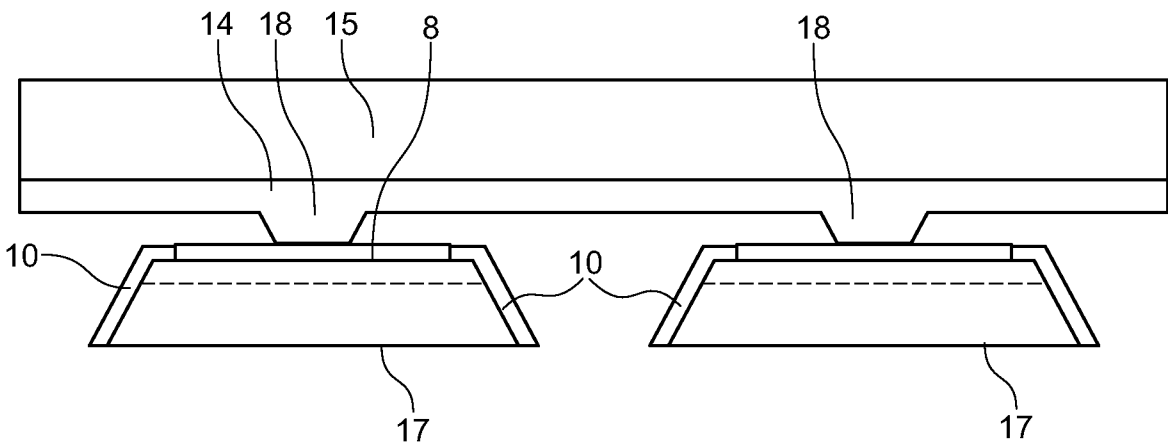


FIG. 11B

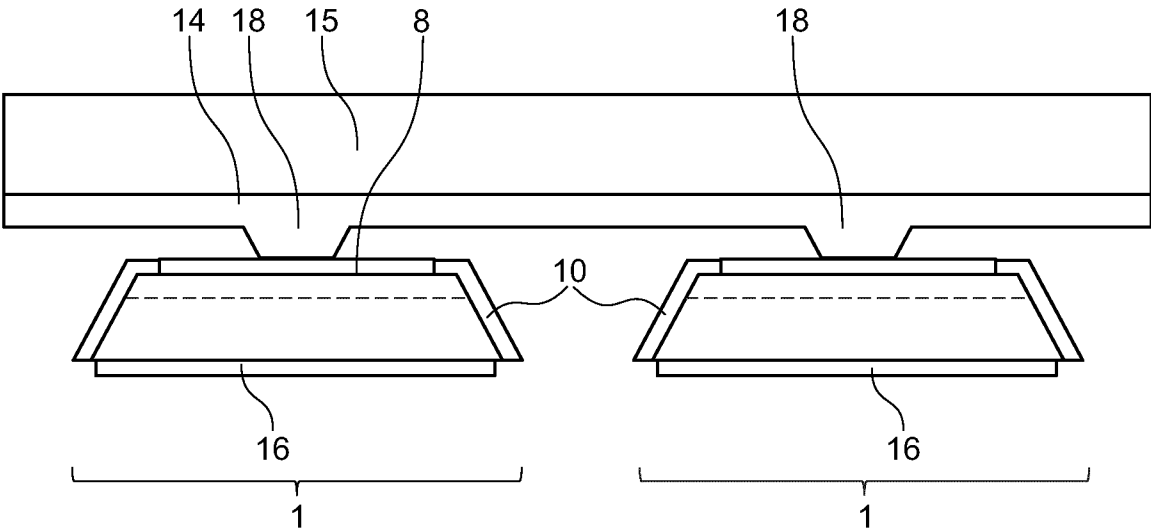


FIG. 12A

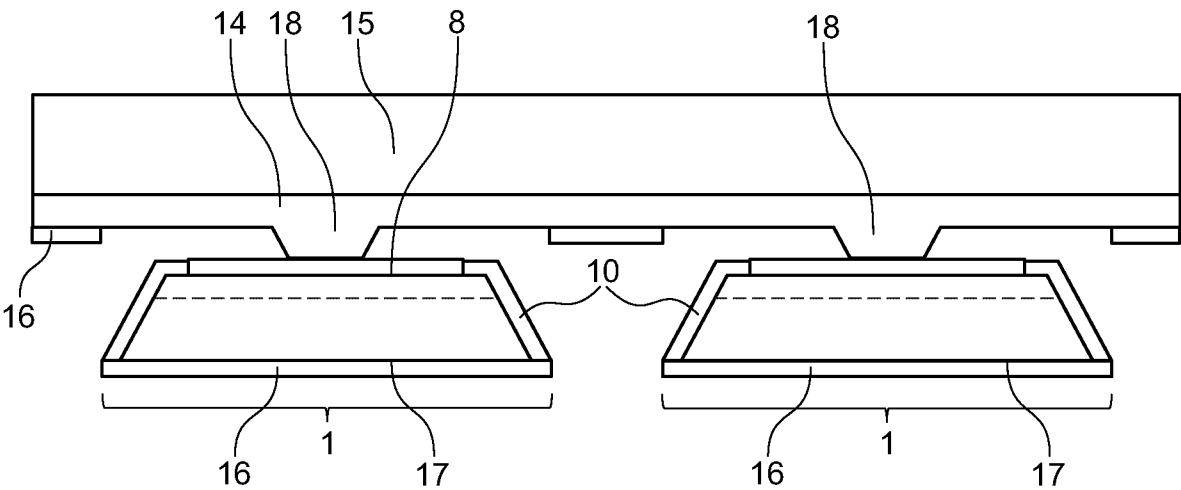


FIG. 12B

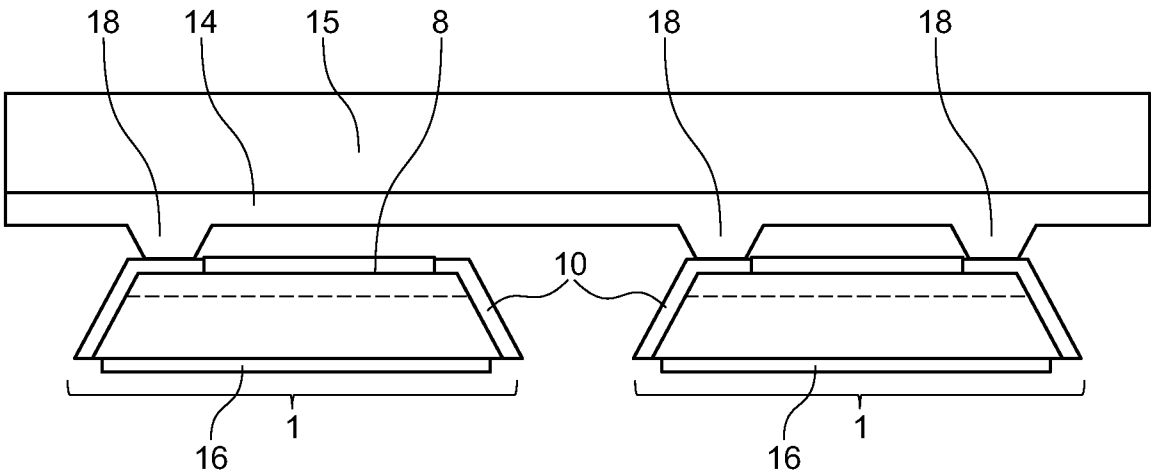


FIG. 13A

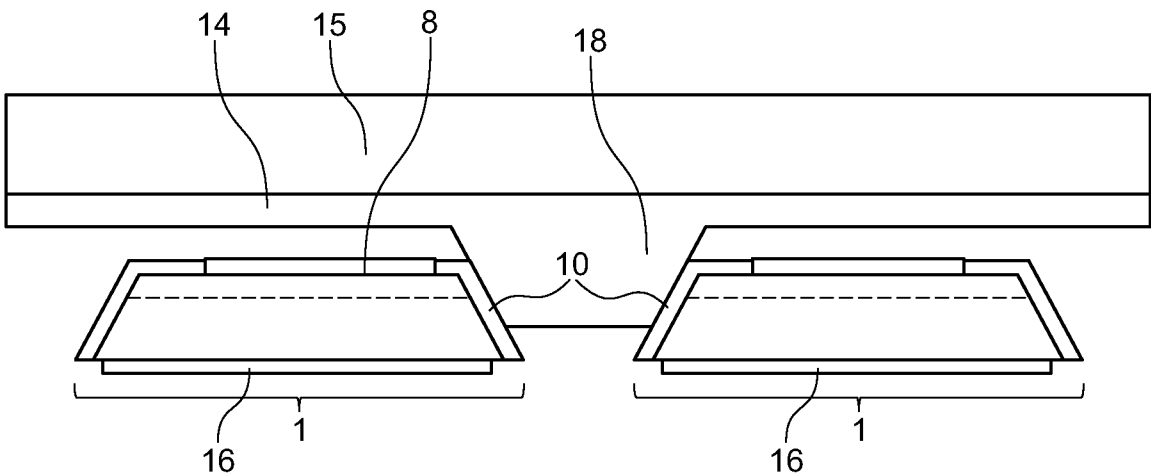


FIG. 13B

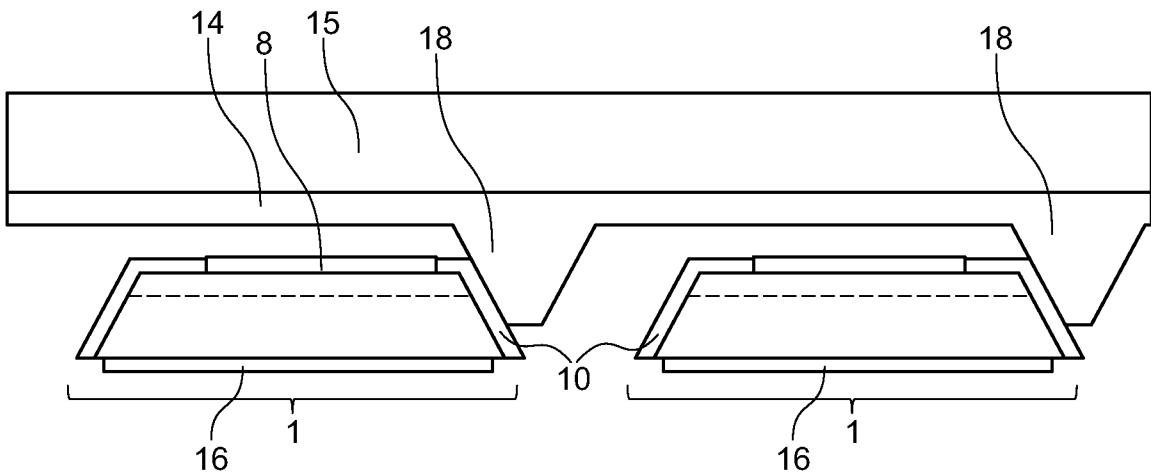


FIG. 13C

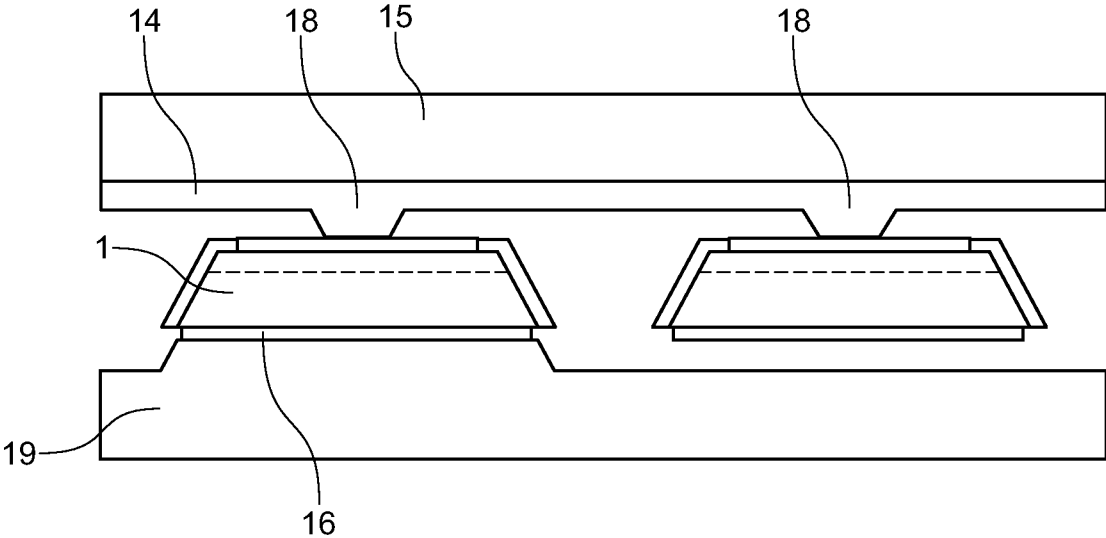


FIG. 14A

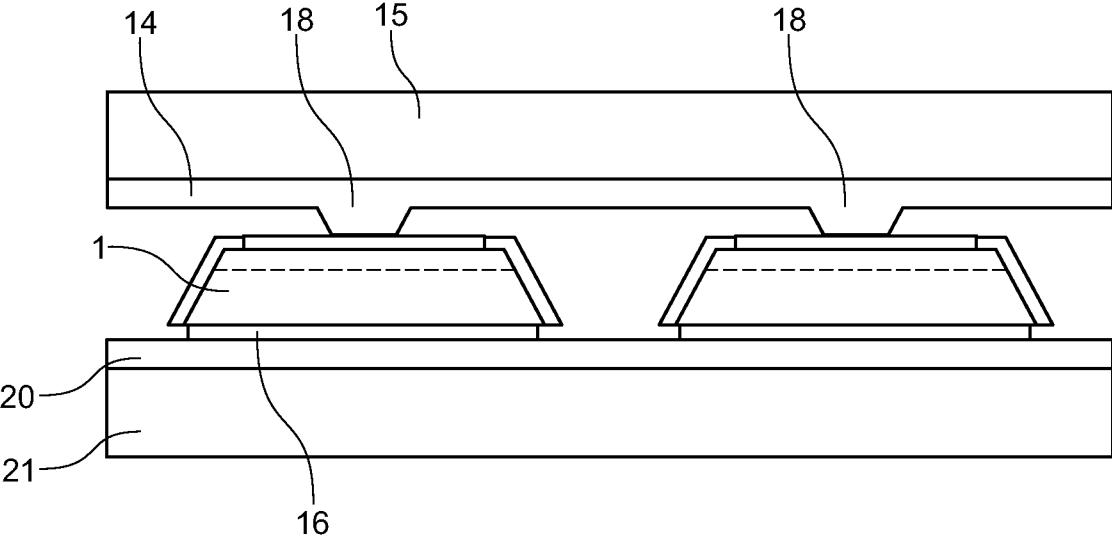


FIG. 14B

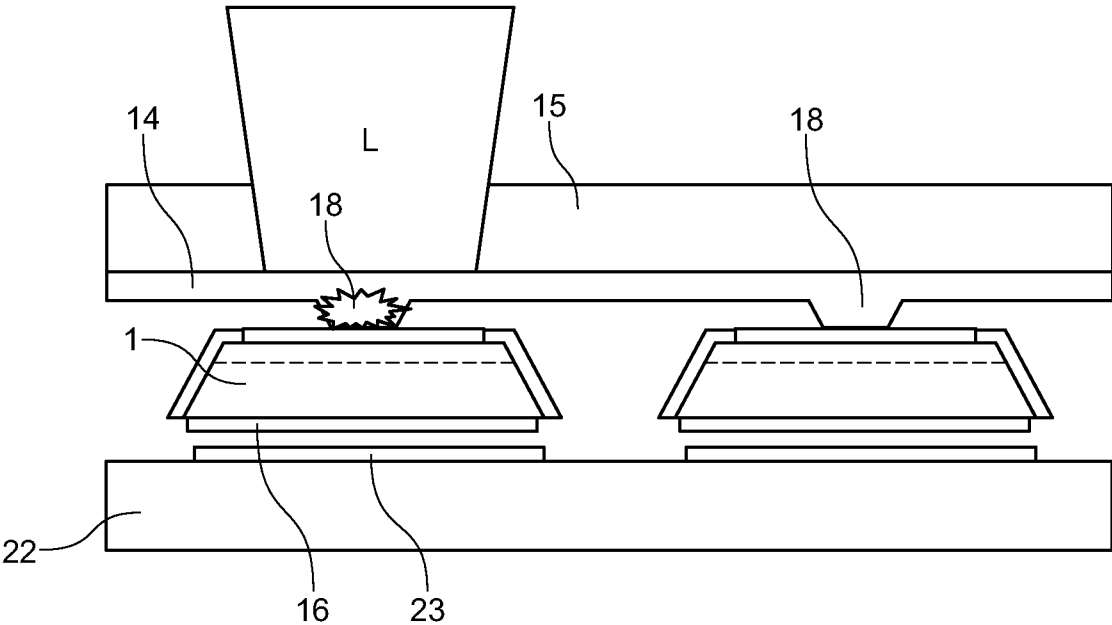


FIG. 14C

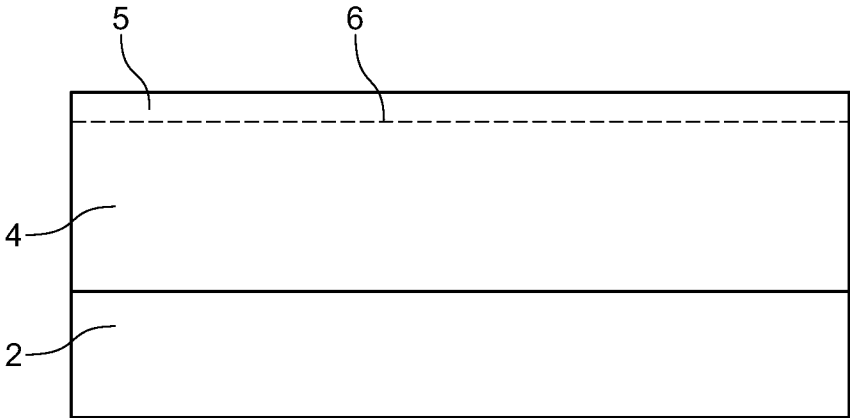


FIG. 15

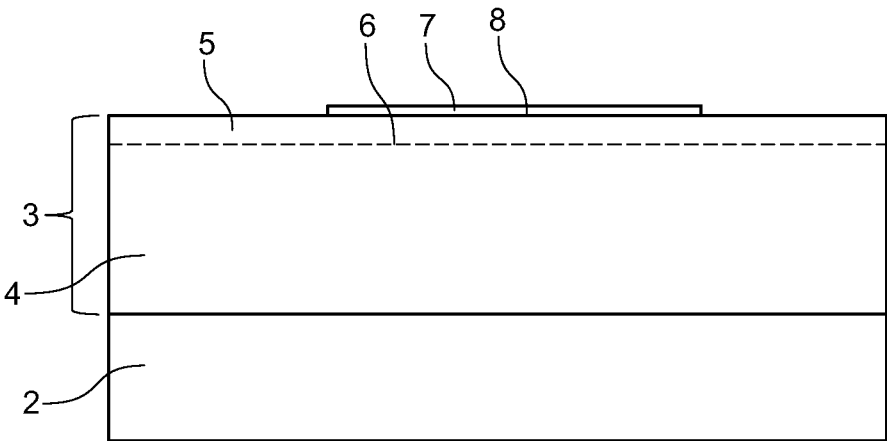


FIG. 16

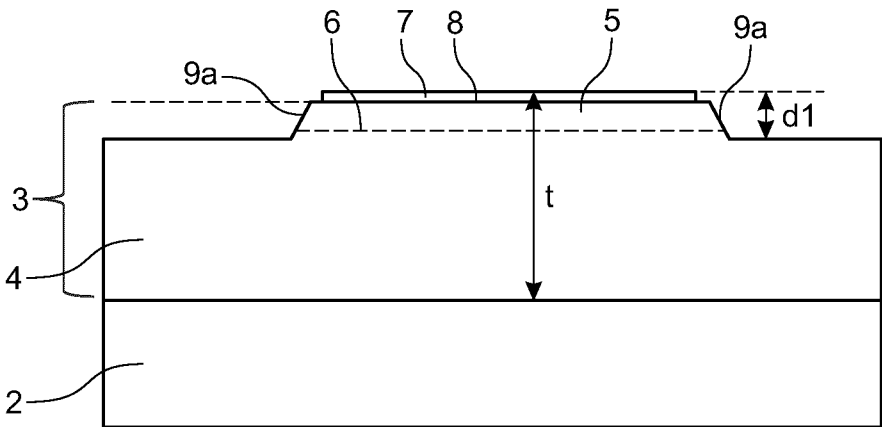


FIG. 17

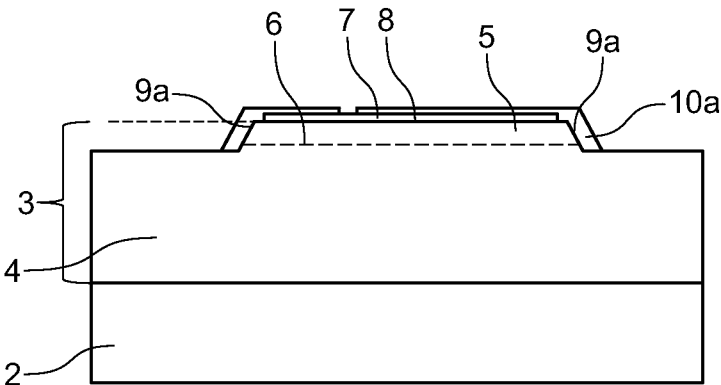


FIG. 18

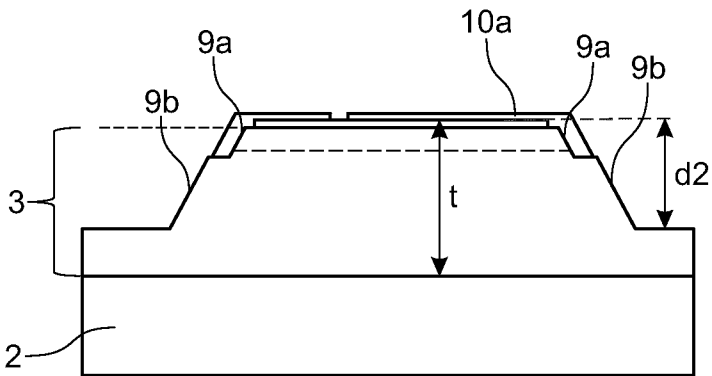


FIG. 19

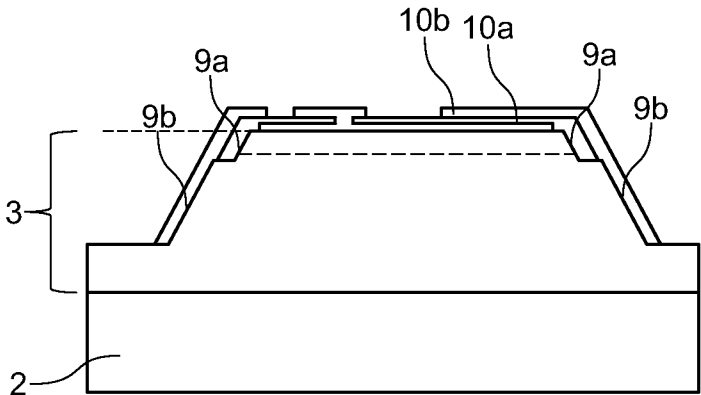


FIG. 20A

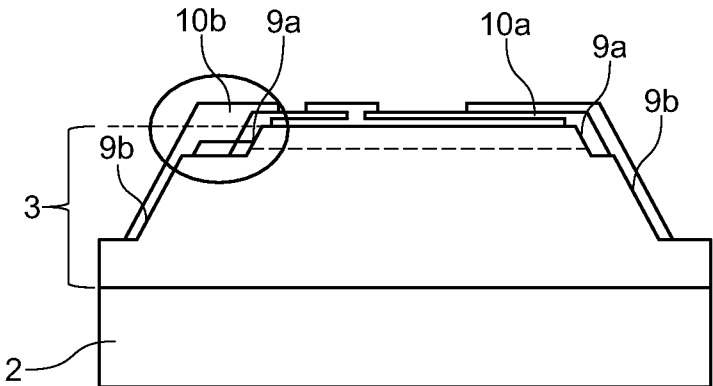


FIG. 20B

10/13

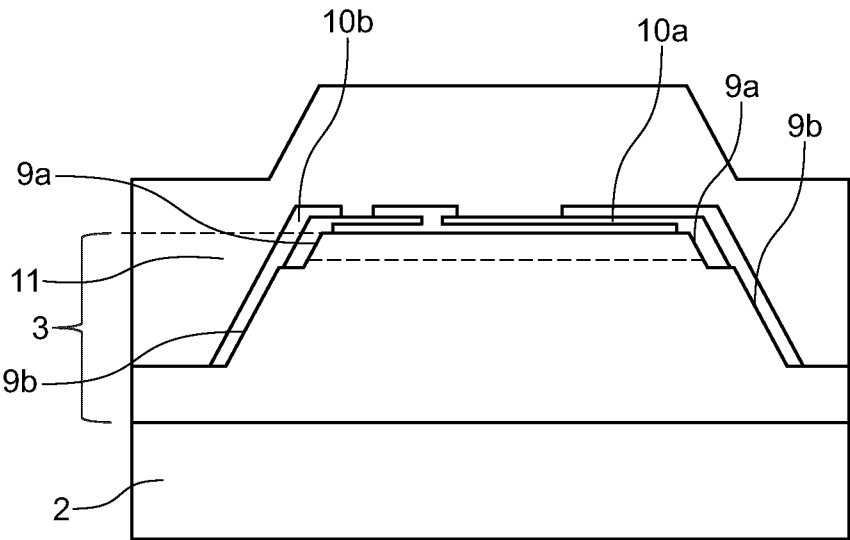


FIG. 21

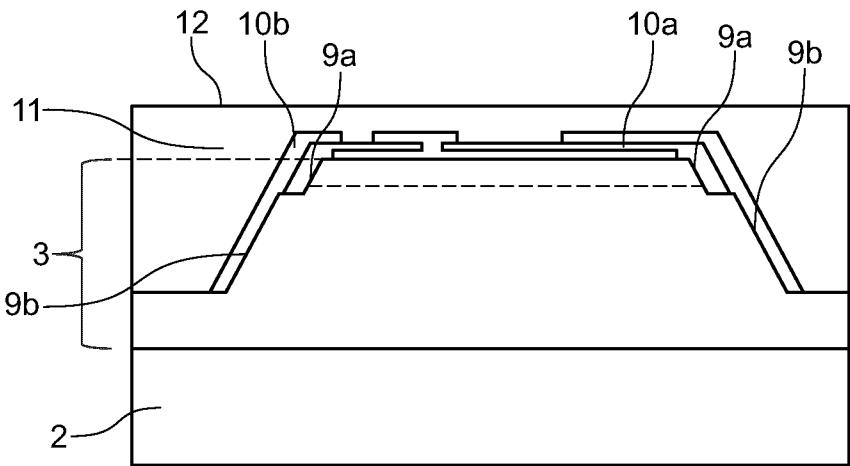


FIG. 22

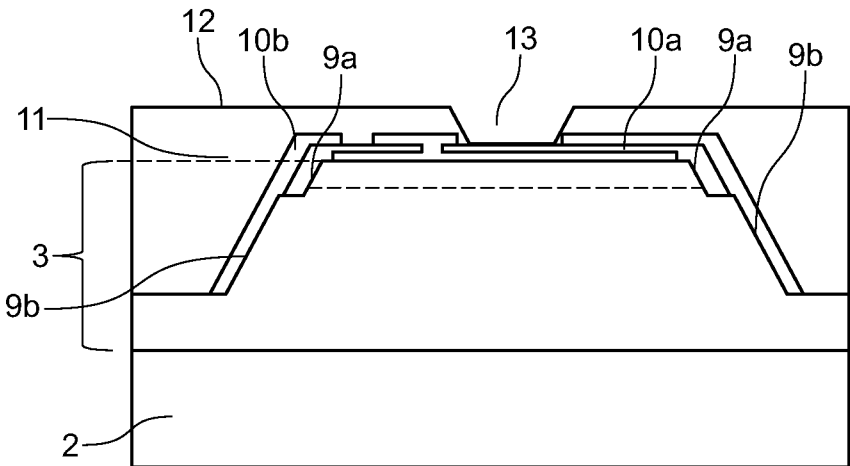


FIG. 23

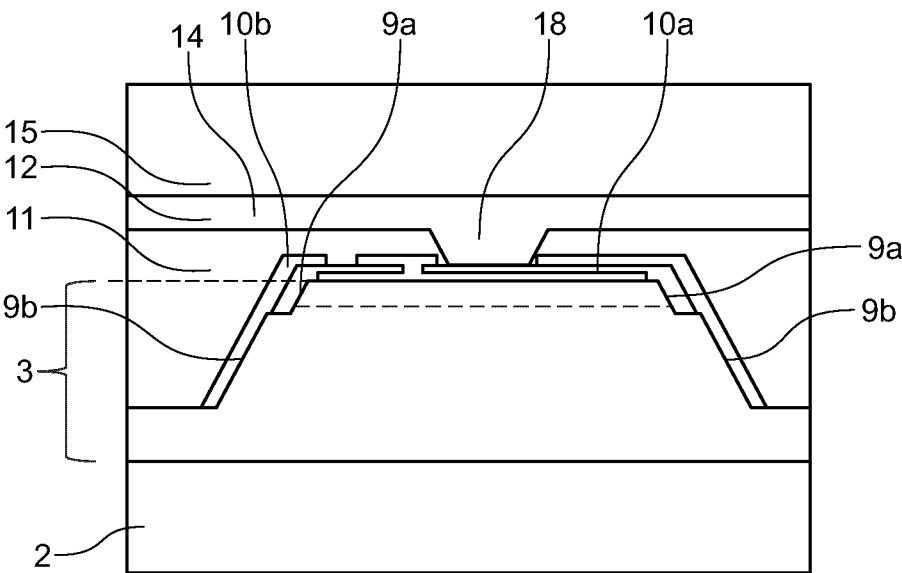


FIG. 24

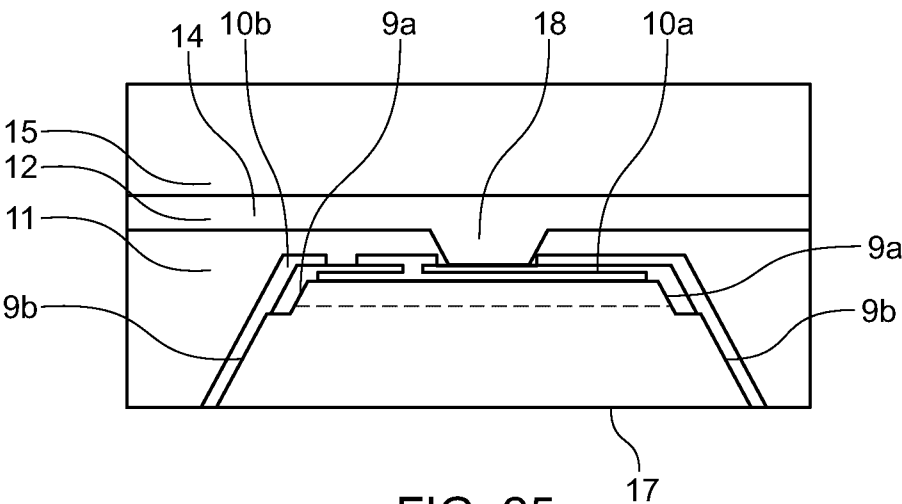


FIG. 25

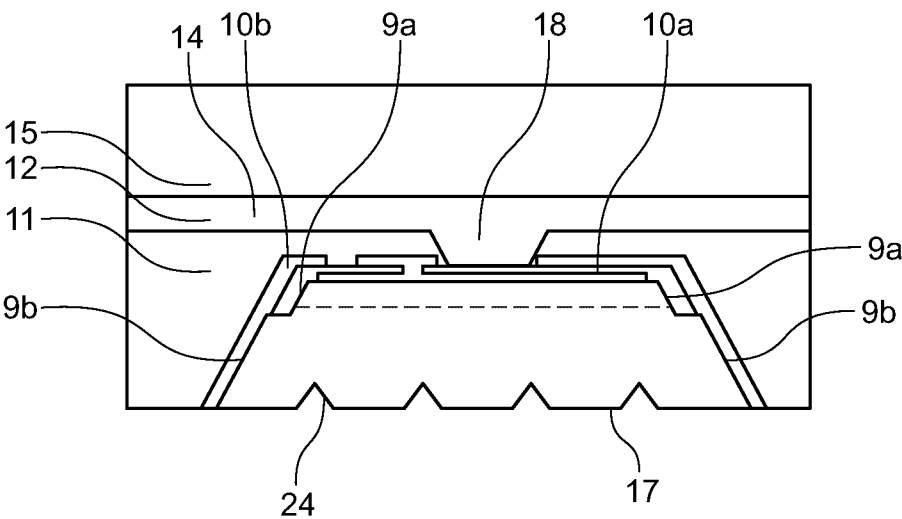


FIG. 26

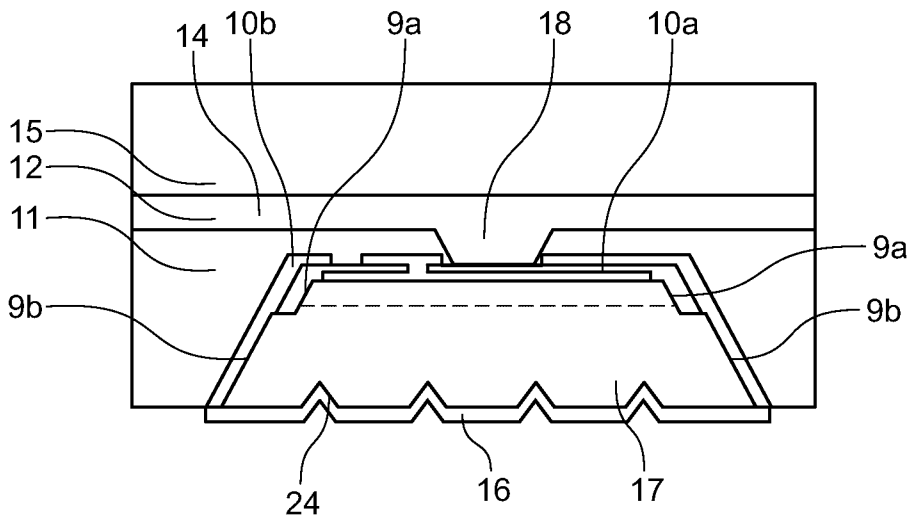


FIG. 27

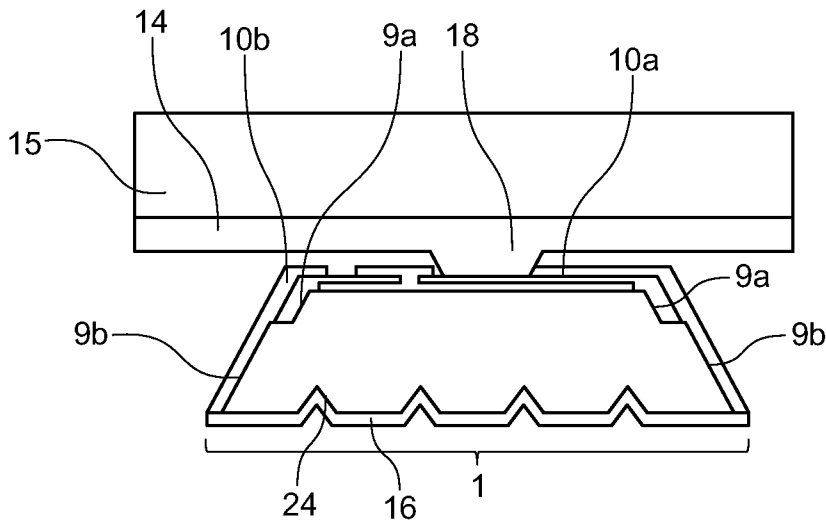


FIG. 28A

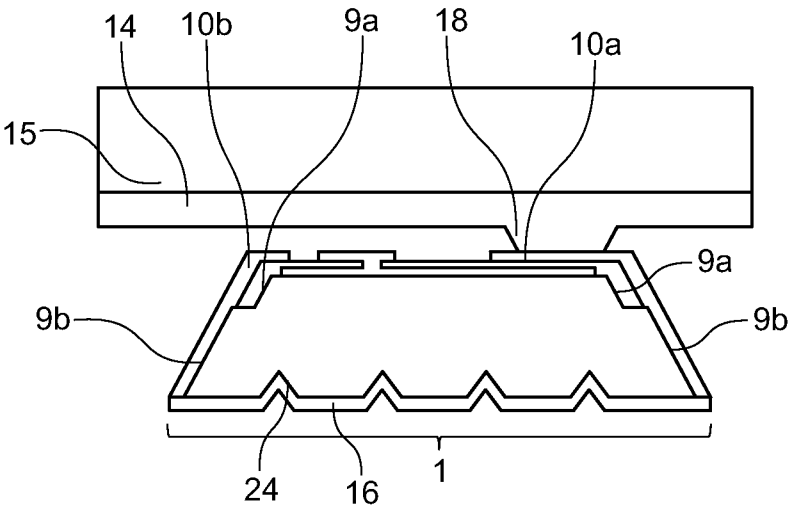


FIG. 28B

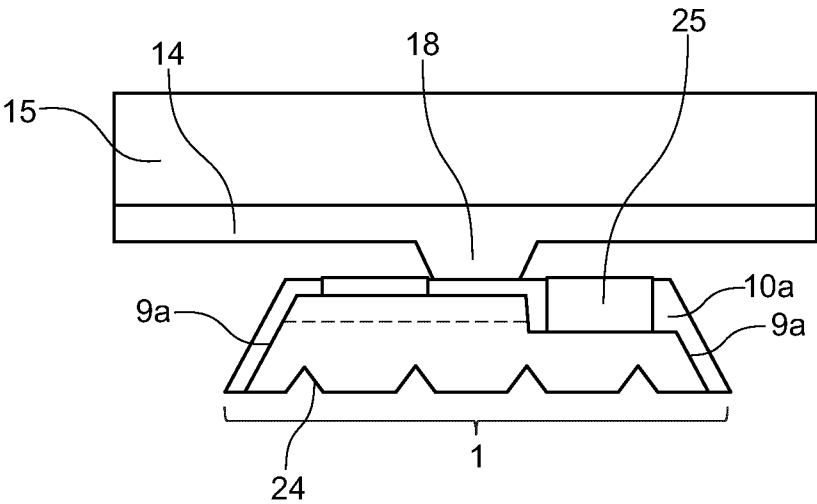


FIG. 28C

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/071604

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L33/00 H01L33/44 H01L33/40 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 9 035 279 B2 (LUXVUE TECHNOLOGY CORP [US]) 19 May 2015 (2015-05-19) column 9 - column 14; figures 2-10 -----	1 - 18
Y	TW I 671 811 B (UNIV ILLINOIS [US]) 11 September 2019 (2019-09-11) the whole document -----	1 - 18
A	US 2021/288222 A1 (YOUNG ERIK WILLIAM [US] ET AL) 16 September 2021 (2021-09-16) paragraph [0040] - paragraph [0083]; figures 1A-10 -----	1 - 18
A	KR 2014 0058080 A (SEOUL VIOSYS CO LTD [KR]) 14 May 2014 (2014-05-14) claims 1-20; figures 1-5 ----- - / - -	1 - 18
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 25 October 2024		Date of mailing of the international search report 07/11/2024
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer But, Gabriela-Ileana

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2024/071604

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015/179876 A1 (HU HSIN-HUA [US] ET AL) 25 June 2015 (2015-06-25) paragraph [0058] - paragraph [0083]; figures 2-15 -----	1 - 18

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2024/071604

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 9035279	B2	19-05-2015	CN	105359283 A	24-02-2016
			KR	20160018706 A	17-02-2016
			TW	201513405 A	01-04-2015
			US	2015008389 A1	08-01-2015
			US	2015214420 A1	30-07-2015
			US	2016071827 A1	10-03-2016
			US	2016308103 A1	20-10-2016
			WO	2015006000 A1	15-01-2015

TW I671811	B	11-09-2019	EP	2430652 A1	21-03-2012
			KR	20120065273 A	20-06-2012
			KR	20170018112 A	15-02-2017
			TW	201113940 A	16-04-2011
			TW	201606863 A	16-02-2016
			TW	201711095 A	16-03-2017
			US	2010317132 A1	16-12-2010
			US	2015132873 A1	14-05-2015
			US	2017200707 A1	13-07-2017
			WO	2010132552 A1	18-11-2010

US 2021288222	A1	16-09-2021	CN	115191033 A	14-10-2022
			EP	4118686 A1	18-01-2023
			JP	2023518180 A	28-04-2023
			KR	20220153042 A	17-11-2022
			US	2021288222 A1	16-09-2021
			WO	2021183411 A1	16-09-2021

KR 20140058080	A	14-05-2014	NONE		

US 2015179876	A1	25-06-2015	TW	201530809 A	01-08-2015
			US	2015179876 A1	25-06-2015
			WO	2015094600 A1	25-06-2015