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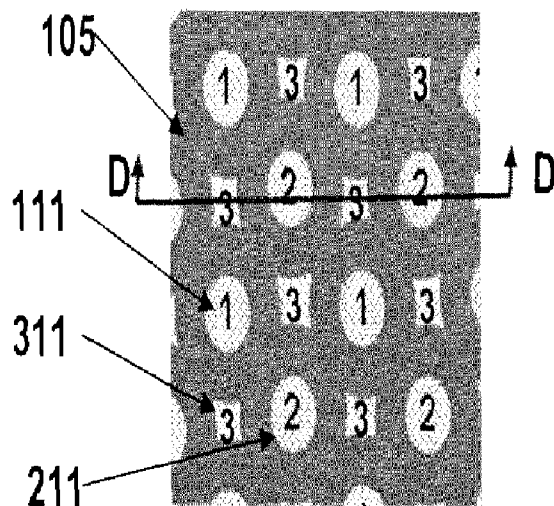


Fig. 2D

(57) Abstract: A method of making a device includes forming a first photoresist layer over a sacrificial layer, patterning the first photoresist layer to form first photoresist features, rendering the first photoresist features insoluble to a solvent, forming a second photoresist layer over the first photoresist features, patterning the second photoresist layer to form second photoresist features, forming a spacer layer over the first and second photoresist features, etching the spacer layer to form spacer features and to expose the first and second photoresist features, forming third photoresist features between the spacer features, removing the spacer features, and patterning the sacrificial layer using the first, second and third photoresist features as a mask to form sacrificial features.



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PATTERNING METHOD FOR HIGH DENSITY PILLAR STRUCTURES

BACKGROUND OF THE INVENTION

[0001] The invention generally relates to a method of making a semiconductor device, and more particularly, to a method of making semiconductor pillar structures.

[0002] Devices made from semiconductor materials are used to create memory circuits in electrical components and systems. Memory circuits are the backbone of such devices as data and instruction sets are stored therein. Maximizing the number of memory elements per unit area on such circuits minimizes their cost. As the dimensions for structures formed on a semiconductor wafer diminish, tools currently available to create these devices reach their limits.

SUMMARY

[0003] One embodiment of the invention provides a method of making a device including forming a first photoresist layer over a sacrificial layer, patterning the first photoresist layer to form first photoresist features, rendering the first photoresist features insoluble to a solvent, forming a second photoresist layer over the first photoresist features, patterning the second photoresist layer to form second photoresist features, forming a spacer layer over the first and second photoresist features, etching the spacer layer to form spacer features and to expose the first and second photoresist features, forming third photoresist features between the spacer features, removing the spacer features, and patterning the sacrificial layer using the first, second and third photoresist features as a mask to form sacrificial features.

[0004] Another embodiment of the invention provides a method of making a device including forming a sacrificial layer over a semiconductor seed layer, forming a hard mask layer over the sacrificial layer, forming a first photoresist layer over the hard mask layer, patterning the first photoresist layer to form first photoresist features, rendering the first photoresist features insoluble to a solvent, forming a second photoresist layer over the first photoresist features, patterning the second photoresist layer to form second photoresist features, forming a spacer layer over the first and

second photoresist features, etching the spacer layer to form spacer features and to expose the first and second photoresist features, forming third photoresist features between the spacer features, removing the spacer features, etching the hard mask layer using the first, second and third photoresist features as a mask to form hard mask features, trimming the hard mask features, etching the sacrificial layer using the hard mask features as a mask to form sacrificial features, etching the semiconductor seed layer using the sacrificial features as a mask, forming an insulating filler layer between the sacrificial features and between remaining portions of the etched semiconductor seed layer, removing the sacrificial features to form openings in the insulating filler layer, and forming semiconductor pillars in the openings over the remaining portions of the etched semiconductor seed layer.

[0005] Another embodiment of the invention provides a method of making a device including forming a hard mask layer over a sacrificial layer, forming a first photoresist layer over the hard mask layer, patterning the first photoresist layer to form first photoresist features, rendering the first photoresist features insoluble to a solvent, forming a second photoresist layer over the first photoresist features, patterning the second photoresist layer to form second photoresist features, etching the hard mask layer using both the first and the second photoresist features as a mask to form hard mask features, forming a spacer layer over the hard mask features, etching the spacer layer to form spacer features and to expose the hard mask features, forming third masking features between the spacer features, removing the spacer features, etching the sacrificial layer using the hard mask features and the third masking features as a mask to form sacrificial features, forming an insulating filler layer between the sacrificial features, and removing the sacrificial features to form openings in the insulating filler layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figures 1A-1E are side cross-sectional views illustrating a process flow of one embodiment.

[0007] Figures 2A-2E are illustrative top views of the structures shown in Figures 1A-1E, respectively.

[0008] Figures 3A-3D are side cross-sectional views illustrating non-limiting examples of the method which is generally shown in Figures 1A-1E.

[0009] Figures 4A and 4C are side cross-sectional views illustrating a process flow of one embodiment. Figures 4B and 4D are top images of the structures shown in Figures 4A and 4C, respectively.

[0010] Figures 5A-5E are side cross-sectional views illustrating a process flow of one embodiment. Figure 5F is a perspective view of the structure shown in Figure 5E.

[0011] Figures 6A-6E are side cross-sectional views illustrating a process flow of an alternative embodiment. Figure 6F is a perspective view of the structure shown in Figure 6E.

[0012] Figures 7A-7B are side cross-sectional views illustrating a process flow of an alternative embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] One embodiment of the invention provides a method of making a device including forming a first photoresist layer over a sacrificial layer, patterning the first photoresist layer to form first photoresist features, rendering the first photoresist features insoluble to a solvent, forming a second photoresist layer over the first photoresist features, patterning the second photoresist layer to form second photoresist features, forming a spacer layer over the first and second photoresist features, etching the spacer layer to form spacer features and to expose the first and second photoresist features, forming third photoresist features between the spacer features, removing the spacer features, and patterning the sacrificial layer using the first, second and third photoresist features as a mask to form sacrificial features. The method may further comprise forming an insulating filler layer between the sacrificial

features, and removing the sacrificial features to form openings in the insulating filler layer. The openings formed in the insulating filler layer can be pillar shaped, and at least some of the openings are cylindrical and others are quasi-cylindrical.

[0014] In some embodiments, the sacrificial layer comprises an inorganic hard mask material over an organic hard mask material. In these embodiments, the step of patterning the sacrificial layer using the photoresist features comprises etching the inorganic hard mask layer to form inorganic sacrificial features, trimming the inorganic hard mask sacrificial features, and etching the organic hard mask layer using the trimmed inorganic hard mask sacrificial features as a mask.

[0015] The openings formed in the insulating filler layer may be then filled by any desirable materials. For example the openings may serve as contact holes and be filled by conductive material, such as metal, silicide or polysilicon, which forms electrodes of an underlying device, such as a diode or transistor, or interconnects to lower level electrodes or metallization. In another embodiment, the openings may be filled by semiconductor material, resulting in pillar-shape semiconductor devices, such as pillar-shaped diodes.

[0016] Figures 1A through 1E show side cross-sectional views illustrating stages in formation of a device according to a method a first embodiment. Figures 2A through 2E show top views of the corresponding stages.

[0017] Referring to Figure 1A, a first photoresist layer can be formed over a sacrificial layer 200, followed by patterning the photoresist layer to form first photoresist features 111. The first photoresist features 111 are pillar-shaped (e.g., cylindrical shaped pillar), as illustrated by circles 1 in Figure 2A. Figure 1A is a side cross sectional view along line A-A in Figure 2A. Additional layers may be formed below, above or between layers 111 and 200 as will be described in more detail below.

[0018] The first photoresist features 111 are then rendered insoluble to a solvent used for forming more photoresist features between the first photoresist features 111. Any suitable methods can be used to render the first photoresist features 111

insoluble. For example, the methods described in U.S. Patent Application No. 11/864,205 and in U.S. Patent Application No. 12/216,107, which are incorporated by reference in their entirety, may be used. In some embodiments, the first photoresist features 111 may be rendered insoluble by applying a reactive reagent, causing the residual acids in the photoresist features 111 to chemically react with the reactive reagent to form a barrier layer or coating on upper and side surfaces of the first photoresist features 111 (i.e., to “freeze” the first photoresist features 111). This barrier layer can be formed by causing cross-linking on the surface of the pattern 111 or by any other suitable methods. The barrier layer may comprise a thin polymer film having a thickness of less than 10 nm, preferably about 1-2 nm. This layer is disposed on a surface of first photoresist features 111, protecting the first photoresist features 111 from being dissolved by the solvent used during the step of forming second photoresist features.

[0019] Turning to Figure 1B, the pitch of the photoresist features patterns is doubled by forming a second photoresist layer over the first photoresist features 111, followed by patterning the second photoresist layer to form second photoresist features 211. The second photoresist features 211 are also pillar-shaped, as illustrated by circles 2 in Figure 2B. Figure 1B is a side cross sectional view along line B-B in Figure 2B. If desired, the first and second photoresist features 111 and 211 may optionally be trimmed to reduce their diameter.

[0020] The first and second photoresist materials may be any suitable photoresist material(s), preferably acrylate materials, such as poly(methyl acrylate) or poly(methyl methacrylate). The first and second photoresist materials may be same or different. For example, the second photoresist material may have a thinner viscosity than the first photoresist material.

[0021] In some embodiments, when the first photoresist is an acrylic material, the reactive reagent may be the same acrylic material with an active functional group on the side chain. The reactive reagent can be a chemical shrink material, such as CSX004, FZX F112 or FZX F114 which comprises a poly(methyl) acrylate derivative, melamine resin, and other ingredients including water, methyl isobutyl

carbinol, n-butyl alcohol, or combinations thereof. For example, FZX F114 comprises a poly(methyl) acrylate derivative, and a solvent containing methyl isobutyl carbinol and n-butyl alcohol having a volume ratio of 70:30 to 90:10, such as a volume ratio of 80:20. CSX004, FZX F112 and FZX F114 are all available from JSR Micro (<http://www.jsrmicro.com>). Another chemical shrink material, RELACS[®] available from AZ Electronic Materials or other reactive reagents which are used in the prior art to reduce the dimensions of openings between adjacent resist patterns (i.e., which are used to widen small resist patterns), may also be used.

[0022] Other freezing methods may also be used to protect the first photoresist features 111 from being dissolved by solvent(s) used (i.e., to render the first photoresist features 111 insoluble) in the step of patterning the second photoresist layer. For example, a protective agent may selectively replace some functional groups of the first photoresist polymer, which in turn renders the first photoresist insoluble to the solvent(s). Alternatively, the first photoresist may crosslink with a compatible chemistry under a desired condition, such as an application of heat (e.g., a high temperature bake), or other desired treatments, to “freeze” the first photoresist features 111.

[0023] Next, spacer features 105 (e.g., a sidewall spacer) can be formed surrounding the first and second photoresist features 100 (111, 211), as shown in Figures 1C and 2C. Spacer features 105 may be formed by conventional sidewall spacer formation methods, such as by depositing a film over the photoresist features 110 and then anisotropically etching the film to leave the cylindrical spacer features 105 surrounding the photoresist features 110. The spacer features 105 may be made of a conductive, insulating or semiconductor material different from that of the photoresist features 110. For example, the spacer material, such as silicon oxide or silicon nitride, can be deposited by a low temperature CVD process on the photoresist features 110 and etched by wet etching methods. Of course, other suitable material combinations of the spacer features 105 and the photoresist features 110 may also be used. The step of forming the spacer features 105 exposes the sacrificial layer 200 in

the openings 3, as shown in Figure 2C. Figure 1C is a side cross sectional view along line C-C in Figure 2C.

[0024] Turning to Figure 1D, third photoresist features 311 can be formed in the openings 3 between the spacer features 105. The third photoresist features 311 can be formed by any suitable methods. In some embodiments, the third photoresist features 311 can be formed by applying a flowable layer of photoresist first such that it is planarized by filling the space between the spacer features 105 with a relatively planar surface. Alternatively, the photoresist layer may be chemically or mechanically planarized, such as by etchback or CMP, using the top surface of the spacer features 105 as a stop. The third photoresist features 311 may be pillar-shaped, as illustrated by shapes 3 in Figure 2D. Figure 1D is a side cross sectional view along line D-D in Figure 2D. If desired, the photoresist features 110A (111, 211 and 311) may optionally be trimmed to round the third photoresist features 311 and reduce the diameter of photoresist features 111 and 211.

[0025] As shown in Figure 2D, the first 111 and second 211 photoresist features (circles 1 and 2) have a cylindrical shape while the third photoresist features 311 (shapes 3) have a quasi-cylindrical shape. A quasi-cylindrical shape is a shape that has a cross section formed by four bordering annular spacer features 105. This shape has a cross section that is similar to a distorted circle, square or a rectangle depending on the distance between adjacent spacer features 105 and may include concave sidewalls which mirror the convex shape of the bordering spacer features 105.

[0026] The spacer features 105 are then selectively removed, such as by selective etching, leaving the photoresist features 110A (111, 211, and 311) over the sacrificial layer 200, as shown in Figure 1E. Figure 1E is a side cross sectional view along line E-E in Figure 2E.

[0027] The first photoresist features 111 may be arranged in a repeating square pattern with one second photoresist feature 211 located in the middle of the imaginary square formed by first photoresist features 111 at each corner, and with a respective third photoresist feature 311 located at the center point of each imaginary line which

makes up the sides of the imaginary square between the first photoresist features 111, as shown in Figure 2E. Another way to describe this pattern is that first photoresist features 111 and the second photoresist features 211 form overlapping squares with the corner of each square of second photoresist feature 211 located in the middle of each square of first photoresist features 111 and vice-versa. The third photoresist features 311 form a rhombus having the first photoresist features 111 or the second photoresist features 211 in the center. Thus, the adjacent imaginary horizontal lines in Figure 2E extend through alternating first 111 and third 311 photoresist features or second 211 and third 311 photoresist features, while adjacent imaginary diagonal lines extend through either third photoresist features 311 or alternating first 111 and second 211 photoresist features. Thus, the original pitch of photoresist features 111 and 211 has been doubled by adding the third photoresist features 311.

[0028] In some optional embodiments, one or more of bottom antireflective coating (BARC) layer (which can be an organic dielectric material) and/or dielectric antireflective coating (DARC) layer may be formed over the sacrificial layer the prior to forming the first photoresist features 111. Preferably, the BARC layer is formed over the DARC layer, which in turn is formed over the sacrificial layer 200. In these embodiments, the DARC layer is patterned using the combination of the first, second and third photoresist features as a mask, and the step of patterning the sacrificial layer uses at least the patterned DARC layer as a mask. The photoresist may be removed before or after patterning the DARC layer using the BARC layer as a mask.

[0029] Figures 3A-3D illustrate non-limiting examples of the method which is generally shown in Figures 1A-1E. As shown in Figure 3A, a DARC layer 402 (a 30-50 nm thick, such as 40 nm thick SiON layer) can be formed above the sacrificial layer 200 (100-150 nm thick, such as 150 nm thick amorphous carbon (a-C) and a BARC layer 401 (15-40 nm thick, such as 25 nm thick) can be formed above the DARC layer 402. The BARC layer 401 is etched using the photoresist features 110 (111 and 211) as a mask and thus the patterned BARC layer 402 adopts the pattern of the photoresist features 110, resulting in resist/BARC pillars shown in Figure 3A. A thin p⁺ or n⁺ doped polysilicon seed layer 391 (5-15 nm thick, such as 10 nm thick)

can be provided below the a-C sacrificial layer 200, and a switching material layer 328 (3-10 nm thick, such as 5 nm thick, which will be described in more detail below) can be located between two conductive layers 404 and 405, such as titanium and/or TiN layers (5-15 nm thick, such as 10 nm thick). The above described stack of layer is further located over rail-shaped bottom electrodes 301 separated by insulating material 410, which are located over a substrate 100. The photoresist features 110 (111 and 211) may comprise 193, 120 and 80 nm lithography resist. If the pitch of features 111 is 90-100 nm, such as 95-96 nm, then the same lithography mask may be shifted 45 nm (e.g., half pitch) in the X and Y directions to expose the second photoresist features 211. The final pitch of features 111 and 211 is about 64-68 nm. Of course other pitches may be used.

[0030] As shown in Figure 3B, spacer features 105 can then be formed surrounding the photoresist features 111 and 211. The spacer features 105 may also extend around the patterned BARC layer 401. The third photoresist features 311 can then be formed by filling photoresist material over and between the spacer features 105, resulting in a structure as shown in Figure 3C. Next, the spacer features 105 can be removed, leaving the photoresist features 110A (111, 211, and 311) over the DARC layer 402, as shown in Figure 3D.

[0031] The DARC layer 402 is then etched using the photoresist features 110A (111, 211 and 311) as a mask. The BARC layer and the photoresist features may then be removed, resulting in a structure as shown Figure 4A. The patterned DARC layer 402 adopts the pattern of the photoresist features 110A (111, 211 and 311). Thus, some of the DARC features (circles 1 and 2) have a cylindrical shape while other DARC features (shapes 3) have a quasi-cylindrical shape, as shown in Figure 4B, which is a top image of the structure shown in Figure 4A.

[0032] Next, the DARC features may be optionally trimmed to round the quasi-cylindrical features (shapes 3) and reduce the diameter of the cylindrical DARC features (circles 1 and 2), resulting in a structure as shown Figures 4C (side cross-sectional view) and 4D (top image).

[0033] Further, the a-C sacrificial layer 200 is then etched using the patterned DARC layer as a mask to form a-C sacrificial features 200A. If desired, the patterned BARC layer and/or the resist patterns 110A may be left in place over the patterned DARC layer during patterning of layer 200. The features 200A comprise cylindrical pillars. If the DARC trimming step is omitted, then some features 200A that are located in the location of features 311 have a quasi-cylindrical steps while the other features 200A have a cylindrical shape.

[0034] In this non-limiting example, the thin polysilicon seed layer 391, the switching material layer 328, and the two conductive layers 404 and 405 are also etched using the patterned DARC layer 402 and/or the a-C sacrificial features 200A as a mask. The etching of the a-C sacrificial layer 200, the thin polysilicon seed layer 391, the switching material layer 328, and the two conductive layers 404 and 405 stops on the insulating layer 410 which separates the rail shaped bottom electrodes 301. The DARC layer 402 is then removed, resulting in a structure shown in Figure 5A.

[0035] An insulating filler layer 612 is then formed between a-C sacrificial features 200A, resulting in a structure shown in Figure 5B. The insulating filler layer 612 may comprise an optional silicon nitride liner on pillars 200A/391/404/328/405 (not shown) and a silicon oxide gap fill material filling the space between adjacent liner portions. Layer 612 may be formed over the a-C sacrificial features 200A followed by planarization by CMP with the tops of the a-C sacrificial features 200A. Preferably, the DARC layer 402 is completely removed prior to the step of removing a-C sacrificial features 200A. Residual DARC may impede the complete removal of the a-C features 402.

[0036] The sacrificial features 200 can then be removed, such as by selective etching or ashing, exposing the thin polysilicon seed layer 391 in the openings 81, as shown in Figure 5C. The semiconductor features 392 can then be selectively deposited in the openings 81 over the seed material 391, resulting in a structure shown in Figure 5D. The seed material 391 and the semiconductor features 392 may form diodes 320. Alternatively, the semiconductor features 392 may be deposited non-

selectively followed by optional planarization, as will be described in more detail below. The diodes 320 may have a bottom heavily doped n-type region 391 (e.g., an n-type seed layer), an optional intrinsic region 393 (a region which is not intentionally doped), and a top heavily doped p-type region 394. The orientation of the diodes may be reversed. The diodes 320 may be formed by depositing intrinsic semiconductor material on the n-type or p-type seed material followed by implanting the other one of the n-type or p-type dopants into the upper portion of the semiconductor features 392. Alternatively, the upper regions of the p-i-n diodes may be formed by depositing a doped semiconductor material on the intrinsic semiconductor material. Other diodes, such as p-n diodes, punch through diodes, etc. may be formed instead of the p-i-n diodes.

[0037] In some embodiments, the diodes 320 are steering elements of non-volatile memory cells 300 and the switching material features 328 are storage elements of the non-volatile memory cells 300.

[0038] The top electrodes 302 extending in a direction different (e.g., perpendicular) from that of the bottom electrodes 301 can then be formed over the non-volatile memory cells 300 by depositing one or more conductive layers which are then patterned into rails, as shown in Figures 5E (side cross-sectional view) and Figure 5F (perspective view). The non-volatile memory cells 300 adopt the shape of the DARC features, and thus may have a cylindrical shape. Alternatively, if the DARC trimming step is omitted, then the cells 300 may have both the cylindrical and quasi-cylindrical shapes, as described above.

[0039] While specific device and sacrificial layers are described above, it should be noted that the device and sacrificial layers may be made of any suitable materials including insulating, semiconductor or a conductive layers. Also, one or more layers in the stack described above may be omitted if desired, for example the conductive layers 404 and 405 may be omitted in some embodiments.

[0040] In the above described embodiment, the storage element 328 is located below the diode steering element 320 in the resulting device. Alternatively, the storage

element 328 may be located over the diode steering element 320. Figures 6A through 6E show side cross-sectional views illustrating stages in formation of such a device in an alternative embodiment.

[0041] Referring to Figure 6A, the switching material layer 328 and the conductive layers 404 and 405 are not included in the initial stack. The DARC layer 402 is formed over the sacrificial layer 200. The DARC layer 402 is patterned using the method shown in Figures 1A-1E and 4A-4C.

[0042] The sacrificial layer 200 is then patterned using patterned DARC layer 402 as a mask, followed by filling the openings between the sacrificial features with an insulating layer 612 and removing the sacrificial features 200A to leave openings as shown in Figures 5A-5D. The openings 61 in the insulating layer 612 are shown in Figure 6B.

[0043] Semiconductor features 392 can then be formed by partially filling the openings 61, leaving recesses 62 over the semiconductor seed layer 391, resulting in a structure shown in Figure 6C. The semiconductor features 392 can be formed by any suitable methods. For example, the semiconductor features 392 may be formed by selectively depositing the semiconductor material to partially fill the openings 61 in the insulating layer 612 to leave recesses 62 over the semiconductor features 392. Alternatively, the step of forming the semiconductor features 392 may comprise depositing semiconductor material to completely fill the openings 61 first, followed by a step of recessing the semiconductor material to form recesses 62 over the semiconductor features 392, as by selective etching. The semiconductor material may also optionally be deposited over the top of insulating layer 612 followed by planarization with the top of layer 612 by chemical mechanical polishing (CMP) or other suitable methods prior to the recessing etch step.

[0044] Next, switching material features 328 can then be formed over the semiconductor features 392 (e.g., over diodes 320), resulting in a structure shown in Figure 6D. The switching material features 328 may be formed by depositing switching material in the recesses 62 and optionally over the top of layer 612 followed

by optional planarization by CMP or other suitable methods using top of features 612 as a stop.

[0045] Similarly, the top electrodes 302 can be formed over the non-volatile memory cells 300 extending to a direction different from that of the bottom electrodes 301, resulting in a structure shown in Figures 6E (side cross-sectional view) and Figure 6F (perspective view). The perspective view of the resulting structure shown in Figure 6F is substantially the same as that shown in Figure 5F, except that the switching material 328 is located over, rather than under the diode 320.

[0046] As explained above, in some embodiments, the seed material 391 and the semiconductor features 392 may form diodes 320. In an alternative embodiment, the diodes 320 may be formed by non-selective deposition methods. In this embodiment, the seed material layer 391 may be omitted, and the semiconductor features 392 encompass the entire structure of diodes 320.

[0047] In another alternative embodiment shown in Figures 7A and 7B, rather than forming the spacer features 105 on the photoresist patterns 110, the spacer features are instead formed on the hard mask patterns.

[0048] As shown in Figure 7A, the first and second photoresist features 111, 211 are used to as a mask to etch the BARC layer 401. Then, the photoresist features 111, 211 and/or the patterned BARC layer 401 are used as a mask to pattern the DARC layer 402, which serves as a hard mask layer, to form hard mask features 402A. Of course other hard mask layers may also be used instead or in addition to the DARC layer 402.

[0049] As shown in Figure 7B, the photoresist features 111, 211 and optionally the patterned BARC layer 401 are removed from the hard mask features 402A. Then, the spacer features 105 are formed around the DARC hard mask features 402A by forming a spacer layer over the hard mask features and etching the spacer layer to form the spacer features and to expose the hard mask features.

[0050] Third masking features 411 are then formed between the spacer features 105. The third masking features 411 may comprise a photoresist material similar to that of features 311. Alternatively, features 411 may comprise any insulating, conductive or semiconductor material which allows selective etching of the spacer feature material without being etched away itself. Features 411 may comprise the same material as that of features 402A. For example, features 411 may comprise silicon oxynitride (SiON) features formed by depositing a SiON layer over the features 402A and 105 followed by planarization of this layer by CMP using tops of features 105 as a polish stop to leave features 411 in the space between the spacer feature 105.

[0051] Thereafter, the method proceeds in the same way as in Figures 4 and 5 or in Figures 4 and 6. Thus, the spacer features 105 are selectively removed and the sacrificial layer 200 is etched using the hard mask features 402 and the third masking features 411 as a mask to form sacrificial features 200A.

[0052] The substrate 100 can be any semiconducting substrate known in the art, such as monocrystalline silicon, IV-IV compounds such as silicon-germanium or silicon-germanium-carbon, III-V compounds, II-VI compounds, epitaxial layers over such substrates, or any other semiconducting or non-semiconducting material, such as glass, plastic, metal or ceramic substrate. The substrate 100 may include integrated circuits fabricated thereon, such as driver circuits for a memory device.

[0053] The conductive material of the electrodes 301 and 302 can independently comprise any one or more suitable conducting material known in the art, such as tungsten, copper, aluminum, tantalum, titanium, cobalt, titanium nitride or alloys thereof. For example, in some embodiments, tungsten is preferred to allow processing under a relatively high temperature. In some other embodiments, copper or aluminum is a preferred material.

[0054] The sacrificial layer 200 can be made of any suitable sacrificial materials, for example oxide or nitride materials or organic hard mask materials, including amorphous carbon. In some embodiments, the amorphous carbon material may be an advanced patterning film (APF).

[0055] The insulating material 612 can independently comprise any electrically insulating material, such as silicon oxide, silicon nitride, silicon oxynitride, or other high-k insulating materials.

[0056] Any suitable semiconductor materials can be used for semiconductor diodes 320, for example silicon, germanium, silicon germanium, or other compound semiconductor materials, such as III-V, II-VI, etc. materials. As explained above, the semiconductor material may be formed by any suitable selectively or non-selectively deposition methods. In one embodiment, the semiconductor material in at least one of the first and second device levels is selectively deposited by low pressure chemical vapor deposition (LPCVD). For example, the method described in US Application Number 12/216,924 filed on July 11, 2008 or US Application Number 12/007,781 (published as US Published Application 2009/0179310 A1), incorporated herein by reference in their entirety, may be used to deposit polysilicon. Alternatively, the methods described in US Application Number 11/159,031 filed on June 22, 2005 (which published as US Published Application 2006/0292301 A1) and in US Application Number 12/007,780 filed on January 15, 2008, incorporated herein by reference in their entirety, may be used to deposit the germanium. The semiconductor material may be amorphous, polycrystalline or single crystal. For example, the material may comprise polysilicon. The optional seed layer 391 may comprise any suitable semiconductor or silicide seed material which allows selective growth of the semiconductor materials of the diodes 320. For example, the seed layer 391 may comprise polysilicon to grow additional polysilicon 392 of the diodes 320.

[0057] The non-volatile memory cells 300 may be one-time programmable (OTP) or re-writable. The switching material 328 can be one of antifuse, fuse, metal oxide memory, switchable complex metal oxide, carbon nanotube memory, graphene resistivity switchable material, carbon resistivity switchable material (e.g., amorphous and/or polycrystalline carbon), phase change material memory, conductive bridge element, or switchable polymer memory. The antifuse dielectric layer can be one of hafnium oxide, aluminum oxide, titanium oxide, lanthanum oxide, tantalum oxide, ruthenium oxide, zirconium silicon oxide, aluminum silicon oxide, hafnium silicon

oxide, hafnium aluminum oxide, hafnium silicon oxynitride, zirconium silicon aluminum oxide, hafnium aluminum silicon oxynitride, zirconium silicon aluminum oxynitride, silicon oxide, silicon nitride, or a combination thereof.

[0058] The methods of forming one memory device level have been explained above. Additional memory levels can be formed above or below the memory device level described above to form a monolithic three dimensional memory array having more than one device levels. A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a wafer, with no intervening substrates. The layers forming one memory level are deposited or grown directly over the layers of an existing level or levels. In some embodiments, electrodes can be shared between memory levels; i.e. top electrode 302 shown in Figures 4F and 5H would serve as the bottom electrode of the next memory level. In other embodiments, an interlevel dielectric (not shown) is formed above the first memory level, its surface planarized, and construction of a second memory level begins on this planarized interlevel dielectric, with no shared conductors.

[0059] The foregoing details description has described only a few of the many possible implementations of the present invention. For this reason, this detailed description is intended by way of illustration, and not by way of limitations. Although certain supporting circuits and fabrication steps are not specifically described, such circuits and protocols are well known, and no particular advantage is afforded by specific variations of such steps in the context of practicing this invention. Variations and modifications of the embodiments disclosed herein may be made based on the description set forth herein, without departing from the scope and spirit of the invention. It is only the following claims, including all equivalents, that are intended to define the scope of this invention.

WHAT IS CLAIMED IS:

1. A method of making a device, comprising:
forming a first photoresist layer over a sacrificial layer;
patterning the first photoresist layer to form first photoresist features;
rendering the first photoresist features insoluble to a solvent;
forming a second photoresist layer over the first photoresist features;
patterning the second photoresist layer to form second photoresist features;
forming a spacer layer over the first and second photoresist features;
etching the spacer layer to form spacer features and to expose the first and second photoresist features;
forming third photoresist features between the spacer features;
removing the spacer features; and
patterning the sacrificial layer using the first, second and third photoresist features as a mask to form sacrificial features.
2. The method of claim 1, wherein the step of forming third photoresist features between the spacer features comprises:
forming a third photoresist layer between and over the spacer features;
and
planarizing the third photoresist layer using top of the spacer features as a stop.
3. The method of claim 1, further comprising:
forming an insulating filler layer between the sacrificial features; and
removing the sacrificial features to form openings in the insulating filler layer.
4. The method of claim 3, wherein the openings in the insulating filler layer are pillar shaped, and at least some of the openings are cylindrical and others are quasi-cylindrical.

5. The method of claim 3, wherein the sacrificial layer comprises an inorganic hard mask material over an organic hard mask material.

6. The method of claim 5, wherein the step of patterning the sacrificial layer comprises etching the inorganic hard mask layer to form inorganic sacrificial features, trimming the inorganic hard mask sacrificial features, and etching the organic hard mask layer using the trimmed inorganic hard mask sacrificial features as a mask.

7. The method of claim 3, further comprising:
providing a switching material layer below the sacrificial layer;
providing a semiconductor seed layer between the switching material layer and the sacrificial layer;
etching the semiconductor seed layer using the sacrificial features as a mask;
etching the switching material layer using the sacrificial features as a mask to form switching material features prior to the step of forming the insulating filler layer between the sacrificial features; and
forming semiconductor features in the openings in the insulating filler layer;
wherein:
the switching material features comprise storage elements of non-volatile memory cells;
the etched semiconductor seed layer comprises lower portions of diodes;
the semiconductor features comprise upper portions of the diodes; and
the diodes comprise steering elements of the non-volatile memory cells.

8. The method of claim 3, further comprising:

depositing semiconductor features in the openings in the insulating filler layer;
recessing the semiconductor features to form recesses; and
forming switching material features in the recesses over the semiconductor features;
wherein:
the semiconductor features comprise at least a portion of steering elements of non-volatile memory cells; and
the switching material features comprise storage elements of the non-volatile memory cells.

9. The method of claim 3, further comprising:
selectively growing semiconductor features in the openings in the insulating filler layer to leave recesses over the semiconductor features; and
forming switching material features in the recesses over the semiconductor features;
wherein:
the semiconductor features comprise at least a portion of steering elements of non-volatile memory cells; and
the switching material features comprise storage elements of the non-volatile memory cells.

10. The method of claim 1, wherein:
the first photoresist layer comprises a first composition;
the second photoresist comprises a second composition;
the third photoresist comprises a third composition; and
the first, second and third compositions are the same or different from each other.

11. The method of claim 1, wherein:

the step of rendering the first photoresist pattern insoluble to the solvent forms a barrier layer over the first photoresist pattern;

the barrier layer comprises a thin polymer film having a thickness of less than 10 nm which is disposed on a surface of first photoresist features, such that the sacrificial layer is exposed in area between first photoresist features; and

the barrier layer protects the first photoresist pattern from being dissolved by the solvent used during the step of patterning the second photoresist layer.

12. A method of making a device, comprising:

forming a sacrificial layer over a semiconductor seed layer;

forming a hard mask layer over the sacrificial layer;

forming a first photoresist layer over the hard mask layer;

patterning the first photoresist layer to form first photoresist features;

rendering the first photoresist features insoluble to a solvent;

forming a second photoresist layer over the first photoresist features;

patterning the second photoresist layer to form second photoresist

features;

forming a spacer layer over the first and second photoresist features;

etching the spacer layer to form spacer features and to expose the first and second photoresist features;

forming third photoresist features between the spacer features;

removing the spacer features;

etching the hard mask layer using the first, second and third photoresist features as a mask to form hard mask features;

trimming the hard mask features;

etching the sacrificial layer using the hard mask features as a mask to form sacrificial features;

etching the semiconductor seed layer using the sacrificial features as a mask;

forming an insulating filler layer between the sacrificial features and between remaining portions of the etched semiconductor seed layer;
removing the sacrificial features to form openings in the insulating filler layer; and
forming semiconductor pillars in the openings over the remaining portions of the etched semiconductor seed layer.

13. The method of claim 12, wherein the step of forming third photoresist features between the spacer features comprises:

forming a third photoresist layer between and over the spacer features;
and
planarizing the third photoresist layer using top of the spacer features as a stop.

14. The method of claim 12, wherein the semiconductor pillars and the remaining portions of the etched semiconductor seed layer form pillar shaped diodes.

15. The method of claim 14, wherein the first and second photoresist features comprise cylindrical pillars and the third photoresist features comprise quasi-cylindrical pillars.

16. The method of claim 12, wherein:
the first photoresist layer comprises a first composition;
the second photoresist comprises a second composition;
the third photoresist comprises a third composition; and
the first, second and third compositions are the same or different from each other.

17. The method of claim 12, wherein:
the step of rendering the first photoresist pattern insoluble to the solvent forms a barrier layer over the first photoresist pattern;

the barrier layer comprises a thin polymer film having a thickness of less than 10 nm which is disposed on a surface of first photoresist features, such that the hard mask layer is exposed in area between first photoresist features; and

the barrier layer protects the first photoresist pattern from being dissolved by the solvent used during the step of patterning the second photoresist layer.

18. The method of claim 12, further comprising:

providing a switching material layer below the semiconductor seed layer; and

etching the switching material layer using the sacrificial features as a mask to form switching material features prior to the step of forming the insulating filler layer;

wherein:

the switching material features comprise storage elements of non-volatile memory cells;

the remaining portions of the semiconductor seed layer comprise lower portions of diodes;

the semiconductor pillars comprise upper portions of the diodes; and
the diodes comprise steering elements of the non-volatile memory cells.

19. A method of making a device, comprising:

forming a hard mask layer over a sacrificial layer;
forming a first photoresist layer over the hard mask layer;
patterning the first photoresist layer to form first photoresist features;
rendering the first photoresist features insoluble to a solvent;
forming a second photoresist layer over the first photoresist features;
patterning the second photoresist layer to form second photoresist features;

etching the hard mask layer using both the first and the second photoresist features as a mask to form hard mask features;
forming a spacer layer over the hard mask features;
etching the spacer layer to form spacer features and to expose the hard mask features;
forming third masking features between the spacer features;
removing the spacer features;
etching the sacrificial layer using the hard mask features and the third masking features as a mask to form sacrificial features;
forming an insulating filler layer between the sacrificial features; and
removing the sacrificial features to form openings in the insulating filler layer.

20. The method of claim 19, wherein the step of forming third photoresist features between the spacer features comprises:

forming a third photoresist layer between and over the spacer features;
and
planarizing the third photoresist layer using top of the spacer features as a stop.

21. The method of claim 19, further comprising trimming the hard mask features prior to the step of etching the sacrificial layer.

22. The method of claim 19, wherein the openings in the insulating filler layer are pillar shaped.

23. The method of claim 22, wherein at least some of the openings are cylindrical and others are quasi-cylindrical.

24. The method of claim 22, wherein the hard mask layer comprises an inorganic hard mask material and the sacrificial layer comprises an organic hard mask material.

25. The method of claim 22, wherein:
the first photoresist layer comprises a first composition;
the second photoresist comprises a second composition; and
the first and the second compositions are the same or different.

26. The method of claim 22, wherein:
the step of rendering the first photoresist pattern insoluble to the solvent forms a barrier layer over the first photoresist pattern;
the barrier layer comprises a thin polymer film having a thickness of less than 10 nm which is disposed on a surface of first photoresist features, such that the hard mask layer is exposed in area between first photoresist features; and
the barrier layer protects the first photoresist pattern from being dissolved by the solvent used during the step of patterning the second photoresist layer.

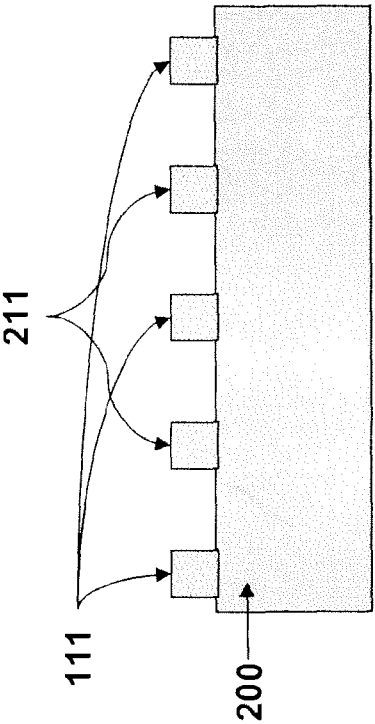


Fig. 1A

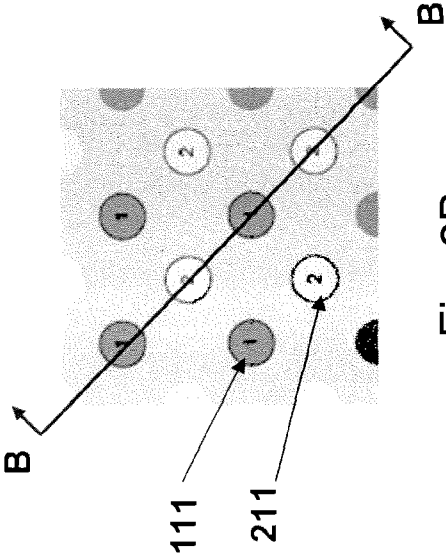


Fig. 2A

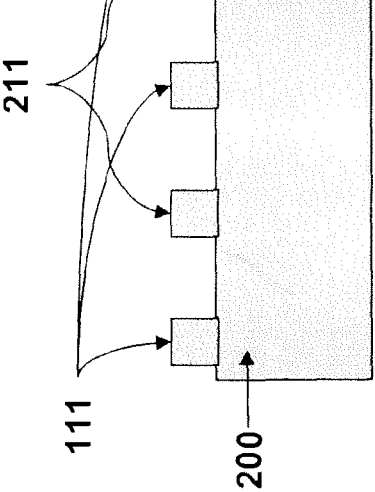


Fig. 1B

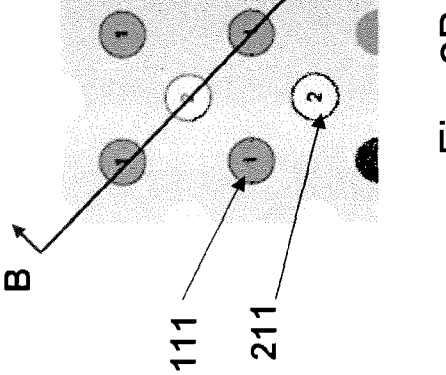


Fig. 2B

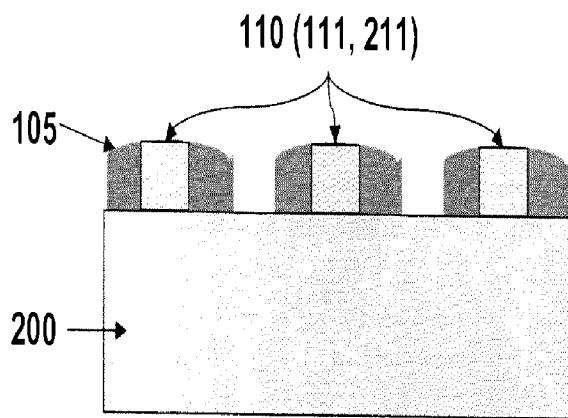


Fig. 1C

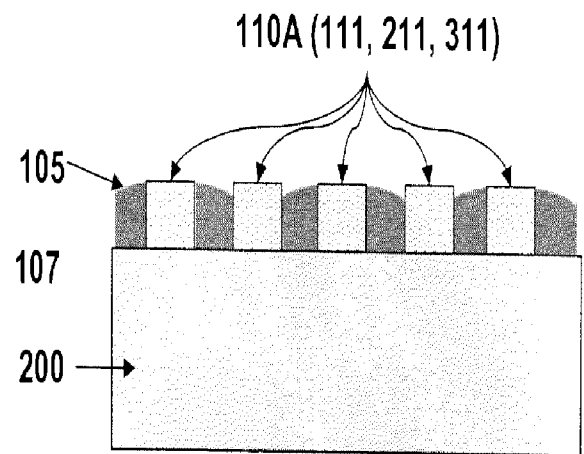


Fig. 1D

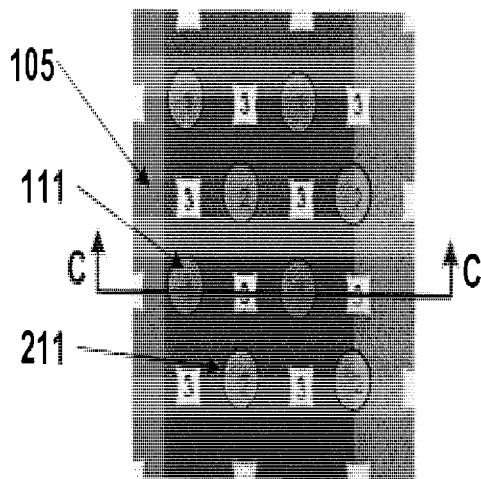


Fig. 2C

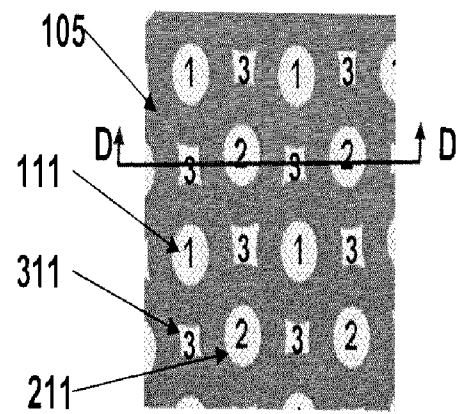


Fig. 2D

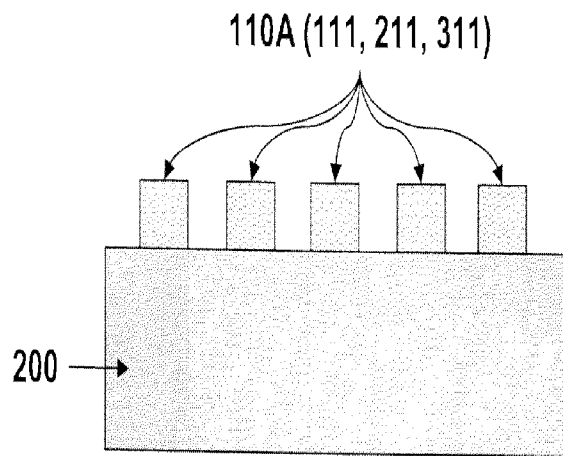


Fig. 1E

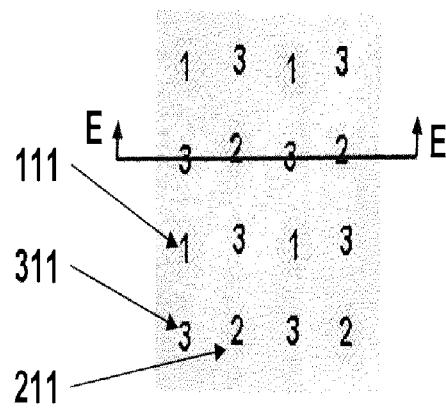


Fig. 2E

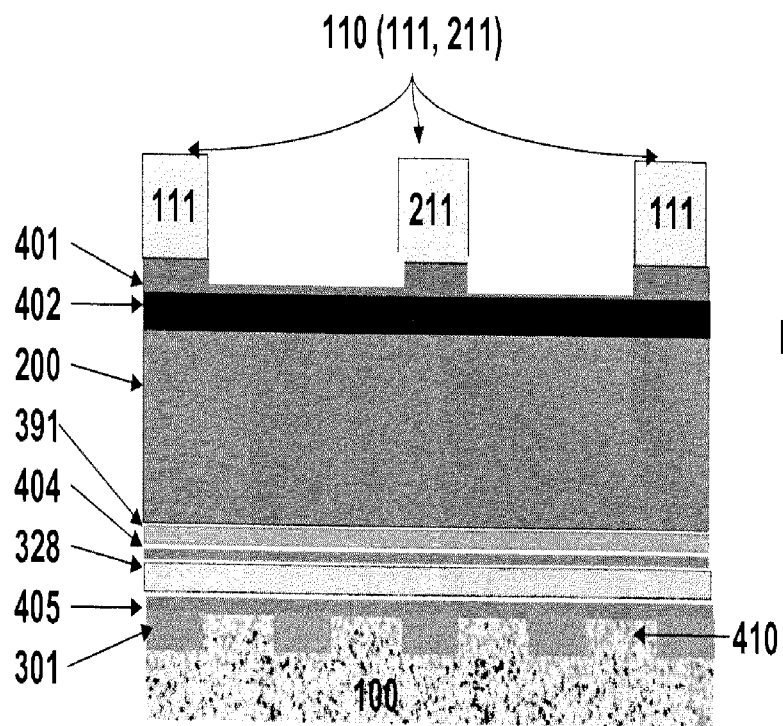


Fig. 3A

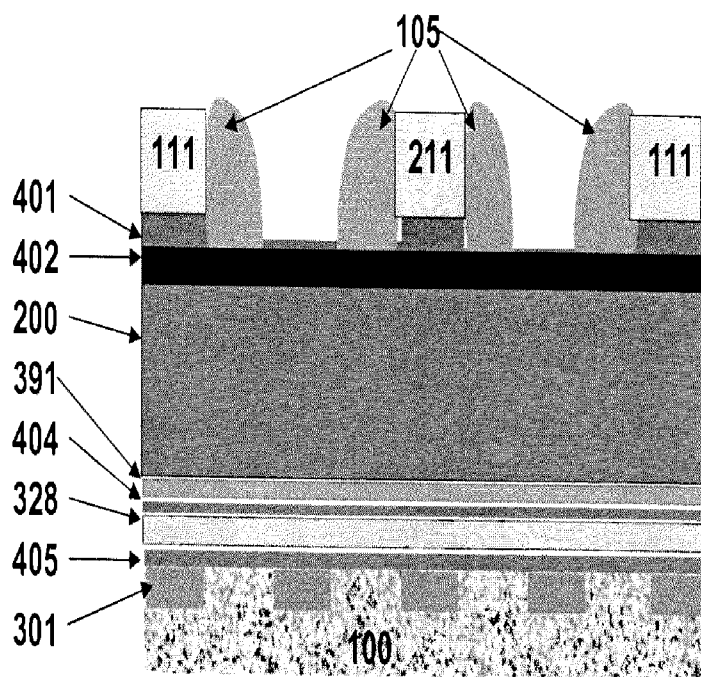


Fig. 3B

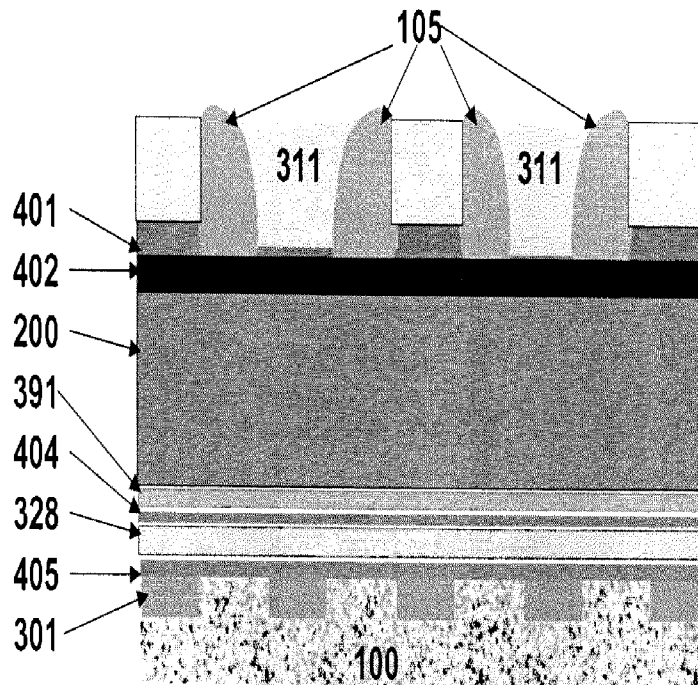


Fig. 3C

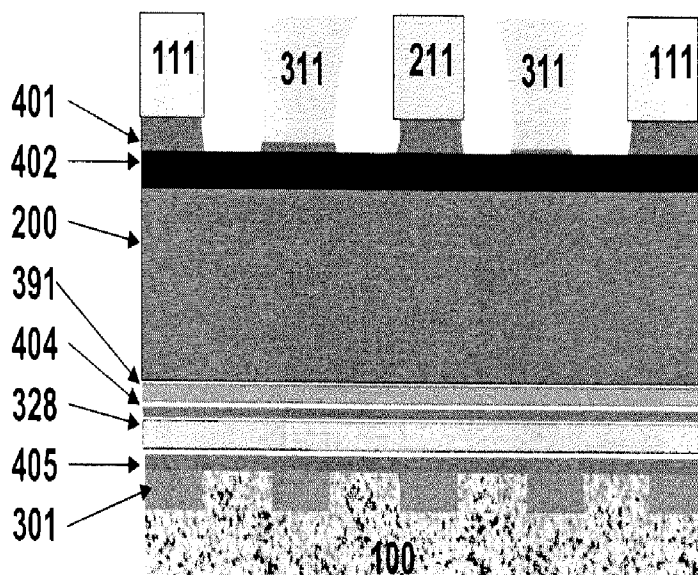


Fig. 3D

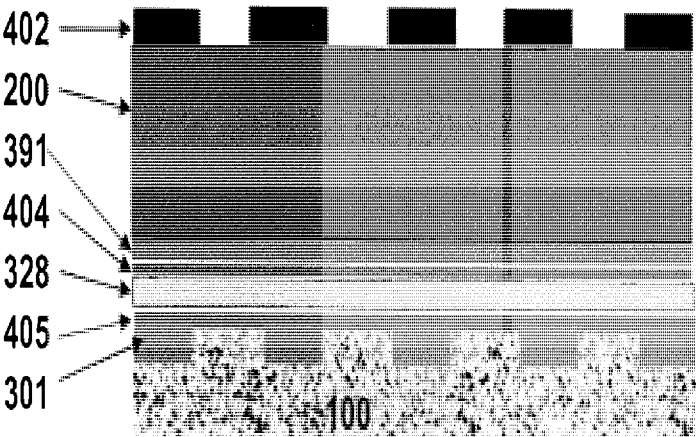


Fig. 4A

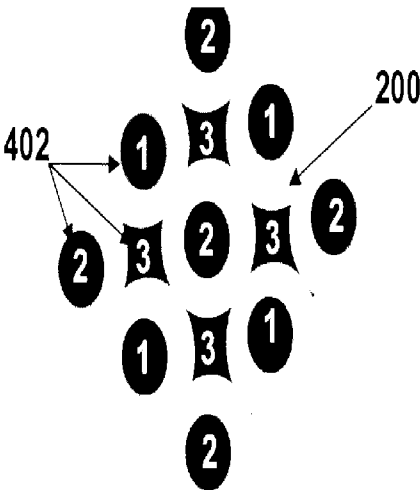


Fig. 4B

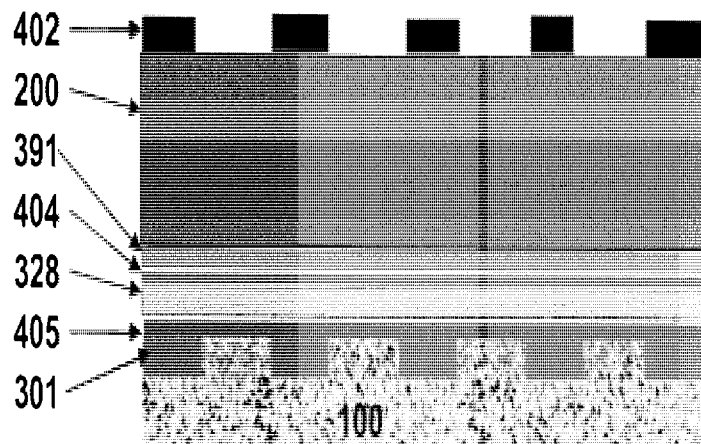


Fig. 4C

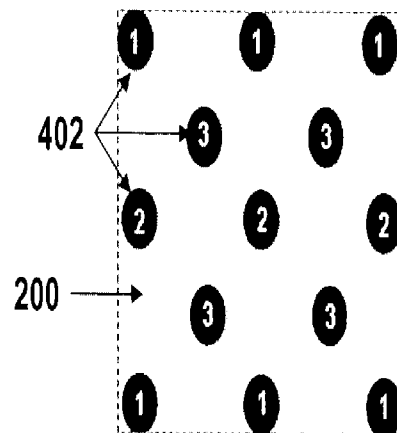


Fig. 4D

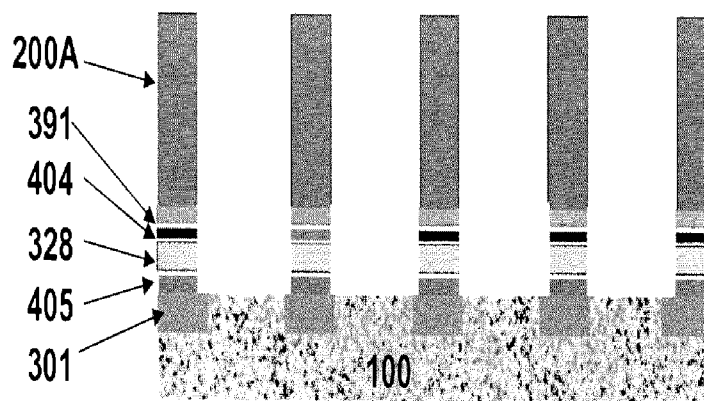


Fig. 5A

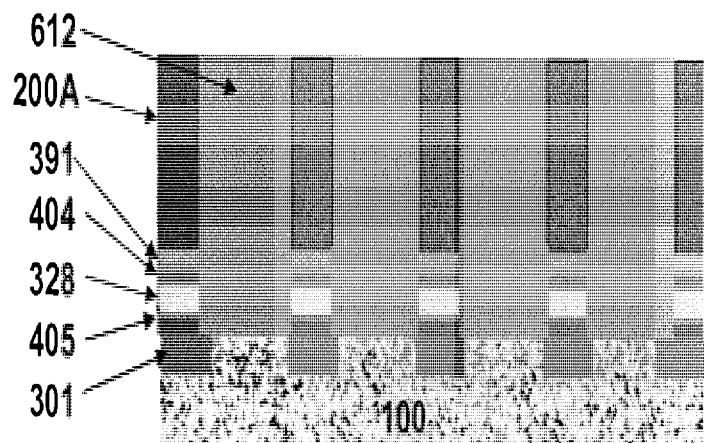
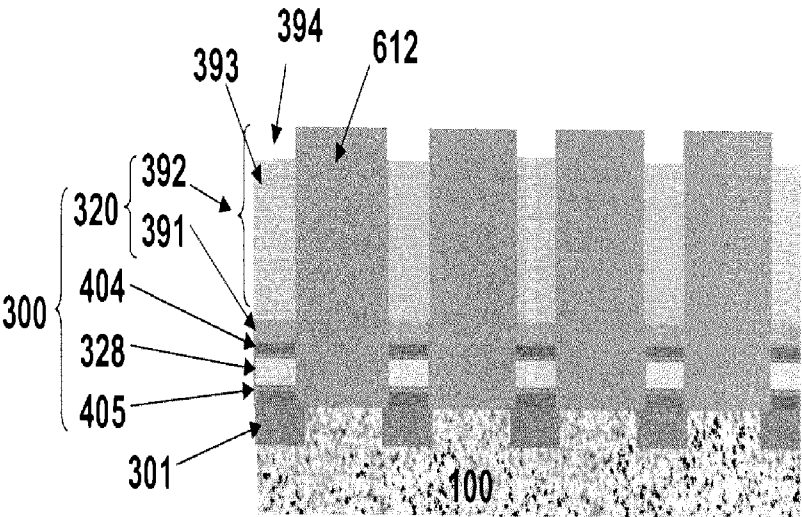
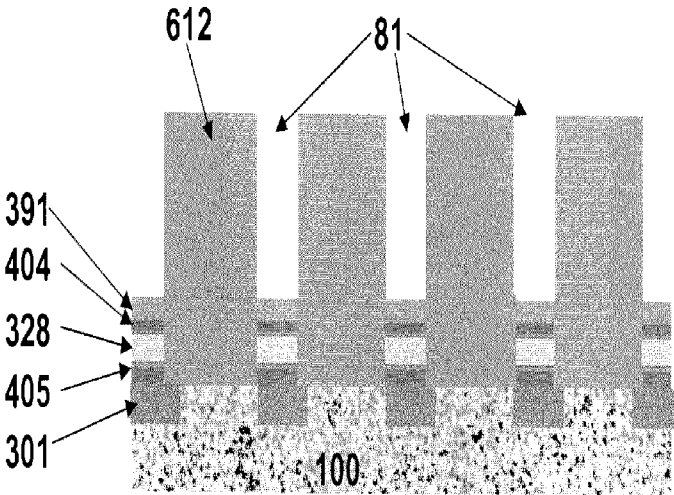


Fig. 5B



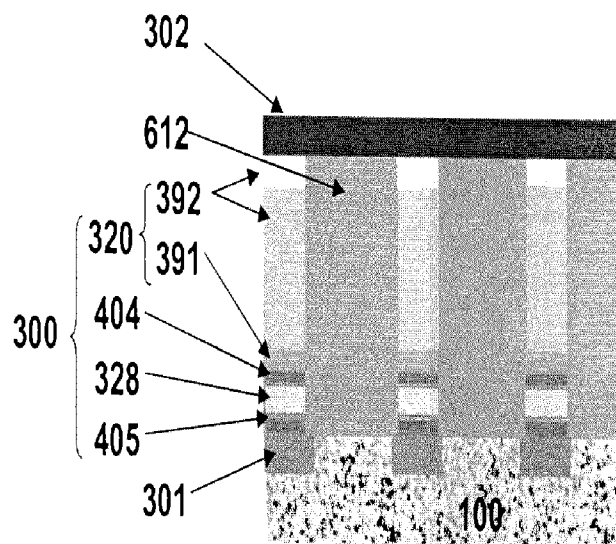


Fig. 5E

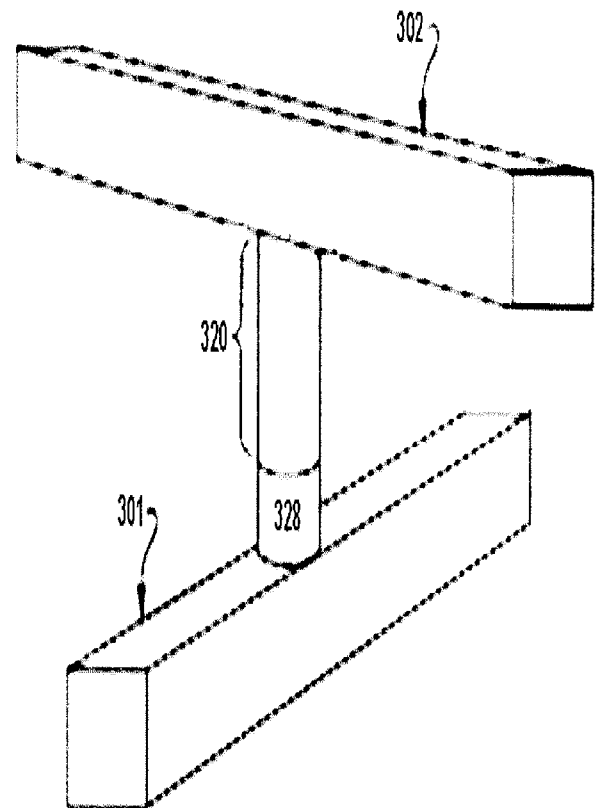


Fig. 5F

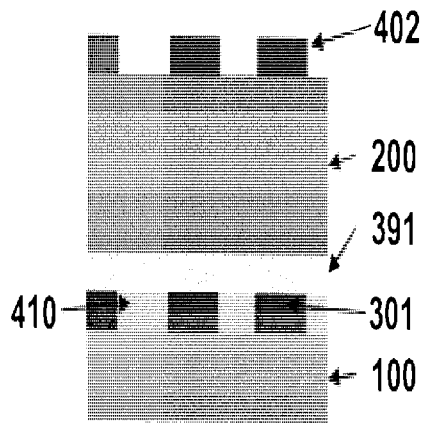


Fig. 6A

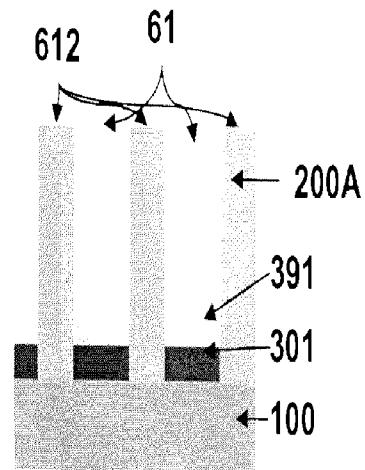


Fig. 6B

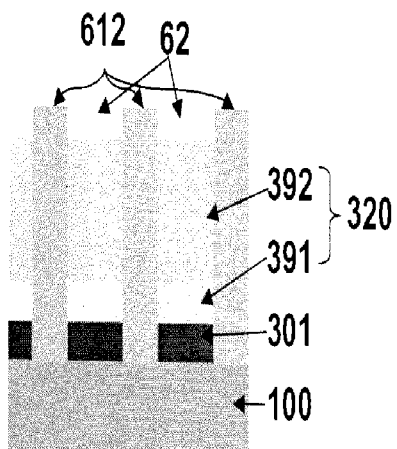


Fig. 6C

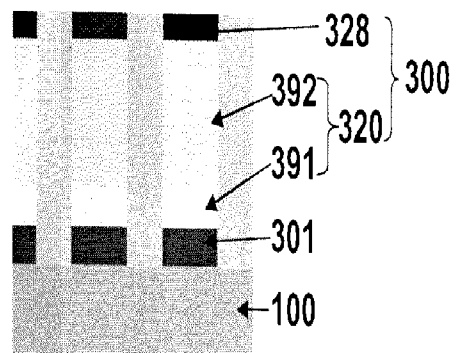


Fig. 6D

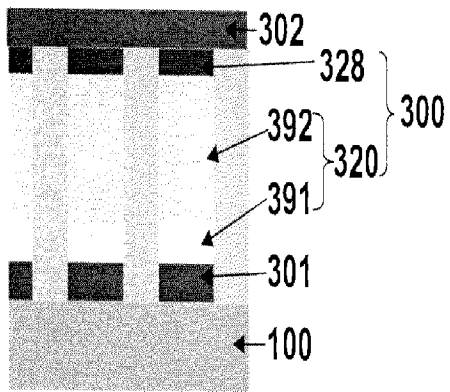


Fig. 6E

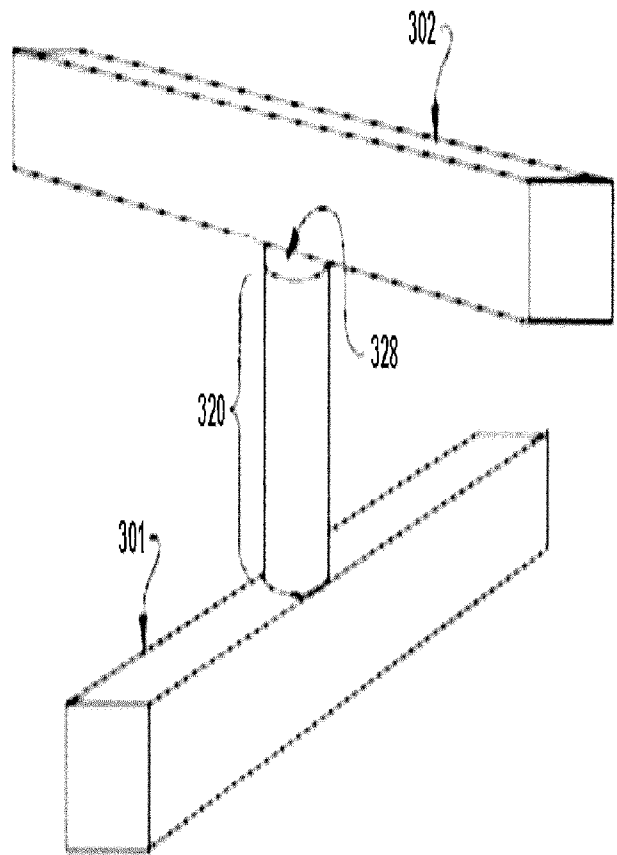


Fig. 6F

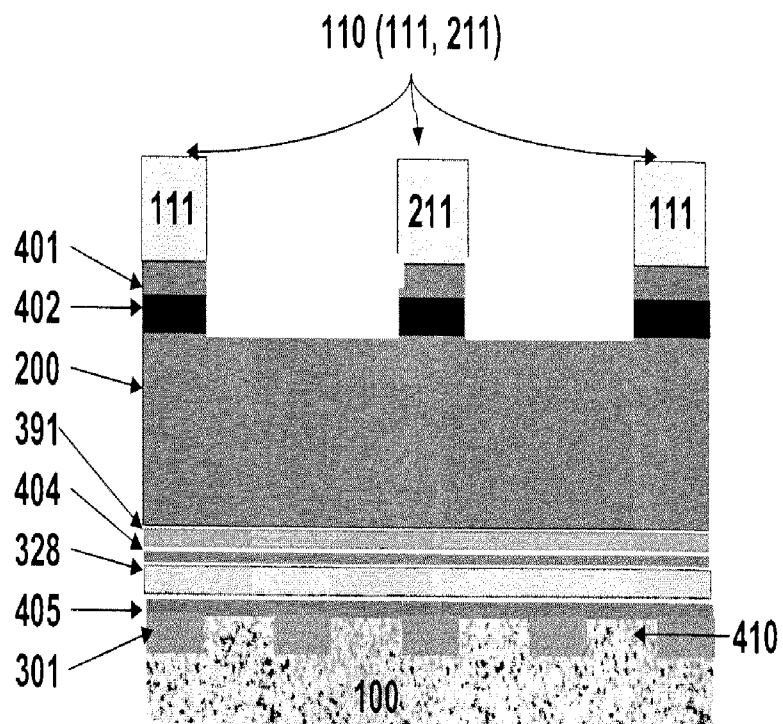


Fig. 7A

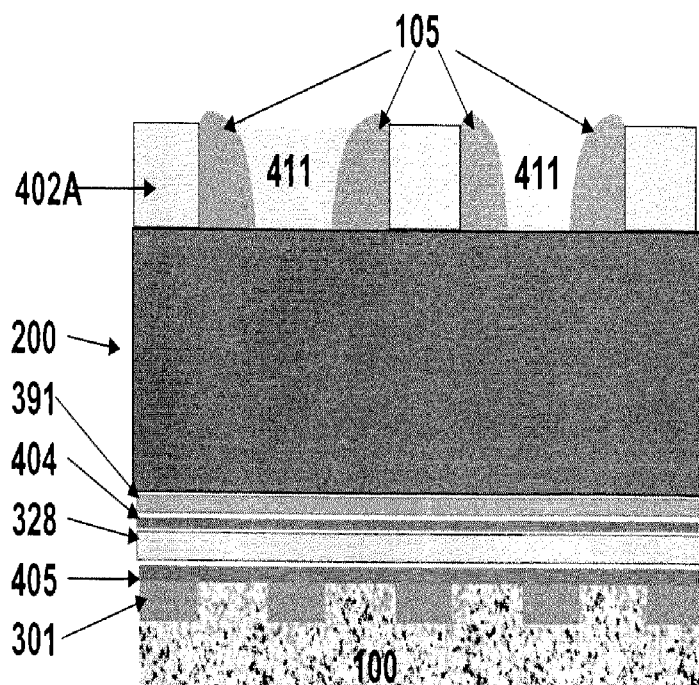


Fig. 7B