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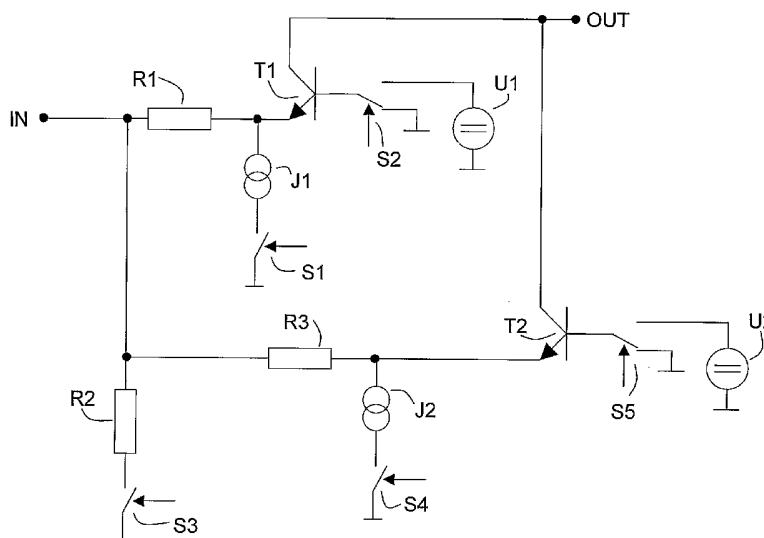
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(54) Title: CONTROLLABLE RF BROADBAND AMPLIFIER WITH A CONSTANT INPUT IMPEDANCE



(57) Abstract: A variable-gain RF amplifier arrangement whose input impedance is essentially independent of the selected gain is proposed, which has a large number of selectable elementary amplifiers, with an input signal being scaled and the input impedance being set to be the same by means of switchable current limiting elements upstream of the elementary amplifiers, which are associated with the elementary amplifiers. The circuit also has a low noise level, which is largely independent of the selected gain, and good linearity. A broadcast radio receiver as well as a receiver for receiving data signals using an amplifier according to the invention are also proposed.

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- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*
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**Controllable RF broadband amplifier with a constant
input impedance**

The invention relates to the field of controllable
5 radio-frequency amplifiers, in particular controllable
gain radio-frequency amplifiers, whose input impedance
is independent of the gain. A further aspect of the
invention relates to receivers for modulated
radio-frequency signals.

10

Signals which have a wide dynamic range are
processed in radio-frequency amplifiers, such as those
used in radio and television receivers, or satellite
receivers. Radio-frequency amplifiers of this type are
15 normally used as input amplifiers. In order to allow
both weak and strong signals to be processed by the
radio-frequency amplifier, it is desirable for the gain
level to be adjustable. The signal level can thus be
matched to the downstream signal processing stages.
20 When a weak signal is applied to the input amplifier,
the amplifier has to operate with high gain while, at
the same time, as little interference as possible may
be added to the signal. Undesirable interference
includes, for example, noise and distortion. When a
25 strong signal is applied to the input of the amplifier,
the amplifier has to operate with less gain, and must
not be saturated by the signal. In both modes, good
linearity and an input impedance which remains the same
over a wide frequency range are desirable.

30

Amplifiers with a constant input impedance and
variable gain are known from the prior art, in which a
symmetrical input signal is passed to two or more
differential amplifiers with different gain factors.
35 The individual differential amplifiers can be connected
depending on the desired gain, and have a high input
impedance. The input impedance of the entire circuit is

set by means of a low impedance, which is connected between the differential inputs and is very small in comparison to the high input impedances of the differential amplifiers. The input impedances of the amplifiers can thus be ignored. Circuits such as these
5 frequently have an undesirable noise response, and the circuit configuration as a differential amplifier for a symmetrical input signal considerably increases the circuit complexity.

10

A variable gain for a radio-frequency amplifier can also be achieved by use of a variable control of the operating point of the amplifier in the linear region. However, shifting the operating point of an amplifier
15 can result in changes in the phase response or in the bandwidth.

One object of the invention is now to propose a radio-frequency amplifier with a constant input
20 impedance, a variable gain, high linearity and an improved noise response. One amplifier such as this is described in claim 1. Advantageous refinements of the amplifier according to the invention are specified in the dependent claims. A further object of the invention
25 is to propose a receiver for modulated radio-frequency signals.

The amplifier according to the invention comprises two or more elementary amplifiers which are connected
30 in parallel and are selected as a function of the desired amplification level. The input signal is passed in parallel to all the elementary amplifiers. The input impedance of one elementary amplifier is in this case at the same time used for scaling the input signal. The
35 individual elementary amplifiers each have essentially the same gain. The selection of one specific elementary amplifier at the same time results in selection of the

input impedance which is associated with this amplifier. Those amplifiers which are not selected as well as the impedances associated with them are disconnected from the circuit via switches, such that
5 they do not have any influence on the input impedance of the active circuit part. The switches are, for example, switching diodes, although transistor switches or the like may also be used. It is also possible to use different types of switch in different circuit
10 parts at the same time. The configuration of the radio-frequency amplifier according to the invention makes it possible to select freely variable and reproducible gain steps with little complexity, while at the same time ensuring an input impedance which is
15 essentially independent of the gain. Furthermore, the circuit is highly suitable for integration in an integrated circuit.

The field of application of the invention is not
20 restricted to the radio, television and satellite receivers mentioned initially. The radio-frequency amplifier according to the invention may be used in all appropriate applications which require constant input impedances and variable gains.

25
In a second aspect of the invention, a receiver is proposed for receiving broadcast radio signals using a radio-frequency amplifier according to the invention. In this case, broadcast radio receivers are receivers
30 for analog or digital audio and/or video transmissions, such as receivers for VHF radio, digital audio broadcast (DAB) or digital television (DVB). Although a receiver according to the invention can be used particularly advantageously for receiving wireless
35 transmissions, the receiver is also suitable for cable transmissions.

In a third aspect of the invention, a receiver is proposed for receiving data signals using a radio-frequency amplifier according to the invention. A receiver such as this is used, inter alia, in wireless or cable communications networks. In this case, communications networks comprise both cable data networks, such as Local Area Networks (LAN) or Controller Area Networks (CAN), and wireless data networks, such as the Universal Mobile Telecommunications System (UMTS), the Global System for Mobile Communication (GSM) or the Digital Enhanced Cordless Telephone (DECT). The data content, the frequency range used and the type of modulation are in this case irrelevant. It is thus possible to receive computer data or else speech data, and the circuit arrangement is not restricted to specific frequency ranges.

The radio-frequency amplifier according to the invention will now be described in more detail with reference to the drawing, in which:

Figure 1 shows a schematic illustration of a radio-frequency amplifier according to the invention having two amplification stages;

Figure 2 shows the circuit of the radio-frequency amplifier according to the invention as shown in Figure 1, with a first selected gain level;

Figure 3 shows the radio-frequency amplifier according to the invention as shown in Figure 1, with a second selected gain level.

In the figures, identical reference symbols denote the same or similar elements.

In the schematic illustration of a radio-frequency amplifier according to the invention as shown in Figure 1, an input signal, which is not shown, is passed to an input IN. The input IN is connected to a first and to a second parallel-connected amplifier branch. The first amplifier branch has a resistor R1, whose first connection is connected to the input IN, and whose second connection is connected to the emitter electrode of a transistor T1. A current source J1 which can be switched on via a switch S1 is also connected to the emitter electrode of the transistor T1. The base connection of the transistor T1 is connected to a switch S2, by means of which the base can be connected either to ground or to a DC voltage source U1. The collector of the transistor T1 forms the output of the circuit, and is connected to the output OUT. The second amplifier branch is also connected to the input IN. The second amplifier branch has a resistor R2, whose first connection is connected to the input IN of the amplifier. The resistor can be connected to ground via a switch S3 which is connected to a second connection of the resistor R2. The first connection of the resistor R2 and the input IN are also connected to a resistor R3 via which the emitter electrode of a transistor T2 is connected to the input IN. The emitter electrode of the transistor T2 is also connected to a current source J2, which is connected in a switchable manner to ground via a switch S4. The base connection of the transistor T2 is connected via a switch S5 to ground or to a DC voltage source U2. The collector connection of the transistor T2 is connected to the collector connection of the transistor T1 and, together with it, forms the output OUT.

The first amplifier branch is activated when the radio-frequency amplifier as shown in Figure 1 is in the configuration shown in Figure 2. For this purpose,

the switch S1 is closed, and the current source J1 is thus activated. The switch S2 connects the base of the transistor T1 to the DC voltage source U1. A signal which is applied to the input IN, but is not
5 illustrated, is now passed via the resistor R1 to the emitter connection of the transistor T1. The current source J1 and the potential U1 at the base of the transistor T1 set the operating point of the transistor. The signal is passed from the collector
10 connection of the transistor T1, which is in this mode operated as a common-base circuit, to the output OUT. Since the switch S3 is open, only a first connection of the resistor R2 is connected to the circuit, and it therefore has no effect. The open switch S4 deactivates
15 the current source J2, and the switch S5 connects the base of the transistor T2 to ground potential. Only one connection of the resistor R3 is thus likewise effectively connected to the circuit, and it has no influence on the input impedance of the active circuit.
20 The current source J1 has a high impedance for high frequencies, and the voltage source U1 represents a short circuit for high frequencies. Owing to the low differential resistance of the base/emitter junction of the transistor T1, the resistor R1 is connected to
25 ground for high frequencies, via the base/emitter junction and the voltage source U1. The input impedance of the circuit is thus essentially governed by R1, and the signal is passed in its entirety to the emitter of the transistor T1.

30

In the illustration of the radio-frequency amplifier according to the invention as shown in Figure 3, the second amplifier branch is activated. For this purpose, the switch S3 is closed, and connects the
35 input IN via the resistor R2 to ground. The input IN is also connected to the resistor R3, which connects the input IN to the emitter connection of the transistor

T2. The current source J2 which is connected to the emitter connection of the transistor T2 is activated by the switch S4, which is now closed. The switch S5 connects the base connection of the transistor T2 to the DC voltage source U2. The switch S1 is open, and the switch S2 connects the base connection of the transistor T1 to ground. Only one connection of the resistor R1, which is likewise connected to the input IN, is thus effectively connected to the circuit, and has no influence on the input impedance. The operating point of the amplifier T2 is set by the DC voltage potential from the DC voltage source U2 at the base connection of the transistor T2 and the current source J2 at the emitter connection of the transistor T2. The input impedance of the amplifier circuit is formed by the resistors R2 and R3 connected in parallel. In this case, as has been described above, the resistor R2 is connected directly to ground, while the resistor R3 is connected to ground via the base/emitter junction of the transistor T2, via the switch S5 and via the DC voltage source U2. The base/emitter junction of the transistor T2 in this case has a very low differential resistance in comparison to the resistance values of the resistors R2 and R3, and is thus negligible. The DC voltage source U2 represents a short circuit to ground for high frequencies, and the current source J2 has a high impedance for high frequencies. The DC voltage source U2 and the current source J2 can thus likewise be ignored. The circuit arrangement of the resistors R2 and R3 results in a part of the signal which is applied to the input IN being tapped off directly to ground, and only a part of the signal being passed via the resistor R3 to the transistor T2. The magnitude of the part of the signal which is passed to the transistor T2 is governed by the ratio of the resistors R2 and R3. The input signal that has been scaled in this way is amplified by the transistor T2 and is produced at the

output OUT. The two resistors R2 and R3 can be selected such that the parallel circuit formed by these resistors has the same value as the resistor R1 which governs the input impedance of the circuit when the first amplifier branch is activated. If, by way of example, the input signal is intended to be halved before amplification, the resistors R2 and R3 may each be twice as large as R1 from the description relating to Figure 2. The input impedance is then calculated as follows:

where $R2 = R3 = 2R1$;

$$Z_{IN} = \frac{R2 \times R3}{R2 + R3} = \frac{2R1 \times 2R1}{2R1 + 2R1} = R1$$

The example described further above with reference to Figure 2 to this extent represents a special case of the situation described with reference to Figure 3, in that there is no resistor corresponding to the resistor R2 from Figure 3. In order to obtain an elementary amplifier according to the invention in the general configuration as described in Figure 3, it would thus be necessary to insert a resistor of infinitely high resistance into the circuit such that it, together with the resistor R1, forms a voltage divider for the signal, and is connected in parallel with the resistor R1 with regard to the calculation of the input impedance.

Owing to the wide range of possible ways of scaling a signal by means of two resistors while at the same time setting an essentially constant input impedance, the circuit can easily be extended by any desired gain factors. One advantageous feature in this case is that only the selected part of the circuit in each case contributes to the amplification and to the input impedance. The simple configuration of the circuit and the use of semiconductor switches particularly

advantageously allow the radio-frequency amplifier according to the invention to be integrated in integrated circuits.

Patent claims

1. An amplifier arrangement with a variable gain factor having at least two elementary amplifiers
5 connected in parallel, **wherein** each elementary amplifier has associated independent current-limiting means (R1; R2, R3) which can be switched selectively for individual scaling of an input signal that is to be amplified, and wherein an
10 input impedance which is essentially the same for each elementary amplifier can be set by means of the current-limiting means (R1; R2, R3).
2. The amplifier arrangement as claimed in claim 1,
15 **wherein** at least one elementary amplifier is a common-base transistor circuit (T1; T2).
3. The amplifier arrangement as claimed in claims 1 and 2, **wherein** means (U1, J1; U2, J2) are provided
20 in order to operate the transistors in the linear region.
4. The amplifier arrangement as claimed in claim 3,
25 **wherein** the means include current sources (J1; J2).
5. The amplifier arrangement as claimed in one or more of claims 1 to 4, **wherein** at least two collector connections of the transistors of the elementary amplifiers form a common output (OUT).
30
6. The amplifier arrangement as claimed in one or more of claims 1 to 5, **wherein** the base connections of the transistors of the elementary amplifiers can be connected via switches (S2; S5) to DC voltage
35 potentials (U1; U2).

7. The amplifier arrangement as claimed in claim 6, **wherein** the switches (S2; S5) are switching diodes and/or electronic switches.
- 5 8. The amplifier arrangement as claimed in one or more of claims 1 to 7, **wherein** the current-limiting means (R1; R2, R3) are resistors.
- 10 9. The amplifier arrangement as claimed in one or more of claims 1 to 8, **wherein** a first part of an input signal can be supplied to one elementary amplifier via a first part of the current-limiting means (R1; R3) which are in each case associated with this elementary amplifier.
- 15 10. The amplifier arrangement as claimed in one or more of claims 1 to 9, **wherein** a second part of an input signal can be tapped off with respect to signal ground via a second part of the current-limiting means (R2) which are in each case associated with one elementary amplifier.
- 20 11. The amplifier arrangement as claimed in one or more of claims 1 to 10, **wherein** the first part and the second part of the current-limiting means (R2, R3) which are in each case associated with one elementary amplifier are connected such that they represent a parallel circuit for the input signal.
- 25 12. The amplifier arrangement as claimed in one or more of claims 1 to 11, **wherein** the resultant impedances of the parallel circuit comprising the first part and the second part of the current-limiting means (R2, R3) of each elementary amplifier essentially
- 30 have the same values.
- 35

13. A broadcast radio receiver having an amplifier arrangement as claimed in one or more of the preceding claims.
- 5 14. A receiver for data signals having an amplifier arrangement as claimed in one or more of claims 1 to 12.

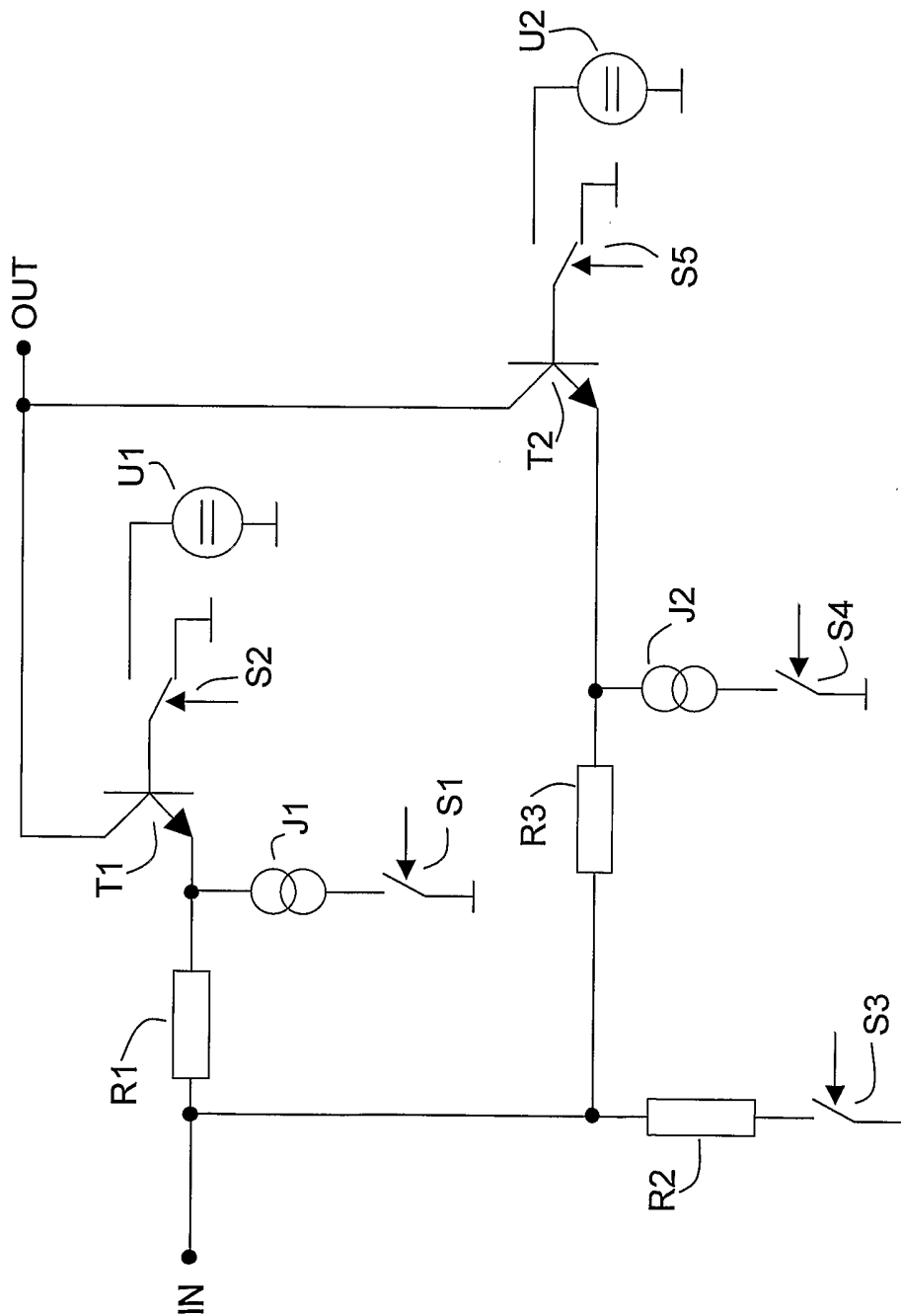


Fig. 1

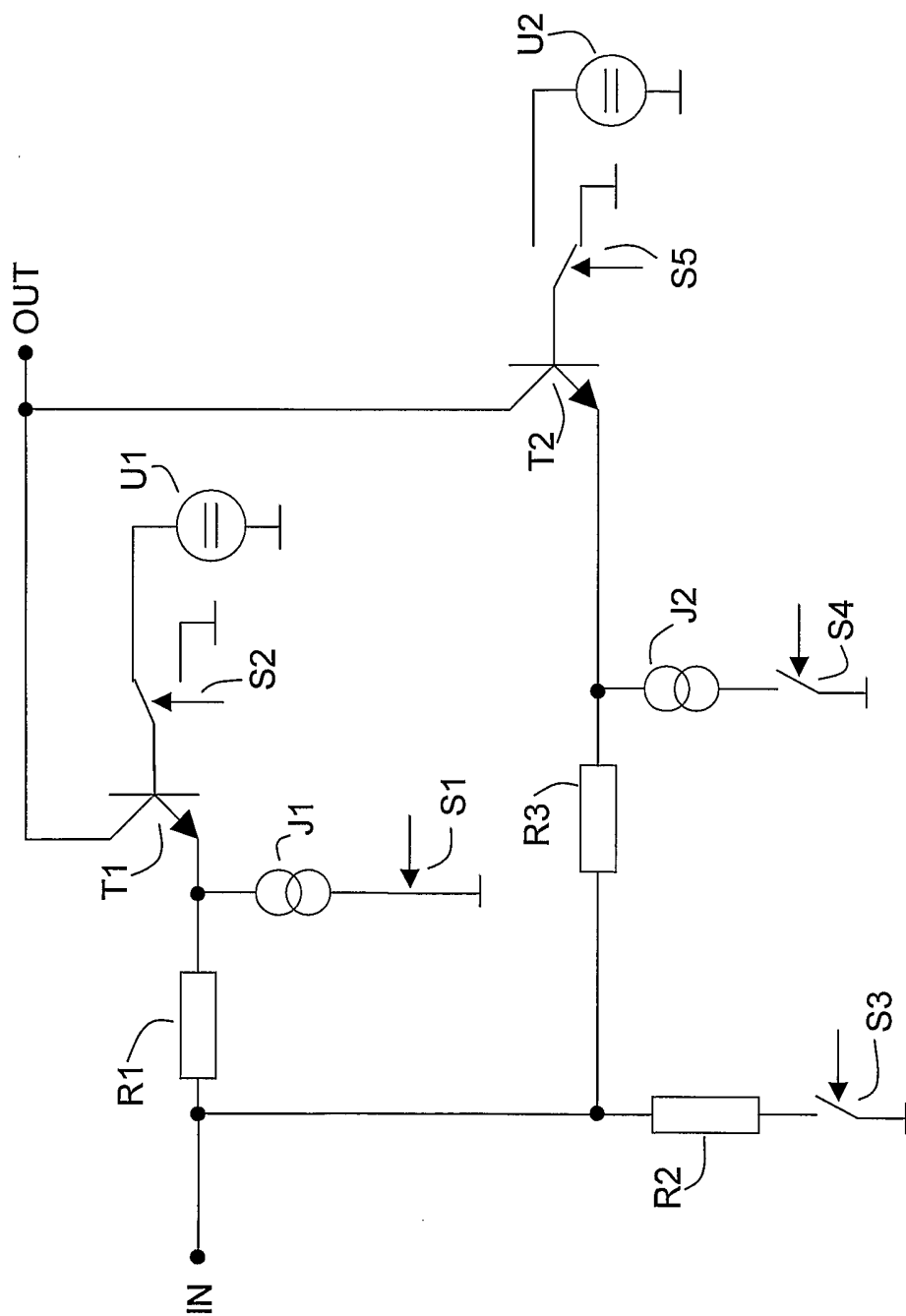


Fig. 2

INTERNATIONAL SEARCH REPORT

International Application No

PCT/EP 03/13741

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H03F3/72 H03G1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03G H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 530 404 A (DEBROUX JEAN-FRANCOIS) 25 June 1996 (1996-06-25) column 2, line 26 - column 3, line 62; figure 2	1-9, 11-14
A	US 5 977 828 A (NISBET JOHN JACKSON ET AL) 2 November 1999 (1999-11-02) column 4, line 53 - column 5, line 38; figure 5	1

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

° Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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Patent document cited in search report	A	Publication date	Patent family member(s)	Publication date
US 5530404	A	25-06-1996	FR 2714237 A1 DE 69413365 D1 DE 69413365 T2 EP 0658977 A1	23-06-1995 22-10-1998 11-03-1999 21-06-1995
US 5977828	A	02-11-1999	NONE	