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(54) **Title**: METHOD AND DEVICE FOR DATA COMMUNICATION BETWEEN TWO CAMERAS

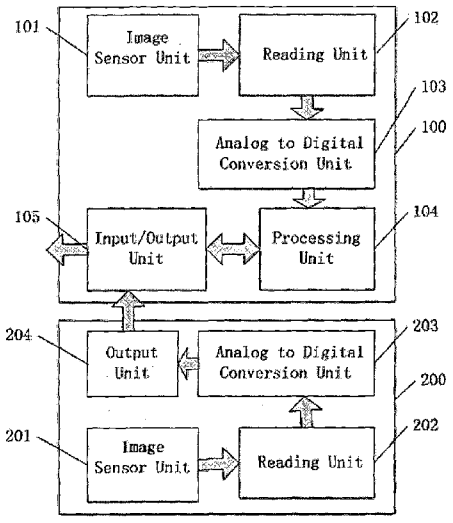

Fig. 2

(57) **Abstract**: A method and a device for data communication between two cameras are provided in the present invention. The method includes: providing a two-camera device, wherein a master chip is arranged in a camera and a slave chip is arranged in the other camera; configuring an alternate working mechanism between the master chip and the slave chip, wherein when the master chip works in a horizontal scan state, the slave chip works in a horizontal blanking state; and when the master chip works in the horizontal blanking state, the slave chip works in the horizontal scan state; and configuring the slave chip to send out digital signals while working in the horizontal scan state and the master chip to receive the digital signals while working in the horizontal blanking state. The present invention can simplify internal structure and reduce size of a two-camera device, thereby reducing cost of the two-camera device.

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METHOD AND DEVICE FOR DATA COMMUNICATION BETWEEN TWO CAMERAS

Cross Reference to Related Applications

[0001] The present application claims the priority of Chinese Patent Application No. 201110027450.6, entitled "Method and device for data communication between two cameras", and filed on January 25, 2011, the entire disclosure of which is incorporated herein by reference.

Field of the Invention

[0002] This invention is generally related to image processing field, and particularly to a method and a device for data communication between two cameras.

Background of the Invention

[0003] As an image acquisition device, the camera chip is widely used in digital products such as mobile phones, PDAs and laptops. To enhance functional performance of products, more and more of the products are equipped with two cameras, for example, one camera facing forwards and the other one facing backwards, to support both taking pictures and video calling. In prior art, the two cameras may communicate with a receiving chip separately by using their own dedicated data buses or communicate with a receiving chip alternatively by sharing one data bus. If the two cameras communicate with a receiving chip alternatively by sharing one data bus, the two cameras can not work and drive the data bus at the same time, wherein each of the two cameras has dedicated functional blocks including an image area, analog circuits and an image processing unit. After analysis herein, the inventor found that, if the two cameras communicate with a receiving chip by sharing one data bus, the two cameras also can share only one image processing unit, which results an image processing unit is removed from a two-camera device formed in the prior art, thereby simplifying internal structure of the two-camera device and reducing cost of the two-camera device.

[0004] Chinese Patent Publication No. CN101877760A discloses a two-camera device solution in which only one digital video port (DVP) data bus is used for supporting mobile phone connection. This solution uses one additional digital signal processing chip to manage two cameras by some of control functions such as setting up, operating, switching and resting. However, the solution only changes the communication way between cameras and the digital signal processing chip by sharing one digital video port (DVP) data bus and does not bring any obvious improvement to simplify internal structure and to reduce cost of the two-camera device.

Summary of the Invention

[0005] An object of the present invention is to simplify internal structure and to reduce cost of a two-camera device by sharing only one image processing unit.

[0006] To achieve this object, an embodiment of the present invention provides a method for data communication between two cameras, including:

providing a two-camera device, wherein a master chip is arranged in a camera and a slave chip is arranged in the other camera;

configuring an alternate working mechanism between the master chip and the slave chip. Wherein when the master chip is working in a horizontal scan state, the slave chip is working in a horizontal blanking state, and when the master chip works in the horizontal blanking state, the slave chip works in the horizontal scan state; and

configuring the slave chip to send out digital signals when the slave chip is in the horizontal scan state and the master chip to receive the digital signals which is sent from the slave chip when the master chip is in the horizontal blanking state.

[0007] Moreover, another embodiment of the present invention further provides a device for data communication between two cameras which includes a mater chip and a slave chip,

wherein the slave chip includes:

a first image sensor unit for acquiring first analog image signals;

a first reading unit for reading the first analog image signals from the first image sensor unit;

a first analog to digital conversion unit for converting the first analog image signals to first digital signals; and

an output unit which includes output interfaces for sending out the first digital signals;

and wherein the master chip includes:

a second image sensor unit for acquiring second analog image signals;

a second reading unit for reading the second analog image signals from the second image sensor unit;

a second analog to digital conversion unit for converting the second analog image signals to second digital signals;

a processing unit for converting the first digital signals and the second digital signals to image data; and

an input/output unit including data interfaces, wherein the data interfaces are adopted for sending the image data to a receiving chip and receiving the first digital signals from the slave chip when the master chip works in the horizontal blanking state.

Optionally, the master chip works in the horizontal scan state when the slave chip works in the horizontal blanking state, and the master chip works in the horizontal blanking state when the slave chip works in the horizontal scan state.

Optionally, when the master chip works in the horizontal blanking state, data interfaces between the master chip and the slave chip receive the first digital signals from the slave chip, and when the master chip works in the horizontal scan state, the data interfaces send the image data from the master chip to the receiving chip.

Compared with the prior art, the embodiments of the present invention have the following advantages: the embodiments of the present invention not only can simplify internal structure of the two-camera devices but also can make it practicable that only one image processing unit is used to control and manage two camera chips in different work states alternately. Therefore, size of the two-camera device becomes smaller and the cost of the two-camera devices is reduced.

Brief Description of the Drawings

[0008] FIG. 1 is a schematic structural view of a camera in a two-camera device in prior art;

[0009] FIG. 2 is a schematic structural view of a two-camera device according to an embodiment of the present invention; and

[0010] FIG. 3 is a schematic view for showing timing comparison between a master chip and a slave chip in a two-camera device according to the embodiment of the present invention;

Detailed Description of the Embodiments

[0011] The above-mentioned and other objectives, features and advantages of the present invention will become clearer through the description according attached drawings.

[0012] Referring to FIG. 1, which shows a schematic structural view of a camera in a two-camera device in prior art, each camera of the two-camera device has a same internal structure, including: an image sensor unit 101 for acquiring analog image signals; a reading unit 102 for reading the analog image signals from the image sensor unit 101; an analog to digital conversion unit 103 for converting the analog image signals to digital signals; a processing unit 104 for processing the digital signals such as noise removal, interpolating, edge enhancement, grayscale correction, color correction; and an input/output unit 105 including data interfaces for sending image information from the processing unit 104 to a receiving chip.

[0013] After research, the inventor found out that the data interfaces are idle in some time slices when the two-camera device is working. Therefore, in these time slices, one camera can receive image signals from the other camera and can send the image signals to its own processing unit. The time slices are defined as idle time periods of the two-camera device. Specifically, in a scan process of a scanning head in a camera which converts optical signals to electric signals, a scanning head always starts from an upper-left corner of an image, and proceeds horizontally. After the scanning head arrives at a right edge of the image, the scanning head returns to the left side again and starts to scan a next line. The state when the scanning head is scanning is defined as a horizontal scan state, and the state when the scanning head is returning from right edge to left edge is defined as a horizontal blanking state. When the camera is working in the horizontal blanking state, the camera stops sending out data and makes output interfaces idle. Therefore, the horizontal blanking state is an idle time period of the camera.

[0014] Therefore, data interfaces of one camera in a two-camera device can receive external image data when the camera works in the horizontal blanking state, and send out processed image information when the camera works in the horizontal scan state. Based on the principle, one processing unit of the other camera in the two-camera device can be removed and only one processing unit is used to process image signals for both of the two cameras in the two-camera device, which not only can ensure signal processing quality but also can reduce the cost and size of the two-camera device. In order to achieve the object, the inventor provides a method for data communication between two cameras in a two-camera device, including:

providing a two-camera device, wherein a master chip is arranged in a camera and a slave chip is arranged in the other camera;

configuring an alternate working mechanism between the master chip and the slave chip, wherein when the mast chip works in a horizontal scan state, the slave chip works in a horizontal blanking state; and when the mast chip works in the horizontal blanking state, the slave chip works in the horizontal scan state; and

configuring the slave chip to send out digital signals when the slave chip works in the horizontal scan state and the master chip to receive digital signals sent from the slave chip when the master chip works in the horizontal blanking state.

[0015] Referring to FIG. 2, the present invention further provides a device for data communication between two cameras, including a mater chip 100 and a slave chip 200.

[0016] The slave chip 200 includes: an image sensor unit 201 for acquiring first analog image signals; a reading unit 202 for reading the first analog image signals from the image sensor unit 201; an analog to digital conversion unit 203 for converting the first analog image signals to first digital signals; and an output unit 204 which includes output interfaces for sending out the first digital signals.

[0017] The master chip 100 includes: an image sensor unit 101 for acquiring second analog image signals; a reading unit 102 for reading the second analog image signals from the image sensor unit 101; an analog to digital conversion unit 103 for converting the second analog image signals to second digital signals; a processing unit 104 for converting the first digital signals and the second digital signals to image data; and an input/output unit 105 including data interfaces, wherein the data interfaces are adopted for sending out the image data to a receiving chip, and receiving the first digital signals from the slave chip when the master chip works in the horizontal blanking state.

[0018] Hereunder, the present invention will be described in detail with reference to embodiments in conjunction with the accompanying drawings.

[0019] Firstly, a two-camera device with a master chip 100 and a slave chip 200 is provided. Continuing to referring to FIG. 2, the slave chip 200 includes: an image sensor unit 201 for first acquiring analog image signals; a reading unit 202 for reading the first analog image signals from the image sensor unit 201; an analog to digital conversion unit 203 for converting the first analog image signals to first digital signals; and an output unit 204 which includes output interfaces for sending the first digital signals to the input/output unit 105 of the master chip 100. Similarly, the master chip 100 includes: an

image sensor unit 101 for acquiring second analog image signals; a reading unit 102 for reading the second analog image signals from the image sensor unit 101; an analog to digital conversion unit 103 for converting the second analog image signals to second digital signals; a processing unit 104 for converting the first digital signals and the second digital signals to image data; and an input/output unit 105 including data interfaces, wherein the data interfaces are adopted for sending the image data to a receiving chip, and receiving the first digital signals from the slave chip 200 when the master chip works in the horizontal blanking state.

[0020] In a first embodiment of the present invention, the master chip 100 communicates with a receiving chip in a DVP parallel port mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 1 data output pin and some other pins, and the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin of the slave chip 200, and one of the rest data output pins in the master chip 100 is connected with the data output pin of the slave chip 200.

[0021] Optionally, the master chip 100 communicates with a receiving chip in DVP parallel port mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 2 data output pin and some other pins, and the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin of the slave chip 200, and two of the rest data output pins in the master chip 100 is connected with the data output pins of the slave chip 200.

[0022] Optionally, the master chip 100 communicates with a receiving chip in DVP parallel port mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 3 data output pin and some other pins, and the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin

of the slave chip 200, and three of the rest data output pins in the master chip 100 is connected with the data output pins of the slave chip 200.

[0023] Optionally, the master chip 100 communicates with a receiving chip in DVP parallel port mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 4 data output pin and some other pins, and the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin of the slave chip 200, and four of the rest data output pins in the master chip 100 is connected with the data output pins of the slave chip 200.

[0024] In a second embodiment of the present invention, the master chip 100 communicates with a receiving chip in a SPI mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 1 data output pin and some other pins, the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin of the slave chip 200, another one of the 8 data output pins in the master chip 100 is connected with the receiving chip as a SPI data pin, and one of the rest data output pins in the master chip 100 is connected with the data output pin of the slave chip 200.

[0025] Optionally, the master chip 100 communicates with a receiving chip in SPI mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 2 data output pin and some other pins, and the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin of the slave chip 200, another one of the 8 data output pins in the master chip 100 is connected with the receiving chip as a SPI data pin, and two of the rest data output pins in the master chip 100 is connected with the data output pins of the slave chip 200.

[0026] Optionally, the master chip 100 communicates with a receiving chip in SPI mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 3 data output

pin and some other pins, and the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin of the slave chip 200, another one of the 8 data output pins in the master chip 100 is connected with the receiving chip as a SPI data pin, and three of the rest data output pins in the master chip 100 is connected with the data output pins in the slave chip 200.

[0027] Optionally, the master chip 100 communicates with a receiving chip in SPI mode. The output unit 204 of the slave chip 200 includes 1 clock output pin, 4 data output pin and some other pins, and the input/output unit of the master chip 100 includes 8 data output pins and some other pins, wherein one of the 8 data output pins in the master chip 100 works as a clock input pin and is connected with the clock output pin of the slave chip 200, another one of the 8 data output pins in the master chip 100 is connected with the receiving chip as a SPI data pin, and four of the rest data output pins in the master chip 100 is connected with the data output pins of the slave chip 200.

[0028] Thereafter, referring to the FIG. 3, the master chip and the slave chip are configured to work under an alternate working mechanism. Specifically, the master chip 100 and the slave chip 200 are configured to work with a same clock frequency. Moreover, the master chip 100 works in the horizontal blanking state when the slave chip 200 works in the horizontal scan state, and, in contrast, the master chip 100 works in the horizontal scan state when the slave chip 200 works in the horizontal blanking state.

[0029] Thereafter, when the master chip 100 works in the horizontal blanking state, the slave chip 200 sends digital image signals to the master chip 100, and the master chip 100 receives the digital image signals from the slave chip 200.

[0030] According to the first embodiment of the present invention described above, the two-camera device may work in two modes: a stand-alone mode in which the master chip works alone and a master-slave mode in which the master chip and the slave chip both work. The master chip 100 communicates with a receiving chip in DVP parallel port mode. Specifically, in the mater-slave mode, the slave chip 200 acquires first image

signals through the image sensor unit 201; After that, the reading unit 202 of the slave chip reads the first image signals and sends the first image signals to the analog to digital conversion unit 203; then the analog to digital conversion unit 203 converts the first analog image signals to first digital signals and sends the first digital signals to the output unit 204; further, when the master chip works in the horizontal blanking state and the slave chip works in the horizontal scan state, the first digital signals in the output unit 204 is sent to the processing unit 104 trough the input/output unit 105 of the master chip, so that the processing unit 104 can receive and process the first digital image signals from the slave chip 200; finally, the processed image information can be sent from the processing unit 104 to DVP interfaces of the receiving chip through the input/output unit 105 when the master chip works in the horizontal scan state and the slave chip works in the horizontal blanking state. Moreover, the communication mode between the master chip 100 and the slave chip 200 includes a parallel communication mode and a serial communication mode. Optionally, the master chip 100 communicates with the slave chip 200 in the serial communication mode, wherein the serial communication mode supports not only unspecified number data bits but also flag bits which is used for marking by the master chip 100. Similarly, in the stand-alone mode, the master chip 100 acquires second image signals through the image sensor unit 101; after that, the reading unit 102 of the master chip reads the second image signals and sends the second image signals to the analog to digital conversion unit 103; then, the analog to digital conversion unit 103 converts the second analog image signals to second digital signals and sends the second digital signals to the processing unit 104; finally, the processing unit 104 processes the second digital signals, and sends the processed image information to the interfaces of an receiving chip through the input/output unit 105.

[0031] According to the second embodiment of the present invention mentioned above, the two-camera device may work in two modes: a stand-alone mode in which the master chip works alone and a master-slave mode in which the master chip and the slave chip both work. The master chip 100 communicates with a receiving chip in a SPI parallel port mode. Specifically, in the mater-slave mode, the slave chip 200 acquires first image

signals through the image sensor unit 201; After that, the reading unit 202 of the slave chip reads the first image signals and sends the first image signals to the analog to digital conversion unit 203; then the analog to digital conversion unit 203 converts the first analog image signals to first digital signals and sends the first digital signals to the output unit 204; further, when the master chip works in the horizontal blanking state and the slave chip works in the horizontal scan state, the first digital signals in the output unit 204 is sent to the processing unit 104 trough the input/output unit 105 of the master chip, so that the processing unit 104 can receive and process the first digital image signals from the slave chip 200; finally, the processed image information can be sent from the processing unit 104 to SPI interfaces of the receiving chip through the input/output unit 105 when the master chip works in the horizontal scan state and the slave chip works in the horizontal blanking state. Moreover, the communication mode between the master chip 100 and the slave chip 200 includes a parallel communication mode and a serial communication mode. Optionally, the master chip 100 communicates with the slave chip 200 in the serial communication mode, wherein the serial communication mode supports not only unspecified number data bits but also flag bits which is used for marking by the master chip 100. Similarly, in the stand-alone mode, the master chip 100 acquires second image signals through the image sensor unit 101; after that, the reading unit 102 of the master chip reads the second image signals and sends the second image signals to the analog to digital conversion unit 103; then, the analog to digital conversion unit 103 converts the second analog image signals to second digital signals and sends the second digital signals to the processing unit 104; finally, the processing unit 104 processes the second digital signals, and sends the processed image information to the interfaces of an receiving chip through the input/output unit 105.

[0032] Although the present invention has been disclosed as above with reference to preferred embodiments, it is not intended to limit the present invention. Any other technologists in this field may modify and vary the embodiments without departing from the spirit and scope of the present invention. Accordingly, the scope of the present invention shall be defined in the appended claim.

CLAIMS

What is claimed is:

1. A method for data communication between two cameras, comprising:

providing a two-camera device, wherein a master chip is arranged in a camera and a slave chip is arranged in the other camera;

configuring an alternate working mechanism between the master chip and the slave chip, wherein when the mast chip works in a horizontal scan state, the slave chip works in a horizontal blanking state; and when the mast chip works in the horizontal blanking state, the slave chip works in the horizontal scan state; and

configuring the slave chip to send out digital signals in the horizontal scan state and the master chip to receive the digital signals sent from the slave chip in the horizontal blanking state.

2. A device for data communication between two cameras, comprising a mater chip and a slave chip,

wherein the slave chip comprises:

a first image sensor unit for acquiring first analog image signals;

a first reading unit for reading the first analog image signals from the first image sensor unit;

a first analog to digital conversion unit for converting the first analog image signals to first digital signals; and

an output unit which comprises output interfaces for sending out the first digital signals;

and wherein the master chip comprises:

a second image sensor unit for acquiring second analog image signals;

a second reading unit for reading the second analog image signals from the second image sensor unit;

a second analog to digital conversion unit for converting the second analog image signals to second digital signals;

a processing unit for converting the first digital signals and the second digital signals to image data; and

an input/output unit comprising data interfaces, wherein the data interfaces are adopted for sending the image data to a receiving chip, and receiving the first digital signals from the slave chip when the master chip works in a horizontal blanking state.

3. The device for data communication between two cameras according to claim 2, wherein when the master chip works in a horizontal scan state, the slave chip works in the horizontal blanking state; in contrast, when the master chip works in the horizontal blanking state, the slave chip works in the horizontal scan state.

4. The device for data communication between two cameras according to claim 3, wherein when the master chip works in the horizontal blanking state, data interfaces between the master chip and the slave chip receive the first digital signals from the slave chip; and when the master chip works in the horizontal blanking state, the data interfaces send the image data from the master chip to the receiving chip.

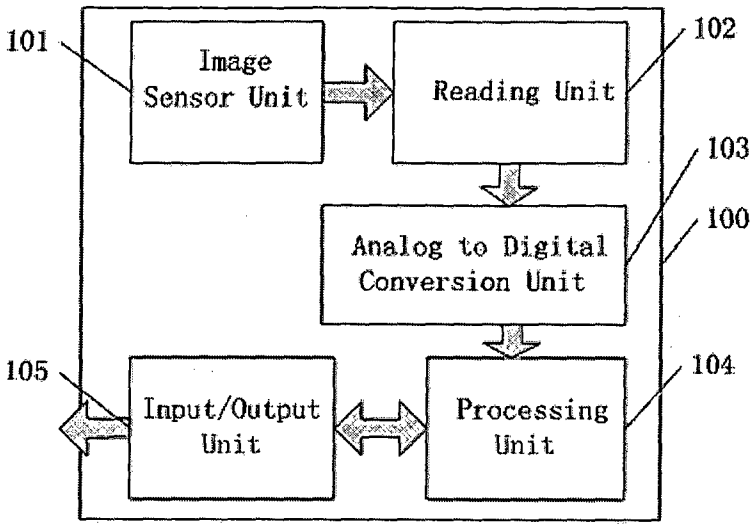

Fig. 1 (prior art)

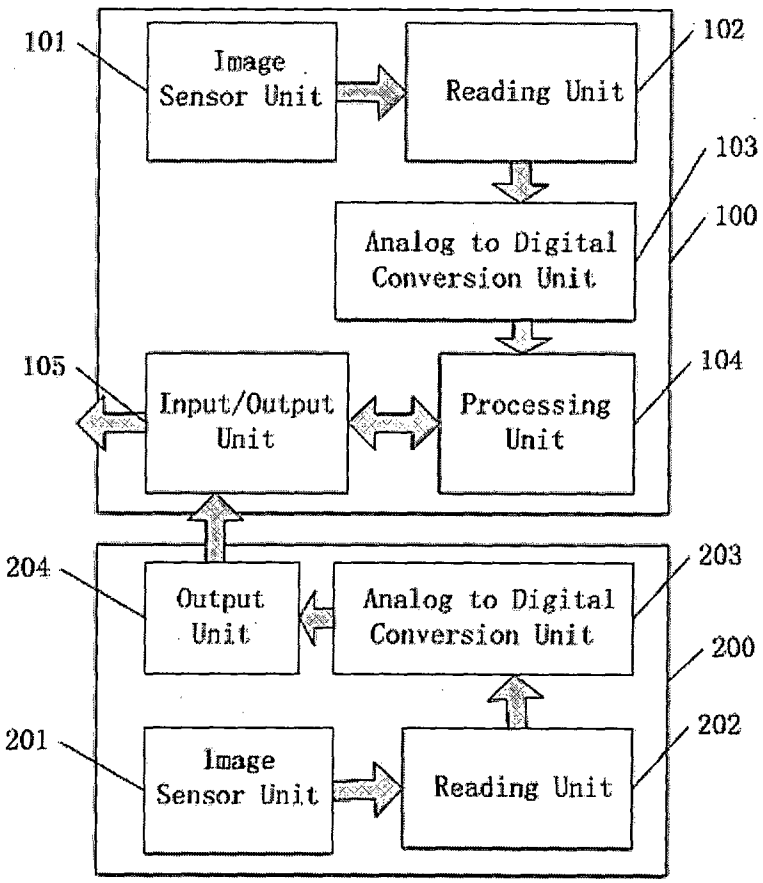

Fig. 2

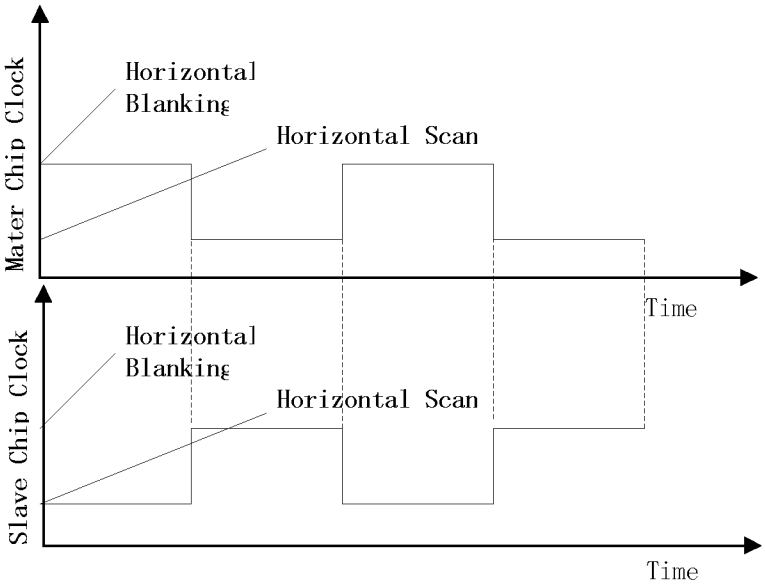
Mater Chip Clock
Horizontal Blanking
Horizontal Scan
Time
Slave Chip Clock
Horizontal Blanking
Horizontal Scan
Time

Fig. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/079527

A. CLASSIFICATION OF SUBJECT MATTER

H04N5/225 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS,CNKI,VEN: two, double, dual, duplex, plural, plurality, camera?, sensor? main, master, slave, communicat???, transmit+, input, output, receiv???, send???, sent, blank???, idle, valid, busy, invalid, scan+, state, mechanism, status

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN102164232A(GALAXYCORE INC.)24 August 2011(24.08.2011) claims 1-4	1-4
Y	CN101849408A(EASTMAN KODAK CO.)29 September 2010(29.09.2010) the description paragraphs 20-32, figure 2	1-4
Y	CN101001388A(MATSUSHITA ELECTRIC IND. CO., LTD.)18 July 2007(18.07.2007) the description page 6 paragraph 2 to page 7 paragraph 3, figures 1-3	1-4
A	US2006024047A1(LG ELECTRONICS INC.)02 February 2006(02.02.2006) the whole document	1-4
A	JP2009260916A(SONY CORP.)05 November 2009(05.11.2009) the whole document	1-4

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 November 2011(29.11.2011)	**15 Dec. 2011 (15.12.2011)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer ZHANG, Zhihua Telephone No. (86-10)62412010

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/079527

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
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