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(54) CIRCUITRY AND GATE STACKS

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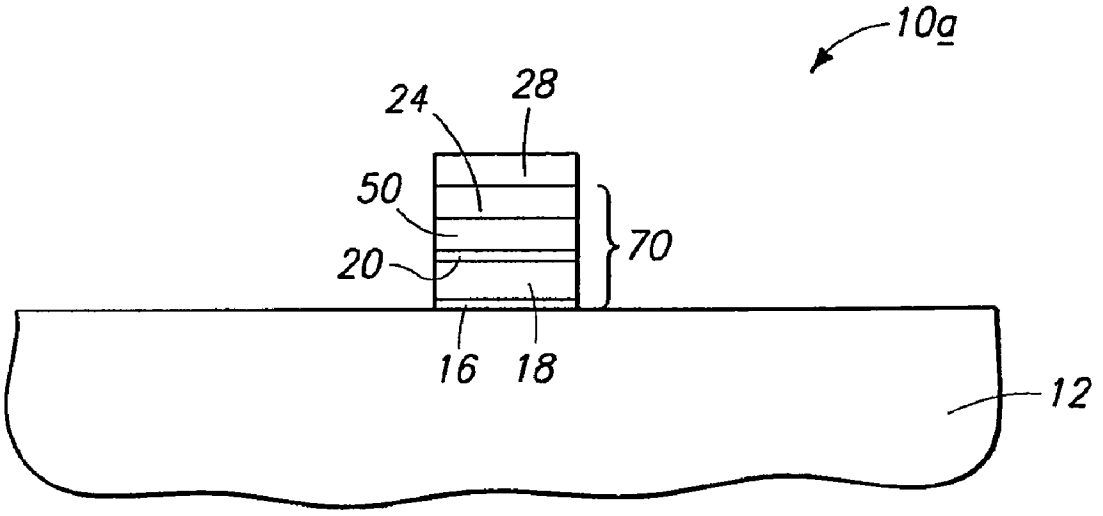
(57) **ABSTRACT**

The present invention includes semiconductor circuitry. Such circuitry encompasses a metal silicide layer over a substrate and a layer comprising silicon, nitrogen and oxygen in physical contact with the metal silicide layer. The present invention also includes a gate stack which encompasses a polysilicon layer over a substrate, a metal silicide layer over the polysilicon layer, an antireflective material layer over the metal silicide layer, a silicon nitride layer over the antireflective material layer, and a layer of photoresist over the silicon nitride layer, for photolithographically patterning the layer of photoresist to form a patterned masking layer from the layer of photoresist and transferring a pattern from the patterned masking layer to the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer. The patterned silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer encompass a gate stack.



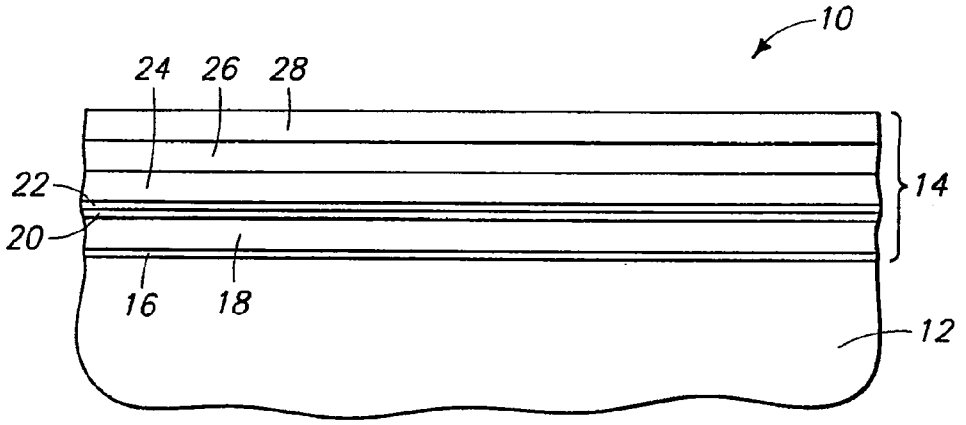


FIG. 1
(PRIOR ART)

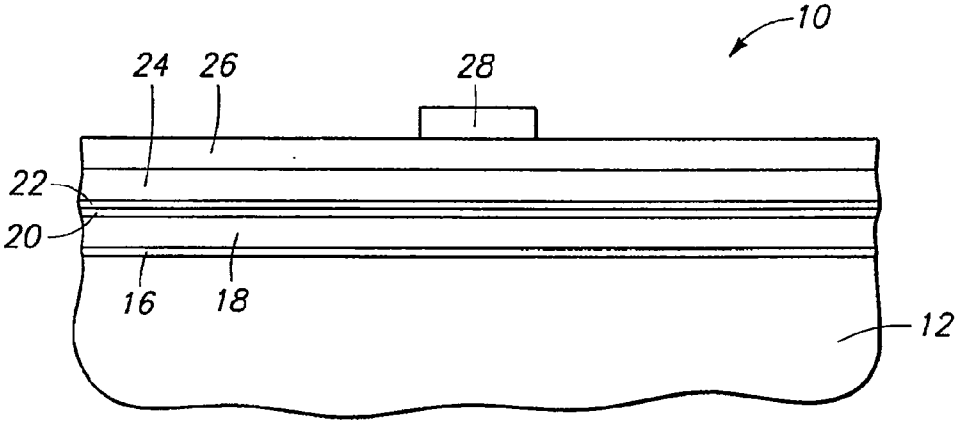


FIG. 2
(PRIOR ART)

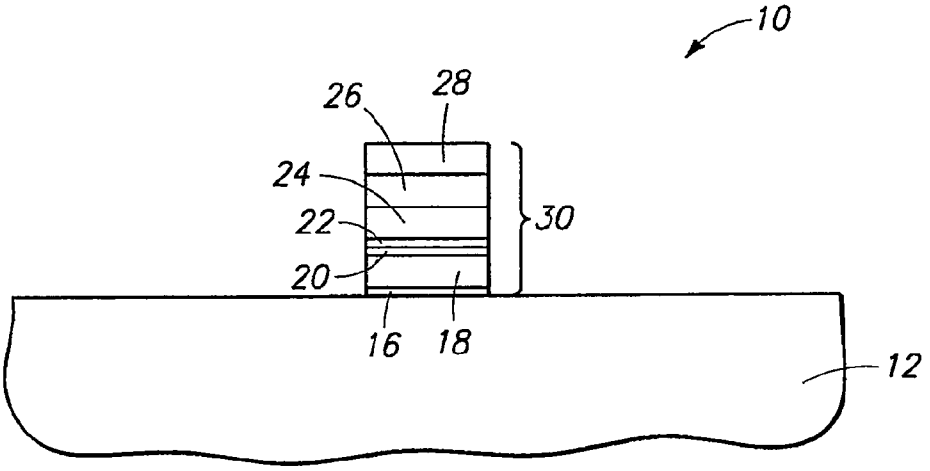


FIG. 3
(PRIOR ART)

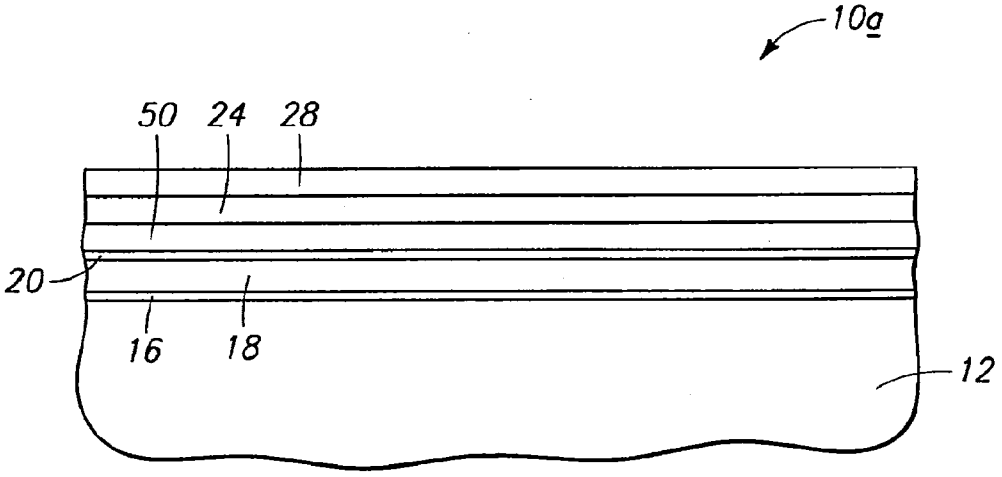


FIG. 4

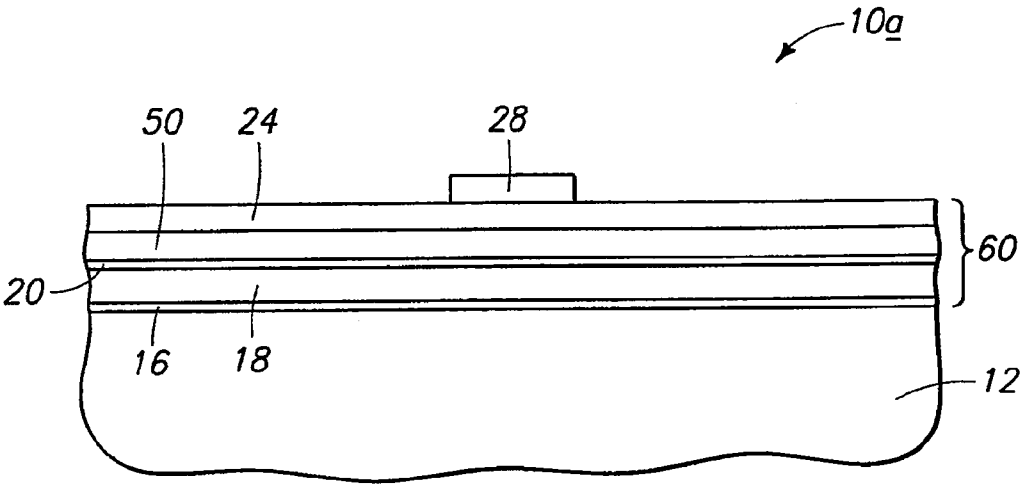


FIG. 5

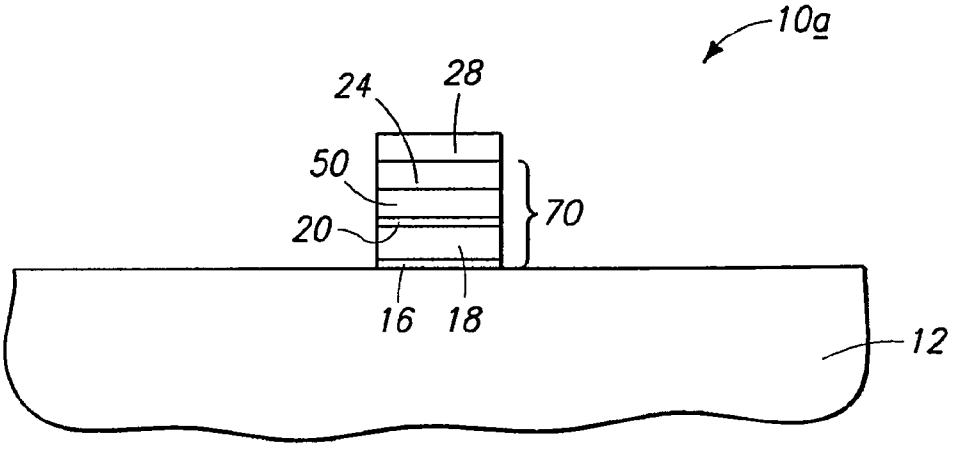


FIG. 6

CIRCUITRY AND GATE STACKS

RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 09/559,903, filed Apr. 26, 2000, which is a divisional of U.S. application Ser. No. 09/146,842, filed Sep. 3, 1998, now issued as U.S. Pat. No. 6,281,100. These applications are incorporated herein their entirety by reference.

TECHNICAL FIELD

[0002] The invention pertains to methods of forming and utilizing antireflective materials. The invention also pertains to semiconductor processing methods of forming stacks of materials, such as, for example, gate stacks.

BACKGROUND OF THE INVENTION

[0003] Semiconductor processing methods frequently involve patterning layers of materials to form a transistor gate structure. FIG. **1** illustrates a semiconductive wafer fragment **10** at a preliminary step of a prior art gate structure patterning process. Semiconductive wafer fragment **10** comprises a substrate **12** having a stack **14** of materials formed thereover. Substrate **12** can comprise, for example, monocrystalline silicon lightly doped with a p-type background dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0004] Stack **14** comprises a gate oxide layer **16**, a polysilicon layer **18**, a metal silicide layer **20**, an oxide layer **22**, a nitride layer **24**, an antireflective material layer **26**, and a photoresist layer **28**. Gate oxide layer **16** can comprise, for example, silicon dioxide, and forms an insulating layer between polysilicon layer **18** and substrate **12**. Polysilicon layer **18** can comprise, for example, conductively doped polysilicon, and will ultimately be patterned into a first conductive portion of a transistor gate.

[0005] Silicide layer **20** comprises a metal silicide, such as, for example, tungsten silicide or titanium silicide, and will ultimately comprise a second conductive portion of a transistor gate. Prior to utilization of silicide layer **20** as a conductive portion of a transistor gate, the silicide is typically subjected to an anneal to improve crystallinity and conductivity of the silicide material of layer **20**. Such anneal can comprise, for example, a temperature of from about 800° C. to about 900° C. for a time of about thirty minutes with a nitrogen (N_2) purge.

[0006] If silicide layer **20** is exposed to gaseous forms of oxygen during the anneal, the silicide layer can become oxidized, which can adversely effect conductivity of the layer. Accordingly, oxide layer **22** is preferably provided over silicide layer **20** prior to the anneal. Oxide layer **22** can comprise, for example, silicon dioxide. Another purpose of having oxide layer **22** over silicide layer **20** is as an insulative layer to prevent electrical contact of silicide layer **20** with other conductive layers ultimately formed proximate silicide layer **20**.

[0007] Nitride layer **24** can comprise, for example, silicon nitride, and is provided to further electrically insulate conductive layers **18** and **20** from other conductive layers which may ultimately be formed proximate layers **18** and **20**. Nitride layer **24** is a thick layer (a typical thickness can be on the order of several hundred, or a few thousand Angstroms) and can create stress on underlying layers. Accordingly, another function of oxide layer **22** is to alleviate stress induced by nitride layer **24** on underlying layers **18** and **20**.

[0008] Antireflective material layer **26** can comprise, for example, an organic layer that is spun over nitride layer **24**. Alternatively, layer **26** can be a deposited inorganic antireflective material, such as, for example, $Si_xO_yN_z$:H, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33. In practice the layer can be substantially inorganic, with the term "substantially inorganic" indicating that the layer can contain a small amount of carbon (less than 1% by weight). Alternatively, if, for example, organic precursors are utilized, the layer can have greater than or equal to 1% carbon, by weight.

[0009] Photoresist layer **28** can comprise either a positive or a negative photoresist. Photoresist layer **28** is patterned by exposing the layer to light through a masked light source. The mask contains clear and opaque features defining a pattern to be created in photoresist layer **28**. Regions of photoresist layer **28** which are exposed to light are made either soluble or insoluble in a solvent. If the exposed regions are soluble, a positive image of the mask is produced in photoresist slayer **28** and the resist is termed a positive photoresist. On the other hand, if the non-radiated regions are dissolved by the solvent, a negative image results, and the photoresist is referred to as a negative photoresist.

[0010] A difficulty that can occur when exposing photoresist layer **28** to radiation is that waves of the radiation can propagate through photoresist **28** to a layer beneath the photoresist and then be reflected back up through the photoresist to interact with other waves of the radiation which are propagating through the photoresist. The reflected waves can constructively and/or destructively interfere with the other waves to create periodic variations of light intensity within the photoresist. Such variations of light intensity can cause the photoresist to receive non-uniform doses of energy throughout its thickness. The non-uniform doses can decrease the accuracy and precision with which a masked pattern is transferred to the photoresist. Antireflective material **26** is provided to suppress waves from reflecting back into photoresist layer **28**. Antireflective layer **26** comprises materials which absorb and/or attenuate radiation and which therefore reduce or eliminate reflection of the radiation.

[0011] FIG. **2** shows semiconductive wafer fragment **10** after photoresist layer **28** is patterned by exposure to light and solvent to remove portions of layer **28**.

[0012] Referring to FIG. **3**, a pattern from layer **28** is transferred to underlying layers **16**, **18**, **20**, **22**, **24**, and **26** to form a patterned stack **30**. Such transfer of a pattern from masking layer **28** can occur by a suitable etch, such as, for example, a plasma etch utilizing one or more of Cl, HBr, CF_4, CH_2F_2, He, and NF_3.

[0013] After the patterning of layers **16**, **18**, **20**, **22**, **24** and **26**, layers **28** and **26** can be removed to leave a patterned gate stack comprising layers **16**, **18**, **20**, **22**, and **24**.

[0014] A continuing goal in semiconductor wafer fabrication technologies is to reduce process complexity. Such reduction can comprise, for example, reducing a number of

process steps, or reducing a number of layers utilized in forming a particular semiconductor structure. Accordingly, it would be desirable to develop alternative methods of forming patterned gate stacks wherein fewer steps and/or layers are utilized than those utilized in the prior art embodiment described with reference to FIGS. **1-3**.

SUMMARY OF THE INVENTION

[0015] In one aspect, the invention encompasses a semiconductor processing method. A metal silicide layer is formed over a substrate. An antireflective material layer is chemical vapor deposited in physical contact with the metal silicide layer. A layer of photoresist is applied over the antireflective material layer and patterned photolithographically.

[0016] In another aspect, the invention encompasses a gate stack forming method. A polysilicon layer is formed over a substrate. A metal silicide layer is formed over the polysilicon layer. An antireflective material layer is deposited over the metal silicide layer. A silicon nitride layer is formed over the antireflective material layer and a layer of photoresist is formed over the silicon nitride layer. The layer of photoresist is photolithographically patterned to form a masking layer from the layer of photoresist. A pattern is transferred from the masking layer to the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer to pattern the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer into a gate stack.

[0017] In yet another aspect, the invention encompasses a gate stack comprising a polysilicon layer over a semiconductive substrate. The gate stack further comprises a metal silicide layer over the polysilicon layer, and a layer comprising silicon, oxygen and nitrogen over the metal silicide. Additionally, the gate stack comprises a silicon nitride layer over the layer comprising silicon, oxygen and nitrogen.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0019] FIG. **1** is a fragmentary, diagrammatic, cross-sectional view of a semiconductive wafer fragment at a preliminary processing step of a prior art process.

[0020] FIG. **2** is a view of the FIG. **1** wafer fragment at a prior art processing step subsequent to that of FIG. **1**.

[0021] FIG. **3** is a view of the FIG. **1** wafer fragment at a prior art processing step subsequent to that of FIG. **2**.

[0022] FIG. **4** is a fragmentary, diagrammatic, cross-sectional view of a semiconductive wafer fragment at a preliminary processing step of a method of the present invention.

[0023] FIG. **5** is a view of the FIG. **4** wafer fragment at a processing step subsequent to that of FIG. **4**.

[0024] FIG. **6** is a view of the FIG. **4** wafer fragment at a processing step subsequent to that of FIG. **5**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[0026] An embodiment encompassed by the present invention is described with reference to FIGS. **4-6**. In describing the embodiment of FIGS. **4-6**, similar numbering to that utilized above in describing the prior art processing of FIGS. **1-3** will be used, with differences indicated by the suffix "a", or by different numerals.

[0027] Referring to FIG. **4**, a semiconductive wafer fragment **10***a* is illustrated at a preliminary processing step. Wafer fragment **10***a*, like the wafer fragment **10** of FIGS. **1-3**, comprises a substrate **12**, a gate oxide layer **16**, a polysilicon layer **18**, and a silicide layer **20**. However, in contrast to the prior art processing described above with reference to FIGS. **1-3**, a layer **50** comprising silicon, nitrogen, and oxygen is formed over silicide **20**, and in the shown preferred embodiment is formed in physical contact with silicide layer **20**. Layer **50** thus replaces the oxide layer **22** of the prior art embodiment of FIGS. **1-3**.

[0028] Layer **50** is preferably formed by chemical vapor deposition (CVD). Layer **50** can be formed by, for example, CVD utilizing SiH_4 and N_2O as precursors, in a reaction chamber at a temperature of about 400° C. Such deposition can be performed either with or without a plasma being present within the reaction chamber. Exemplary conditions for depositing layer **50** include flowing SiH_4 into a plasma-enhanced CVD chamber at a rate of from about 40 standard cubic centimeters per minute (SCCM) to about 300 SCCM (preferably about 80 SCCM), N_2O at a rate of from about 80 SCCM to about 600 SCCM (preferably about 80 SCCM), He at a rate from about 1300 SCCM to about 2500 SCCM (preferably about 2200 SCCM), with a pressure within the chamber of from about 4 Torr to about 6.5 Torr, and a power to the chamber of from about 50 watts to about 200 watts (preferably about 100 watts).

[0029] The above-described exemplary conditions can further include flowing nitrogen gas (N_2) into the reaction chamber at a rate of from greater than 0 SCCM to about 300 SCCM, and preferably at a rate of about 200 SCCM, and/or flowing NH_3 into the reaction chamber at a rate of from greater than 0 SCCM to about 100 SCCM.

[0030] An exemplary composition of layer **50** is $Si_xN_yO_z$:H, wherein x=0.5, y=0.37, and z=0.13. The relative values of x, y, z and the hydrogen content can be adjusted to alter absorbance characteristics of the deposited material. Layer **50** preferably has a thickness of from about 250 Å to about 650 Å.

[0031] Layer **50** is preferably provided over silicide layer **20** before annealing layer **20**. Layer **50** thus provides the above-described function of oxide layer **22** (described with reference to FIGS. **1-3**) of protecting silicide layer **20** from exposure to gaseous oxygen during annealing of the silicide layer.

[0032] A silicon nitride layer **24** is formed over layer **50**, and can be in physical contact with layer **50**. As discussed above in the background section of this disclosure, silicon nitride layer **24** can exert stress on underlying layers. Accordingly, layer **50** can serve a function of prior art silicon dioxide layer **22** (discussed with reference to FIGS. **1-3**) of alleviating such stress from adversely impacting underlying conductive layers **20** and **18**. Silicon nitride layer **24** can be formed over layer **50** either before or after annealing silicide layer **20**.

[0033] A photoresist layer **28** is formed over silicon nitride layer **24**. In contrast to the prior art embodiment discussed with reference to FIGS. **1-3**, there is no antireflective material layer formed between silicon nitride layer **24** and photoresist layer **28**. Instead, layer **50** is preferably utilized to serve the function of an antireflective material. Specifically, nitride layer **24** is effectively transparent to radiation utilized in

patterning photoresist layer **28**. Accordingly, radiation which penetrates photoresist layer **28** will generally also penetrate silicon nitride layer **24** and thereafter enter layer **50**. Preferably, the stoichiometry of silicon, oxygen and nitrogen of layer **50** is appropriately adjusted to cancel radiation reaching layer **50** from being reflected back into photoresist layer **28**. Such adjustment of stoichiometry can be adjusted with routine experimentation utilizing methods known to persons of ordinary skill in the art. Another way of describing the adjustment of layers **24** and **50** is that layers **24** and **50** can be tuned in thickness (by adjusting thickness of one or both of layers **24** and **50**) and stoichiometry (by adjusting a stoichiometry of layer **50**) such that reflection back into an overlying layer of photoresist is minimized.

[0034] Referring to FIG. **5**, photoresist layer **28** is patterned to form a patterned mask over a stack **60** comprising layers **16**, **18**, **20**, **50** and **24**.

[0035] Referring to FIG. **6**, a pattern from photoresist layer **28** is transferred to stack **60** (FIG. **5**) to form a patterned gate stack **70** comprising layers **16**, **18**, **20**, **50** and **24**. Such transfer of a pattern from layer **28** can be accomplished by, for example, a plasma etch utilizing one or more of Cl, HBr, CF_4, CH_2F_2, He and NF_3. Photoresist layer **28** can then be removed from over gate stack **70**. Subsequently, source and drain regions can be implanted adjacent the gate stack, and sidewall spacers can be provided over sidewalls of the gate stack to complete construction of a transistor gate from gate stack **70**.

[0036] The method of the present invention can reduce complexity relative to the prior art gate stack forming method described above with reference to FIGS. **1-3**. Specifically, the method of the present invention can utilize a single layer (**50**) to accomplish the various functions of protecting silicide during annealing, reducing stress from an overlying silicon nitride layer, and alleviating reflections of light during photolithographic processing of an overlying photoresist layer. Accordingly, the method of the present invention can eliminate an entire layer (antireflective layer **26** of FIGS. **1-3**) relative to the prior art process described with reference to FIGS. **1-3**. Such elimination of a layer also eliminates fabrication steps associated with forming and removing the layer. Accordingly, methods encompassed by the present invention can be more efficient semiconductor fabrication processes then prior art methods.

[0037] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

1. A gate structure, comprising:
a gate oxide layer disposed on a semiconductor substrate;
a polysilicon layer disposed on the gate oxide layer;
a metal silicide layer disposed on the polysilicon layer;
a $Si_xN_yO_z$:H layer disposed on the metal silicide layer, wherein the metal silicide layer is subjected to an anneal treatment after the $Si_xN_yO_z$:H layer is disposed to protect the metal silicide layer during the anneal; and
a silicon nitride layer disposed on the $Si_xN_yO_z$:H layer, wherein the polysilicon layer, the gate oxide layer, the metal silicide layer, the $Si_xN_yO_z$:H layer and the silicon nitride layer are patterned to form the gate structure, wherein the final thicknesses of both the silicon nitride layer and the $Si_xN_yO_z$:H layer are optimized to cooperatively minimize reflection back into an overlying layer of photoresist.

2. The gate structure of claim **1**, wherein the relative values of x, y and z are selected to alter an absorbance characteristic.

3. The gate structure of claim **2**, wherein x ranges between approximately 0.39 and 0.65, y ranges between approximately 0.02 to 0.56 and z ranges between approximately 0.05 to 0.33.

4. The gate structure of claim **1**, wherein the metal in the silicide layer comprises one of titanium and tungsten.

5. The gate structure of claim **1**, wherein the $Si_xN_yO_z$:H layer ranges in thickness between approximately 300 Å and approximately 650 Å.

6. A gate structure, comprising:
a gate oxide layer formed on a supporting substrate;
a polysilicon layer formed on the gate oxide layer;
a metal silicide layer formed on the polysilicon layer;
an antireflective layer formed on the metal silicide layer, wherein the metal silicide layer is annealed after the antireflective layer is disposed on the metal silicide layer; and
a silicon nitride layer formed on the antireflective layer, wherein the polysilicon layer, the gate oxide layer, the metal silicide layer, the antireflective layer and the silicon nitride layer are patterned to define a gate stack, further wherein the selected thicknesses of at least one of the silicon nitride layer and the antireflective layer cooperatively minimize reflection back into an overlying layer of photoresist.

7. The gate structure of claim **6**, wherein the antireflective layer comprises silicon, nitrogen, oxygen and hydrogen in a predetermined composition.

8. The gate structure of claim **7**, wherein the predetermined composition comprises $Si_xN_yO_z$:H, wherein x ranges between approximately 0.39 and 0.65, y ranges between approximately 0.02 to 0.56 and z ranges between approximately 0.05 to 0.33.

9. The gate structure of claim **6**, wherein the metal silicide layer comprises one of a titanium silicide and a tungsten silicide.

10. A gate structure, comprising:
a metal silicide layer;
an antireflective layer abutting the metal silicide layer that is subjected to an anneal treatment to protect the metal silicide layer during the anneal; and
a silicon nitride layer abutting the antireflective layer wherein the metal silicide layer, the antireflective layer and the silicon nitride layer are patterned to form the gate structure, wherein the selected thicknesses of the silicon nitride layer and the antireflective layer cooperatively minimize reflection back into a layer of photoresist.

11. The gate structure of claim **10**, comprising a supporting substrate that includes a gate oxide layer disposed on the substrate, and a polysilicon layer disposed on the gate oxide layer, wherein the polysilicon layer abuts the metal silicide layer.

12. The gate structure of claim **10**, wherein the antireflective layer comprises $Si_xN_yO_z$:H, wherein x ranges between approximately 0.39 and 0.65, y ranges between approximately 0.02 to 0.56 and z ranges between approximately 0.05 to 0.33.

13. The gate structure of claim **10**, wherein the metal silicide layer comprises one of a titanium silicide and a tungsten silicide.

14. The gate structure of claim **11**, wherein the gate oxide layer and the polysilicon layer are patterned with the metal silicide layer, the antireflective layer and the silicon nitride layer.

15. A gate structure, comprising:

a gate oxide layer disposed on a semiconductor substrate;

a polysilicon layer disposed on the gate oxide layer;

an annealed, metal silicide layer disposed on the polysilicon layer;

a $Si_xN_yO_z$:H layer disposed on the metal silicide layer during the anneal and configured to act as an antireflective layer; and

a silicon nitride layer disposed on the $Si_xN_yO_z$:H layer and wherein the thicknesses of the silicon nitride layer and the $Si_xN_yO_z$:H layer are optimized in combination to cooperatively minimize reflection back into a layer of photoresist.

16. The gate structure of claim **15**, wherein the silicon nitride layer has a thickness greater than 1000 Å.

17. The gate structure of claim **15**, wherein the relative values of x, y and z are selected to alter an absorbance characteristic.

18. The gate structure of claim **17**, wherein x ranges between approximately 0.39 and 0.65, y ranges between approximately 0.02 to 0.56 and z ranges between approximately 0.05 to 0.33.

19. The gate structure of claim **15**, wherein the metal silicide layer comprises one of a titanium silicide and a tungsten silicide.

20. The gate structure of claim **15**, wherein the $Si_xN_yO_z$:H layer ranges in thickness between approximately 300 Å and approximately 650 Å.

* * * * *